Understanding the Clock Architecture of the OMAP36xx - Public -

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ABSTRACT

This application note describes the clock architecture of OMAP36xx from the perspective of the PRCM. A single diagram of the clock architecture summarizes all of the clock signals including the PRCM register bits that affect them. Using this diagram, SW developers can quickly understand and find the relevant register bits necessary for configuring the clocks within the OMAP36xx.

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Table 1. Document History

Version	Date	Author	Notes
1.0	May/20/2010	A0783816	1

1. Created Document

1 Introduction

This application note provides an overview of the clock architecture for OMAP36xx. A power reset clock manager (PRCM) module has multiple registers that are used to control the clocks for each module in the OMAP device. It is useful to find which bits should be set to enable a module.

2 How to use this clock architecture diagram

Please read the important information in this section before using the diagram.

2.1 Supported Silicon Revision

This figure supports OMAP36xx ES1.0 device.

2.2 Multiple Instances of a Module

OMAP36xx has multiple instances of some modules. For example, there are multiple instances for the GPIO, McBSP and GPTimer modules. For simplicity's sake, these modules are combined. However some modules are not assigned to the same power domain, so they are drawn separately. For example, GPIO1 & GPIO2-6 are drawn separately since they are in different power domains.

2.3 Power Domain Colors

Background colors show the assigned power domain. The color details are as follows:

Light Gray : Core domain
Light Blue : Wakeup domain
Purple : MPU domain
Red : IVA domain
Pink : SGX domain
Yellow : CAM domain
Light Green : DSS domain
Gray : PERIPHERAL domain
Blue : DPLLx domain
Emerald Green : USB HOST domain
Green : SmartReflex domain
Blown : EMU domain

2.4 Not supported in the figure

This figure does not support all clock control features for the OMAP36xx because some modules have an internal clock that is not controlled by the PRCM. This figure comes from the PRCM's standpoint.

For example: DSI PLL output can be used for DSS_FCLK instead of DSS1_ALWON_FCLK. It is controlled by DISPC_CLK_SWITCH bit in DSS.

3 Figure of the Clock configuration

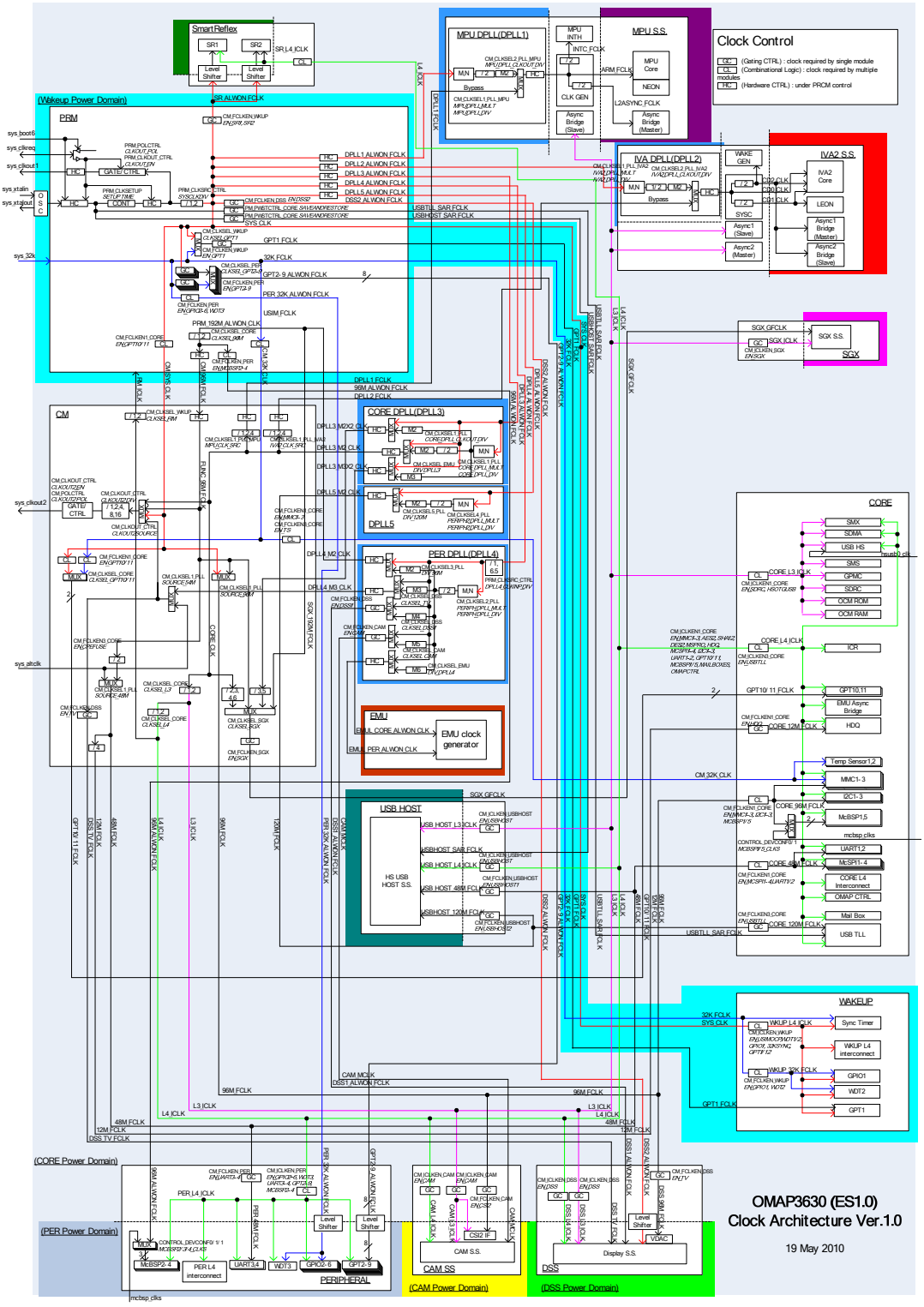

Figure 1. OMAP36xx Clock Architecture

References

1. *Understanding the OMAP34xx Clock Architecture* – Public - (SWPAxxx)
2. *CTT-OMAP3630ES1.0-v1.6.0.1-Public*

OMAP36xx Disclaimer

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