Background on the Digital RF Processor (DRP): Revolutionary Approach to Wireless Communications

The basic paradox of developing cellular handsets is that even as the complexity of these devices increases, users continue to demand products that are lighter weight, less expensive, and more power efficient. Complexity is driven by today's cellular handsets having to support multi-band transceivers, diverse modulation schemes and multiple protocols. Add to the mix color displays, cameras, GPS location technology, Bluetooth® personal area networking, and wireless LAN (WLAN) connectivity for high-speed local-area data access, as well as enough processing capacity and additional memory to support digital audio and video, games, and PDA applications, and you've got a fair description of a modern handset. These demands put handset manufacturers in the unenviable position of meeting customer expectations while maintaining their own profitability.

Delivering increased levels of functionality in a handheld form-factor while continuing to improve battery life and lower cost is possible only through the aggressive integration of the handset electronics. Analog RF components are an obvious integration target, as they occupy as much as 30 to 40 percent of total board real estate, and functions such as Bluetooth, GPS, and WLAN only increase that requirement. However, as designers strive to integrate more analog components, integration becomes a complex technological challenge in itself. As any engineer will attest, RF design is probably the trickiest of design challenges, even when working with highly specialized, stand-alone components. There is no question that highly integrated analog radios can be manufactured, but if they don't reduce design complexity, cost, and power consumption, then the value of such integration is questionable.
Several years ago, TI recognized the difficulties of RF integration and began work on developing digital alternatives that could leverage the cost and power benefits of volume CMOS process manufacturing. Today, TI’s Digital RF Processor (DRP) architecture provides an efficient and cost-effective migration path for RF analog integration that promises to have a profound effect on the future of wireless technology. TI has already produced two single-chip Bluetooth devices incorporating the DRP design, the BRF 6100 and BRF6150, with radio and baseband processing integrated on a single die, and will deliver the most integrated single-chip GSM device in the world by the end of 2004. TI sees a future where RF is easily configurable and modularized so that it can add to your application as easily as other wired interfaces are today.

The two fundamental analog RF architectures used in cellular handsets are the super-heterodyne radio receiver and the direct-conversion radio receiver. They have been widely used for many decades in literally billions of cellular handsets. Most “alternative” analog radio architectures are, in fact, minor variations of either the super-heterodyne or the direct-conversion architecture.

Designers of modern handset radios using these architectures or their variations must meet severe performance requirements, including working with highly sensitive receivers capable of processing voltage levels of only a few microvolts without losing the ability to reject energy in adjacent frequency bands. These stringent performance demands impact integration options. Technology challenges aside, integration must also be practical. Users
simply won't accept a phone that is feature laden and compact that consumes power too quickly and is significantly more expensive. The handset market is driven by volumes in the hundreds of millions each year, making cost a driving consideration for integration.

Integrating a classical analog radio on a single chip can be done in a relatively simple bipolar or BiCMOS process. The resulting radio die could then be assembled with the digital logic chip using a multi-chip packaging technology (system-in-package technology). However, since the radio employs an analog design, an analog radio test method is needed, requiring either a multi-pass test flow, using both digital and RF test solutions, or an expensive mixed-signal tester. In either case, when an RF IC fails to meet requirements, the entire module, including the digital baseband die, must be discarded. Such yield limitations and the high cost of testing devices make it unlikely for such an approach to achieve the commercial viability necessary for volume markets.

Alternatively, integration of both digital and analog functions could be undertaken in an advanced BiCMOS process using Silicon Germanium (SiGe) wafers. However, the resulting die would bear the additional expense of the several reticles associated with processing the SiGe transistors – normally 4-5 additional reticles are used to add a SiGe device. More problematic, however, is that fact that SiGe BiCMOS technologies lag CMOS at state-of-art lithography levels. Today, SiGe processes at 130-nm are available from only a few sources, while several CMOS implementations of digital baseband processing functions at 90-nm have already been announced. Given the tremendous pressure to add handset features while reducing cost, it is simply not prudent to adopt a wafer process technology strategy that doesn’t keep the system logic at the lowest possible cost at all times.

The final option until now for radio electronics integration has been making a classical analog radio design in CMOS. While several CMOS cellular radio designs have been produced, implementation of the analog mixers, filters, and amplifiers in CMOS technology has proven difficult and generally resulted in higher overall power consumption than a similar design based in SiGe. Scaling analog designs to lower voltage levels also becomes more difficult as process technologies advance, compounded by the fact that device modeling and process maturity early in the development of a new process node are generally inadequate for the highly accurate parametric modeling that would be required for such severely constrained designs.

Clearly, no easy and readily available integration strategy exists for analog radio integration. System-in-package approaches, as described, suffer from high cost. Monolithic integration in SiGe BiCMOS cannot offer adequate logic density. And monolithic CMOS integration suffers from fundamental performance limitations for analog radio functions.
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TI's digital RF processor architecture

TI's Digital RF Processor design is possible because silicon wafer processing has progressed to a point where large blocks of CMOS logic can be clocked at multi-GHz frequencies. By applying its digital expertise to the RF analog problem, Texas Instruments has developed sampled-data processing techniques, samplers, switched-capacitor filters, oversampling converters, and digital signal processors that can take over the role of analog amplifiers, filters, and mixers. Rather than an inefficient implementation of analog blocks in a digital process technology, with the DRP the analog signal is oversampled and processed in the digital domain. Since radio signals at the antenna are always analog, a small amount of analog processing is included in the DRP between the input and the first sampling function. Once in the sampled-data domain, digital signal processing takes over.

The more signal processing that can take place in the digital domain, the more direct benefits are realized from process technology scaling. Additionally, as process switching speed increases at each node, it becomes possible to sample at even higher rates. Oversampling of the input signal reduces noise aliasing problems, allowing designers to "relax" the design of the input networks. By adding more complex filtering, as well as analog-to-digital conversion taking place closer to the antenna, more of the signal processing burden can take place in the digital domain where the full benefits of logic scaling can be realized.

Practical limitations of RF integration

The technical capability to design a digital radio, of course, is only one aspect of bringing CMOS radio integration into the mainstream wireless market. The feasibility of wafer processes and radio architectures must be considered along with the manufacturability of such a radio. With volumes of several hundred million handsets per year, integration of the radio must result in real cost savings when you consider the total cost of ownership.

Conventional radios, for example, are normally tested on specialized test equipment that can accurately measure a circuit's ability to meet RF performance requirements. Production RF testers are not usually able to test large arrays of digital logic, while logic testers offer little or no analog/RF capability. From a testing perspective, the primary concern is that the RF sections of a large SoC cannot be allowed to materially impact the device's production yield, nor can the challenges associated with the radio integration be allowed to slow the migration of a SoC design to the latest available wafer processes.

Fortunately, as radio designs evolve toward greater use of digital signal processing, the challenges of test, yield, and process migration clearly become more similar to those of logic-only devices. Of course, a full migration will never be possible, as some level of analog and mixed-signal functions will always be present.

However, the power of digital techniques can also be brought to bear on testing the mixed signal sections of the design. Given that the analog radio signal is converted to a digital signal on a device that includes an advanced digital signal processor – and potentially other programmable processing elements as well – the test process can utilize the processing capabilities of the SoC itself to fully analyze the baseband signal characteristics it receives. With minimal external analog electronics, loop-back tests can assess the quality of complete
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transmit and receive channels in series. Since there are few external components, radio performance measures can be assessed at the system level as opposed to the functional block level, reducing the number of measurements required. Additionally, with a Built In Self-Test (BIST) capability in place, the SoC can self-calibrate its analog circuits and reduce the effect of parametric variations on yield.

Through the aggressive use of such techniques, the production yield of SoCs with integrated Digital RF radios can approach defect-density limitations, while at the same time actually reducing the test cost for radio functions.

CMOS process technology, leveraging digital radio designs comprised of digital and sampled-data architectures, provides a promising path for radio integration for the next generation of handsets simply not possible with classical radio architectures. Whereas implementation of classical radio architectures pose an almost insurmountable challenge in deep submicron CMOS, sampled-data systems yield the chief benefit of using CMOS: the ability to scale with process advances.

CMOS process technology also offers radio performance characteristics that are attractive for radio integration. Device frequency capability, noise levels, and the availability of passive elements enable the integration of high performance radio functions in CMOS.

TI is at the forefront of Digital RF technology. Sampled-data systems have been widely developed and deployed in many high volume product areas in the 1980s and 90s, proving out the technology for today's higher frequency applications. While the challenges of CMOS are many – including practical considerations such as test cost, yield, and design migration time – it is clear that the benefit of an extremely dense, low-cost logic capability provides a substantial incentive for dealing with these challenges. Texas Instruments continues to invest and innovate with its DRP design, leading the way to the next generation of handsets.