

Manufacturing and Technology Development at Texas Instruments

The Strategy Behind TI's Manufacturing Model

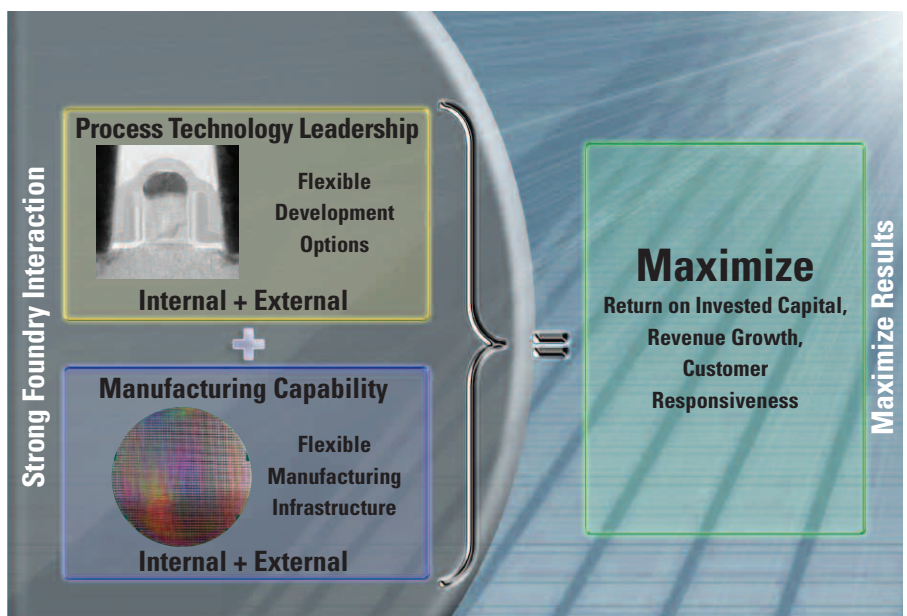
Overview

- TI will increasingly partner with foundries to develop advanced CMOS technology nodes. Starting with the 32-nanometer (nm) node in 2008, silicon process technology development wafers will be run in foundry partners' fabs.
- This change reduces TI's capital expenditures and frees TI resources for more highly differentiated R&D programs.
- TI's strategy for manufacturing leading-edge digital CMOS has not changed. TI will continue its strategy of using both internal and external manufacturing.
- Our strategy for developing analog process technology remains unchanged, and the majority of TI's analog products continue to be manufactured internally.
- TI invests significantly in R&D for our customers and our products, with about \$2.2 billion forecast for 2007.
- Our 45-nm product samples will be delivered this year, and we are on schedule for qualification in mid-2008.

Today's semiconductor industry is a complex ecosystem of highly specialized suppliers of equipment, chemicals and gases, wafers and contract services. Device manufacturers like TI that once had to master every step in the semiconductor supply chain today focus on specific areas of differentiation for their customers and the markets they serve.

TI has historically focused its manufacturing expertise in two primary areas: 1) the process technology, or recipe, for building transistors and interconnecting those transistors on integrated circuits, and 2) taking its chip designs to high-volume production in its factories ahead of the competition. This strategy has led to market leadership in delivering TI's digital and analog products to its customers on the most advanced manufacturing processes.

Manufacturing/Development Strategy



Strategic Changes in 2007

In January 2007, TI announced a shift in its internal technology development to take advantage of its foundry partners' R&D capabilities. With foundries now supplying more than half of TI's digital CMOS capacity during the peak periods of the demand cycle, the regular exchange of process technology information at the 130-nm, 90-nm and 65-nm nodes made it clear that there was no longer a significant gap between the foundries' development and our own. Now the processes that the foundries develop for TI will be the starting point for TI's own internal production.

As a result, starting at the 32-nm node TI will collaborate closely with the foundries to develop processes that specifically address our products' requirements and our customers' needs. The resulting digital CMOS development wafers will run in the foundries' clean rooms instead of our own. Later, when the process is ready to transition to production, wafers will be produced both in TI's factories and at the foundries.

This flexible model for silicon technology development allows TI significant opportunity to tailor the process technology to the specific needs of our customers. TI also remains focused on being first in its markets to ramp products to volume production at each node.

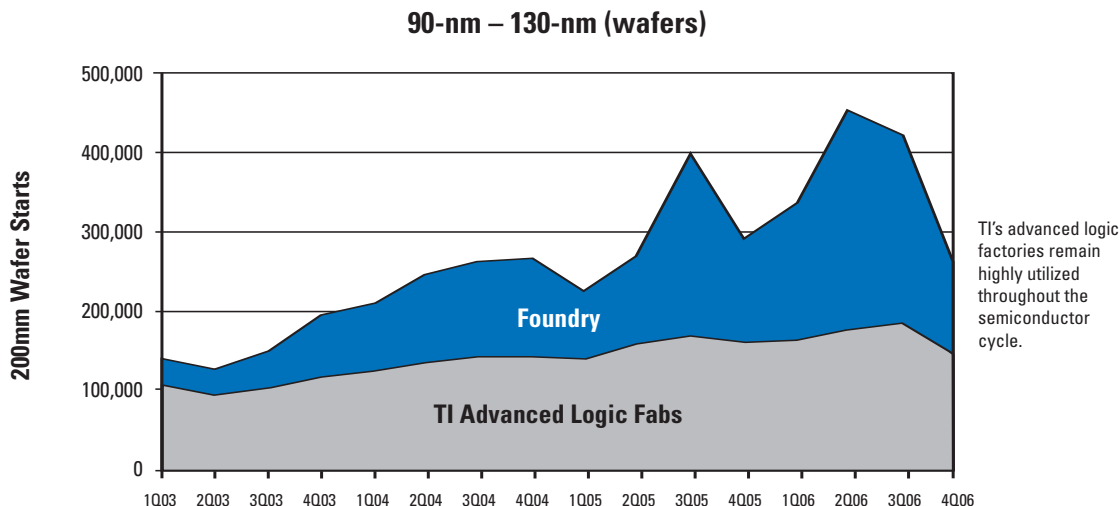
As one of our foundry partners' largest customers, TI will receive unique support in addressing our products' requirements and our customers' needs. Just as we have always done when transferring products to our foundry partners, we will specify a Process Development Kit (PDK) that outlines in detail the specifications the process must meet or exceed to support our design needs.

TI will leverage the digital CMOS technologies developed by our foundry partners to support our highly differentiated design libraries. TI will continue to differentiate its digital CMOS designs in many ways, including:

- Low-power design
- High-density embedded SRAM
- Analog and RF integration
- Software
- Development tools
- Signal processing cores

In addition, this change frees TI's R&D resources to focus on highly differentiated circuit design, software, development tools and support.

Foundries Enhance Manufacturing Responsiveness



Committed to Manufacturing

Changes in process technology development aside, TI remains committed to maintaining its in-house manufacturing capabilities. Running our own wafer fabrication facilities, or fabs, continues to:

- Provide TI with critical insight into the interaction between design and the manufacturing process.
- Give TI leverage in its foundry negotiations.
- Protect a significant portion of our supply from unforeseen disruptions.

Analog and mixed-signal process technology development remain in-house, along with almost all analog manufacturing. Our DMOS6 300-mm digital CMOS fab, recently named Fab of the Year by Semiconductor International magazine, is a high-volume factory with leading-edge immersion lithography capability for 45-nm production.

Customers should see no change in their relationship with TI as we make these adjustments to our process technology development. We are confident this new strategy will further enhance TI's ability to quickly deliver the products our customers need at the right price and performance.

Research and Development Commitment

With about \$2.2 billion forecast to be spent in 2007 on research and development, TI continues to invest significantly in innovation. These investments touch areas where TI sees opportunity to differentiate for its customers, including intellectual property (IP) at the circuit, system and software level. Advances in packaging and analog process technology are regularly contributing to TI's competitive position.

Here are just a few of the areas where TI research and development is focused:

Low Power/Power Management

Reducing system power consumption is no longer only a matter of longer battery life or reducing heat dissipation, it's a global environmental concern. TI has committed teams working solely on reducing power consumption at both the chip and system level. SmartReflex™ is the company's holistic approach combining a number of proprietary TI technologies to dramatically reduce both static and dynamic power throughout an application.

Digital RF

With an eye toward putting mobile communications technology into the hands of more people, including people in third-world countries who may have never made a phone call, TI is leading the way in lowering costs by integrating large portions of wireless systems onto single-chip, high-volume digital CMOS technology. TI's DRP™ architecture uses sampled data processing techniques to build robust transceivers that require no off-chip intermediate filtering stages or more costly SiGe or BiCMOS RF technologies, dramatically reducing total system cost, bill of materials and power consumption.

Embedded SRAM

TI has consistently led the industry in its SRAM memory technology, specifically the size of its memory cell. As applications demand increasing amounts of extremely fast memory on-chip, the amount of chip area dedicated to memory has also grown, increasing manufacturing costs to produce the device. TI's use of 193-nm immersion tools has resulted in the development of what TI believes to be the smallest 45-nm SRAM memory cells in the industry, occupying only 0.24 square microns. That's up to 30 percent smaller than other 45-nm memory cells devices announced to date.

Analog Process Technology

In a world where chip companies race to introduce advanced digital technology, it's important to remember the key role that analog technology plays. Analog chips connect digital signal processors (DSPs) and other types of logic to the outside world, changing real-world signals such as light and sound into binary pulses and back again. Many analog functions are not optimized for high-speed digital logic integration. In those cases, TI analog product development teams focus on analog-only integration, with optimized components for precision, speed and power. Different TI processes are devoted to the various needs of signal conditioning, data conversion and power supply in customers' systems.

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