1394 Open HCI Systems

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Presentation Overview

1394 Open HCI systems

- What, Where, Why of 1394 Open HCI
- OHCI hardware choices
  - What to look for in Open HCI devices
  - A look at Open HCI power management
- 1394 PC system design issues
  - Cable power management
  - PHY and link layout
  - PC 98/99 and 1394 systems
What Is IEEE1394 OHCI?

Open Host Controller Interface

- A 1394 link layer implementation
- Asynchronous and isochronous
- Defines high-performance DMA engines
- Release 1.00 October 20, 1997
- 1394 Open HCI promoters as of 10/97
  - Apple, Compaq, Intel, Microsoft, National Semiconductor, Sun, Texas Instruments
  - austin.ibm.com/pub/chrptech/1394ohci
OHCI And The 1394 System

Windows and Applications

Host Controller - OHCI

PHY

PC

DTV

DVCR

SET-TOP

PRINTER

SCANNER

CAMERA

CD

HDD

DEVICE BAY
## Microsoft WDM 1394 Stack

The diagram illustrates the structure of the Microsoft WDM 1394 Stack, which is a collection of drivers and software components designed to support multimedia devices. The stack is organized into several layers, each with specific functions and components:

### Applications
- **DV Capture**
- **DV Editing**

### AV framework
- **DirectShow**
  - **DV Codec**
  - **MPEG2 Codec**

### Device Drivers
- **Storage Class Driver**
  - **SBP Mini Driver**
- **Streaming Class Driver**
  - **DV MD**
  - **MPEG MD**
  - **Conference Camera MD**
  - **USB Speaker MD**

### Bus Drivers
- **1394 Class Driver**
  - **OHCI Mini Driver**
  - **PCILynx Mini Driver**
  - **Other Mini Driver**
- **USB Class Driver**
  - **Mini Driver**

### Hardware
- **OHCI Hardware**
- **PCILynx Card**
- **Adaptec and Sony Cards**
- **USB I/F**

The diagram also includes other components such as **Mini Driver**, **OHCI Hardware**, and **USB I/F**, which are integral parts of the stack's architecture.
Open HCI Implementations

- Stand alone and integrated solutions for motherboards
- Core logic integration
- Desktop and notebook computers
- Palmtops

- Expansion solutions
- PCI option cards
- CardBus designs
Benefits Of 1394 Open HCI

- Common WDM driver interface
  - Windows 98 and Windows NT 5.0
- High performance and robustness
  - Outperforming earlier 1394 HC designs
  - Higher tolerance of excessive latencies
  - Improved error handling
- Dedicated committee with wide industry participation
- Security improvements
Security Improvements

- Security requires both software and hardware
  - OHCI does not in itself provide security
- Hardware filters used for security
  - Asynchronous request filter
  - Physical request filter
  - Tag filter for isoch copy protection
- OHCI protected GUID
- OHCI does not support bus snooping
Logical Open HCI Blocks

- Four major blocks of Open HCI
  - Link interfaces with physical layer
  - FIFO buffers 1394 packet data
  - DMA controls transfers to/from memory
  - Host Bus interfaces with host I/O bus
Link Layer Block
Open HCI fundamentals

- Link compatible with both 1394-1995 and 1394A PHYs
- IEEE 1394A considerations
  - Standardized PHY/Link interface
  - 1394 bus snoop mode not allowed
  - Supports asynchronous streams
  - Ping timer implemented in Link
  - PHY/Link turn around idle insertion
Link Layer Block
More Open HCI fundamentals

- CYCLE_TIME cannot move backwards
- Extensive async and isoch filtering
- Improvements to existing controllers
  - Bus manager registers in Link
  - Bus_info_block implemented in Link
  - GUID protected with one-time-write
  - Software reset is clearly defined
  - Improved PHY register access
Link Layer Block
Recommendations

- Support IEEE 1394A arbitration enhancements
- `PRIORIVITY_BUDGET` is optional
  - Issue priority LREQs for all response and PHY packets
- Implement bus holders for isolation
- Cycle starts sent with a minimum offset to account for PHY jitter and drift
FIFO RAM Block

Open HCI fundamentals

- No requirement on number of FIFOs
- No requirement on FIFO sizes
- Rules for combining FIFOs
  - Response not blocked by busied request
  - Receive contexts proceed independently
- Open HCI allows for big-endian and little-endian host environments
FIFO RAM Block
Sizing guidelines

- Recommend ~ 2K per FIFO that handles the entire 1394 throughput
- For 32bit/33MHz PCI based Open HCI
- FIFO size dependent upon
  - Host bus b/w and latency
  - Host bus b/w utilization
  - Internal arbitration latency
  - 1394 throughput

For 32bit/33MHz PCI based Open HCI
All DMA engines are host bus contenders

Requires minimum of 4 isoch receive and 4 isoch transmit DMA engines

Isochronous transmit
- Prefetch up to two periods ahead
- Designed to accommodate cycle skips

DMA engines have robust error reporting to the host
OHCI DMA Engines
More Open HCI fundamentals

- Physical DMA engine
  - Handles 1394 configuration ROM access
  - Gives nodes direct host memory access
  - Supports write posting up to the number of error reporting reporting
  - Can post as many write requests as error reporting registers
- ARQQ synthesized bus reset packets
  - Pair requests with bus reset generation
OHCI DMA Engines

Recommendations

- Allow physical DMA to make forward progress while responses are queued
- Implement at least three physical posted write error reporting registers
- Implement priority internal arbitration
  - Limits access latency to a critical FIFO
Host Bus Interface
Open HCI fundamentals

- OHCI Annex A addresses PCI configuration space
  - Includes PCI global byte swap bit
- PCI b/w required to implement OHCI
  - 50 MB/s for 1394 data throughput
  - Plus ~ 10 MB/s DMA engine overhead
PCI Interface Block
Recommendations

- Design for multiple cacheline bursting
- Use appropriate PCI commands
  - MRL, MRM, MWI
- Truncate bursting to prevent starvation
- Implement PCI Power Management

![Total PCI Bandwidth vs. Average Burst Length (quads)](chart)
OHCI Power Management

PCI Power Management

- 1394 HC Device Class Power Management
  - Addressed in Open HCI 1.1 committee
  - Microsoft is ready to support D0 and D3
- D0: On. Fully operational
- D3: Off. PCI clock may stop
- OHCI software is responsible for LPS
- Wake event supported from D3
- D3 - D0 transition requires internal reset retaining the PME# context
OHCI Power Management
Suspend / Resume

- Link Power Status (LPS) is required
  - OHCI software controls the LPS signal
  - PHY drives SCLK when LPS is asserted
  - PHY may save power when de-asserted
- LinkOn is an optional OHCI input
  - Wakes up host when LPS is de-asserted
  - Indicates LinkOn packet received
  - Indicates port connection change
OHCI Power Management
Mobile considerations

◆ Consider D3\textsubscript{COLD} device power state
  ◆ May need auxiliary power supply
  ◆ May require separate reset to initialize the PCI Power Management registers

◆ Unlikely standard power provider

◆ Implement CLKRUN#

◆ Need high performance CardBus controllers for OHCI PC Cards
## Cable Power Management

### Self ID POWER_CLASS options

<table>
<thead>
<tr>
<th>POWER_CLASS</th>
<th>Node Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3’b000</td>
<td>Does not need power and does not repeat power</td>
</tr>
<tr>
<td>3’b001</td>
<td>Self-powered and provides a min of 15W to the bus</td>
</tr>
<tr>
<td>3’b010</td>
<td>Self-powered and provides a min of 30W to the bus</td>
</tr>
<tr>
<td>3’b011</td>
<td>Self-powered and provides a min of 45W to the bus</td>
</tr>
<tr>
<td>3’b100</td>
<td>May be powered from the bus and is using up to 3W</td>
</tr>
<tr>
<td>3’b101</td>
<td>Node is bus powered, and is using up to 3W No additional power is needed to enable the Link</td>
</tr>
<tr>
<td>3’b110</td>
<td>Node is bus powered, and is using up to 3W An additional 3W is needed to enable the Link</td>
</tr>
<tr>
<td>3’b111</td>
<td>Node is bus powered, and is using up to 3W An additional 7W is needed to enable the Link</td>
</tr>
</tbody>
</table>
Cable Power Management

Standard power provider

- Cable Power Source
- Current Limit
- Internal PHY Power
- PHY
- PHY Gnd
- 1394 Conn
- VP
- VG
- VP
- VG
- VP
- VG
Cable Power Management

Standard power provider summary

- Creates power domains for better power distribution management
- Launch voltage of 20 to 33 volts
- Never consume cable power
- Per port diode isolation is required
- Will not pass 1394 bus power
- Provides current limited to less than or equal to 1.5 A per port
Cable Power Management
Alternate power provider

Cable Power Source

Optional Current Limit

Current Limit

PHY Power

V Reg

PHY

PHY Gnd

1394 Conn

VP
VG

1394 Conn
VP
VG

1394 Conn
VP
VG
Cable Power Management

Alternate power provider summary

- Power class 4 may use cable power
- May pass 1394 bus power
- Current limit for 1.5 A peak per port
  - Protection from $V_p$ short circuits
- Launch voltage of 8 - 33 Volts
  - Per port diode isolation required for launch voltage of 20V or greater
Open HCI System Layout

Cable / PHY interface

- Minimize distance differential signals must propagate etch
  - PHY as close as possible to connectors
- Match etch impedance to cable and termination network
  - Match differential signal etch lengths
- Locate differential signal termination resistors as close as possible to PHY
Open HCI System Layout

More PHY layout recommendations

- Keep crystal close to PHY
- Keep cable power regulator (if used) far away from PHY
  - Especially crystal and differential signals
- Keep PHY-Link interface short
  - Signals should have same trace length
- Texas Instruments 1394 app notes
  - www.ti.com/sc/docs/psheets/app_mixed_signal_and_analog.htm
Microsoft PC 98 Guidelines

IEEE 1394 bus design

- Controllers are OHCI, S400 capable
- Config ROM provides GUID
- Other configuration ROM requirements
- PCs use standard 6-pin connectors
- Recommend 3 ports minimum
- PCs source cable power
- Recommend minimum of 20V at 15W
- Comply with Cable Power Distribution
Microsoft PC 99 Guidelines

IEEE 1394 bus design

- PC 99 requirements are not closed
- Mandatory 1394A features are required
- All devices provide at least two ports
- All host controller ports that are externally accessible should support the 6-pin connector
- PC 99 includes recommended use of Device Bay connector
Call To Action

- Test hardware to existing Windows driver stack
- OHCI and IEEE 1394A compliance
  - austin.ibm.com/pub/chrptech/1394ohci
  - symbios.com/pub/standards/io/1394/P1394a
- Build PC 98/99 compliant systems
- Submit OHCI hardware to Windows 98 team for testing
  - E-mail nmdriver@microsoft.com