

Virtual Test Bed

Power Converters



Ali Keyhani & M. Nanda Marwali

Department of Electrical and Computer Engineering

Gerald Baumgartner

Department of Computer and Information Science

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An Integrated Learning System for Power Converter Development





Main Features

- System/Process Visualization Using Graphic Simulation
- Modular Instructional Technology Curricula
- Balanced Knowledge Content for Optimal Transfer of Information

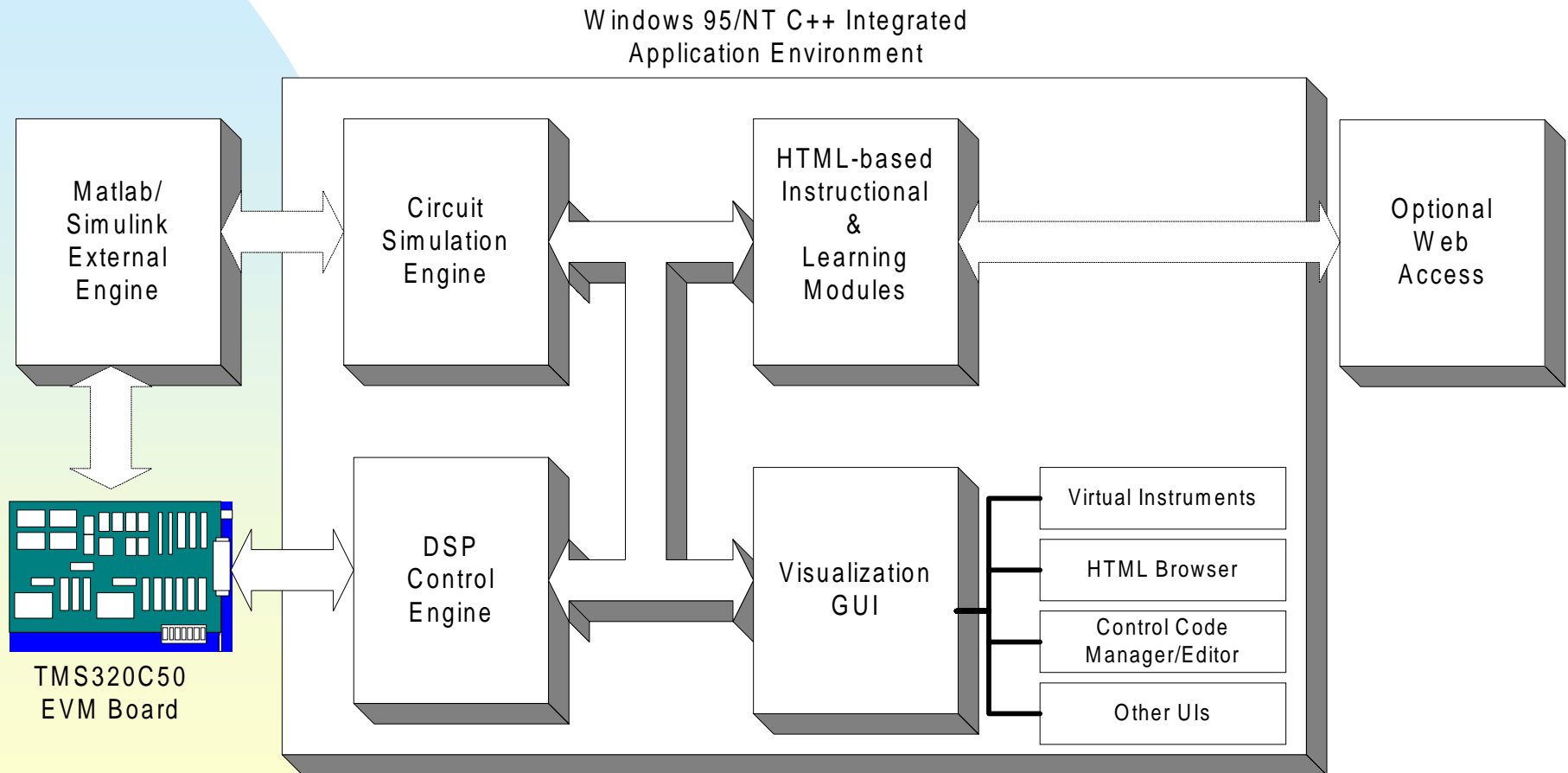


Structure of the Modules

- An Explanation Layer
 - ◆ Information Related to the Basic Fundamental Notions
- An Exploration Layer
 - ◆ Students Apply the Acquired Knowledge to a Practical Example
- An (Instructional) Diagnostic Layer
 - ◆ Interactive Question Tree
 - ◆ Student Performance Evaluation



System Structure (1)



System Structure (2)

- Integrated Application Software
 - ◆ To Integrate Instructional & Learning Modules and Hardware
- Web Access Supported
- Virtual Learning Environment Supported by Various GUI
 - ◆ HTML Browser
 - ◆ Virtual Instruments

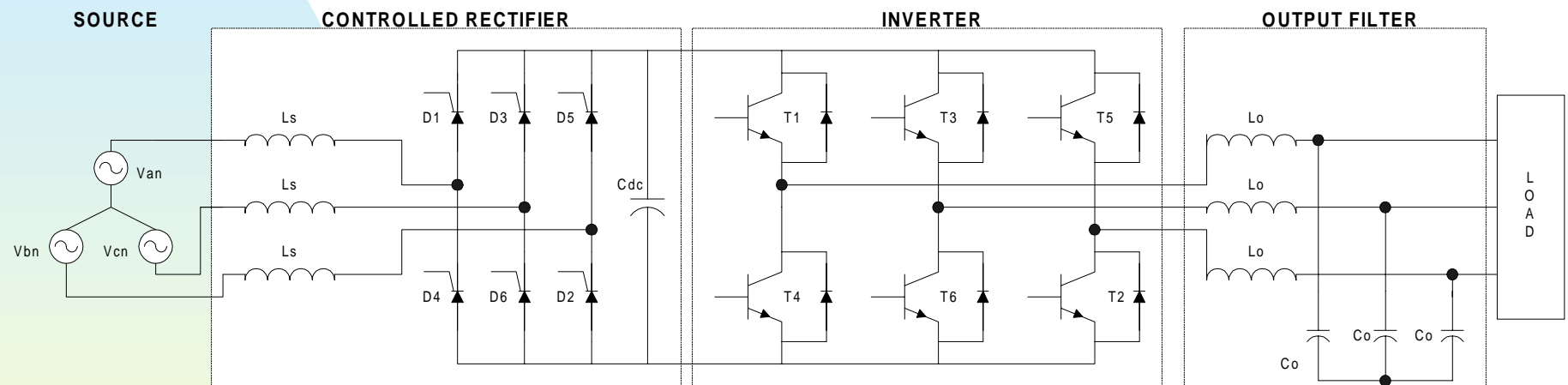


The C++ Integrated Application Environment

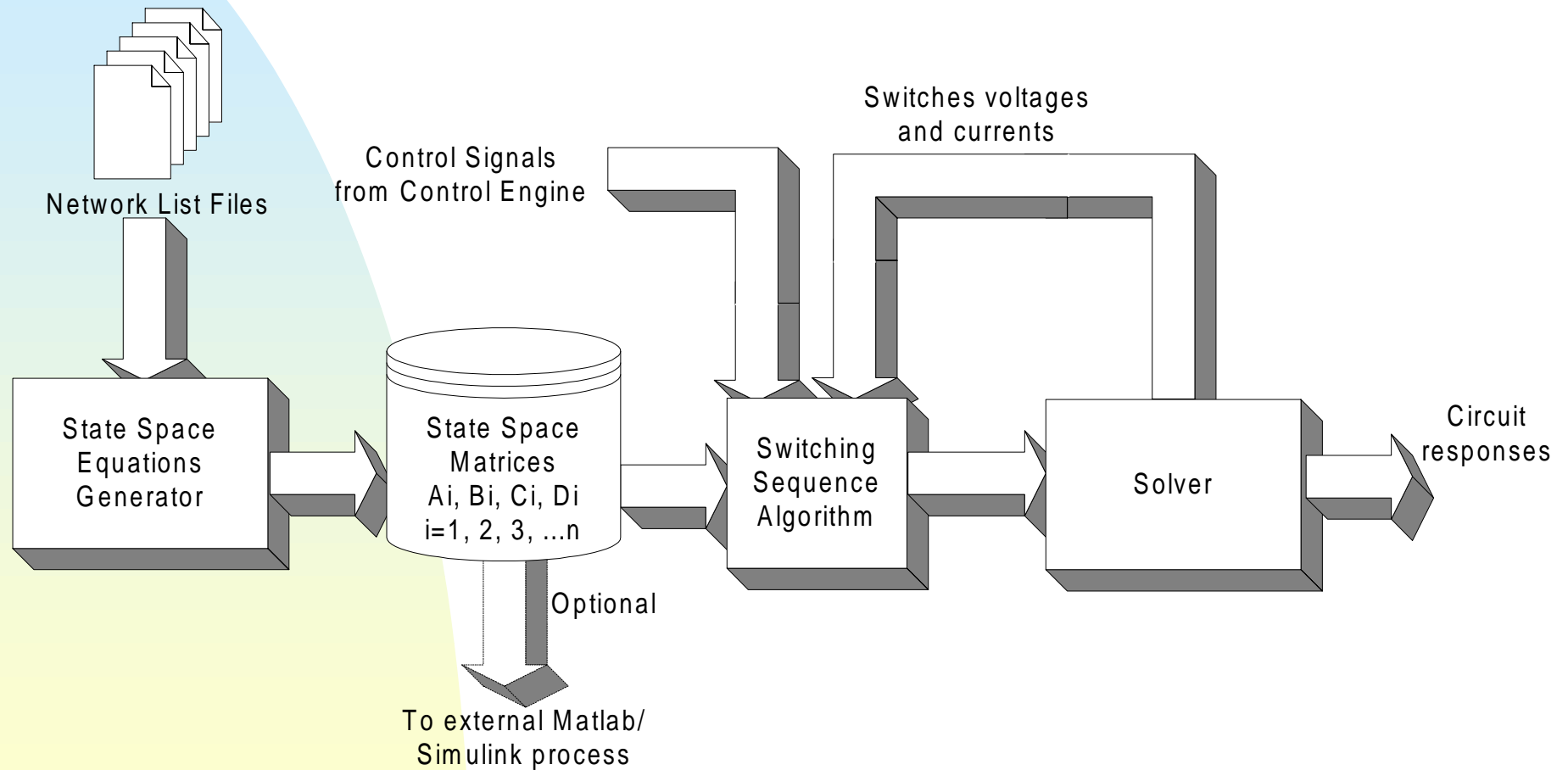
- Objected-Oriented (OO) Design and Implementation
 - ◆ Better System Partitioning via OO (Modularity)
 - ◆ Parallelism in Implementation
 - ◆ Ease of Maintenance
 - ◆ Better Reusability
 - ◆ Better Expandability



Circuit Diagram of Power Converter



The Circuit Simulation Engine (1)



The Circuit Simulation Engine (2)

- Simulation of the Circuit Responses
 - ◆ State Space Based Approach
 - ◆ Ideal Power Switch Model
- Controlled by the Instructional & Learning Module
- Structure
 - ◆ Equation Generator
 - ◆ Switching Sequence Algorithm
 - ◆ The Solver



The DSP Control Engine

- Compiling & Downloading User Control Codes to the EVM Board
- Control the Execution of Control Code
- Retrieve & Pass A/D Signals
- Pass Control Signals
- Retrieve Control Code Variables



Instructional & Learning Modules

- An Example about Power Converter
 - ◆ Explanation Layer
 - ◆ Turn ON/OFF Time
 - ◆ Inverter Operation
 - ◆ Exploration Layer
 - ◆ Experiments and Result Observation
 - ◆ Diagnostic Layer
 - ◆ Level-by-Level Tests and Step-by-Step Understanding
- HTML Format and Remote Access



GUI (1) - Learning Module

Virtual Testbed for Design of Power Converter
Simulation View Sessions Setup Learning modules Window Help

End Continue Exit Step Continuous Cycle Graphic Resolution Optimizer 0.1 us

Basic Inverter Operation - Exploration Layer

Experiment with basic inverter topology:

1. Experiment with different combinations of switch condition

T1 T2
 T4 T5

Output Voltages
 $V_{an} = +V_{dc}$

HU pos(1) HU neg(1) HV pos(1) HV neg(1) HW pos(1) HW neg(1)

Basic Inverter Operation - Explanation Layer

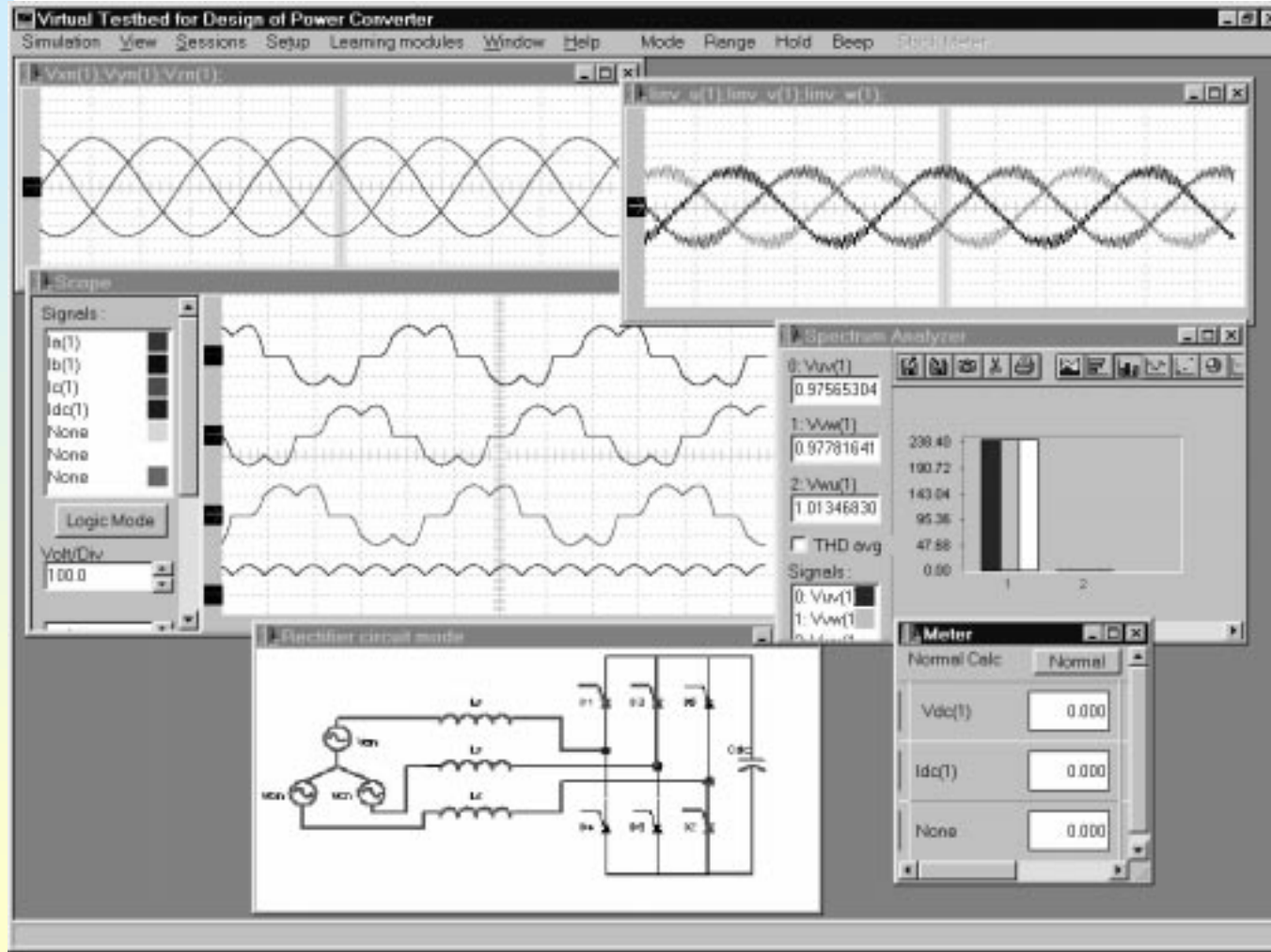
BASIC INVERTER OPERATION

Figure 1. Basic Three-phase inverter topology

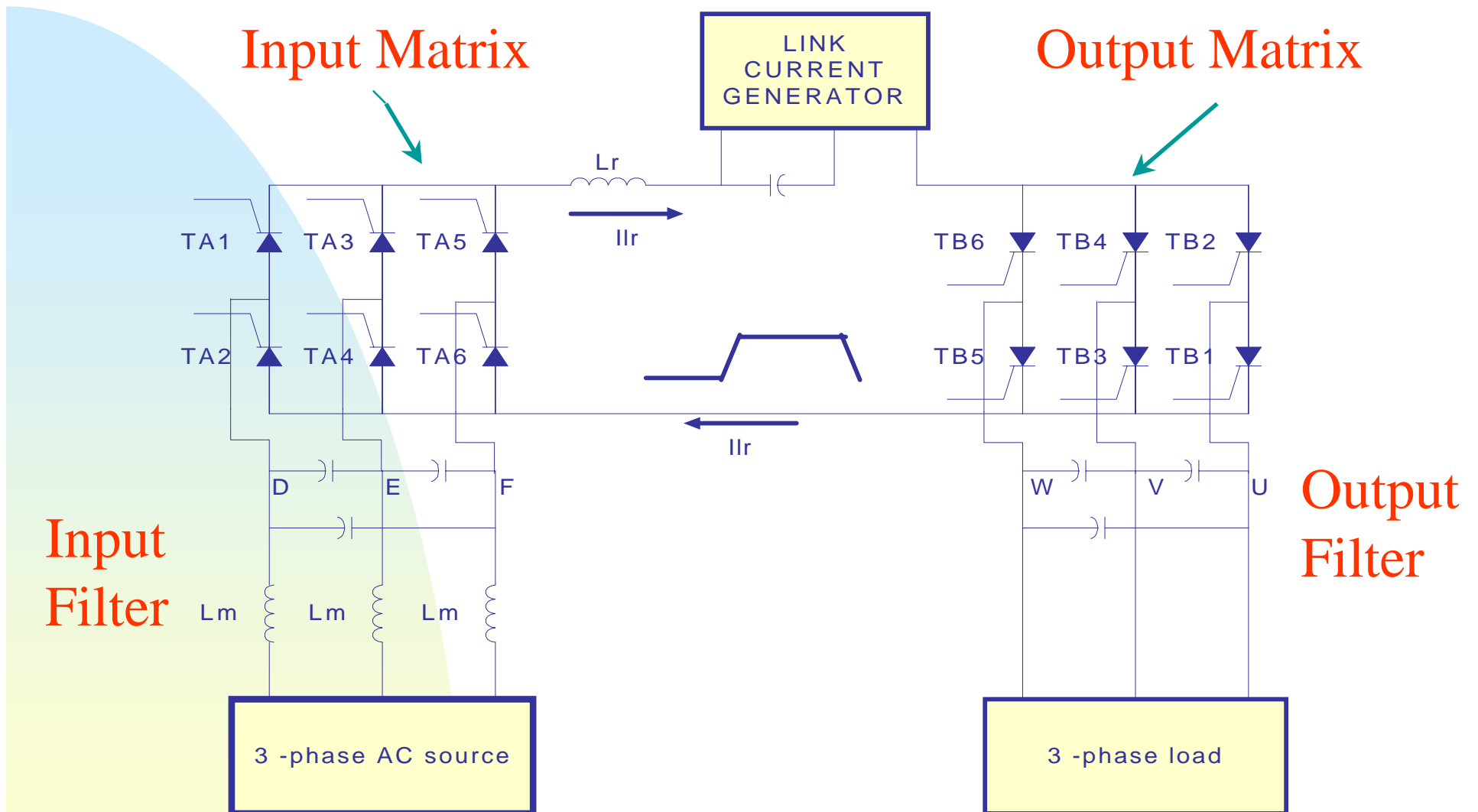
A basic three-phase inverter topology of the power converter is shown in Fig. 1. The basic operation of the converter requires that both switches can not be closed at the same time. Furthermore, since the turn on time and turn off time of the power switching devices need a finite amount



GUI (2) - Virtual Instruments and Circuit Mode



Unipolar Series Resonant Power Converters



Also known as : DC-Link Converter



Features of USRC

- **Series Resonant Converter**
 - ◆ Resonant circuit is in series with the load
 - ◆ All switches are turned on/off in ZVS/ZCS : reduced switching losses.
 - ◆ Switching frequency 7.14 kHz
- **Unipolar (DC) Link Current :**
 - ◆ Allow the use of less expensive unidirectional switches : thyristors for the mains.
 - ◆ Less main switches count
- **Square-wave Link Current :**
 - ◆ Less peak current required compared to sinusoidal-like link current.



USRC Applications

- 3-phase AC Power Conditioner
- DC/AC Inverter in UPS
- Electric Motor Drives
- High power applications



USRC for 3-phase conditioner

Power Transfer Objectives :

- 3-phase 60 Hz output voltages with small THD and good regulation
- Input power factor close to unity

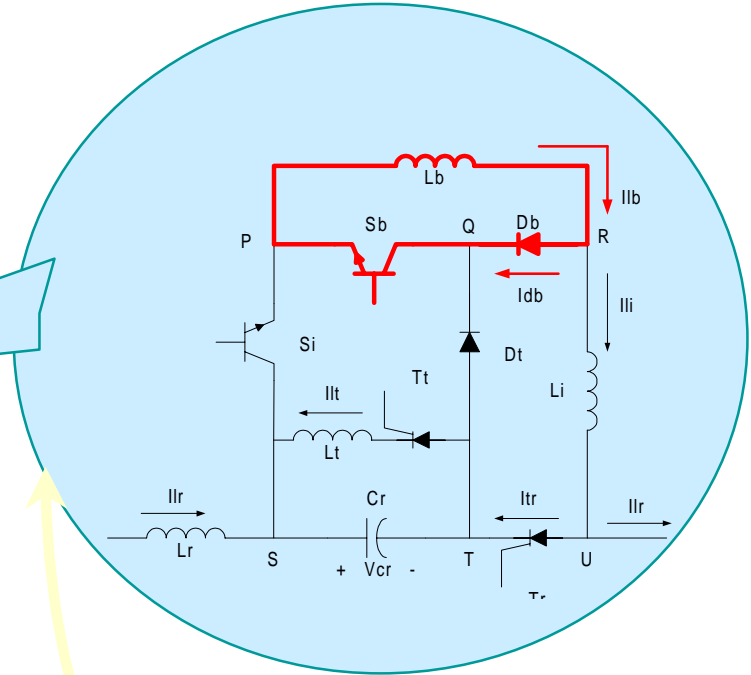
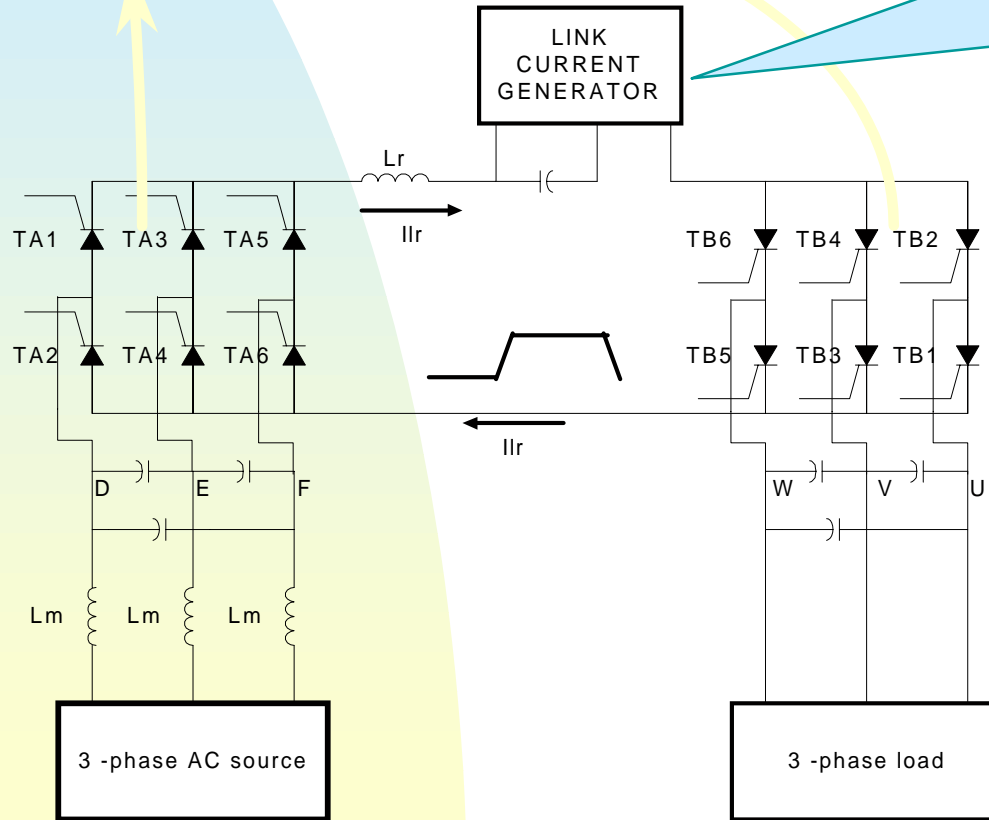


Hardware implementation:

Link Current Generator

DSP-based
Controller

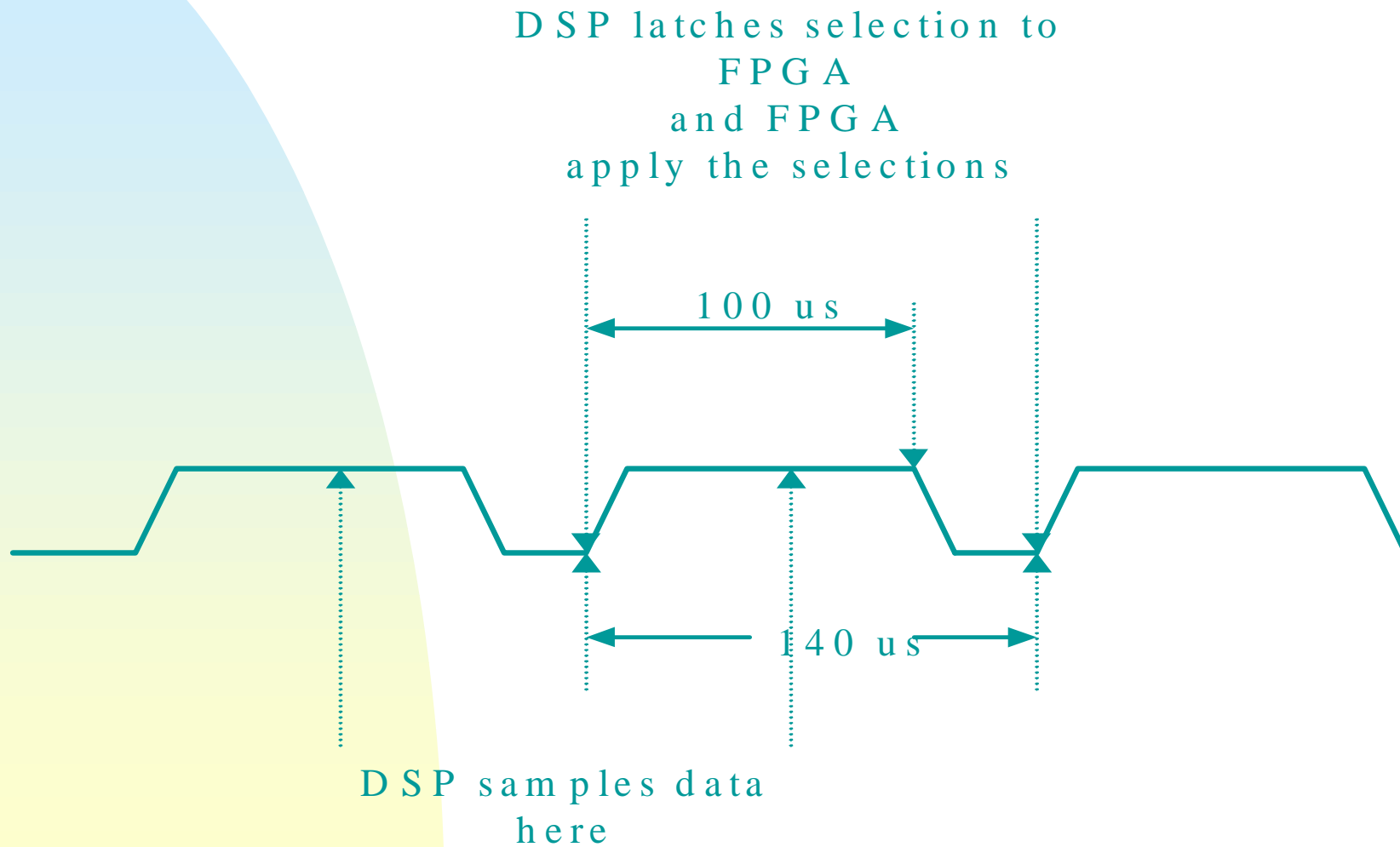
*Controls matrix
selection*



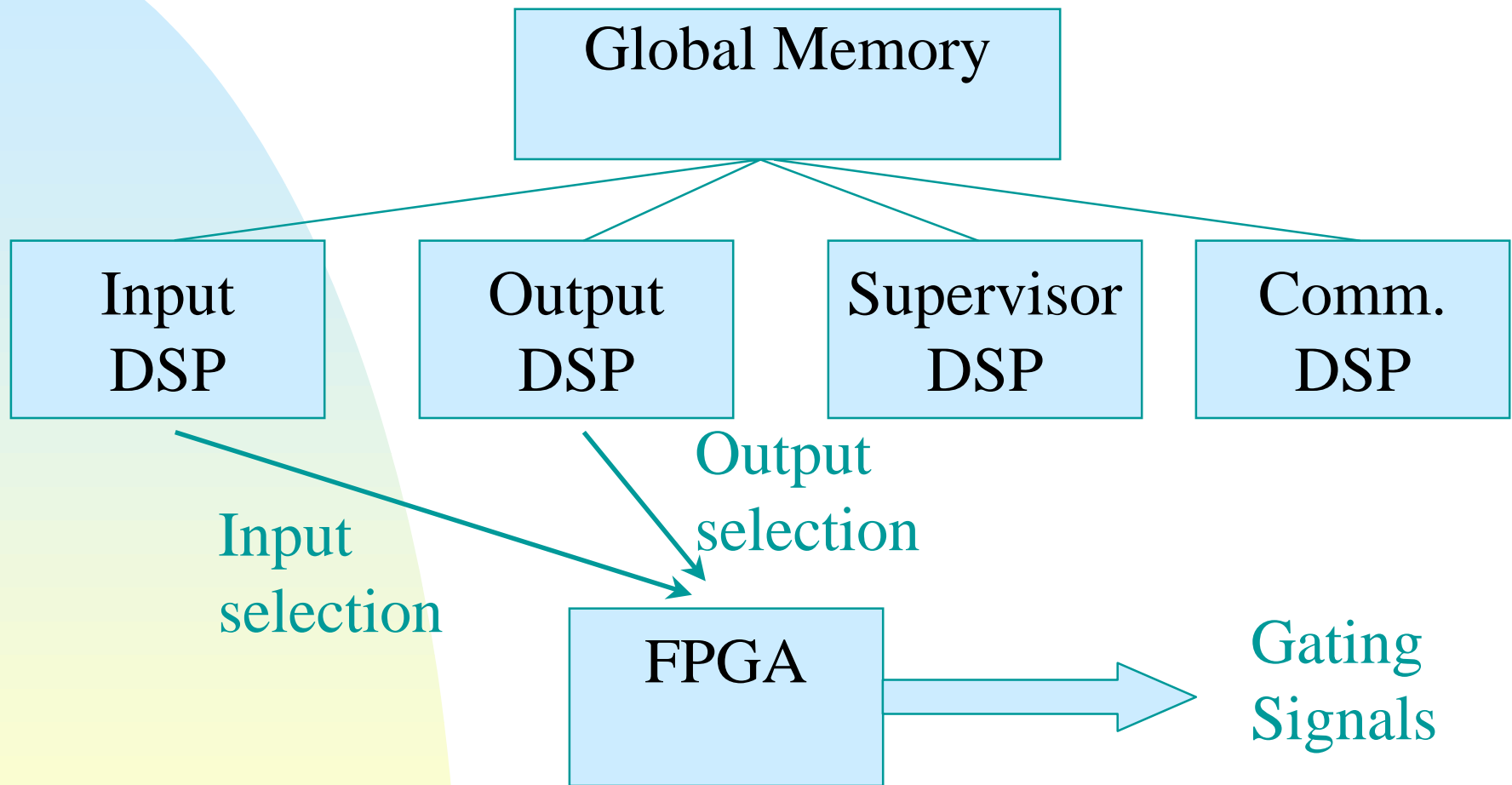
FPGA

*Controls devices
switching time*

Link Current Waveforms: 7.14 kHz



USRC Controller Structure

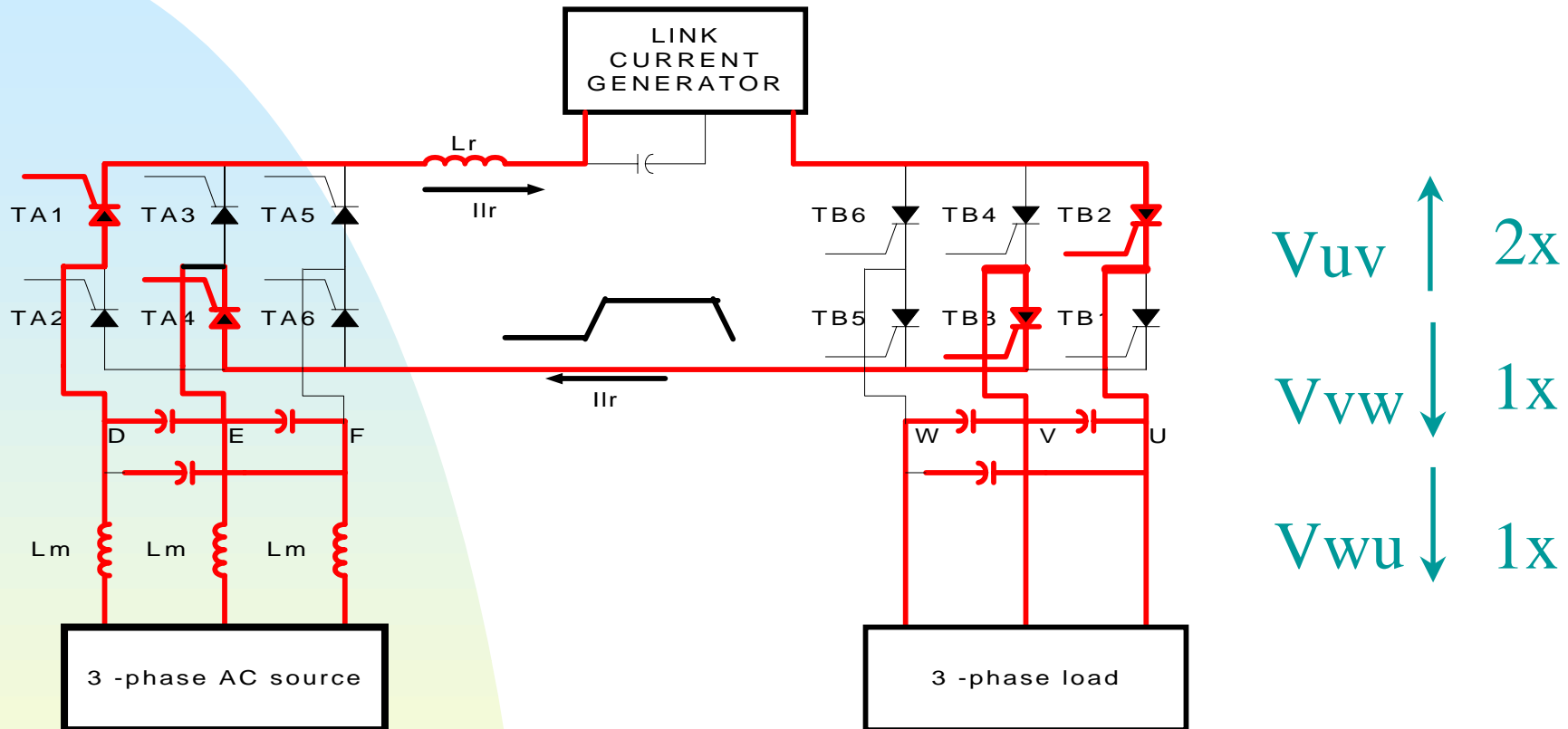


DSPs used : **TMS320C50 16 bit fixed point 80 MHz**

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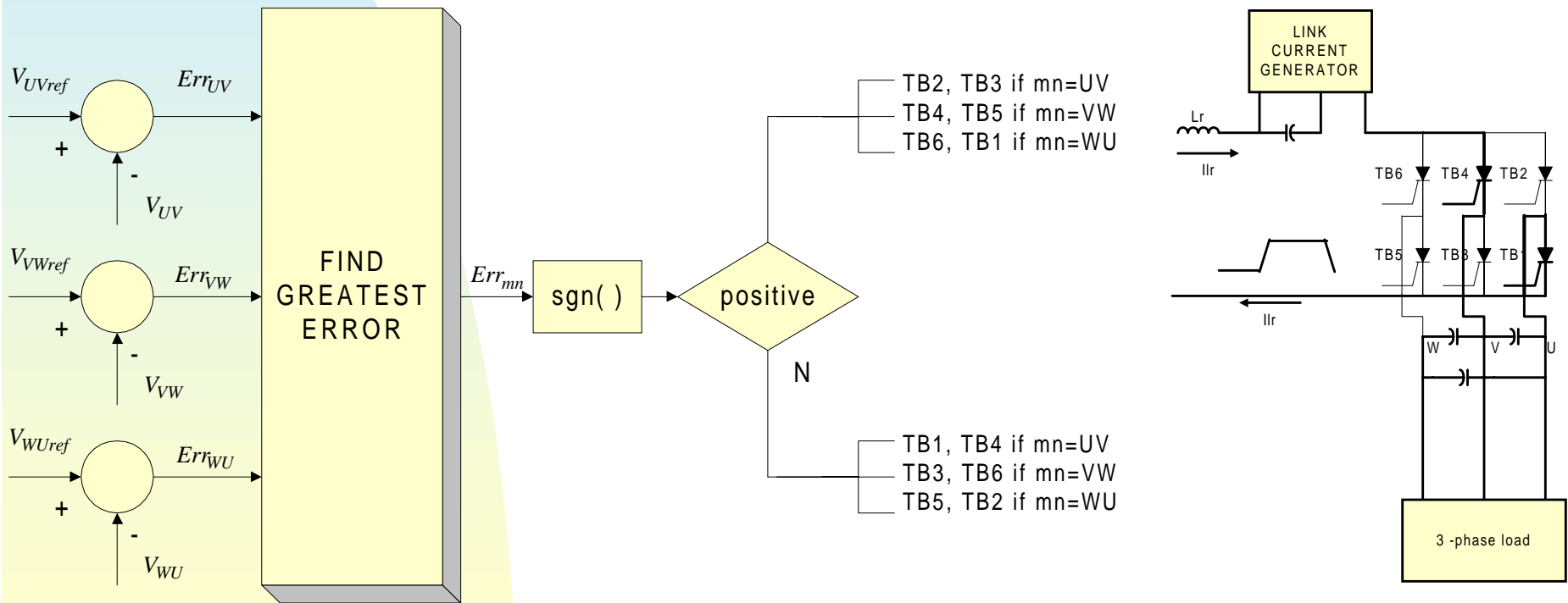
Principles of Operation



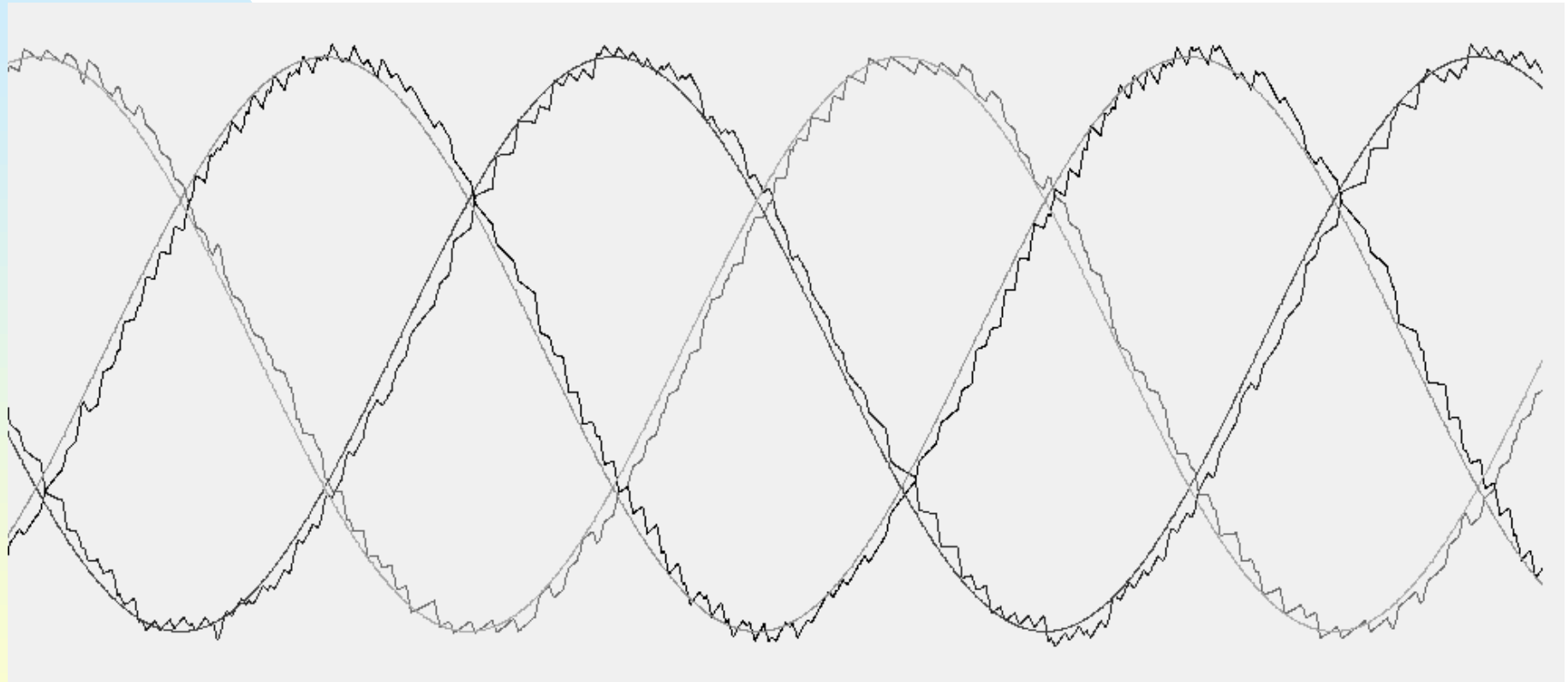
Based on charging-discharging of the filter capacitors

Output Control Example

- **Largest Error Algorithm:** Find phase with largest error and use the selection on that phase to correct the error.



Typical Output Voltages Waveforms



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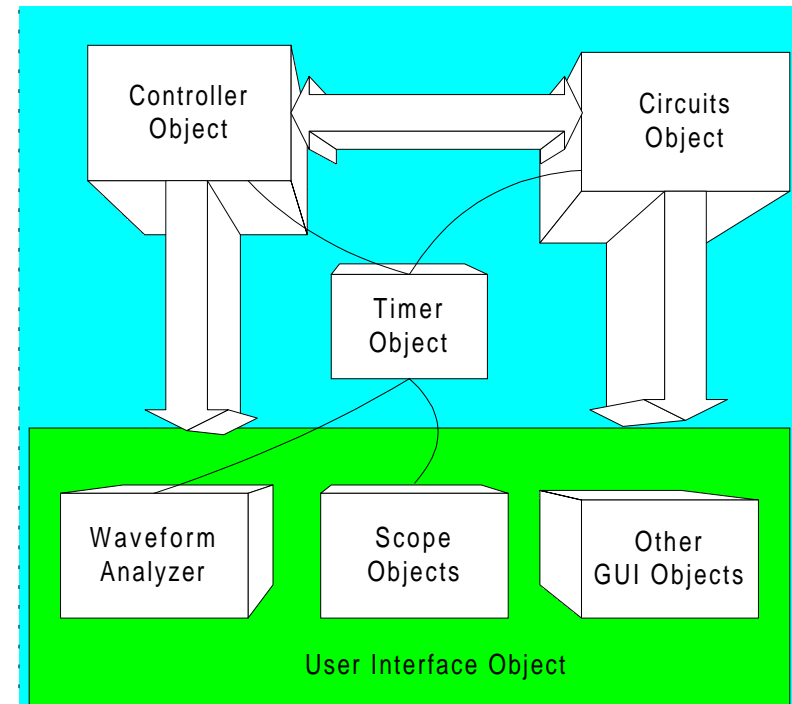
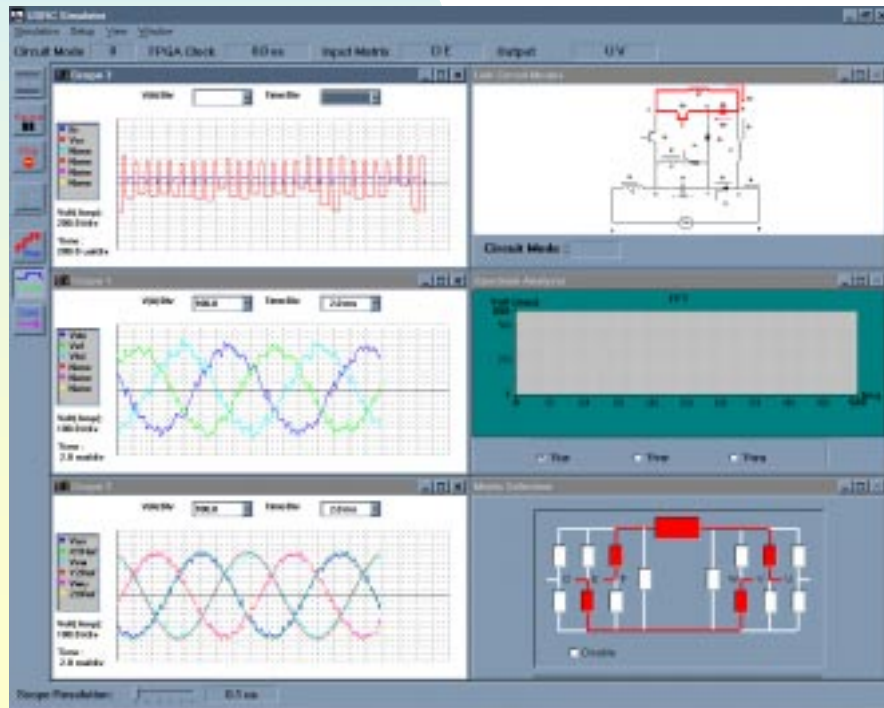
Virtual Test Bed

- A software test bed for rapid prototyping of the machine
- Simulates the machine as in the actual hardware implementation
- Capable of simulating the DSP native code for rapid evaluation of control algorithm
- Fast, user friendly, and easy to use



Virtual Test Bed for USRC

- Custom written software in C++ with object oriented Design and Windows 95 environment
- DSP-based system for controller's native code implementation



Why not general purpose simulator (MATLAB, PSPICE etc)?

- Speed
- Flexible accuracy
- Better handling of discontinuous events
- Cost
- Availability of Rapid Application Development: Borland C++ Builder, MS Visual C++



Virtual Test bed Graphical User Interface

The screenshot displays the USRC Simulator graphical user interface. At the top, the title bar reads "USRC Simulator" with standard window controls. Below the title bar is a menu bar with "Simulation", "View", "Sessions", "Setup", and "Window".

The main control area includes a toolbar with buttons for "End", "Continue", "Exit", "Run USRC", "Step", "Continuous", and "Cycle". To the right, there is a "Graphic Resolution" field set to "E:\dqout" and a "Push in to compile, Out means dont compile" checkbox. Below these are buttons for "Input", "Output", "Super", "Coms", "Evm", "DII", "RST", "Compile", "Set Paths", and "Editor".

The interface is divided into several panels:

- Meter:** A panel with a "Mode" dropdown set to "Normal Calc" and a "Normal" button. It contains a 3x3 grid of meters, each showing "None" and a value of "0.000".
- CircuitModeForm:** A panel showing a circuit diagram of a power converter. It includes a "Mode" dropdown set to "0" and an "FPGA Time" field set to "0.0". A "Continue" button is located below the FPGA time field.
- Scope:** A panel displaying a waveform plot. The "Signals" list on the left includes: 0: Ilb, 1: Vab, 2: Vde, 3: Id, 4: Vuv, 5: Iu, and 6: IlbRegA. The "Logic Mode" button is visible. The "Volt/Div" is set to "200.0" and the "Time/Div" is set to "4 ms".

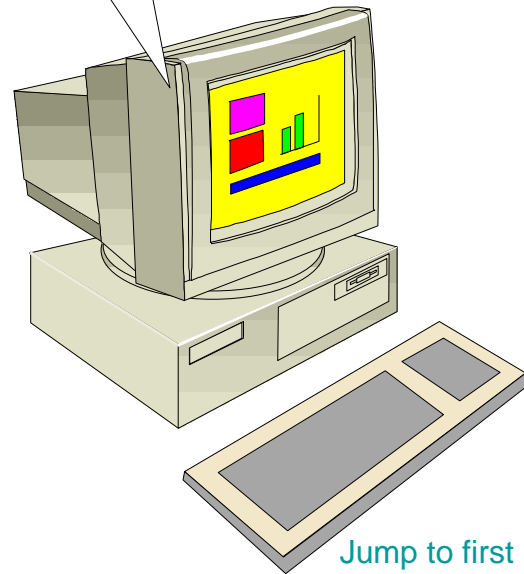
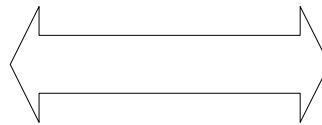
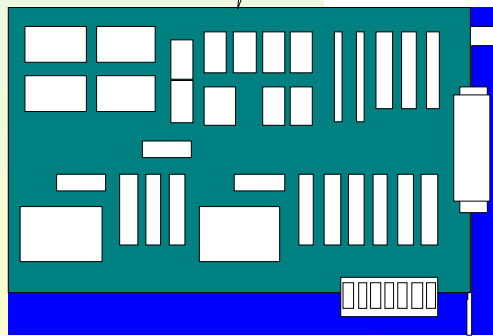
The Windows taskbar at the bottom shows the Start button, several open applications (pcA..., Micr..., Digit..., Lieb..., Usr...), the address bar with "e:\dqout\dspcodes\output", and the system tray with the time "8:32 PM".

DSP-based testbed for controller's native code simulation

- Allow quick test and evaluation of controller's native code in simulation environment

-Executes DSP native codes
- Communicates with simulator program on PC

-Runs simulation program including :
a. Circuit simulations
b. Analyzer
c. User Interface
-Controls the simulation timing



C5x Evaluation Module TI

DSP controller bo

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Conclusions

- Preliminary Concepts for the Development of a Virtual Learning System
- Detailed Development of a Virtual Test Bed for the Design and Control of a Power Converter
- Multi-Purpose Applications



Conclusions

USRC provides efficient power transfer suitable for high power applications

Virtual Test bed for USRC allows rapid prototyping of control algorithm and performance evaluation of the machine

