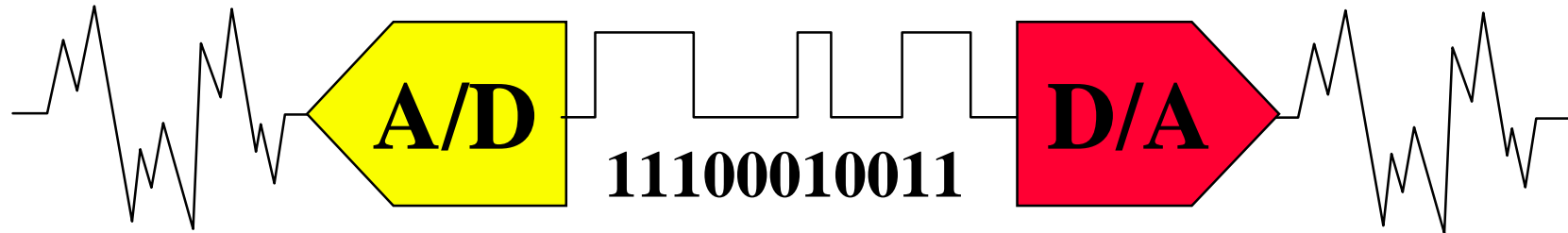


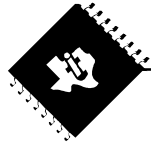


Data Converters

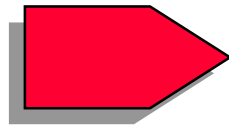


Bridging the Analog & Digital Worlds

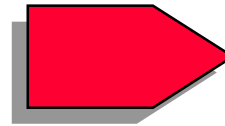
CommsDAC Quick Product Overview



THS56x1
8-14 bit
100 MSPS
RTP now

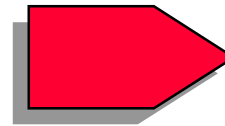


CMOS



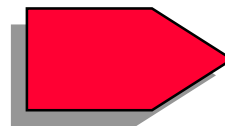
THS56x2
10-14 bit, dual-channel
50/100 MSPS
low power, low cost

CMOS



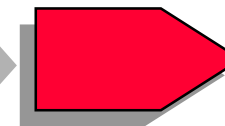
THS56x3
10-14 bit
140 MSPS
Enhanced SFDR

BiCMOS



THS56x5
10-14 bit
400 MSPS
Single-IF, LVDS

SiGe



THS56..
10-14 bit
400-800 MSPS
Bandpass interpolator

TI's New Low Power DAC Family



New TLC/TLV56xx 10-Bit Family

Device	No. of DACs	Settling Time	Clock Rate	Power Dissipation	Internal Voltage Ref.	Serial/Parallel Interface
TLC5615	1	12.5 μ s	20 MHz	1.15 mW	No	serial
TLC5617A	2	12.5 / 2.5 μ s	20 MHz	3 / 8 mW	No	serial
TLV5604	4	8.5/2.5 μ s	20 MHz	3 / 9 mW	No	serial
TLV5637*	2	3 / 1 μ s	20 MHz	6 / 15 mW	Yes	serial

New TLC/TLV56xx 12-Bit Family

Device	No. of DACs	Settling Time	Clock Rate	Power Dissipation	Internal Voltage Ref.	Serial/Parallel Interface
TLV5616	1	9 / 3 μ s	20 MHz	0.9 / 2.1 mW	No	serial
TLV5613	1	3.5 / 1 μ s	---	1.2 / 4.2 mW	No	parallel
TLV5619	1	1 μ s	---	4.3 mW	No	parallel
TLC5618A	2	12.5 / 2.5 μ s	20 MHz	3 / 8 mW	No	serial
TLV5614	4	9 / 3 μ s	20 MHz	3.6 / 9.6 mW	No	serial
TLV5636	1	3 / 1 μ s	20 MHz	5 / 10mW	Yes	serial
TLV5638	2	3 / 1 μ s	20 MHz	6 / 15mW	Yes	serial
TLV5633	1	3 / 1 μ s	---	10 / 20 mW	Yes	8+4 bit parallel
TLV5639	1	3 / 1 μ s	---	10 / 20 mW	Yes	12 bit parallel

TLV320AIC10 Performance/Features



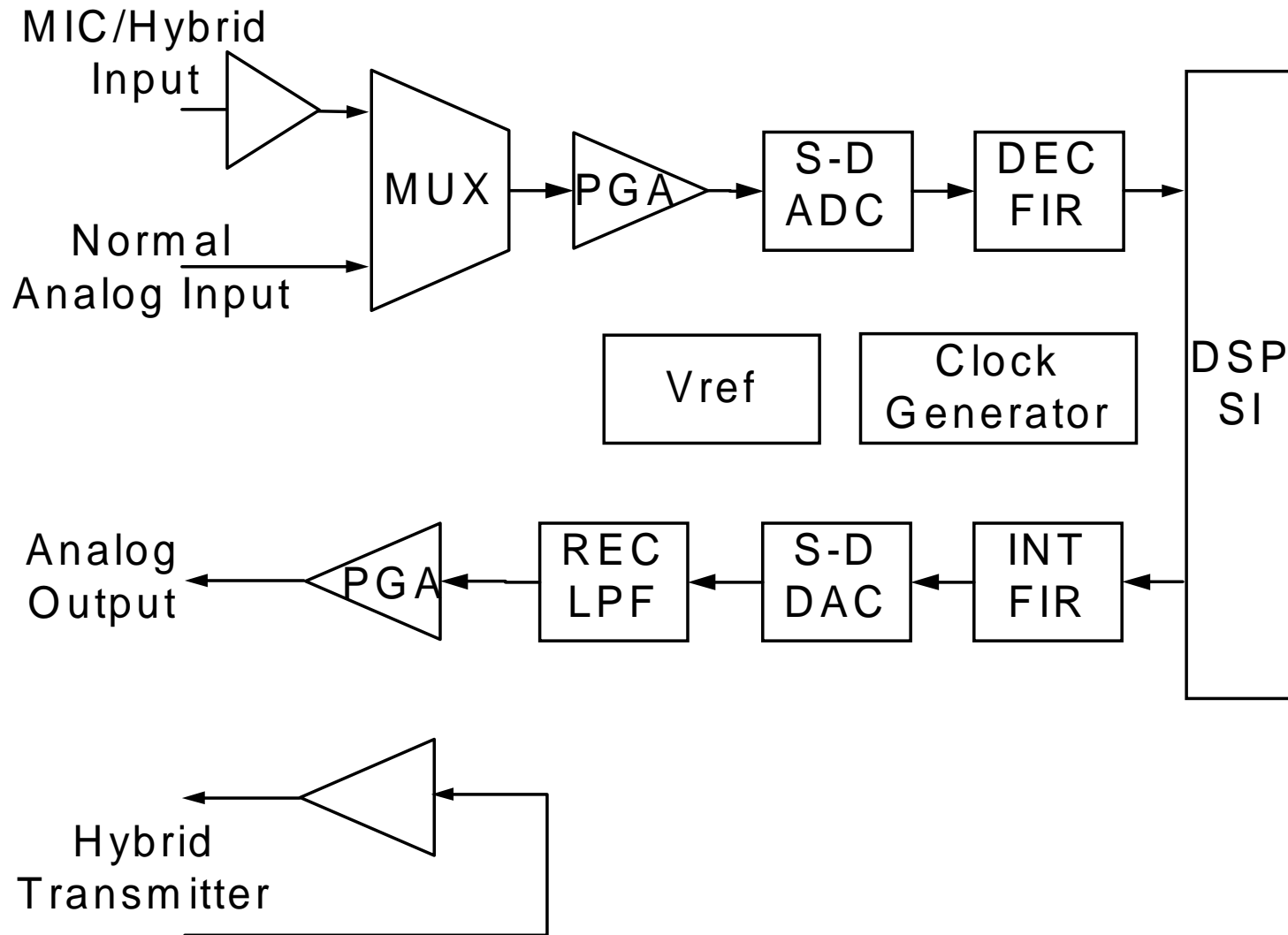
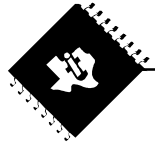
- ◆ **Glueless SI to TI DSP**
- ◆ **Support SPI**
- ◆ **Bypassable On-chip FIR**
- ◆ **Programmable Sampling Rate**
- ◆ **PGA**
- ◆ **Built-in Anti-Alias Filter**
- ◆ **Built-in MIC interface**
- ◆ **Built-in Hybrid Interface**
- ◆ **Low Power (48mW@8Ksps)**

TLV320AIC10 Performance/Features



- ◆ **Cascade**
 - **ACD makes cascade programming simple**
 - **Support up to 01 Master and 07 Slaves**
- ◆ **On-fly Reconfigure**
 - **Direct Communication Protocol**
 - **HW/SW Request Secondary Communication Protocol**
- ◆ **Continuous Data Transfer**
- ◆ **Power Supply**
 - **3.3V-5.5V Analog**
 - **3.3V-5.5V Digital**

Typical AIC Block Diagram



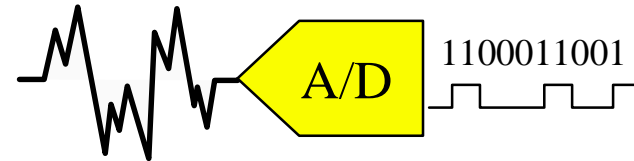
12 Bit 65 MSPS IF Sampling Communications A/D



Features

- ◆ 65 MSPS Max Sample Rate
- ◆ 12 Bit Resolution
- ◆ Single 5 V Supply
- ◆ No Missing Codes
- ◆ On Chip T/H and Reference
- ◆ 68dB SNR
- ◆ 77 dB TYP. Spurious Free Dynamic Range
- ◆ 270 MHz Bandwidth Differential Analog Input

TLV1265



Schedule

- ◆ Samples- June/99
- ◆ Production - Dec/99

Applications

- ◆ Cellular/PCS Base Stations
- ◆ Communications Receivers

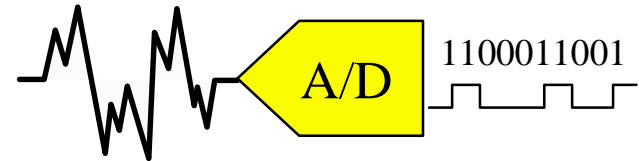
14 Bit 70 MSPS IF Sampling Communications A/D



Features

- ◆ 70 MSPS Sample Rate
- ◆ 14 Bit Resolution
- ◆ No Missing Codes
- ◆ On Chip T/H and Reference
- ◆ 78dB SNR
- ◆ 95 dB Spurious Free Dynamic Range
- ◆ 500MHz Bandwidth Differential Analog Input

TLV1470



Schedule

- ◆ Samples- Aug./99
- ◆ Production - Dec./99

Applications

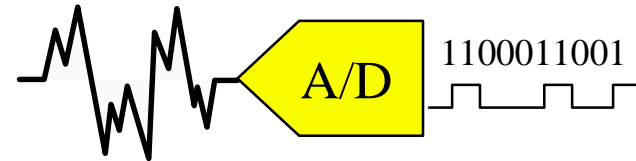
- ◆ Cellular/PCS Base Stations
- ◆ Communications Receivers

14 Bit Evaluation Board With Digital Mixer and Filter



Features

- ◆ 70 MSPS Sample Rate
- ◆ 2, 3 or 5 stage CIC filter
- ◆ Digital Mixer with NCO
- ◆ Decimating user definable FIR filters
- ◆ Multi-stage decimating filter reduces power consumption
- ◆ Synchronized multi-receiver frequency hop
- ◆ High speed C6202 Interface
- ◆ 32 Mbit/sec serial DDC-DSP interface
- ◆ 30Mword/sec parallel FIFO DDC-DSP interface



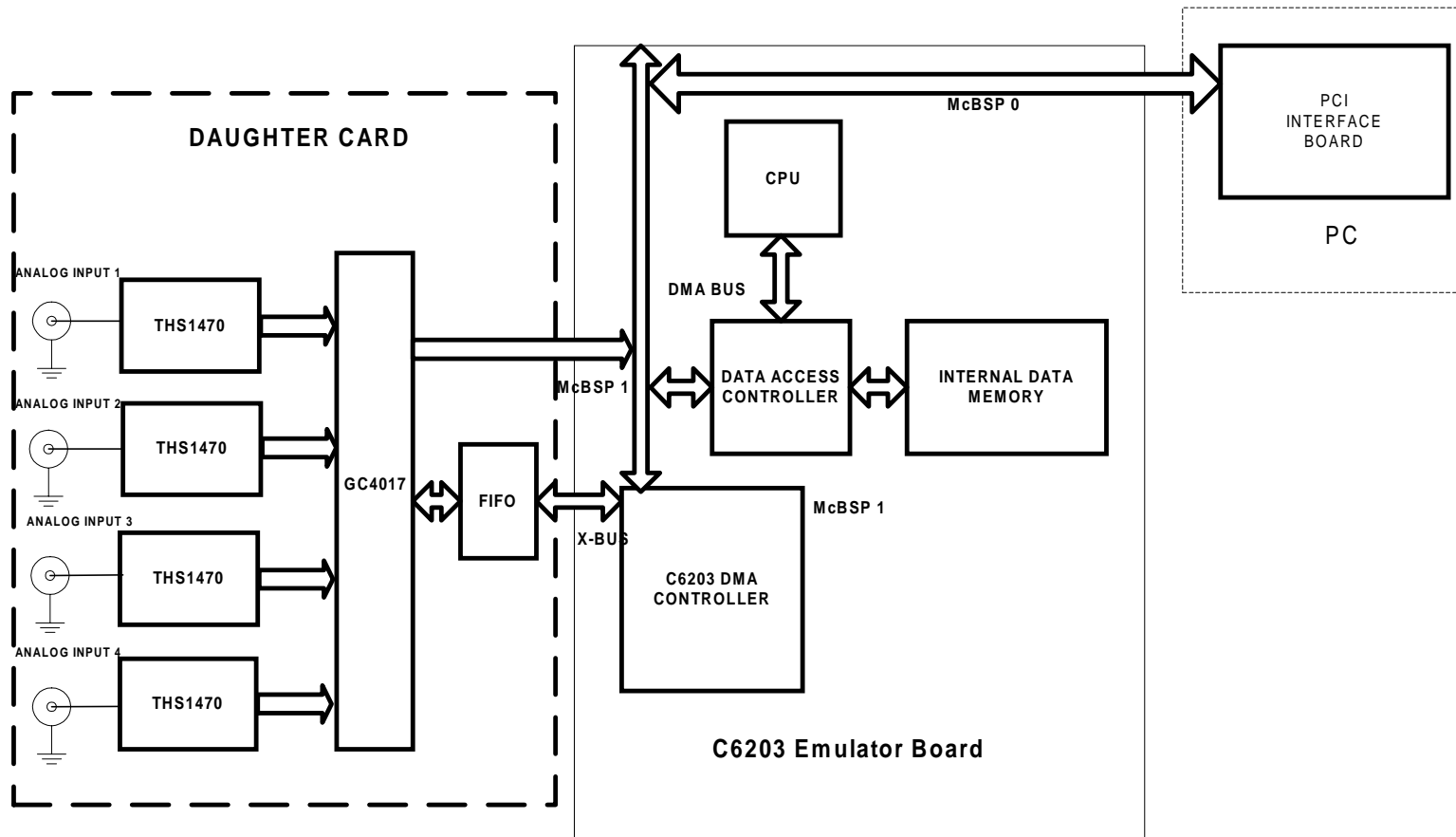
Schedule

- ◆ Sample - Sept. / 99

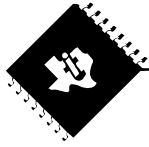
Applications

- ◆ Cellular/PCS Base Stations
- ◆ Communications Receivers

IF / BASE-BAND REFERENCE DESIGN



IF / BASE-BAND DEMO



AGC Stage for THS1470AGC

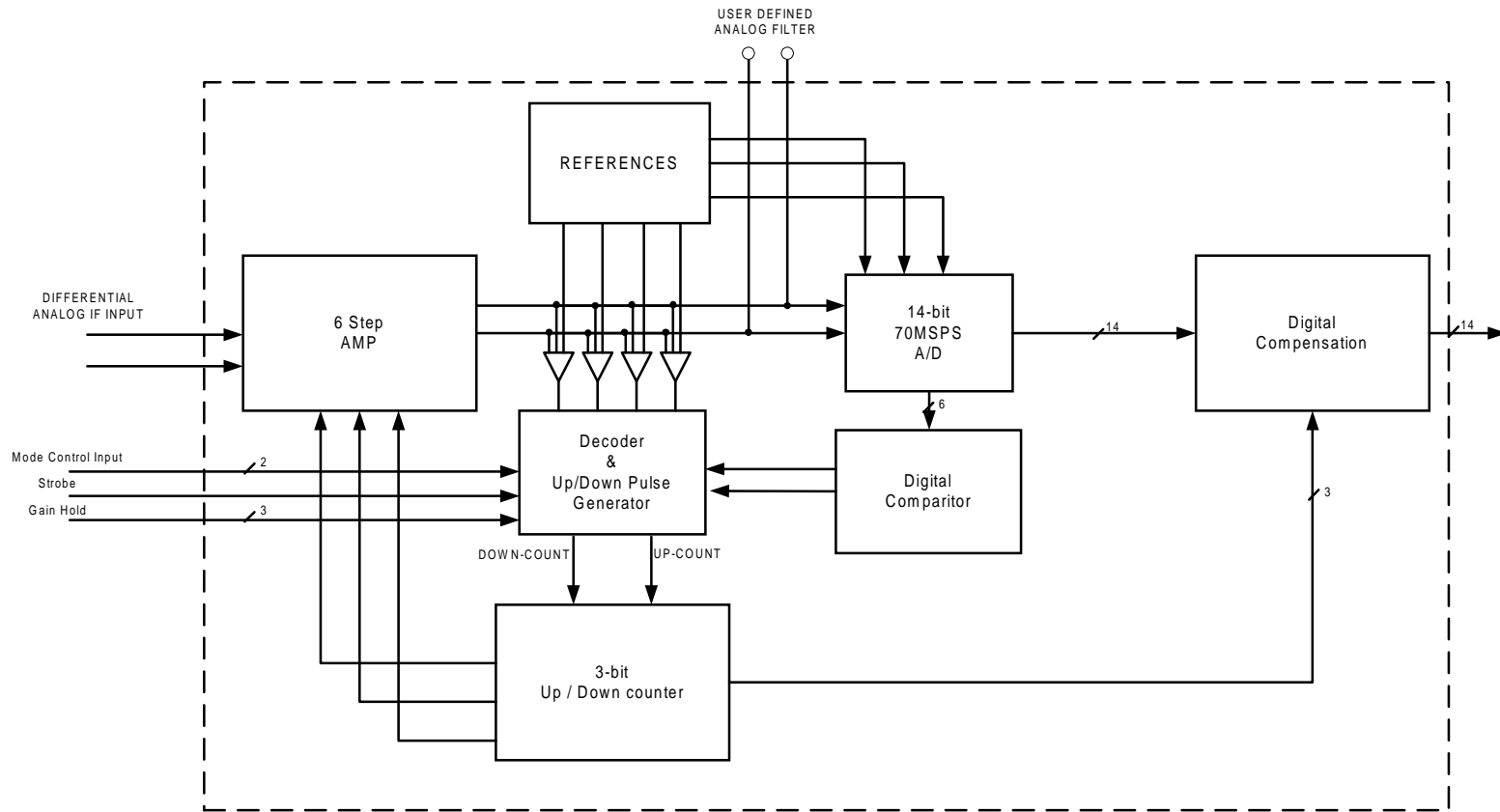


Fig.1 AGC AMPLIFIER and 14-BIT ADC