TI’s PCI2040
PCI-to-DSP Bridge

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Agenda

- Introduction to the PCI Bus
- DSP Host Port Interface (HPI) Overview
- What is a PCI-to-DSP Bridge?
- The PCI204x Family of PCI-to-DSP Bridges
- PCI2040 PCI-to-DSP Bridge Overview
- PCI2040 Evaluation Module (EVM)
- Questions & Answers
Introduction to the PCI Bus

- Ubiquitous local bus in PCs today (ISA bus is fading)
- Processor-independent bus
- Most slots are 5-V, 32-bit, 33-MHz with support for 3.3-V, 64-bit and 66-MHz operation
- Supports Plug and Play operation (no jumpers required)
- Central arbiter with support for multiple bus masters
- Master initiates transaction and slave is the target
- Various types of transactions (configuration, memory, I/O)
- Multiplexed addr/data bus with synchronous transfers
- Address phase followed by one or more data words (burst support)
- Level-sensitive interrupts enable interrupt sharing
- Compact PCI for industrial applications based on PCI with 3U/6U form factors and support for hot swapping
**DSP Host Port Interface (HPI)**

- 8 or 16-bit interface for host/DSP data transfers (depending on DSP)
- The host is always the master (DSP cannot initiate transfers)
- Host can read and write DSP memory
- C54x HPI transfers to/from fixed 2Kword on-chip memory or anywhere in on-chip memory depending on specific device
- C6x HPI transfers to/from anywhere in the DSP memory space
- HPI can be used for program and data downloads from host
- Host accesses DSP memory using (3) HPI registers in DSP
  - HPI control (HPIC) register - Provides control and status bits
  - HPI address (HPIA) register - Selects DSP memory address for transfer
  - HPI data (HPID) register - Contains data read from DSP or data to write to DSP
- HPI supports consecutive data transfers with auto-inc addressing to reduce overhead during block transfers with 4th “pseudo” register
What is a PCI-to-DSP Bridge?

◆ Device which provides a glueless connection between the PCI bus and one or more DSPs
  ◆ DSP-specific - optimized for data transfers with the DSP
  ◆ No external logic required to use general-purpose PCI controller/bridge
  ◆ Single-chip PCI interface solution and data pipe between host/DSP

◆ DSP interface is typically via HPI, but may also support memory I/F

◆ Optional support for other memory-mapped devices on DSP board
  ◆ JTAG test bus controller
  ◆ FIFO memory
  ◆ Programmable logic device
  ◆ Other peripheral devices
**TI’s PCI204x Family**

- Family of PCI-to-DSP bridges
- Glueless interface solutions to TMS320C54x/62x DSPs
- Fully compliant to the latest PCI specifications
- Useful in a variety of applications that use multiple DSPs
- First family member is the PCI2040 target-only device
- Future devices to support new DSPs, more DSPs and other features such as bus mastering
PCI2040 Overview

- Specification Compliance
  - PCI Local Bus Specification 2.2
  - PCI Bus Power Management Interface Specification 1.1
  - CompactPCI Hot Swap PICMG 2.1 R 1.0 Specification
- Supports 3.3-V and 5-V, 32-bit, 33-MHz PCI buses
- Supports up to four DSP devices via HPI interface
- DSPs Supported: C54x, C6201, C6211, C6701
- Target (slave) device
- Low-cost at about $9 (1000)
PCI2040 Overview

◆ Glueless connection to configuration serial EEPROM
  ◆ Class Code
  ◆ Subsystem Vendor and Device IDs
  ◆ HPI implementation and width selection

◆ 16-bit general-purpose bus (GP bus)
  ◆ Host can access on-board memory and peripherals via PCI bus
  ◆ Supports glueless connection to JTAG Test Bus Controller

◆ Six general-purpose I/O pins

◆ Bidirectional interrupt support
PCI2040 Description

- The PCI2040 is a PCI bus device that provides glueless connectivity to Texas Instruments TMS320C54x and TMS320C6x families of DSPs.

- The device allows the connection of up to four DSPs to the PCI bus via the Host Port Interface (HPI) on the DSP:
  - PCI2040 provides chip selects that uniquely select each DSP’s HPI port
  - Four sets of control signals (chip select, reset, interrupt and ready)

- By this means, the PCI2040 can be used in a variety of applications that use multiple DSPs where there is a need for a high-speed data transmission solution.
PCI2040 Block Diagram

- PCI Power Management
- Serial EEPROM Interface
- HPI Registers & PCI Registers
- 8-bit or 16-bit Host Port Interface
- GPIO
- General Purpose Bus Interface

PCI2040

DSP

CompactPCI Hot Swap

PCI Bus Interface

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PCI2040 Features & Benefits

**Features**
- PCI Local Bus Specification 2.2
- PCI Bus Power Management Interface Specification 1.1
- CompactPCI Hot Swap Specification 1.0 compliant
- Supports up to four DSP devices on HPI interface
- Includes serial EEPROM interface
- General-purpose bus and six I/O pins
- 3.3-V core logic with universal PCI interface compatible with 3.3-V or 5-V signaling environments
- 144-pin device and choice of packaging:
  - Quad flat package (QFP)
  - Chip scale packaging (Microstar™ BGA)

**Benefits**
- Ensures highest level of compatibility and compliance
- For power-sensitive designs
- Enables inserting and removing printed circuit boards without effecting a running system
- Provides flexibility for a number of C54x and C6x DSP designs
- Simple and direct method for loading subsystem ID and subsystem vendor ID
- Supports on-board peripheral devices including glueless interface to JTAG TBC
- Supports current and legacy PCI bus designs
- Minimizes board size without increasing number of board layers
PCI2040’s DSP Memory Mapping

Address Bit Selection

<table>
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<tr>
<th>AD31</th>
<th>...</th>
<th>AD15</th>
<th>AD14</th>
<th>AD13</th>
<th>AD12</th>
<th>AD11</th>
<th>AD10</th>
<th>...</th>
<th>AD0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control Space Base Address</td>
<td>CS1</td>
<td>CS0</td>
<td>CT1</td>
<td>CT0</td>
<td>Not Decoded (Don’t Care)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

C54x

- 0x0000: HPI Control Register
- 0x0800: HPI Data (Auto-Inc) Register
- 0x1000: HPI Address Register
- 0x1800: HPI Data Register

C6x

- HPI Control Register
- HPI Address Register
- HPI Data (Auto-Inc) Register
- HPI Data Register

32 Kbyte Memory Window
Hot Swap Support

- *Hot swap* defines a process for installing and removing CPCI boards without adversely affecting a running system
- The PCI2040 is hot-swap friendly silicon
  - Compliant with Hot Swap specification R1.0
  - Tolerant of Vcc from early power
  - Asynchronous reset
  - Tolerant of precharge voltage
  - I/O buffers meet modified V/I requirements
  - Limited I/O pin voltage at precharge voltage
  - Hot swap control and status programming
- Hot swap pins: HSENUM-, HSSWITCH, HSLED
Power Management Support

- *Power management* consists of four device states that reduce power consumption

- The PCI2040 supports power management
  - Compliant with Power Management specification 1.1
  - Supports all four states (D0-D3)
  - D0 is fully operational state
  - Power reduction by disabling HPI state machine in D1-D3
  - D3 to D0 state does not reset all internal states
  - PME- pin provides indication of power management event to host processor when external interrupt received
PCI2040 Documentation

◆ PCI2040 PCI-DSP Bridge Controller Data Manual (SCPS048)

◆ PCI2040 Implementation Guide

◆ PCI2040 Application Notes
  ◆ Interfacing To TMS320C54x or TMS320C6x DSP’s to a PCI Bus Using the TI PCI2040 PCI-to-DSP Bridge
  ◆ Interfacing the PCI2040 to the TMS320C5420 DSP

◆ TI Web Site URL
PCI2040 EVM

Support Software

→ Code Composer Studio Driver
→ Windows 9x and NT 4.0 Drivers
→ Windows 9x Wave Device Driver
→ Win32 User-Mode DLL API
→ COFF Application Loader Utility
→ Board Control Utility
→ Board Confidence Test Utility
→ Host File I/O Support
→ CPLD and EEPROM Programming Utilities
→ Example Host/DSP Source Code

PCI2040 PCI-DSP Reference Design
→ 100 MHz TMS320VC5410 DSP
→ 64 kW Internal SRAM
→ 64 kW Program SRAM (256 kW option)
→ 64 kW Data SRAM (256 kW option)
→ Stereo, 8-96 kHz, 16-bit Audio Codec
→ Mic & Line In/Out
→ JTAG Debugging via PCI Bus or XDS510
→ Memory & Peripheral Expansion Connectors
→ Supports 32-bit, C6x EVM Daughterboards

TI Ordering #: PCI2040EVM
Contact local TI sales office or
TI Product Information Center
(972) 644-5580

→ 100 MHz TMS320VC5410 DSP
→ 64 kW Internal SRAM
→ 64 kW Program SRAM (256 kW option)
→ 64 kW Data SRAM (256 kW option)
→ Stereo, 8-96 kHz, 16-bit Audio Codec
→ Mic & Line In/Out
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Summary

→ TI is committed to providing PCI-to-DSP bridge solutions with their new PCI204x family

→ The PCI2040 is available now
  → 3.3/5V, 32-bit, 33-MHz
  → Supports up to four C54x and/or C6x DSPs
  → Target device

→ The PCI2040 EVM provides a low-cost reference design and development/evaluation platform

→ TI has made it easier to design PCI/CPCI boards based on TI DSPs