TECHNOLOGY IN THE INTERNET ERA

Dennis Buss
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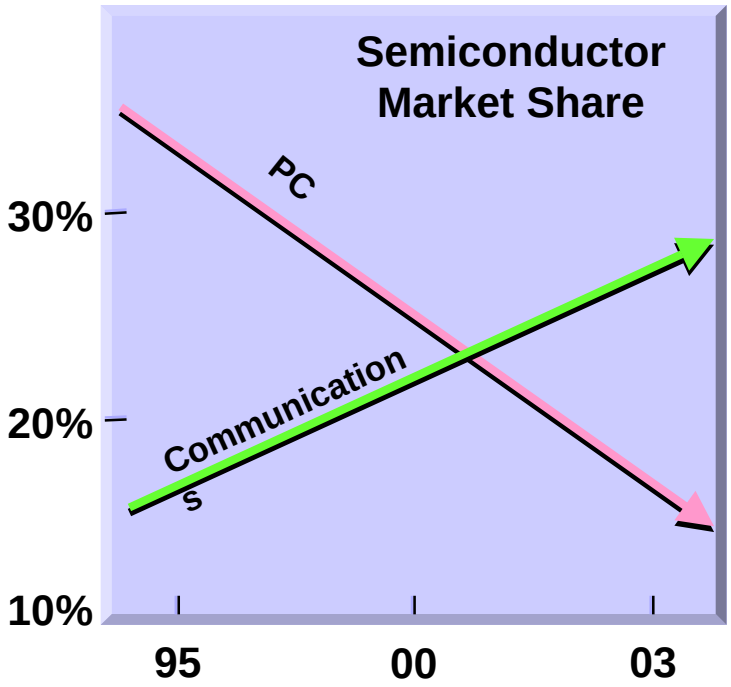
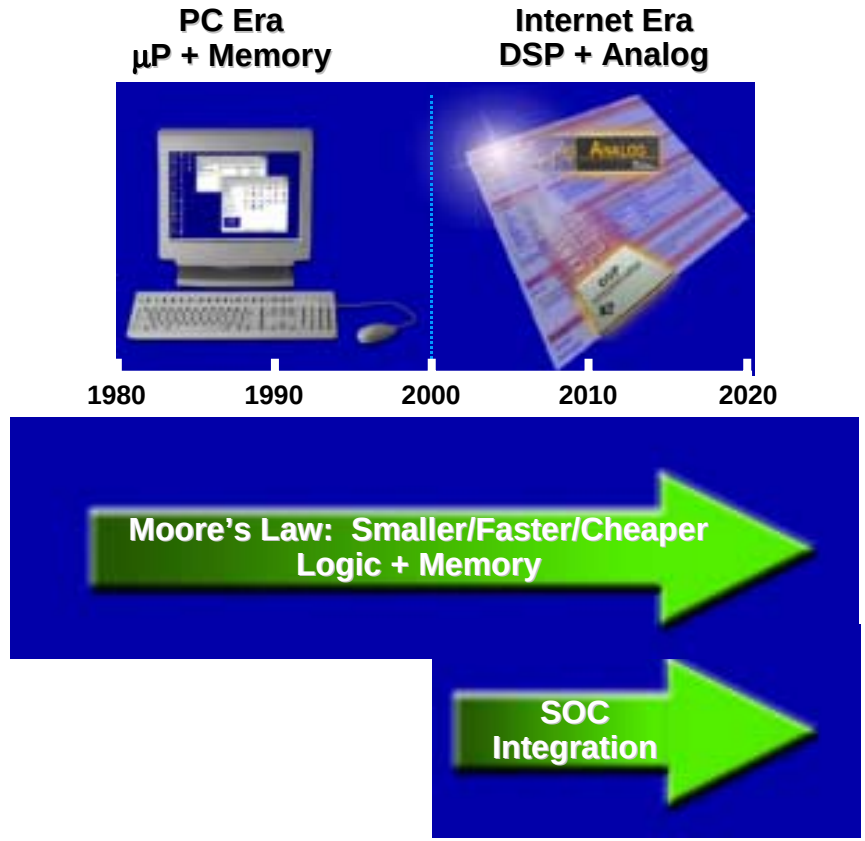
Dallas, Texas

SOC INTEGRATION IN INTERNET ERA

DSPS Fest 2000

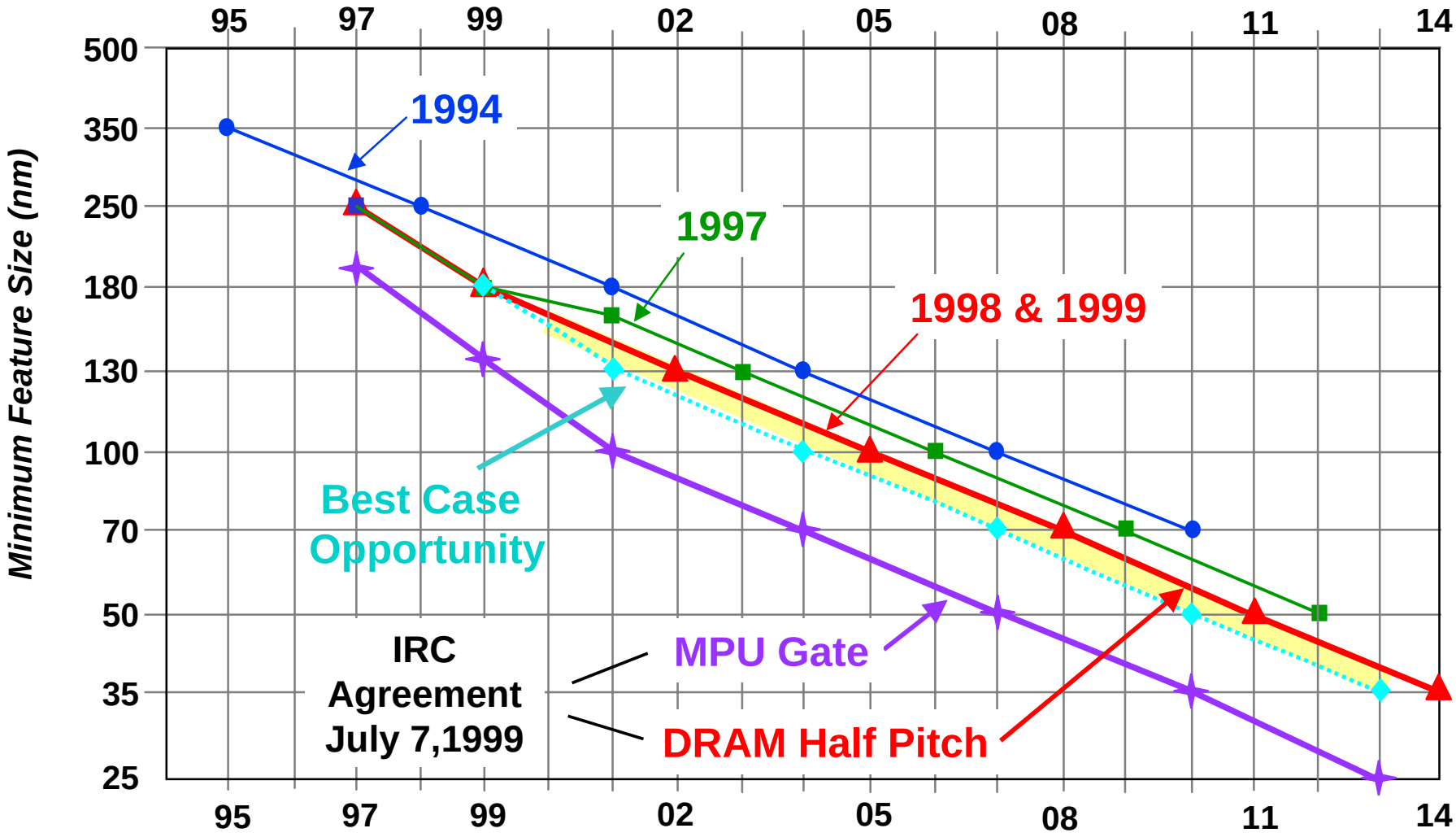
Dawn of Internet Era





Transistor Scaling will continue to be an important Technology Driver in the Internet Era. But it will no longer be the sole driver: SOC Integration will be increasingly important.

CMOS Scaling Roadmap (ITRS'99)



DSP Integration Through the Years

Typical Device Capabilities

	1980	1990	2000	2005	2010
Die size (mm)	• 50	• 50	• 50	• 50	• 50
Technology (μm)	• 3	• 0.8	• 0.18	• 0.05	• 0.01
MIPS	• 5	• 40	• 2000	• 20K	• 50K
MHz	• 20	• 80	• 500	• 2,000	• 10,000
RAM (bytes)	• 256	• 2K	• 32K	• 5M	• 10M
Price	• $150.00	• $15.00	• $1.50	• $1.50	• $1.50
Power (mW/MIPS)	• 250	• 12.5	• 0.1	• 0.01	• 0.001
Transistors	• 50K	• 500K	• 5M	• 50M	• 100M
Wafer size	• 3”	• 6”	• 12”	• 12”	• 12”

Gene Frantz, IEDM 99

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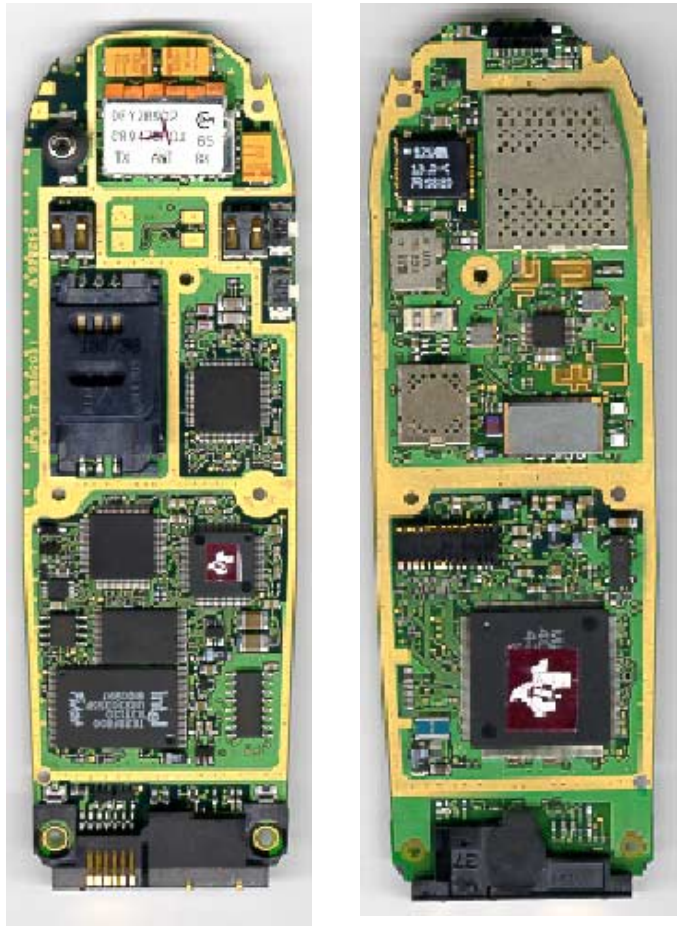
Today's Cell Phone

ICs	12
Discretes	16
Passives	214
Other	8
Total	250



- Transistor scaling is not the most significant enabler for cost reduction
- SOC integration requires technologies for
  - DSP
  - SRAM
  - FLASH
  - Radio RF/IF
  - Analog functions
  - Power management

TECHNOLOGY IN THE INTERNET ERA

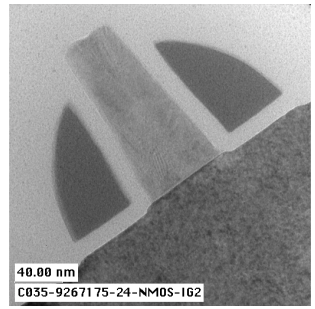
DSPS Fest 2000

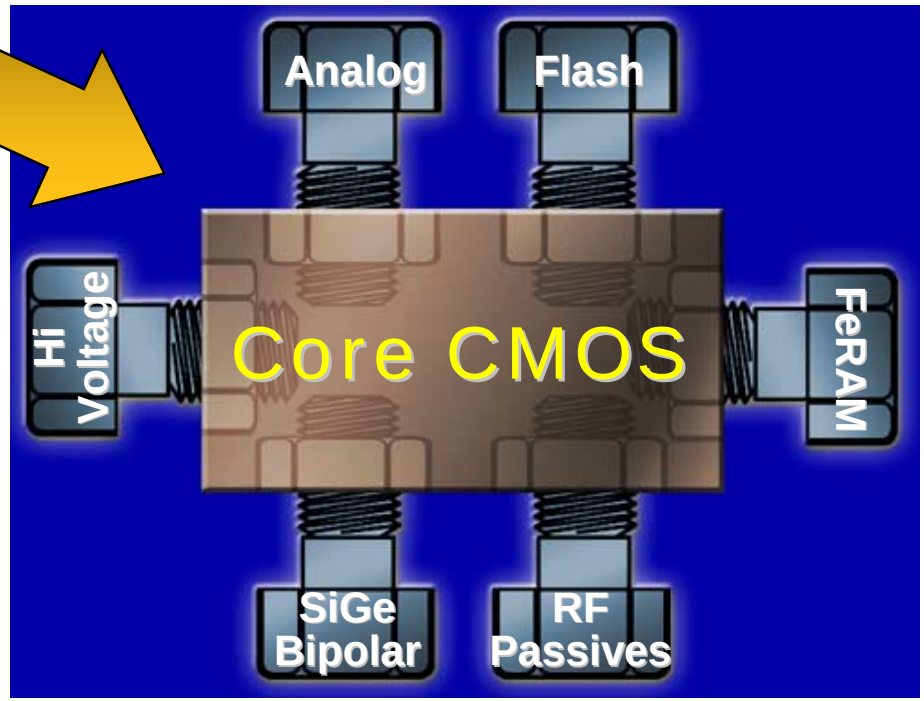
Leaders On Moore's Law Curve

0.18µm Generation
- 0.18µm Since Sept. 99
- 0.13µm Currently
- Cu in Sept. 00

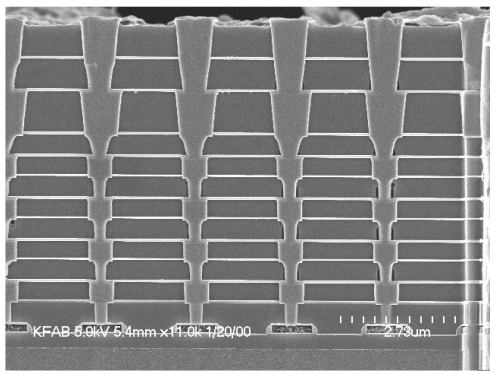
0.13µm Generation
- 0.11µm in March 01
- 0.085µm in June 01
- SOI in June 02

70nm TRAN





Differentiated Technology for SOC Integration



Six Level Cu Interconnect

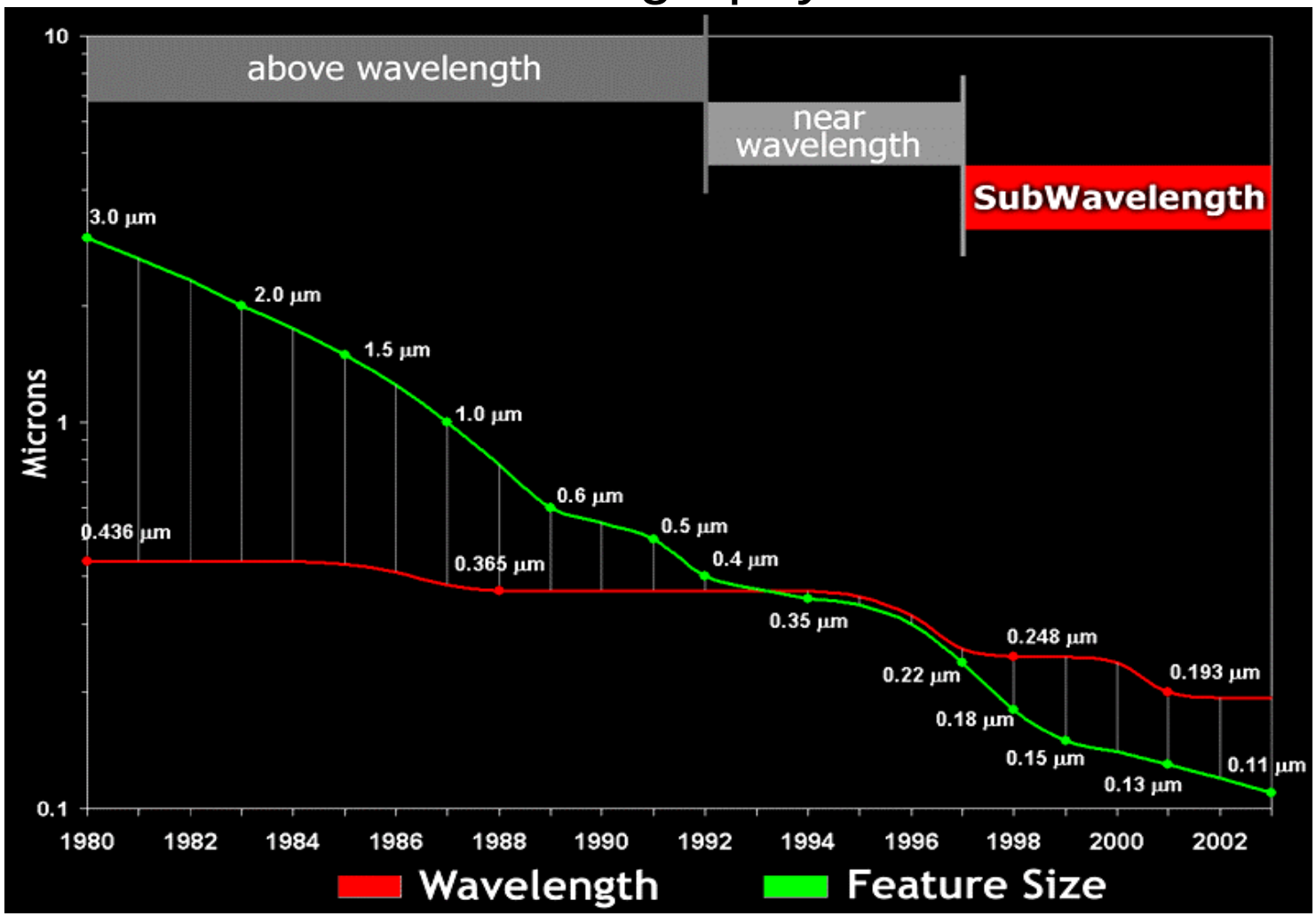
TECHNOLOGY IN THE INTERNET ERA

AGENDA

- Introduction
- Grand Challenges of Scaling
- SOC Integration
- TI Strategy

TECHNOLOGY IN THE INTERNET ERA

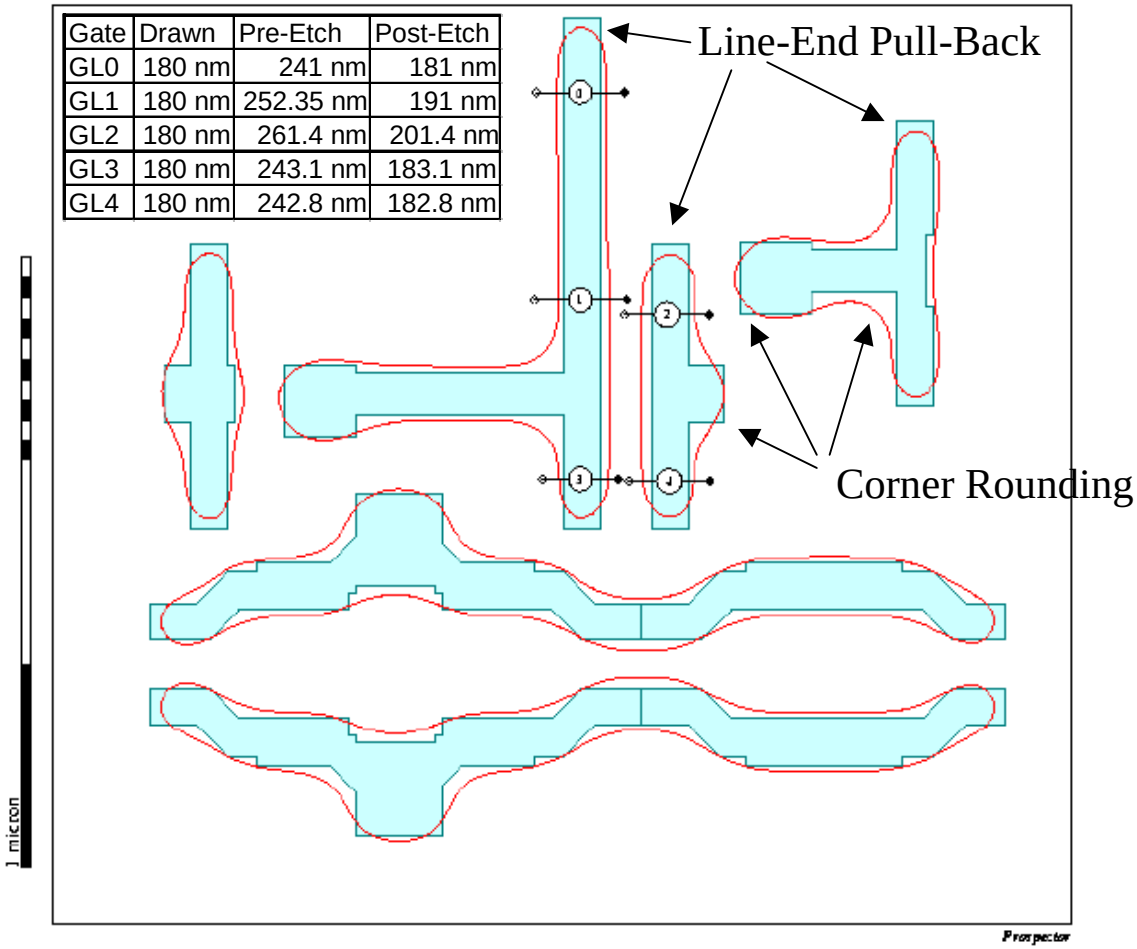
Lithography



TECHNOLOGY IN THE INTERNET ERA

Lithography Beyond the Wavelength of Light

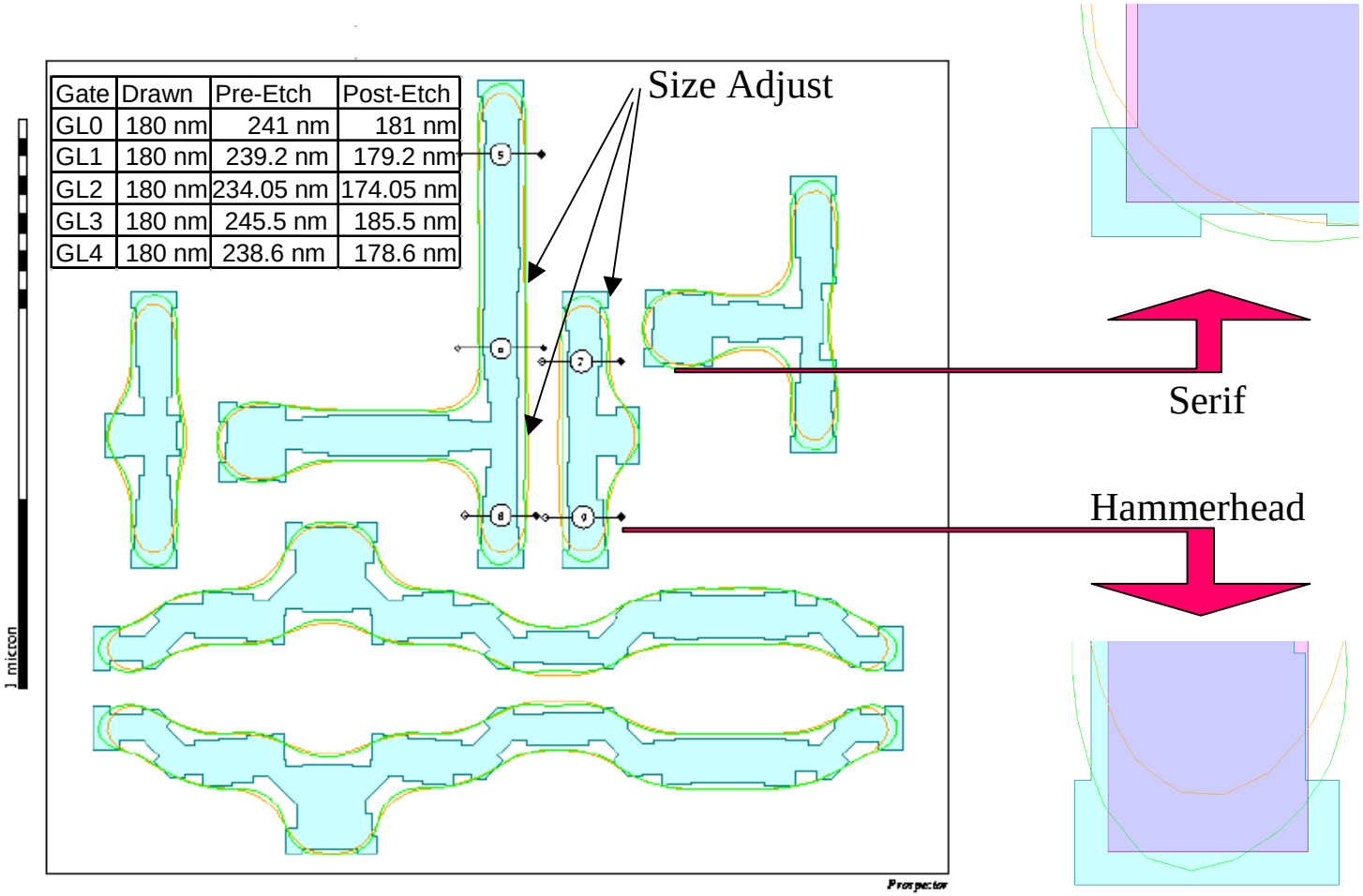
Gate	Drawn	Pre-Etch	Post-Etch
GL0	180 nm	241 nm	181 nm
GL1	180 nm	252.35 nm	191 nm
GL2	180 nm	261.4 nm	201.4 nm
GL3	180 nm	243.1 nm	183.1 nm
GL4	180 nm	242.8 nm	182.8 nm



TECHNOLOGY IN THE INTERNET ERA

Lithography Beyond the Wavelength of Light

Gate	Drawn	Pre-Etch	Post-Etch
GL0	180 nm	241 nm	181 nm
GL1	180 nm	239.2 nm	179.2 nm
GL2	180 nm	234.05 nm	174.05 nm
GL3	180 nm	245.5 nm	185.5 nm
GL4	180 nm	238.6 nm	178.6 nm



TECHNOLOGY IN THE INTERNET ERA

Grand Challenges of Moore's Law Scaling

- Lithography
- Gate insulator
- Transistor leakage in "off" state

TECHNOLOGY IN THE INTERNET ERA

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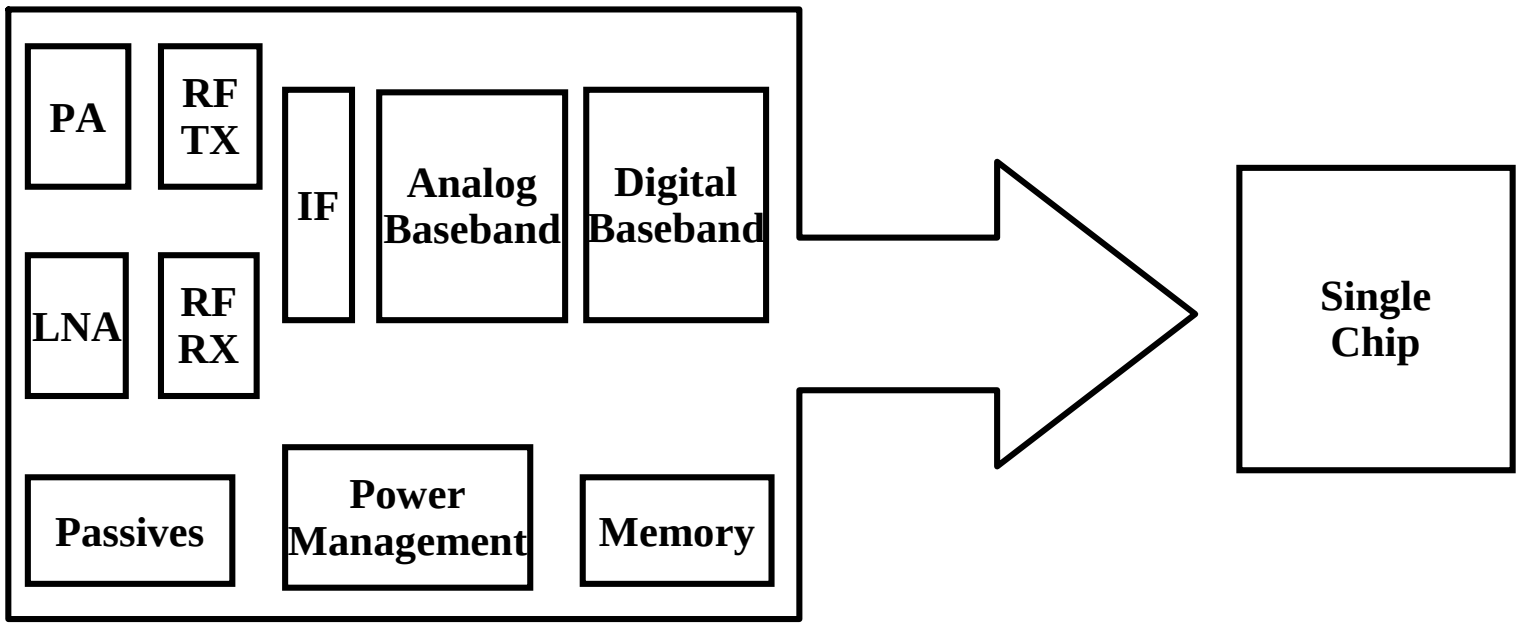
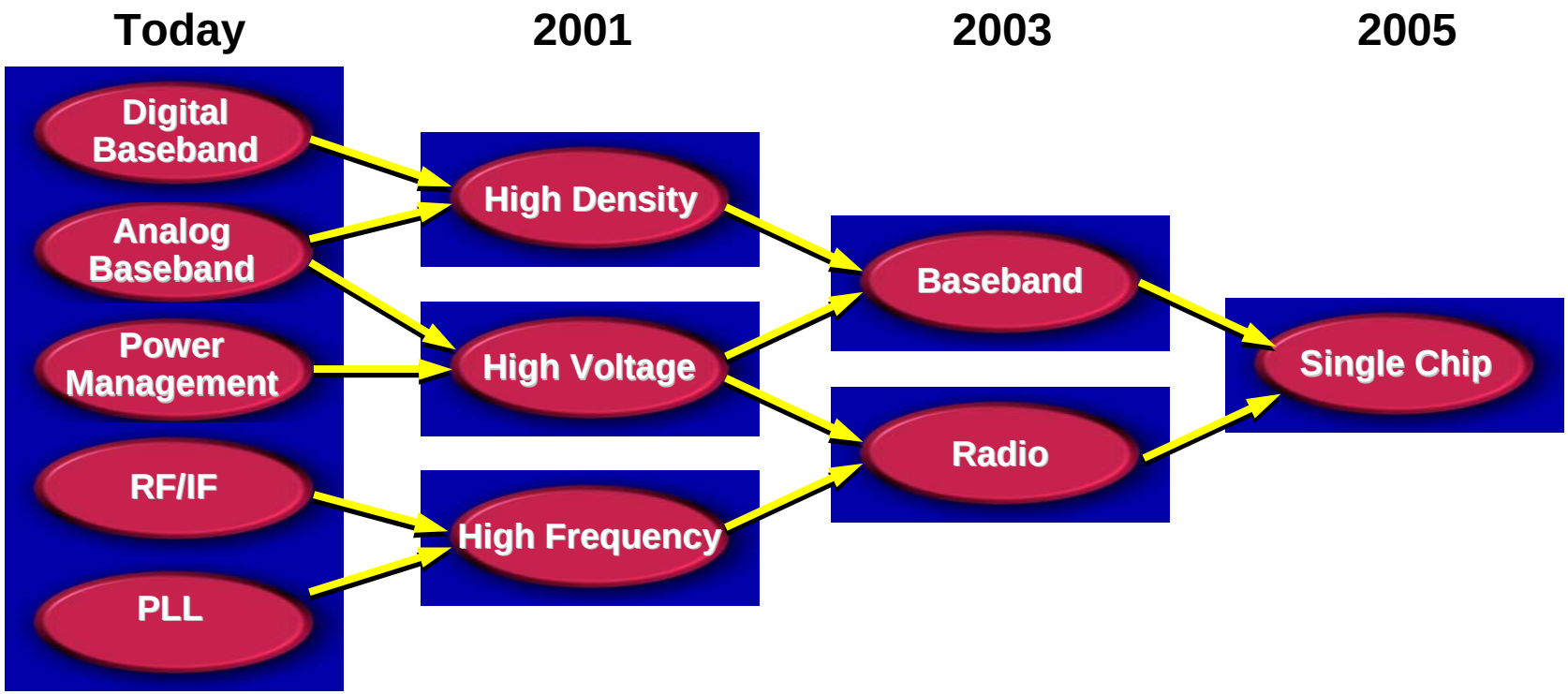
TECHNOLOGY IN THE INTERNET ERA

SOC Integration: Cell Phone



TECHNOLOGY IN THE INTERNET ERA

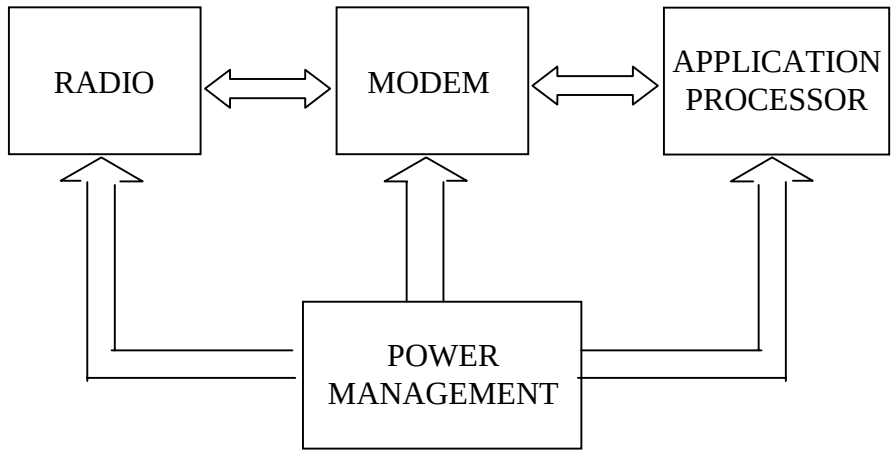
SOC Integration: Cell Phone



TECHNOLOGY IN THE INTERNET ERA

SOC Integration

- Technology Strategy also needs to support SOC Integration strategies for
  - Mass Storage
  - ADSL Modems
  - Short Distance Wireless
  - Cable Modems
  - VoIP/VoDSL
  - Digital Still Camera

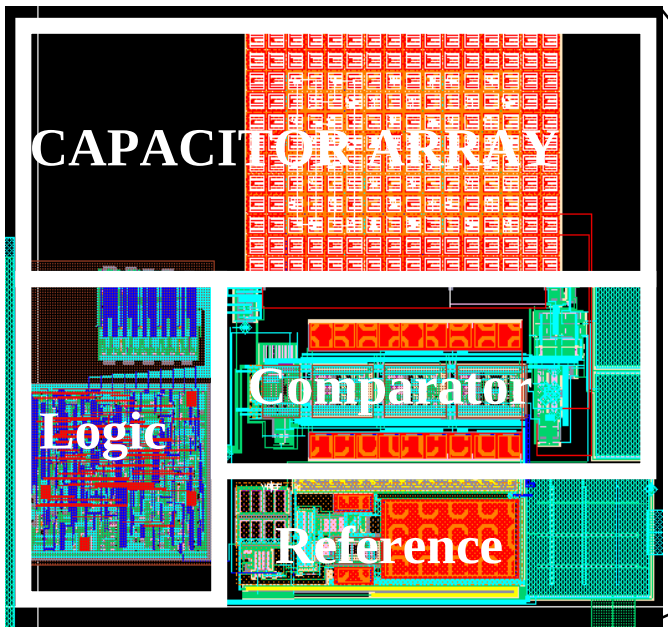


TECHNOLOGY IN THE INTERNET ERA

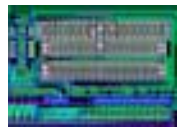
Technologies Required for SOC Integration

- High performance, high density digital CMOS logic having low active power, and in portable applications, low standby power
- Embedded RAM: SRAM or DRAM
- FLASH EEPROM or non-volatile memory replacement such as FeRAM
- Analog CMOS for Analog Baseband functions
- RF BiCMOS or CMOS for radio or tuner functions
- Extended Drain CMOS capable of withstanding 5-10V voltage surges
- Technologies to enable passive integration: capacitors, inductors, varactors

Shrinking Analog Functions



10-bit SAR ADC


0.5 µm
0.52 mm²

54%


0.35 µm
0.28 mm²


0.18µm
0.08 mm²

29%

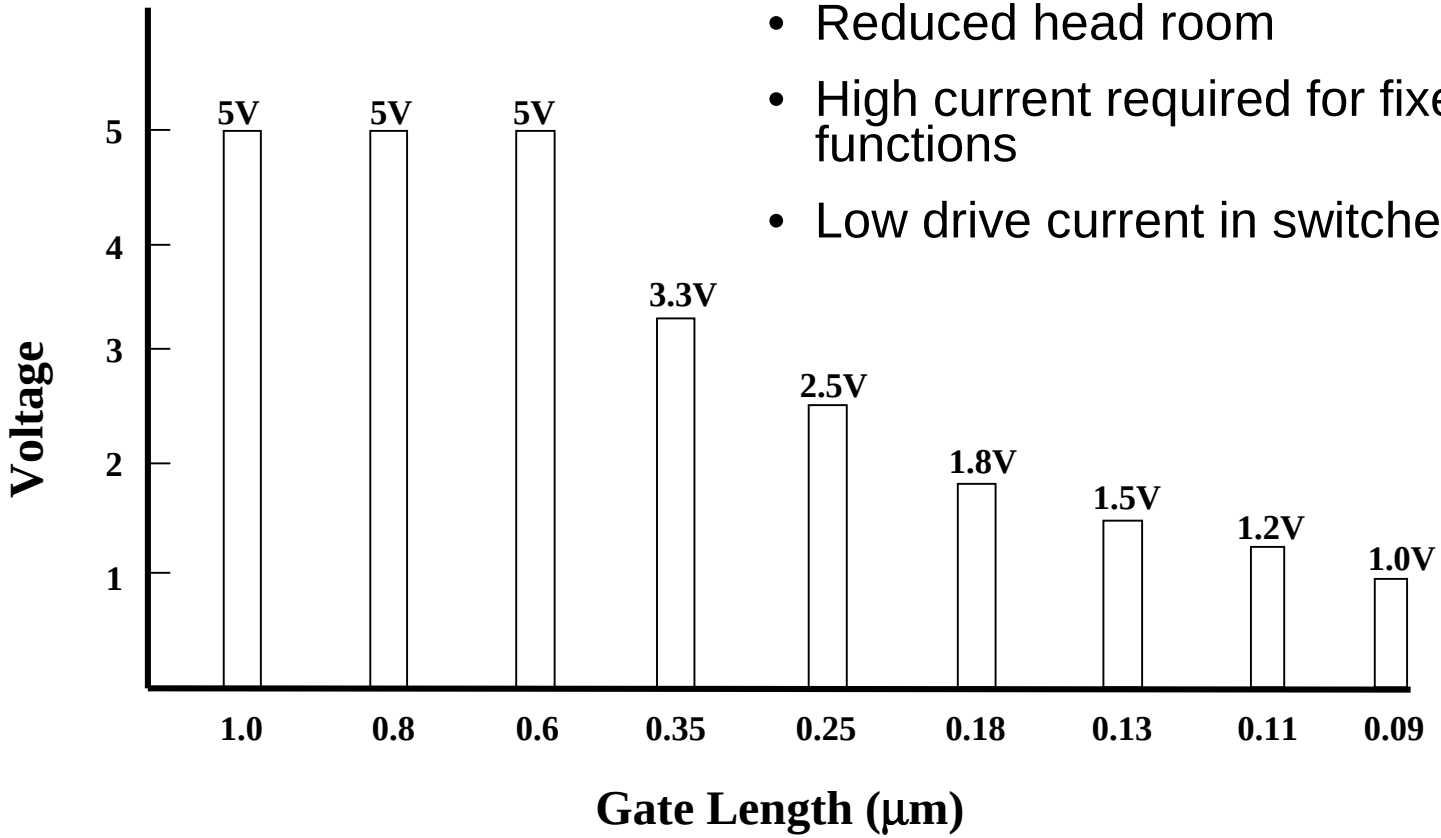
On average, the area of analog functions shrinks linearly with feature size, eg: 50% reduction in feature size results in 50% shrink in chip area.

Analog SOC Integration

- SOC integration does not always mean integration of “digital functions” together with analog functions
- Analog functions benefit from shrinking feature size
- New architectures for “analog functions” use extensive digital logic
  - Digital compensation for fractional-N PLLs
  - On channel modulation for phase modulated systems (GSM)
  - Digital error correction in ADCs
  - Digital linearization of amplifiers and tuners

Analog SOC Integration: #1 Problem

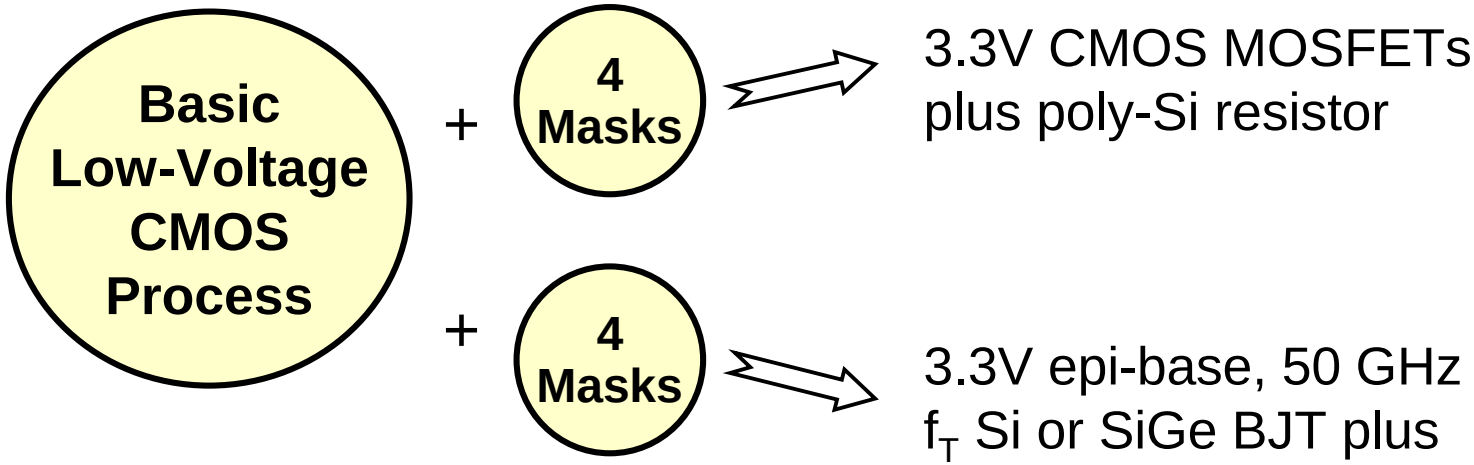
- Reduced dynamic range: KT/C noise
- Reduced head room
- High current required for fixed power functions
- Low drive current in switches



TECHNOLOGY IN THE INTERNET ERA

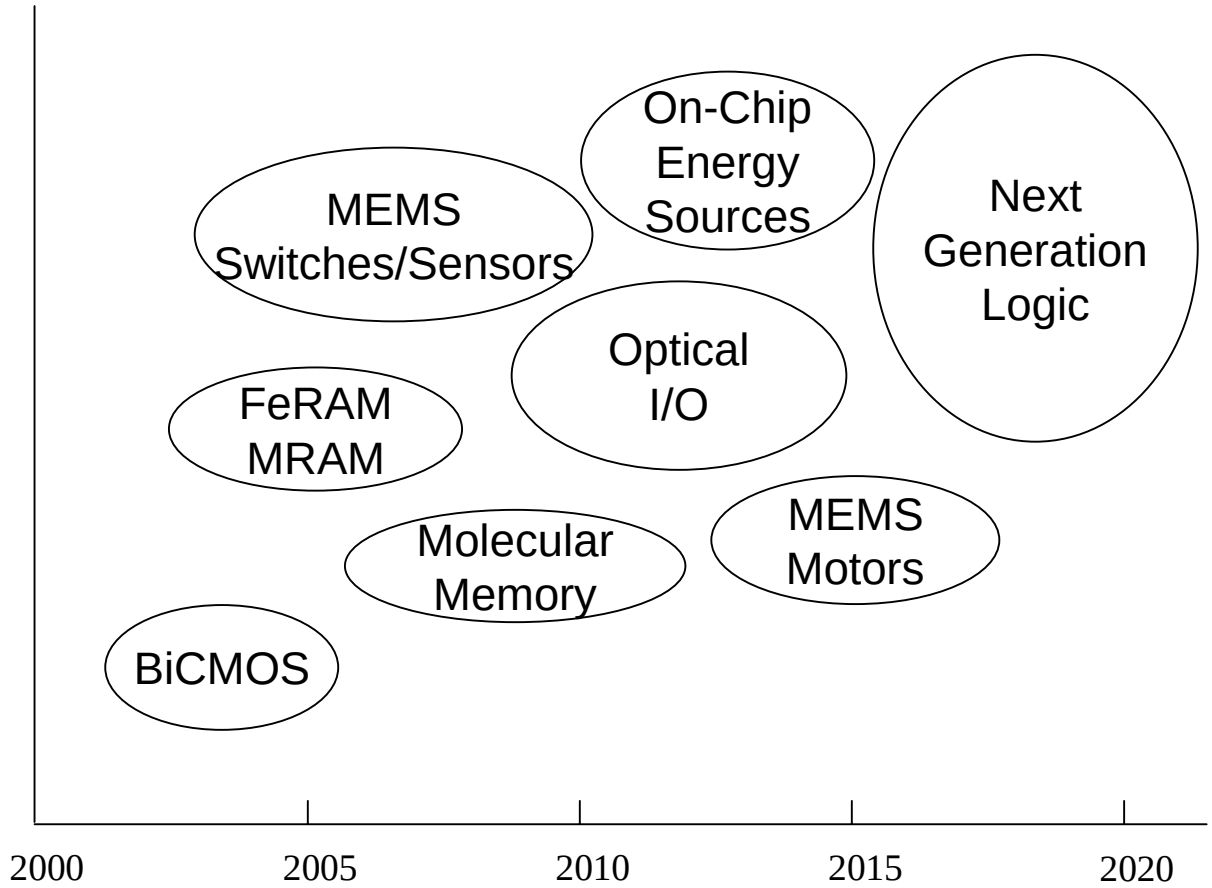
Analog SOC Integration

- In some cases, a higher voltage MOSFET is required: 3.3V → 2.5V
- This in general costs three masking steps
- Food for thought



TECHNOLOGY IN THE INTERNET ERA

Other SOC Technologies



TECHNOLOGY IN THE INTERNET ERA

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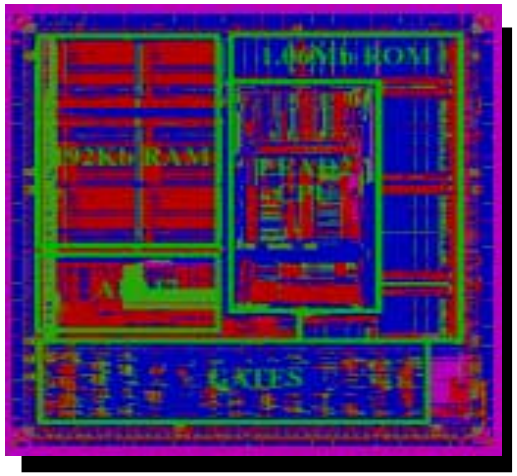
TECHNOLOGY IN THE INTERNET ERA

In order to be the leader in DSP & Analog Internet Access Products, internal technology and manufacturing are essential

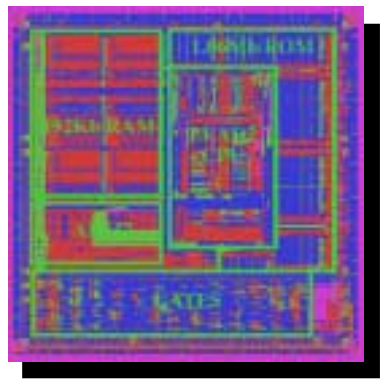
- Differentiated Technology
- Lowest Cost
- Rapid Ramp to Volume

TECHNOLOGY IN THE INTERNET ERA

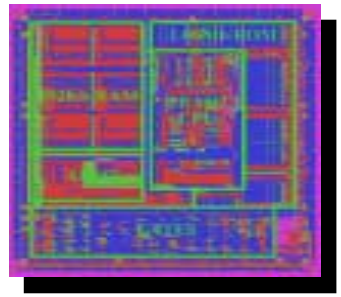
TECHNOLOGY ENTITLEMENT



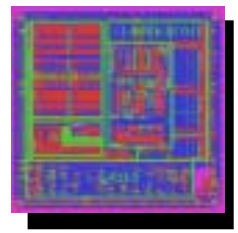
C12:
80.7 mm²



C10:
46.6 mm²



C07:
19.2 mm²



C05:
10.7 mm²

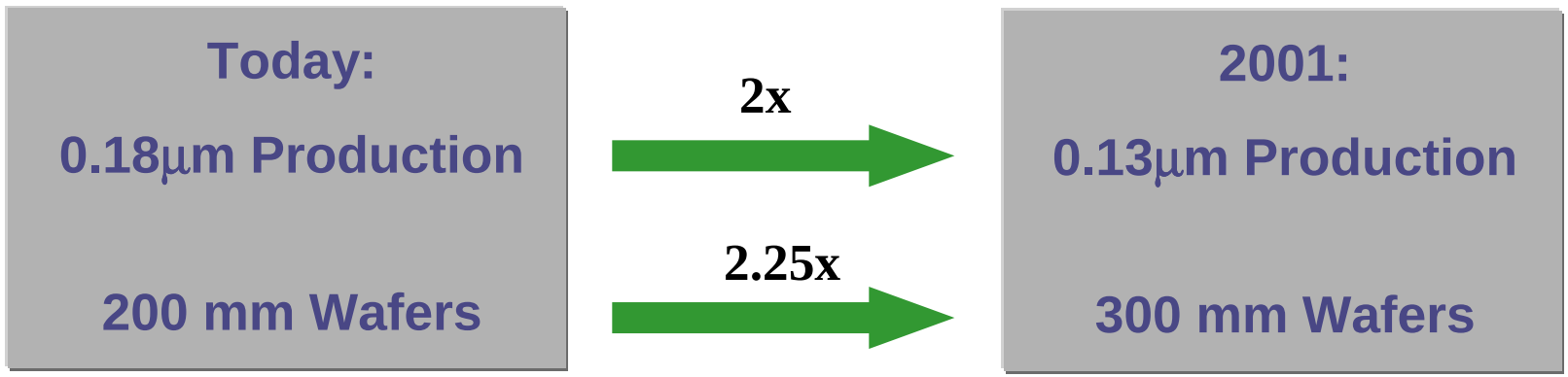
Dies Per Wafer:

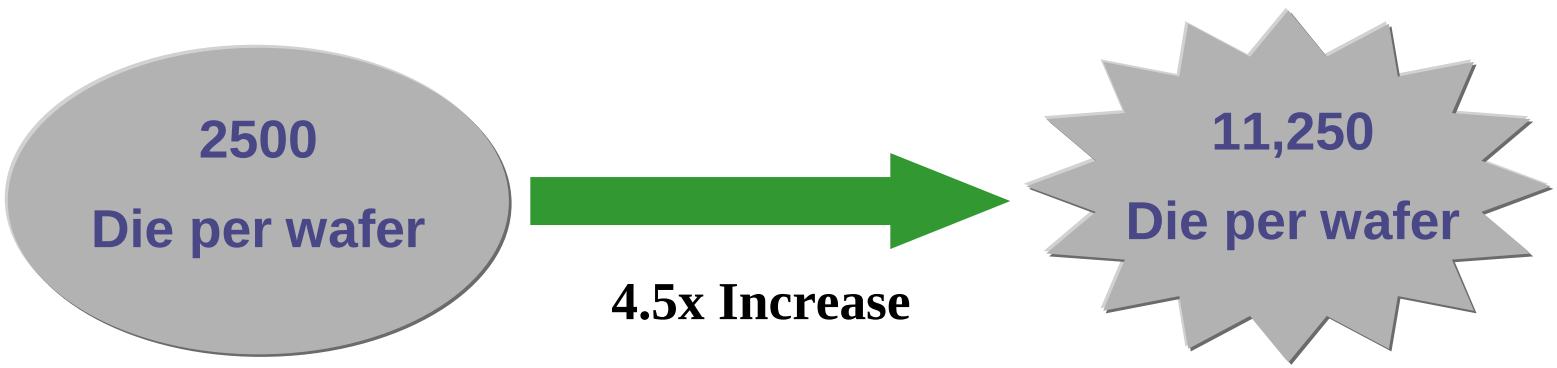
310 → 558 → 1435 → 2616

800% increase in dpw

TECHNOLOGY IN THE INTERNET ERA

Lowest Cost





TECHNOLOGY IN THE INTERNET ERA

DSPS Fest 2000

300 mm

Did you know...

Roughly the size of three football fields, DMOS6 will be TI's largest fab

Fast Facts:

300mm Project Capital: $2.2B

Final Wafer Size: 300mm

Final Capacity: 30K wfs/month

Final Tech Mix: C035/C027 Cu

Clean Room Space: 135K sq ft

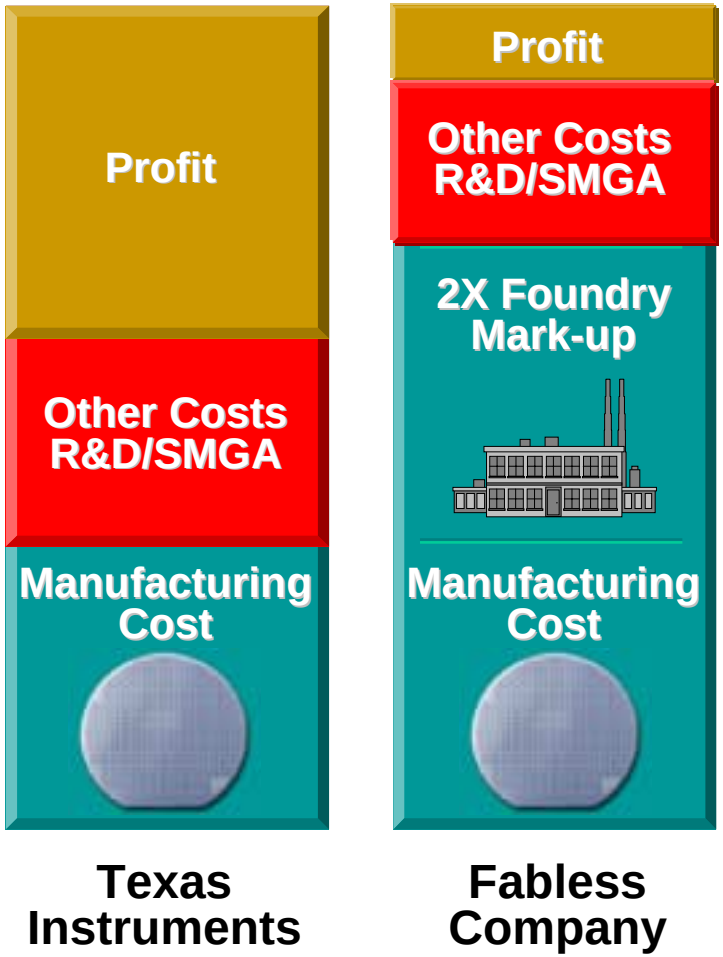
Key dates:

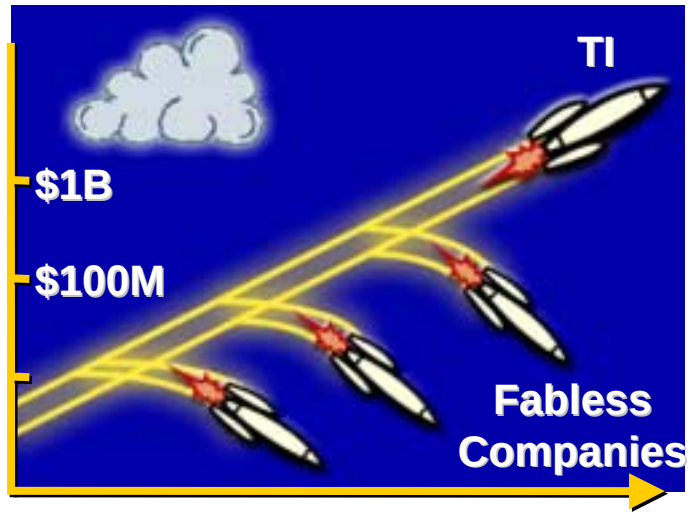
- **Shell constructed: 1996**
- **Cleanroom complete: 7/2000**
- **300mm production: 11/2001**

Location: Dallas

TECHNOLOGY IN THE INTERNET ERA

Lowest Cost





- Fabless + Foundry model is successful for new/niche products.
- Internal manufacturing provides cost structure for profitability for high volume products.

TECHNOLOGY IN THE INTERNET ERA

SiTD Vision

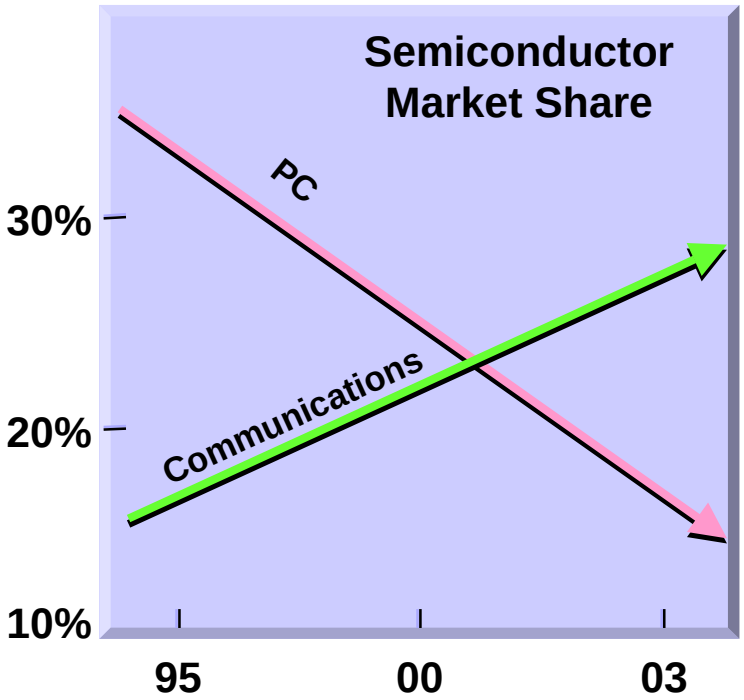
World Class Technology for the World's Premier Company in DSP/Analog Internet Access Products

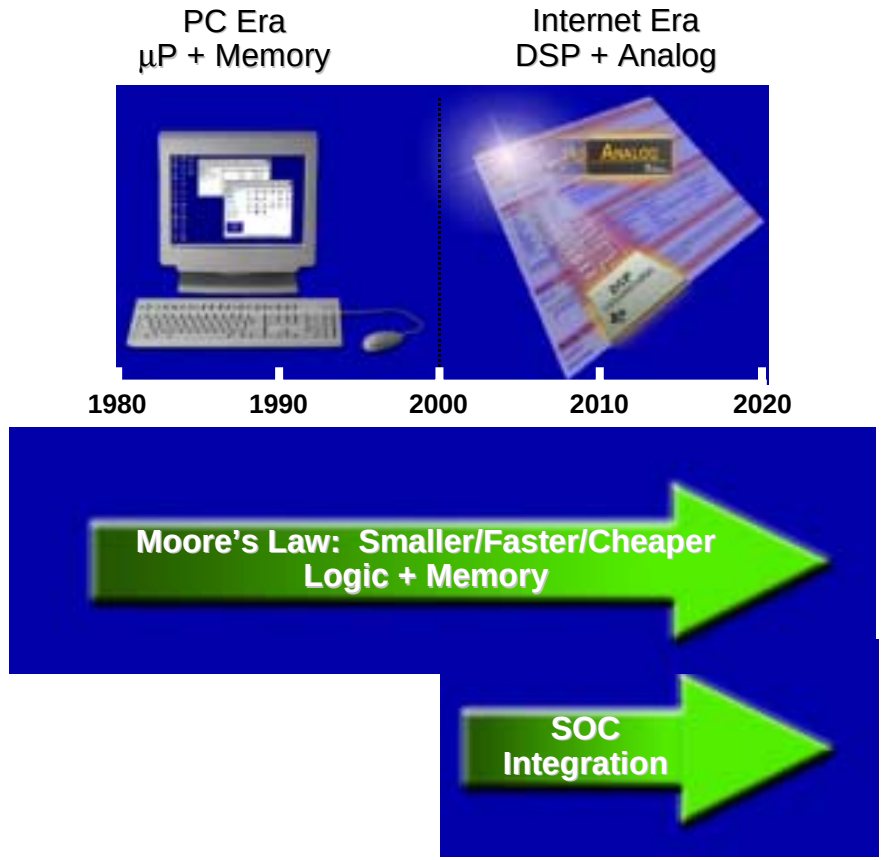
- State-of-the-art feature size
- Lowest cost manufacturing
- Technology matched to DSP & Analog product needs
- Rapid ramp of newest technology: First to 100M units

TECHNOLOGY IN THE INTERNET ERA

DSPS Fest 2000

Dawn of Internet Era





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