TECHNOLOGY IN THE INTERNET ERA

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Si Technology Development
Dallas, Texas
Transistor Scaling will continue to be an important Technology Driver in the Internet Era. But it will no longer be the sole driver: SOC Integration will be increasingly important.
CMOS Scaling Roadmap (ITRS’99)

- **Minimum Feature Size (nm)**

  - 500
  - 350
  - 250
  - 180
  - 130
  - 100
  - 70
  - 50
  - 35
  - 25

- **Best Case Opportunity**
- **IRC Agreement July 7, 1999**
- **1994**
- **1997**
- **1998 & 1999**
- **DRAM Half Pitch**
- **MPU Gate**

**Graph Details:**
- **Features:** Minimum Feature Size, IRC Agreement, Best Case Opportunity, MPU Gate, DRAM Half Pitch

**Source:** The World Leader in DSP and Analog

**Company:** Texas Instruments
## DSP Integration Through the Years

### Typical Device Capabilities

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Die size (mm)</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>Technology (µm)</td>
<td>3</td>
<td>0.8</td>
<td>0.18</td>
<td>0.05</td>
<td>0.01</td>
</tr>
<tr>
<td>MIPS</td>
<td>5</td>
<td>40</td>
<td>2000</td>
<td>20K</td>
<td>50K</td>
</tr>
<tr>
<td>MHz</td>
<td>20</td>
<td>80</td>
<td>500</td>
<td>2,000</td>
<td>10,000</td>
</tr>
<tr>
<td>RAM (bytes)</td>
<td>256</td>
<td>2K</td>
<td>32K</td>
<td>5M</td>
<td>10M</td>
</tr>
<tr>
<td>Price</td>
<td>$150.00</td>
<td>$15.00</td>
<td>$1.50</td>
<td>$1.50</td>
<td>$1.50</td>
</tr>
<tr>
<td>Power (mW/MIPS)</td>
<td>250</td>
<td>12.5</td>
<td>0.1</td>
<td>0.01</td>
<td>0.001</td>
</tr>
<tr>
<td>Transistors</td>
<td>50K</td>
<td>500K</td>
<td>5M</td>
<td>50M</td>
<td>100M</td>
</tr>
<tr>
<td>Wafer size</td>
<td>3”</td>
<td>6”</td>
<td>12”</td>
<td>12”</td>
<td>12”</td>
</tr>
</tbody>
</table>

Gene Frantz, IEDM 99
Transistor scaling is not the most significant enabler for cost reduction. SOC integration requires technologies for:

- DSP
- Radio RF/IF
- SRAM
- Analog functions
- FLASH
- Power management

**Today's Cell Phone**

ICs 12
Discretes 16
Passives 214
Other 8
Total 250
Leaders On Moore’s Law Curve

0.18μm Generation
- 0.18μm Since Sept. 99
- 0.13μm Currently
- Cu in Sept. 00

0.13μm Generation
- 0.11μm in March 01
- 0.085μm in June 01
- SOI in June 02

Differentiated Technology for SOC Integration

Core CMOS

70nm TRAN

Six Level Cu Interconnect

The World Leader in DSP and Analog
TECHNOLOGY IN THE INTERNET ERA

AGENDA

- Introduction
- Grand Challenges of Scaling
- SOC Integration
- TI Strategy
TECHNOLOGY IN THE INTERNET ERA

Lithography

[Graph showing the evolution of wavelength and feature size over time, with a focus on subwavelength technology.]
## TECHNOLOGY IN THE INTERNET ERA

Lithography Beyond the Wavelength of Light

<table>
<thead>
<tr>
<th>Gate</th>
<th>Drawn</th>
<th>Pre-Etch</th>
<th>Post-Etch</th>
</tr>
</thead>
<tbody>
<tr>
<td>GL0</td>
<td>180 nm</td>
<td>241 nm</td>
<td>181 nm</td>
</tr>
<tr>
<td>GL1</td>
<td>180 nm</td>
<td>252.35 nm</td>
<td>191 nm</td>
</tr>
<tr>
<td>GL2</td>
<td>180 nm</td>
<td>261.4 nm</td>
<td>201.4 nm</td>
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<tr>
<td>GL3</td>
<td>180 nm</td>
<td>243.1 nm</td>
<td>183.1 nm</td>
</tr>
<tr>
<td>GL4</td>
<td>180 nm</td>
<td>242.8 nm</td>
<td>182.8 nm</td>
</tr>
</tbody>
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- **Line-End Pull-Back**
- **Corner Rounding**
TECHNOLOGY IN THE INTERNET ERA

Lithography Beyond the Wavelength of Light

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<tr>
<td>GL0</td>
<td>180 nm</td>
<td>241 nm</td>
<td>181 nm</td>
</tr>
<tr>
<td>GL1</td>
<td>180 nm</td>
<td>239.2 nm</td>
<td>179.2 nm</td>
</tr>
<tr>
<td>GL2</td>
<td>180 nm</td>
<td>234.05 nm</td>
<td>174.05 nm</td>
</tr>
<tr>
<td>GL3</td>
<td>180 nm</td>
<td>245.5 nm</td>
<td>185.5 nm</td>
</tr>
<tr>
<td>GL4</td>
<td>180 nm</td>
<td>238.6 nm</td>
<td>178.6 nm</td>
</tr>
</tbody>
</table>

Size Adjust

Serif

Hammerhead
TECHNOLOGY IN THE INTERNET ERA

Grand Challenges of Moore’s Law Scaling

- Lithography
- Gate insulator
- Transistor leakage in “off” state
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SOC Integration: Cell Phone

[Diagram showing components like PA, RF TX, IF, Analog Baseband, Digital Baseband, Power Management, Memory, LNA, RF RX, Passives, and Single Chip]

THE WORLD LEADER IN DSP AND ANALOG
Mass Storage
ADSL Modems
Short Distance Wireless
Cable Modems
VoIP/VoDSL
Digital Still Camera
TECHNOLOGY IN THE INTERNET ERA

Technologies Required for SOC Integration

- High performance, high density digital CMOS logic having low active power, and in portable applications, low standby power
- Embedded RAM: SRAM or DRAM
- FLASH EEPROM or non-volatile memory replacement such as FeRAM
- Analog CMOS for Analog Baseband functions
- RF BiCMOS or CMOS for radio or tuner functions
- Extended Drain CMOS capable of withstanding 5-10V voltage surges
- Technologies to enable passive integration: capacitors, inductors, varactors
On average, the area of analog functions shrinks linearly with feature size, e.g., 50% reduction in feature size results in 50% shrink in chip area.
SOC integration does not always mean integration of “digital functions” together with analog functions.

Analog functions benefit from shrinking feature size.

New architectures for “analog functions” use extensive digital logic:

- Digital compensation for fractional-N PLLs
- On channel modulation for phase modulated systems (GSM)
- Digital error correction in ADCs
- Digital linearization of amplifiers and tuners
Analog SOC Integration: #1 Problem

- Reduced dynamic range: KT/C noise
- Reduced head room
- High current required for fixed power functions
- Low drive current in switches
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Analog SOC Integration

- In some cases, a higher voltage MOSFET is required: 3.3V → 2.5V
- This in general costs three masking steps
- Food for thought

![Diagram](chart.png)

- Basic Low-Voltage CMOS Process
- 4 Masks
- 3.3V CMOS MOSFETs plus poly-Si resistor
- 4 Masks
- 3.3V epi-base, 50 GHz $f_T$ Si or SiGe BJT plus poly-Si resistor
TECHNOLOGY IN THE INTERNET ERA

Other SOC Technologies

- BiCMOS
- FeRAM
- MRAM
- MEMS Switches/Sensors
- Molecular Memory
- Optical I/O
- On-Chip Energy Sources
- MEMS Motors
- Next Generation Logic
TECHNOLOGY IN THE INTERNET ERA

AGENDA

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In order to be the leader in DSP & Analog Internet Access Products, internal technology and manufacturing are essential.

- Differentiated Technology
- Lowest Cost
- Rapid Ramp to Volume
TECHNOLOGY IN THE INTERNET ERA

TECHNOLOGY ENTITLEMENT

Dies Per Wafer:

C12: 80.7 mm²

C10: 46.6 mm²

C07: 19.2 mm²

C05: 10.7 mm²

310

558

1435

2616

800% increase in dpw
TECHNOLOGY IN THE INTERNET ERA

Lowest Cost

Today:
0.18μm Production
200 mm Wafers

2x

2.25x

2001:
0.13μm Production
300 mm Wafers

Die per wafer

2500

11,250

4.5x Increase

Die per wafer
TECHNOLOGY IN THE INTERNET ERA

300 mm

Fast Facts:
- 300mm Project Capital: $2.2B
- Final Wafer Size: 300mm
- Final Capacity: 30K wfs/month
- Final Tech Mix: C035/C027 Cu
- Clean Room Space: 135K sq ft

Key dates:
- Shell constructed: 1996
- Cleanroom complete: 7/2000
- 300mm production: 11/2001

Location: Dallas

Did you know...
Roughly the size of three football fields, DMOS6 will be TI’s largest fab
Fabless + Foundry model is successful for new/niche products.

Internal manufacturing provides cost structure for profitability for high volume products.

Texas Instruments

Fabless Company

TECHNOLOGY IN THE INTERNET ERA
TECHNOLOGY IN THE INTERNET ERA

SiTD Vision

World Class Technology for the World’s Premier Company in DSP/Analog Internet Access Products

- State-of-the-art feature size
- Lowest cost manufacturing
- Technology matched to DSP & Analog product needs
- Rapid ramp of newest technology: First to 100M units
In order to be the leader in DSP & Analog Internet Access Products, internal technology and manufacturing are essential.