# A DSP-Based Switching Amplifier for Capacitive Loads

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**Abstract**

The design of a DSP-based, medium-power ($100VA$), amplifier for capacitive loads is presented. The design goals were a $200V$, $1A$ (peak) output into a load of $0.5\mu F$, a power bandwidth of $1.6kHz$, and a small-signal bandwidth of $20kHz$. The design was based on a TMS320F240 processor, and an analog version was built for comparison. One of the major difficulties encountered is the fact that the load capacitance is widely variable, which makes shaping of the frequency response very difficult. An attractive feature of the DSP-based approach is its potential to adapt to the variable load while maintaining an optimal frequency response. Other advantages and disadvantages of both the analog and DSP-based approaches are also discussed, and extensions to more complicated (variable-frequency) PWM algorithms are explored. Finally, the potential contribution of these ideas to an undergraduate power electronics/control lab is discussed.

## 1 Introduction

The design of a power amplifier to drive piezoelectric actuators presents several unusual challenges. The two most important of these are, first, that such actuators present a highly capacitive load to the amplifier, and, second, that they require voltages which are much higher than those encountered in mainstream electronics, ranging from 80V to 1500V or more. Although linear amplifiers have been used in the past, mainly in laboratory work, much of the potential advantage in size and weight is lost because the inefficiency of the linear amplifiers makes the use of heavy, bulky, heat-sinks mandatory. It should be noted here that the inefficiency of a linear amplifier in driving a reactive load is much worse than in the resistive case, since linear amplifiers have no way of returning energy to the power supply, and so must dissipate all of the reactive energy in the output stage of the amplifier.

The use of switching amplifiers to drive piezoelectric actuators has therefore become attractive, or in some situations unavoidable, as the technology transitions out of the laboratory; the potential of piezoelectric actuators has been seriously limited by the inefficiency of the driving electronics [1]. In addition to their usual efficiency advantages, such amplifiers also return reactive energy from the load to the power supply, making them especially suitable for reactive loads. This technology, of course, is well-developed and widely-used for inductive loads, but its application to capacitive loads presents some new problems.

The major problem is that, for a given power level, the voltage is usually much higher, and the current much lower, than in the more usual inductive load. The switching losses therefore become more significant, and the conduction losses less significant, and so more attention must be given to low-loss switching. While much work has been done on this problem for switching power supplies, far less has been done in the case of switching amplifiers, with some basic papers appearing only recently [2].

Another problem arises since the amplifier will almost always have a D.C. voltage source as power supply; an inductor (or inductor-input filter) must then be used between the switching devices and the load, and this resonates with the capacitive load. While this resonance can be easily damped without resistive loss, it does make the frequency response of the amplifier vary widely with the load capacitance connected to the amplifier.

In the following, some background will be given on switching power amplifiers, and the circumstances under which resonant transitions can be achieved will be described. It will be shown that the ability of a DSP-based approach to easily vary the switching frequency extends the range of output voltages and currents for which resonant switching occurs.

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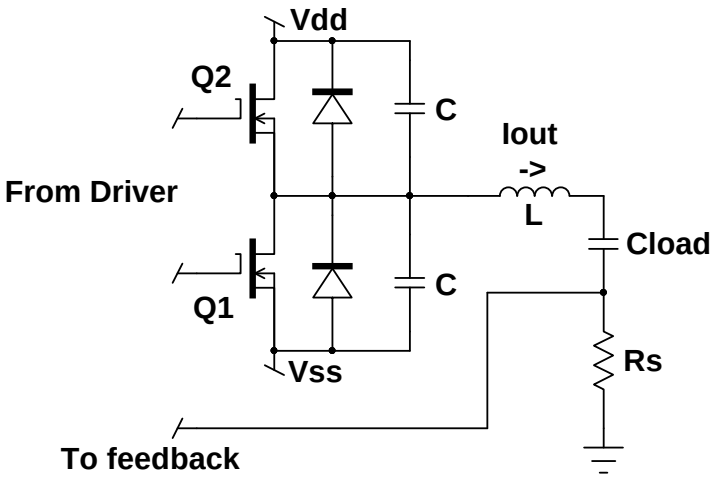


Figure 1: Typical Power Stage of Switching Amplifier

# 2 Background

## 2.1 Frequency Response

As can be seen from the schematic in Figure 1, the resonant frequency of the filter is dependent on the load capacitance. This is no problem if the load is fixed; however, for an amplifier with an external load, the load capacitance will normally consist of a fixed value to guard against open-circuit operation, and an external, variable capacitor.

The resonant frequency causes no problems for the frequency response, since it can easily be damped without significant resistive loss by using feedback from the capacitor current (as shown by $R_S$ in Figure 1). This feedback sets the corner frequency of the filter to be the resonant frequency, and so the (small-signal) bandwidth of the amplifier decreases with increasing load capacitance. Of greater significance is the fact that, for a fixed current feedback gain, the damping decreases with increasing load capacitance. For this reason, one of the most attractive features of a DSP-based implementation is the potential to adapt the gain to the load, in order to give a smooth frequency response under varying loads.

## 2.2 Switching Losses

As discussed above, one of the most critical parameters in the type of amplifier under discussion is the switching loss. To clarify this, a diagram of the output stage of a standard switching amplifier is shown in Figure 1, with the body diodes and parasitic output capacitances, C, of the MOSFETs shown explicitly. On each switching cycle, each of the two capacitances C has to be charged and discharged. If the energy in these capacitances is lost, as it will be with hard switching, the switching power loss will be given by

$$P_{sw} = CV^2 f_{sw}$$

The amplifier under discussion is required to have a peak output voltage of $200V$, a peak output current of $1A$, and a small-signal bandwidth of $20kHz$ into a load of $0.5\mu F$. The total power supply voltage (positive to negative) must then be at least $400V$, and, in practice, will have to be at least $450V$ to $500V$, so that MOSFETs with a breakdown voltage of $600V$ must be used. Also, for a bandwidth of $20kHz$, the switching frequency must be at least $200kHz$, and preferably higher.

To give some idea of the relative magnitudes, a typical MOSFET for use in this situation would be the IRFIB6N60A, with breakdown voltage of $600V$ and on-state drain-to-source resistance of $r_{ds} = 0.75\Omega$. The data sheet gives the effective output capacitance as about $100pF$, and the above formula then gives the switching loss as $P_{sw} = 5W$. This is actually an underestimate of the loss, since it does not take into

account the reverse conduction losses in the body diodes under hard switching; the diode switching losses are more difficult to quantify analytically, but can be equal to or higher than the losses due to the output capacitance. By contrast, the conduction losses (considering both the load current and the ripple current) would be about $1W$ at maximum load current. The switching losses are therefore the dominant losses with the present voltages and currents.

### 2.3 Resonant Switching

The normal way of minimizing the switching losses is to use resonant transitions. To explain this, let us assume that we have reached the end of a switching cycle with the lower MOSFET, Q1, switched on, and the upper MOSFET, Q2, switched off. To begin the transition, Q1 is turned off. At this point, the current in L will begin to charge the lower parasitic capacitance, which starts at zero voltage, and discharge the upper, *provided that the current in the inductor is flowing from right to left, that is, into the switching node.* If the current is flowing in the opposite direction, it will merely flow through the lower diode until Q2 is switched on, at which point the energy in the upper parasitic capacitance will be dissipated in Q2 — this is hard switching, and is where the switching losses arise. At the next switching instant (from high to low) the same analysis holds, but the current in L must be flowing from left to right to effect the resonant transition. Therefore, for resonant transitions to occur, *it is essential that the current in L change sign on each cycle.* In other words, the magnitude of the load current must be less than the peak value of the ripple current in the inductor (See Figure 2). This is not quite sufficient, since a minimum energy is required in the inductor to complete the resonant transition, and so the load current magnitude must be somewhat less than the peak ripple current. For present purposes, however, we will work with the simpler criterion that the current must change direction on each switching cycle to ensure resonant transitions.

## 3 Theory

The difficulty with having the inductor current change sign in each switching period is that, with normal fixed-frequency PWM, the peak value of the ripple current varies with the level of the output voltage. This can be analyzed as follows.

### 3.1 Analysis

The discussion below assumes that the power supply voltages are $\pm V_S$. The voltage $V_0 = kV_S$ across the load can be considered constant over a single switching cycle.The instantaneous inductor current is denoted by $i(t)$, and its average over a single cycle is denoted by $I_L$. For purposes of the present analysis, the time taken for a resonant transition is assumed to be negligible.(This time will be calculated and used in the design part.) It is also assumed that the on-resistance of the MOSFETs, $r_{DS}$, and the parasitic resistances, have negligible effect on the current ramping in the inductor.

Assume that the up transition has completed at $t = 0$, and current $I_0 = i(0)$ is flowing, as shown in Figure 2. Also assume that the down transition occurs at $t = T_1$ and up transition occurs at $t = T_2$ . ($T_2$ is therefore the period.) Also let $I_1 = i(T_1)$, and $I_2 = i(T_2)$.

Then, for the first part of the cycle

$$\begin{aligned} i(t) &= I_0 + t(V_S - V_0)/L \\ &= I_0 + t(1-k)V_S/L \end{aligned}$$

and so

$$I_1 = I_0 + T_1(1-k)V_S/L$$

Even under ideal conditions, a resonant transition requires $I_1 \geq 0$.

For the second part of the cycle,

$$\begin{aligned} i(t) &= I_1 - (t - T_1)(V_S + V_0)/L \\ &= I_1 - (t - T_1)(1+k)V_S/L \end{aligned}$$

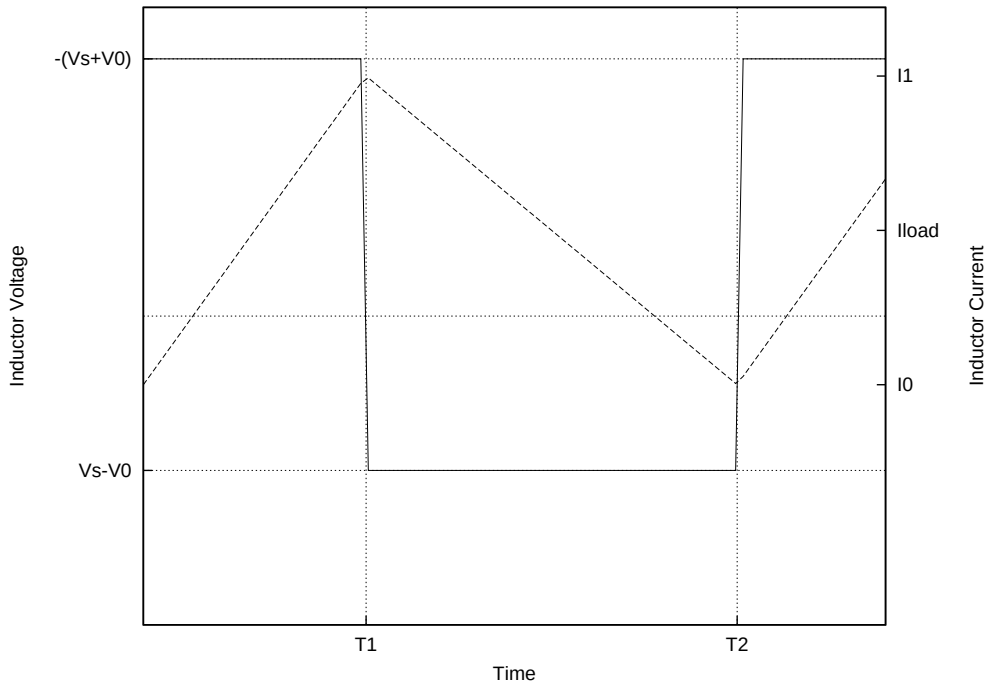


Figure 2: Voltage and Current Waveforms over a Switching Cycle

and so

$$\begin{aligned} I_2 &= I_1 - (T_2 - T_1)(1+k)V_S/L \\ &= I_0 + T_1(1-k)V_S/L - (T_2 - T_1)(1+k)V_S/L \\ &= I_0 + (T_2 - 2T_1 + kT_2)V_S/L \end{aligned}$$

Again, any possibility for a resonant transition requires $I_2 \leq 0$

Since periodicity requires $I_2 = I_0$, it follows that $T_1 = (1+k)T_2/2$ (which is also clear from looking at the duty cycle needed to ensure that $V_0 = kV_S$).

The currents $I_0$ and $I_1$ can then be expressed in terms of the average load current, $I_L$, and the ratio $k$:

$$\begin{aligned} I_1 &= I_L + (1-k^2)T_2V_S/(4L) \\ I_0 &= I_L - (1-k^2)T_2V_S/(4L) \end{aligned}$$

As described above, resonant transitions can not occur unless the current waveform crosses zero on each cycle; this requirement reduces to

$$|I_L| \leq (1-k^2)T_2V_S/(4L)$$

or

$$|I_L| \leq K(V_S^2 - V_0^2) \tag{3.1}$$

where

$$K = T_{period}/(4V_SL) \tag{3.2}$$

This inequality gives the boundary in the $I_L - V_L$ plane of the region where resonant transitions occur under ideal conditions, or, more accurately, it gives the boundary outside which completely non-resonant transitions are unavoidable.

### 3.2 Fixed-Frequency PWM

It follows from inequality 3.1 that the the load currents for which resonant transitions are possible are less than the peak ripple current in the inductor when the output voltage is zero. With fixed frequency switching, this current capability decreases, however, as the output voltage moves towards either supply rail, and reduces to zero when the the voltage reaches either supply value. This limits the range of outputs into a capacitive load if resonant switching is desired, and is an even greater restriction for resistive loads.

### 3.3 Variable-Frequency PWM

It follows from inequality 3.1 for the output current, and equation 3.2, that the output current capability can be kept constant independent of the output voltage by varying the switching period $T_{period}$ so that $(1-k^2)T_{period}$ remains constant, while keeping the correct duty cycle. The switching frequency is then highest at zero output voltage, and falls as the output voltage approaches the supply voltages. Since this would give a zero frequency as the output voltage goes to the rails, it is necessary to limit the output voltage to less than the rails; in practice, it should be limited so that the switching frequency stays well above the cutoff frequency of the filter. It should be noted that fixed-frequency PWM has similar restrictions dictated by the minimum pulse-width of which the output MOSFETs are capable. Minimum pulse-width is not an issue for this variable-frequency algorithm, since it can be shown that the minimum pulse-width is half of the pulse width at the highest frequency. For this reason, the switching frequency at zero voltage can be taken much higher than the the frequency for constant-frequency switching.

One of the major advantages of a DSP-based implementation is the ease with which such variable-frequency algorithms can be implemented. Although this particular variable-frequency algorithm has a simple analog circuit implementation (given in [3] for a different application), it becomes increasingly difficult to implement variations, enhancements, and other variable-frequency algorithms without using DSP.

One such enhancement is to vary the frequency by directly sensing the load current, and choosing the period so that the peak inductor ripple current is slightly larger. In this case, the switching frequency will also have to be limited on the high side to prevent arbitrarily high-frequency switching with zero load current.

## 4 Implementation

### 4.1 Design

A fixed-frequency switching amplifier with the above specifications had previously been implemented, but had higher than expected dissipation since little attention was paid to resonant transitions.

To derive the parameters for such an amplifier, we take the cutoff frequency of the output filter to be the resonant frequency. Since the load capacitance is $0.5\mu F$, the inductance value is given by $125\mu H$.

The supply voltages are taken to be $\pm 225V$, and the peak inductor ripple current at zero output voltage is taken to be $1A$ since a peak output current of $1A$ is specified. The (zero-voltage) switching frequency can then be derived from the relation $V = LdI/dt$, where $V = 225$, $dt = 2$ (2A peak-to-peak), and $dt = T_{period}/2$. This gives $f_{sw} = 450kHz$. Also, the dead-time (between when one MOSFET turns off and the other turns on) is taken to be the time for a full resonant transition, and is given by $(\pi/2)\sqrt{2CL} = 250nSec$.

### 4.2 Problems

At this point, two problems arise.

First, since the minimum pulse-width must be somewhat bigger than the dead-time, the maximum voltage range for the fixed-frequency algorithm is given, as a fraction of the supply voltage, by (period-2*minimum-pulse-width)/period, or approximately 0.775. Since, for high-voltage amplifiers, the voltage ratings of the output devices are a critical limiting factor, this much loss of voltage swing is very significant. For example, in the present situation, it implies that power supply voltages of about $\pm 260V$ are needed to obtain a swing of $\pm 200V$. This raises the maximum voltage stress on the output devices to about $520V$, with the result that $600V$ devices have a margin of only 16%. This is usually too low for good design practice, and so more expensive, higher-voltage MOSFETs must be used. The other alternative is to reduce the switching

frequency (to $200kHz$ for a 90% swing), but since this reduces the peak ripple current, it severely restricts the range over which resonant switching occurs, and so increases the power dissipation and noise.

The variable-frequency modulator has no such problems; its minimum pulse-width is one quarter of the period at zero voltage output, or $1/(4(450kHz))$, which is about $550nSec$ — comfortably greater than the $250nSec$ minimum. The voltage range for the variable-frequency modulator is set by the lowest switching frequency that we allow. For a voltage swing to 90% of the supply voltage, the switching frequency will be about one fifth of its maximum value, or $90kHz$, which is far enough above the filter cutoff frequency of $20kHz$. A $\pm 200V$ swing can therefore be obtained from the $\pm 225V$ supplies. This advantage is in addition to the wider range of loads over which resonant switching occurs for the variable-frequency modulator.

The second problem has to do with the implementation of the amplifier using the TMS320F240. Since the clock for the event timer has a maximum frequency of $20MHz$ [4], there are only 44 counts per cycle at a switching frequency of $450kHz$. This resolution is too low for a good amplifier, and, in particular, it is very difficult to set the dead-time accurately. In addition, the A/D converter has a conversion time of $6\mu Sec$, which gives a maximum switching rate of $166kHz$. While the A/D converter is much faster on the '243 part, and the '28x parts will have faster event clocks, only the '240 was available when the tests were being done. For this reason, only a scaled-down version of the amplifier, as described below, was constructed to test the concepts.

### 4.3 DSP-Based Test Amplifier

The test amplifier was scaled as follows: the supply voltages were taken to be $\pm 25V$, and the load capacitance was unchanged at $0.5\mu F$. Since the most appropriate switching frequencies (in terms of resolution) for the TMS320F240 were in the range 50 to $100kHz$, the cutoff frequency was scaled down by a factor of four, to about $5kHz$. The filter inductor was then taken to have a value of $2mH$ to give this resonant frequency. The MOSFETs used were IR510s, which gave a dead-time of $1\mu Sec$. In order to get a 90% voltage swing, the switching frequency was taken to be $50kHz$ for the fixed-frequency case. Since the variable-frequency algorithm does not have this constraint,a frequency of $75kHz$ at zero-voltage output was chosen. Both fixed and variable frequency algorithms were implemented by using one of the PWM and Full Compare Units together with its Programmable Dead-Band Unit on the TMS320F240, and using one of the A/D converter channels for input.

## 5 Results and Discussion

The results were as expected; while the fixed-frequency unit had lower quiescent power consumption than the variable-frequency (because of the lower switching frequency), the situation was reversed at large-signal outputs, as the fixed-frequency amplifier dropped out of resonant switching. Also, for low-amplitude signals, fixed-frequency switching gave lower distortion than variable-frequency, with the opposite occurring at large amplitudes. In fact, the fixed-frequency amplifier could not reach the 90% amplitude level, since the minimum pulse-width must be somewhat greater than the dead-time, while the variable-frequency amplifier reached this amplitude level without difficulty.

One other noticeable feature was that both types of DSP-controlled amplifiers were significantly less stable with the current feedback than was the analog-controlled version. This is almost certainly due to the phase-lag resulting from the delays associated with sampling and conversion of the input and feedback data.

### 5.1 Comments on Undergraduate Lab

One of the difficulties in teaching an undergraduate laboratory in digital signal processing is that the applications of digital signal processing which are shown tend to fall into a narrow range. In particular, is would be desirable to see digital signal processing applied to something other than purely processing signals. The most obvious candidate for an application area would be control, but a control lab is quite expensive to equip, since it requires much mechanical equipment which is usually far more expensive than electronic parts, and also is not standard equipment in an electrical engineering department. It is possible that control of power electronics would be an interesting, and relatively inexpensive, way of introducing some real control applications into a DSP lab; this idea is currently under consideration.

# 6 Conclusions

More complex, variable frequency PWM algorithms, which are best implemented using DSP control, have been demonstrated, both experimentally and theoretically, to have some advantages over fixed-frequency PWM in the present application. Further advantages, such as the ability to adapt to the load so as to give a flat frequency response, are potentially available, but have not yet been implemented. However, the speed and performance of the available DSP-based PWM controllers is not yet adequate to provide full bandwidth. In particular, it is clear that *much* faster event clocks (e.g., 100MHz) would be useful in these applications.

# 7 References

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