

## Advanced DSP Based Single Phase Power Factor Correction Approach

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**Abstract - In this paper an advanced DSP based single-phase power factor correction approach for clean power is presented. The proposed approach draws near sinusoidal input current even when the input utility voltage is distorted. A closed loop digital algorithm is implemented on a low cost DSP (TMS320F243). The DSP control enables the input current to be synchronized to the fundamental content of the input voltage and be immune to the harmonic voltage distortions. Extensive simulations conducted so far demonstrate input current THD less than 10% in the presence of input voltage distortion.**

### 1. Introduction

Single-phase switching power supplies have been used in commercial, residential, and many other applications due to the advantages in efficiency and smaller size. Rapid growth in computers and communication equipment requiring this type of power supply provides a promising future for the switching power supply industry.

Typical switching power supply utilizes dc-dc converter stage to regulate the output voltage. A problem caused by the converter stage is that it draws pulsating current that contains significant amount of harmonics. These harmonics have been identified to be a major source of problems in electric distribution systems [1]. Harmonic distortion also contributes to poor input power factor (0.6 or less). Current harmonics also cause distortion in the voltage waveform at the point of common coupling and result in problems, such as over heating, over voltage, and many others that lead to equipment malfunction. It is important to reduce the harmonic contents in order to save energy and to comply with harmonic standards such as the IEC-1000-3.

Efforts have been done to improve the performance of switching power supplies by implementing control strategy to improve power factor and reducing the harmonics in the input current. Traditionally, this has been accomplished by using analog power factor correction (PFC). Analog PFC IC's are available from several manufacturers and have been able to provide quality input current. Analog control provides continuous processing of signal, thus allowing very high bandwidth. It also gives infinite resolution of the signal they are measuring.

Analog control, however, also possesses some drawbacks. The number of parts required in the system and their susceptibility to aging and environment variations is an issue. This also leads to high cost of maintenance. Further, analog control once designed is inflexible and performance cannot be optimized for various utility distortions.

In view of this, this paper explores digital implementation of switching power supply control via DSP. Digital control provides advantages such as programmability, less susceptibility to environmental variations and fewer part counts [2]. It also reduces the size of the power supply by containing the complexity of control system within the software.

This paper proposes application of PFC using TMS320F243 DSP. Improvement over regular PFC strategy is proposed. Analysis and design along with experimental results are discussed.

## 2. DSP based single phase PFC

The paper discusses the digital control of single-phase power supply based on analog implementation of average current mode control [3]. A boost converter is chosen for the power stage because the input current is continuous and this produces the lowest level of conducted noise and the best input current waveform. The average current mode control is a type of active PFC. This scheme makes the induction current to track a reference, which is a scaled rectified input voltage. It comprises of two control loops as illustrated in Figure 1. The inner loop responsible for controlling the shape of the inductor current, while the outer loop maintains the output voltage at a certain level. Each loop employs a PI controller to perform its task.

In the voltage loop, the output voltage level is scaled and compared with a voltage reference. The error becomes the input for the PI controller. Output of this particular controller is the scaling factor for the rectified input voltage that is used as the current reference.

In the current loop, the inductor current is compared to the reference current obtained from the step mentioned above. Again, the error goes to the current loop's controller. The controller outputs duty cycle for the switch.

At the existence of power quality problems such as flickers, sag, etc., the input voltage waveform is distorted. The source of the distorted input voltage waveform is the existence of higher frequency harmonics in addition to the voltage's fundamental frequency. This results in the distorted current reference waveform. Unless the problem is fixed, the resulting inductor current will mimic the shape of the distorted voltage. A solution to the problem is to add a bandpass filter in the input voltage feedforward path as shown in Figure 1.

The purpose of proposed bandpass filter is to eliminate unwanted higher harmonic contents that may appear on the input voltage waveform. The pass band of this filter is set around the fundamental frequency (60 Hz). With the higher harmonics eliminated, the current reference  $I_{ref}$  will become half sinusoidal. Ultimately, the inductor current can be maintained at its desired shape. Addition of bandpass filter can be easily done on DSP by adding a new software module. Simulation results in the next section will show how the bandpass filter improves the performance of the PFC circuit under distorted input voltage waveform conditions

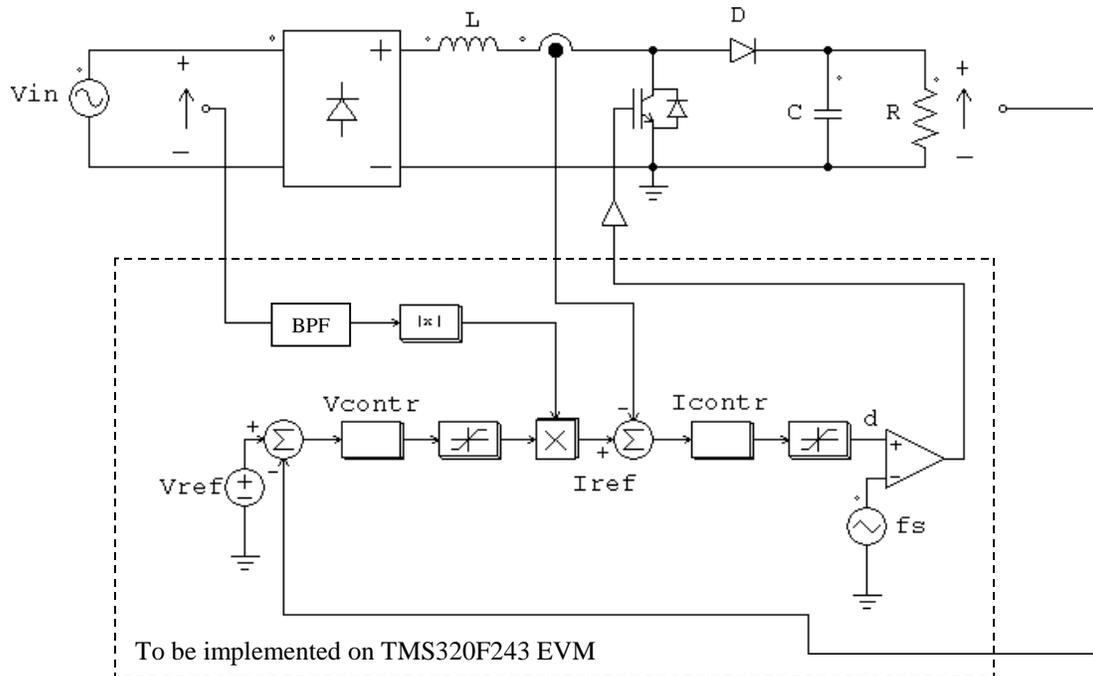


Figure 1. Schematic of the proposed approach.

The DSP used for this purpose is the TMS320F243. This DSP is optimized for digital control and comes with on-chip peripherals, such as 8 channels ADC, Timers, PWM generators, and many others that greatly reduce programming requirement and leaves plenty of processing time for the implementation of PFC algorithms.

### 3. Simulation

Simulation results showed that the designed controllers performed well on full load condition, as shown in Figure 2. The total harmonic distortion (THD) at this condition is 7.63% and near unity power factor at 99.71%.

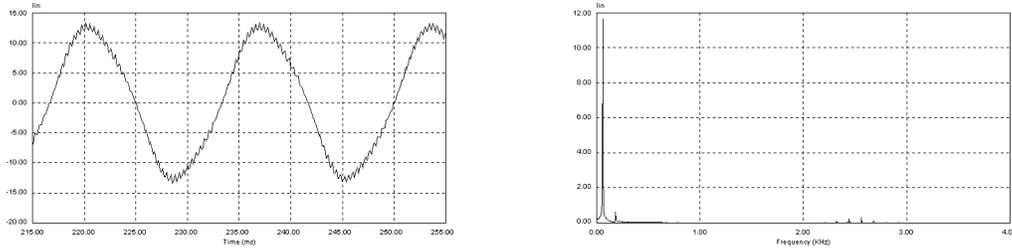


Figure 2. Input line current and its FFT at full load.

Figure 3 shows the performance of the controller under power quality problems, namely third harmonic distortion and voltage notches. Note that the input current waveforms (bottom ones) follow the exact shape of the input voltage waveforms (top ones).

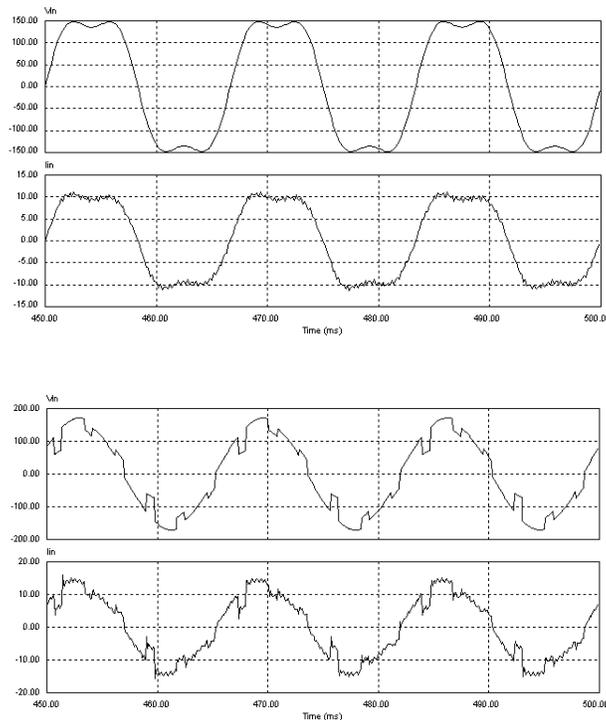


Figure 3. Input voltage and current waveform under power quality problems.

With addition of the bandpass filter, the unwanted harmonics in the input voltage are eliminated in the feedforward path. The resulting control performance with bandpass filter is shown in Figure 4.

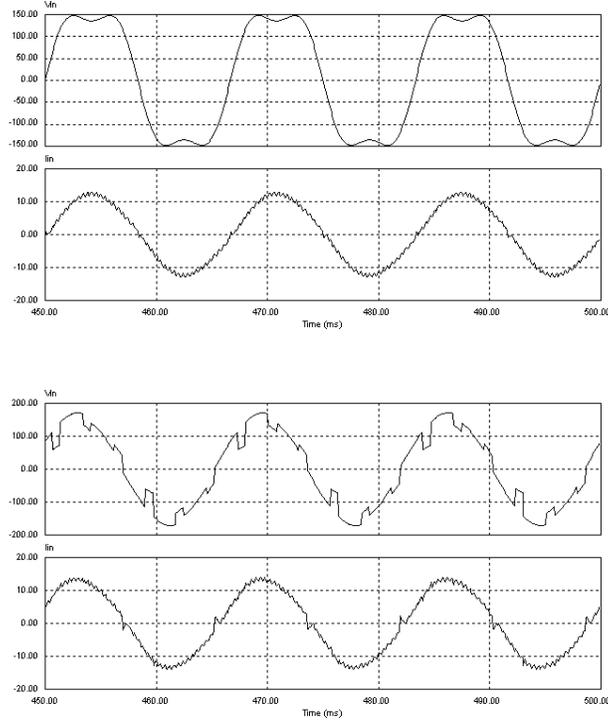


Figure 4. Input voltage and current waveform under power quality problems with addition of bandpass filter.

## 4. DSP implementation

### 4.1. Software

The software developed for the PFC implementation consists of a series of modules performing individual tasks. These modules are linked together under the control of a main program to perform as a complete system. The modular design makes the software more manageable and portable.

Based on the functionality, the main PFC software can be divided into two parts. The first part is the DSP initialization, which includes register, interrupt, and subroutine initializations. These tasks are done once when the program starts. Upon completion of the initialization, the program waits for interrupt calls while performing an infinite loop. The initialization routine flow diagram is shown in Figure 5.

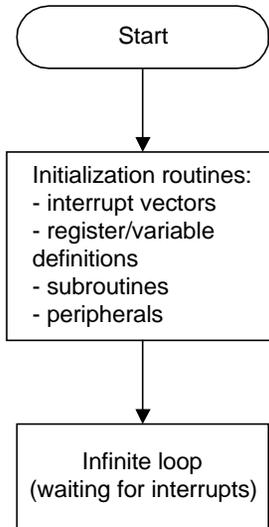


Figure 5. Software initialization diagram.

The other part of the software is the interrupt service routines. These routines are called when a specific event (timer period) occurred, as set in the initialization process. When an interrupt occurs, the main program breaks the infinite loop and goes to the proper interrupt service routine that has been designated to that particular event. Upon finishing the routine, the program continues the infinite loop and waits for the next interrupt call.

The software interrupt routine flows are shown in the diagram in Figure. 6. It utilizes two timer interrupt routines that is called at different frequencies. Timer interrupt 1 has the same frequency as the gate switching frequency. This timer interrupt perform the following tasks:

- Inductor current and output voltage sampling. The values are converted into 15 fractional-bit two's complement representation (Q15), with value ranges from  $-1$  to  $1$ .
- Voltage-loop controller module. This module is basically a PI controller. The proportional gain value of the controller is bigger than  $1$ , so a different number representation than Q15 is chosen. In this case, Q11 format is chosen to allow representation of the integer part of the constant. Accordingly, the output of the controller is also represented in Q11 format to avoid possible overflow.
- Multiplication of the controller output with the rectified input voltage obtained from timer interrupt 2. This is basically a multiplication of two numbers of different formats: Q15 (rectified input voltage) and Q11 (controller output). The product is in Q11 format and becomes the reference current, which will be compared with the inductor current.
- Current-loop controller module. It is also of PI type like the voltage-loop controller. Input of this controller is the difference between the reference current obtained from the previous step and the inductor current sampled at the beginning of the interrupt routine. The controller outputs duty cycle used to generate the switch PWM signal on the next step. Gain constants of this controller are in Q15 format, but since the input is in Q11, the output is also represented in Q11. This number is then converted to non-two's complement representation to generate the PWM signal.
- PWM gate signal generation. Duty cycle is compared with a triangular (saw-tooth) waveform at the switching frequency. The output is the PWM signal from the DSP to be fed to the switch of the boost converter.

Timer 2 calls the other interrupt routine. This routine has frequency slower than the other timer considering that the value that is sampled by this routine has a low frequency. The input voltage has a 60 Hz frequency, and a 4 kHz sample should provide enough accuracy.

Timer interrupt 2 routine does only a couple of tasks. First, it samples the input voltage. Then, it passes the sampled value to a bandpass filter to eliminate harmonic distortion from the waveform. The clean waveform is used to scale the output of voltage loop controller (in timer interrupt 1) and produce the reference for inductor current.

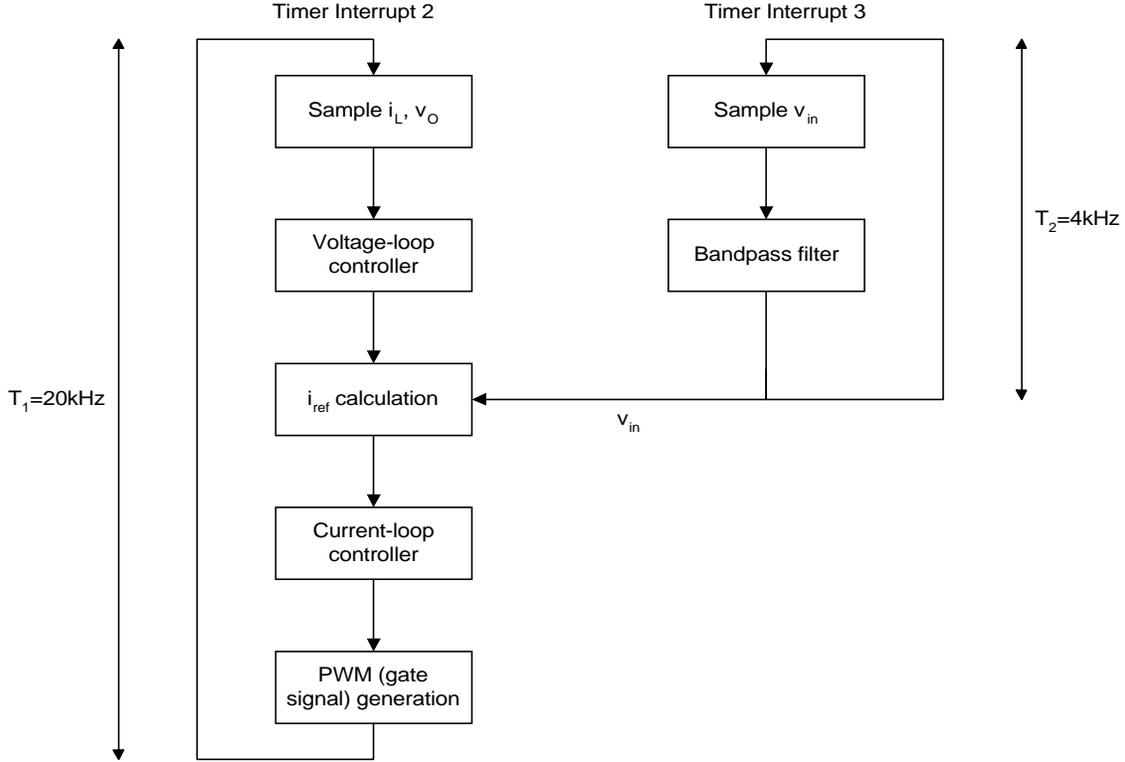


Figure 6. Software flow diagram for interrupt routines.

#### 4.1.1. PI Controller Algorithm

The software was developed based on analog design of the PFC. This fact makes it necessary to convert analog transfer functions to the discrete versions. One of the transfer functions is that of the PI algorithm, which is given by:

$$u(t) = K_p e(t) + K_i \int edt \quad (1)$$

where

- $K_p, K_i$  = PI gain constants
- $u(t)$  = control signal
- $e(t)$  = error signal

To convert to discrete form, the integral term  $edt$  is approximated by summation of rectangles  $\sum e_i T$  where  $T$  is the sampling interval and  $e_i$  is the value of the error signal at sample time  $i$ .

The relation can be written as:

$$\int edt = \sum e_i T \quad (2)$$

The PI algorithm can now be approximate in discrete form by:

$$u_k = K_p e_k + K_i T e_k + K_i T \sum_{n=0}^{k-1} e_n \quad (3)$$

where

$$e_k = y_{ref} - y_k \quad (4)$$

#### 4.1.2. Digital Bandpass Filter Implementation

There are two methods of designing a digital filter in for signal processing, infinite impulse response (IIR) and finite impulse response (FIR). Given a set of frequency-response characteristics, typically a higher-order FIR filter is required to match characteristics of a corresponding IIR filter. FIR filter is normally used in the case when linear phase is important, since only FIR can be designed to have linear phase. Based on the above considerations, IIR filter appears to be a clear choice for the digital filter implementation. It is mainly because of the less memory requirement due to the lower order filter required.

High order IIR filter has a general transfer function given in equation (5).

$$H(z) = \frac{b_0 + b_1 Z^{-1} + \dots + b_M Z^{-M}}{1 + a_1 Z^{-1} + \dots + a_N Z^{-N}} \quad (5)$$

However, when the coefficients ( $a_1 \dots a_N, b_0 \dots b_M$ ) are quantized, the resulting errors can alter the desired filter characteristics. By breaking up the transfer function into lower order sections and connecting them in cascade can reduce the sensitivity to coefficient quantization. It has been suggested in reference [19] to use second order sections for digital IIR filter implementations.

For the implementation, the direct form II network structure [20] is chosen. Consider the transfer function of the second order section given in equation (6).

$$H(z) = \frac{b_0 + b_1 Z^{-1} + b_2 Z^{-2}}{1 + a_1 Z^{-1} + a_2 Z^{-2}} \quad (6)$$

The corresponding direct form II difference equations are:

$$d(n) = x(n) - a_1 d(n-1) - a_2 d(n-2) \quad (7)$$

$$y(n) = b_0 d(n) + b_1 d(n-1) + b_2 d(n-2) \quad (8)$$

The signal flowgraph for this transfer function is shown in Figure 7.

The second order sections can easily be obtained from the high order filter transfer function with help of MATLAB.

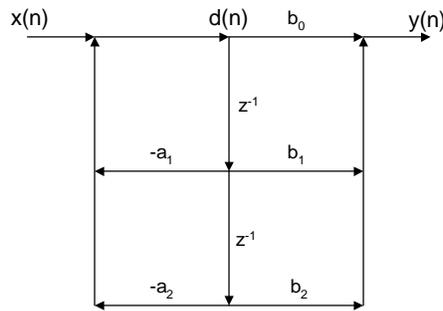


Figure 7. Direct form II structure block diagram.

The next issue is designing the bandpass filter. The bandpass filter to be designed is to filter out the harmonic contents in the input voltage waveform and leaves only the fundamental frequency waveform at 60 Hz. The design parameters for the filter can be set as:

- Center frequency: 60 Hz.
- Passing band: 55-65 Hz (10 Hz wide).
- Stopping band: 0-50 Hz, 70 Hz-infinity.
- Filter order: 4.

Given the above design parameters, an IIR bandpass filter can be designed with help of MATLAB. Elliptic algorithm was chosen and 0.5 dB pass band ripple and 20 dB stop band ripple were selected. The resulting filter frequency and phase responses are shown in Figure 8.

At this point, filter coefficients were obtained. The next step is to convert the 4<sup>th</sup> order filter into two cascaded second order filter. This is done with several MATLAB instructions. The new filter coefficients were then converted to appropriate numbering format and used in the software.

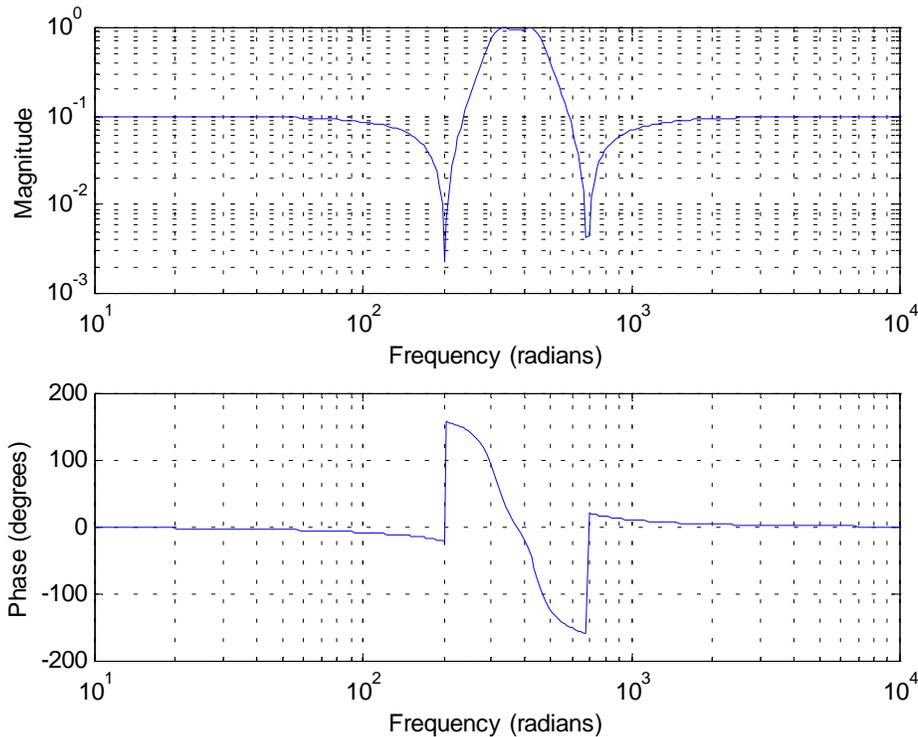


Figure 8. Frequency and phase response of 4<sup>th</sup> order elliptic IIR filter.

#### 4.2. Closed-loop Implementation

Generally, feedback signals from the boost converter are fed to the analog-to-digital converter (ADC) module of the DSP. These signals are isolated and conditioned so that their voltage level is within that of the ADC (0 to 5V). For the voltages, voltage dividers were used to scale down the measured voltages. For the input current sensing, an ASIC type Hall effect current sensor, which has a digital voltage output, was used. Further adjustments (numerical representations) are made within the software.

The output of the DSP is the control signal going to the gate of the boost converter. The gating signal is also isolated by using a shielded optocoupler as shown in the Figure 9. The purpose of this optocoupler is to protect the DSP from voltage spikes or over current from the switch gate that may damage the DSP.

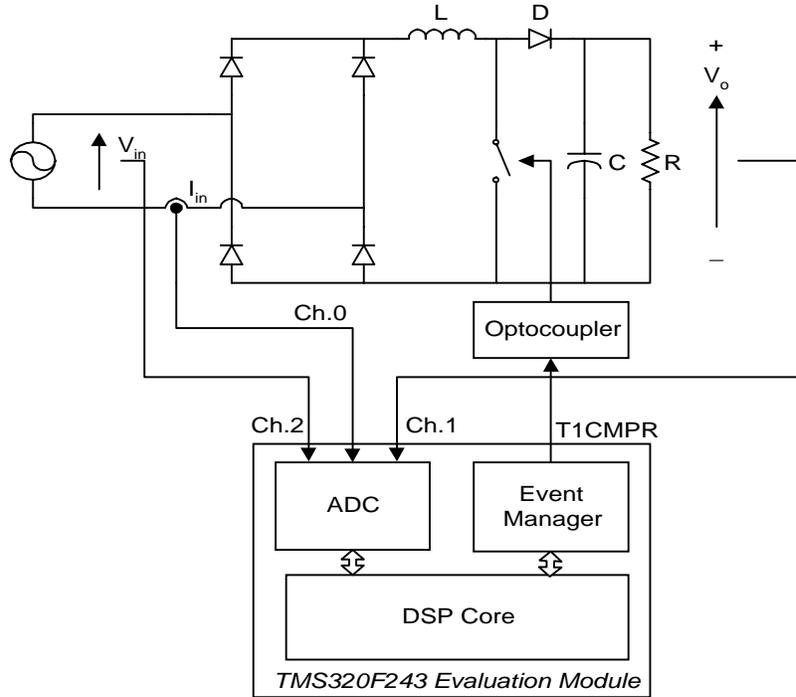


Figure 9. Boost PFC implementation on DSP.

#### 4.3. Preliminary Experimental results and Analysis

The experiment on the implementation of the PFC on the TMS320F243 EVM is currently on going. Figure 10 displays the input voltage waveform (top) and the input current waveform. This preliminary result shows a quite satisfactory performance from the PFC to shape the input current. Further experiments will be done to improve the performance of the PFC and to lower the THD of the input current.

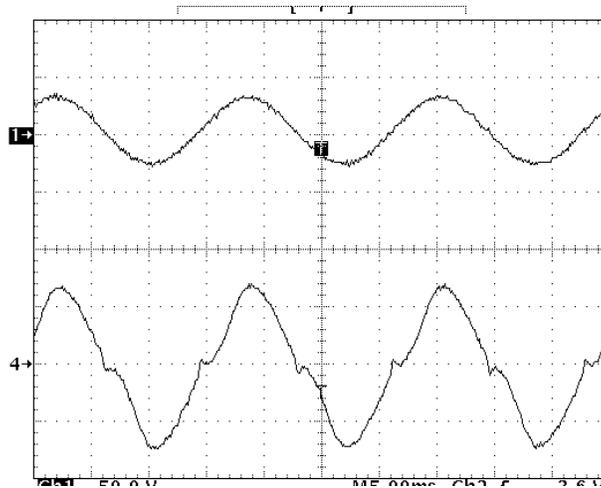


Figure 10. Input voltage and current waveform.

## 5. Conclusion

In this paper, the implementation of power factor correction on TMS320F243 DSP is studied. An improvement over conventional PFC was proposed with addition of a bandpass filter to handle power quality problems. The DSP implementation requires minimum number of external hardware and most of the control algorithms, including the proposed bandpass filter were contained within the software. Preliminary experimental result shows a good performance, while further improvements can be expected.

## 6. References

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