MSP430 Family
Architecture Guide and Module Library

Contents

Figures

Fig. Title Page

Fig. Title Page

Tables

List of Notes

Purpose of guide, and conventions used

The MSP430 User's Guide is intended to assist the development of MSP430 family products by sssemling together and presenting hardware and software information in a manner which will be easy to use by engineers and programmers.

There follows a short description of the nomenclature conventions used for signals and processor states:

- ADC — Analog-to-Digital converter
- CPUOff mode — Low power mode with RAM contents and I/O signals unchanged Modules using auxiliary clock (32 768 Hz crystal) are active
- DCO — Digital controlled oscillator
- LCD — Liquid crystal display
- FF — Flip-Flop
- MAB — Memory address bus. This is the address bus between the individual modules. It can be any width from 16 bits to 4 bits. Together with the MS signal it defines the physical address.
- MDB — Memory data bus. This is the data bus between the individual modules. It can be 8 bits or 16 bits wide.
- MS — Module select. This is the pre-decoded address space. Together with the MAB it defines the physical address.

- MSFR — Module special function register. This is the pre-decoded address space (0h to 0Fh) of the special function registers.
- OSCOff mode — Lowest power mode. RAM contents and I/O signals are unchanged. The crystal oscillator has stopped
- OTP — One-time programmable
- POR — Power-on reset
- PUC — Power-up clea, "1" sets processor's start condition
- SAR — Successive approximation register
- SCI — Serial communication interface to handle synchronous and asynchronous protocols
- SCG — System clock generator
- SFR — Special function register
- SPI — Serial peripheral interface (widely used synchronous serial communication protocol)
- TBD — To be defined
- TOS — Top of stack
- UART — Universal asynchronous receive transmit (most commonly-used serial communication protocol)
- USART — Universal synchronous asynchronous receive transmit
- WD,WDT — Watchdog, Watchdog Timer

Bit Type Convention for Register Bit

- rw: read/write
- r: read only
- r0: read as '0'
- w: write only
- (w): no register bit implemented; writing a '1' will result in a pulse. The register bit is always read as '0'.
- -0,-1: condition after PUC
- -(0),-(1): condition after POR
- h0: cleared by hardware

Symbols

Operations

@	Register indirect addressing
&	Absolute address
-->	Data transfer direction
+	Addition

-	Subtraction
x	Multiplication
/	Division
.AND.	logical AND
.OR.	logical OR
.XOR.	logical Exclusive-OR
.NOT.	logical NOT

Register Symbols

R0 or PC	Register 0 or Program Counter
R1 or SP	Register 1 or Stack Pointer
R2 or SR/CG1	Register 2 or Status Register/Constant Generator 1
R3 or CG2	Register 3 or Constant Generator 2
R4 to R15	Working Register, general-purpose

Contents of Status Register

C	Carry or borrow
Z	Zero
N	Negative
CPUOff	CPU Off Bit
OscOff	System Oscillator Off Bit

GIE	General Interrupt Enable
SCG0	System Clock Generator, Control Bit 0
SCG1	System Clock Generator, Control Bit 1
V	Overflow

Others

=	Equal Sign
‡	Not Equal Sign
>, <,≥,≤	Comparison Signs
" "	ASCII Character inside
h	Hexadecimal Data
b	Binary Data
#	Immediate Data
E	Exponent
&	Absolute Address Mode Indicator

Assembler Directives

.equ	Equate command
.sect	section directive
.word	word data
.byte	byte data
;	comment indicator

1 MSP430 Family

This section discusses the features of the MSP430 family of controllers, having special capabilities for analog processing control. All family members are software compatible, allowing easy migration within the MSP430 family by maintaining a common software base, and common design expertise and development tools.

The concept of a CPU designed for various applications with a 16-bit structure is presented. It uses a "von-Neumann Architecture" and hence has RAM, ROM and all peripherals in one address space.

Topic **Page**

1.1 Features and Capabilities

- Up to 64K byte addressing space as needed, for allocation of ROM, RAM, EERAM and peripherals as needed. Future expansion to 1M byte is planned.
- No limitation of interrupt and subroutine levels due to stack processing
- Only 3 instruction formats. Strong orthogonality without any exception
- 1word/instruction is used, as far as possible
- Seven address modes in the source
- Four address modes in the destination
- External interrupt pins: extended use of Input/Output pins for interrupt capability
- Prioritized interrupts: simultaneously occurring interrupts are handled prioritized)
- Nested interrupt structure: interrupt routines may be interrupted by higher priority interrupts
- Memory mapped peripherals: all registers are in the modules - no RAM space is used
- USART on chip - see device configuration: separate interrupts for transmit and receive
- Timer with interrupt for event counter, timing generation, PWM, ...
- Watchdog
- ADC (10 bits or more) with 8 inputs and current source
- EPROM version (OTP)
- LCD-driver
- Stable processor frequency using a FLL and a clock crystal of 32,768 Hz

- Easy program development because of the orthogonal structure: all instructions with all addressing modes
- C-compiler development has started
- Modular design concept: modules are strictly memory mapped

1.2 System Key Features

- Ultra-low current consumption: CPUOff and OscOff modes
- Full operation down to 2.5 V
- System building blocks: LCD-Drive, A/D-Converter, I/O-Ports, UART, Watchdog Timer, EEPROM ..... all on chip
- Only microcomputer mode; there is no microprocessor mode
- Ease of use
  The powerful and convenient instruction set allows fast software development.
- Software may run in RAM
  Programs loaded into the RAM via the UART or test paths..., can execute jobs under real-time conditions. This reduces test costs and calibration expenses.
- Every ROM/RAM mix is possible in the common address range of 64k byte
- High level language (HLL) programming capabilities
  Large register file (12 general purpose registers)

Stack orientation
Large ROM and RAM spaces
Orthogonal instruction set, without any exceptions
Table processing orientation, due to addressing modes

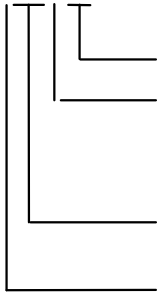
- Fast hexadecimal-to-decimal conversion with special instruction DADD
- Instructions are commonly used for ROM references, RAM access, data handling, I/Os and other peripherals: there are no special instructions!
- Potential of CPU far exceeds the requirements of intelligent sensor signal systems. The real-time capability opens fields in other low power systems, including the usage of other peripherals e.g. DTM transceiver for wired telecom

1.3 MSP430 Family Devices

The MSP430 family of devices can be summarized as follows:

- Nomenclature used:

MSP430CxxxQFN



Package Code, 1 or 2 characters

Temperature range, 1 character
I: -40 degree to +85 degree
A: -40 degree to +125 degree
Q: customized

Unique number for each family member
or software number, 3 characters

Memory Code: C: CMOS, ROM version
P: OTP, on-time programmable - EPROM versior
E: EPROM version, windowed package
S: SRAM, RAM version for code memory

- Development tools include the software simulator **DT430**, assembler and linker **ASM430/LNK430**, C-compiler (under development) **CS430/CW430**, and hardware in-circuit emulator **ICE430**. All development tools are PC-based using integrated desktop features compatible with the windows SAA standard.

The minimum requirements for the PC are:
IBM compatible
DOS 5.0 or later
Windows 3.1, 3.11 or ‘95
Personal computer with a 486 or higher processor running
8 MB of available memory
One 3.5" high-density disk drive
A hard disk with 5 MB available

	MSP430x310	MSP430x320	MSP430x330
Max. internal clock rate Frequency of crystal	1.1 MHz @3V 3.3 MHz @5V 32.768 kHz	1.1 MHz @3V 2.2 MHz @5V 32.768 kHz	1.1 MHz @3V 2.2 MHz @5V 32.768 kHz
Operating Temperature	-40^{o}C to +85^{o}C	-40^{o}C to +85^{o}C	-40^{o}C to +85^{o}C
Program memory MSP430Cxxx: MSP430Pxxx: MSP430Exxx: Memory expansion	 4/8/12k byte ROM 8K byte OTP 8K byte wind. EPROM NO	 8K byte ROM 16K byte OTP 16K byte wind. EPROM NO	 24K byte ROM 32K byte OTP 32K byte wind. EPROM NO
Internal RAM	256/512 Bytes	256 Bytes	1024 Bytes
Data EEPROM	No	No	No

1

Modules			
HW Multiply	No	No	Yes
Port0, 8-bit, all interrupt	Yes	Yes	Yes
Port1, 8-bit, all interrupt			Yes
Port2, 8-bit, all interrupt			Yes
Port3			Yes
Port4			Yes
Watchdog timer	Yes	Yes	Yes
Basic Timer1/Real time	Yes	Yes	Yes
clock	Yes	Yes	Yes
8-bit Timer/Counter	Yes	Yes	Yes
Timer/Port ,1x8-bit	Yes	Yes	Yes
Timer_A,16-bit	No	No	Yes
SPI	No	No	USART, SPI mode
UART	(8b Tim./Cnt. + SW)	(8b Tim./Cnt. + SW)	USART, UART mode or (8b Tim./Cnt. + SW)
LCD	Max. 23x4 segments	Max. 21x4 segments	Max. 30x4 segments
ADC/Current source	Yes/Yes	see Timer/Port	see Timer/Port
DAC	No	No	No
I/O lines	9	9	40
Input lines	1	7	1
Output lines	27	25	34

Interrupts/Reset External Vectors total Sources total	 11 16	 11 16	 1 + 24 16
Package Type	64 QFP	56 SSOP	100 QFP

Table 1.1: MSP430 Family Feature Summary