## 14 Liquid Crystal Display Drive

<table>
<thead>
<tr>
<th>Topic</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>14.1</td>
<td>Basics of LCD Drive</td>
</tr>
<tr>
<td>14.2</td>
<td>LCD Controller/Driver</td>
</tr>
<tr>
<td>14.3</td>
<td>LCD Port Function</td>
</tr>
<tr>
<td>14.4</td>
<td>Application Example showing mixed LCD and Port Mode</td>
</tr>
</tbody>
</table>
14.1 Basics of LCD Drive

Liquid crystal displays use ambient luminescence to display information and do not send out light actively. This results in low power consumption. The requirement for visible displayed information is sufficient ambient luminescence.

The liquid crystal must be driven with alternating voltage. DC drive would destroy the liquid crystal. This AC drive requirement is the main factor for any power consumption. The electrical equivalence for the driving stage is a capacitor. Its electrodes are the back plane or common plane, controlled by signal COMn and the segment driven by SEGn. The frequency of the AC drive is low - in the range of 1000 Hz to 30 Hz. The data sheets of the LCD manufacturer give defined ranges for this frequency.

Different methods of controlling LC displays were developed in the past. The different driving methods are applied as a compromise between number of segments, number of pins at display and driving source, LCD contrast, temperature range, ......

Multiplexing methods reduce the number of pins needed.

The MSP430 Family's LCD module supports four driving methods:

- Static
- 2MUX or 1/2 duty, 1/2 bias
- 3MUX or 1/3 duty, 1/3 bias
- 4MUX or 1/4 duty, 1/3 bias.

The static method needs one pin for common plane (COM0) and one pin for each segment:

\[\text{#-of-pins} = 1 + \#-\text{of-segments}\]

The 2MUX method needs two pins for common plane (COM0, COM1) and one pin for two segments:

\[\text{#-of-pins} = \text{Integer}[2 + (\#-\text{of-segments}/2)]\]

The 3MUX method needs three pins for common plane (COM0, COM1, COM2) and one pin for three segments:

\[\text{#-of-pins} = \text{Integer}[3 + (\#-\text{of-segments}/3)]\]

The 4MUX method needs four pins for common plane (COM0, COM1, COM2, COM3) and one pin for four segments:

\[\text{#-of-pins} = \text{Integer}[4 + (\#-\text{of-segments}/4)]\]

The increase of the multiplex rate reduces the number of pins required. The continuous reduction of pin counts is demonstrated by an application that uses 80 segments:

- **Static method**: \(#-\text{of-pins} = (1 + 80) = 81\)
- **2MUX**: \(#-\text{of-pins} = (2 + 80/2) = 42\)
- **3MUX**: \(#-\text{of-pins} = (3 + 80/3) = 30\)
- **4MUX**: \(#-\text{of-pins} = (4 + 80/4) = 24\)
Static Driving Method

In the static drive method each segment line drives one segment. The example shows one digit of the liquid crystal displaying ‘5’, including an example of the connections together with the output wave forms.

Figure 14.1: Example of static wave form drive
Two MUX, 1/2 Bias

In the 2MUX drive each segment line drives two segments. The example shows one digit of the liquid crystal display displaying '5', including an example of the connections, together with the output wave forms.

Figure 14.2: Example of 2MUX wave form drive
Three MUX, $1/3$ Bias

In the 3MUX drive each segment line drives three segments. The example shows one digit of the liquid crystal display displaying '5', including an example of the connections, together with the output wave forms.

![Diagram of 3MUX drive](image)

**Figure 14.3:** Example of 3MUX wave form drive
Four MUX, $\frac{1}{3}$ Bias

In the 4MUX drive each segment line drives four segments. The example shows one digit of the liquid crystal display displaying '5', including an example of the connections, together with the output wave forms.

![Diagram of 4MUX wave form drive](image)

**Figure 14.4:** Example of 4MUX wave form drive
14.2 LCD Controller/Driver

The LCD controller/driver peripheral generates the segment and common signals according to the data in the display data memory. It contains all functional blocks to drive an external directly connected LCD. The main blocks in the LCD peripherals are:

- Data memory containing the segment information
- Timing generator
- Module bus interface
- LCD Module: Analog voltage applied externally
- LCD+ Module only: Analog voltage generator internally

![LCD Controller/Driver Block Diagram](image)

**Figure 14.5:** LCD Controller/Driver Block Diagram
Differences between LCD Module and LCD+ Module:

<table>
<thead>
<tr>
<th></th>
<th>LCD Module</th>
<th>LCD+ Module</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Voltage Generation</td>
<td>external</td>
<td>internal</td>
</tr>
<tr>
<td>options:</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• 2 inputs R23, R13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_1 = VCC )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_5 = VSS )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• 3 inputs R23, R13, R03</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_1 = VCC )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• 4 inputs R33, R23, R13, R03</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Control bit LCDM1</td>
<td>unused</td>
<td>selects impedance of R-Ladder</td>
</tr>
<tr>
<td>• Control bit LCDM0</td>
<td>• stops timing generator</td>
<td>• stops timing generator</td>
</tr>
<tr>
<td></td>
<td>• stops current through R-Ladder</td>
<td></td>
</tr>
</tbody>
</table>

14.2.1 LCD Controller/Driver Functions

The functions of the LCD Controller/Driver are:

• Reads automatically data from the display memory, and generates the segment and common signals

• Four different display modes are selectable:
  Static mode
  2MUX, 1/2 bias
  3MUX, 1/3 bias
  4MUX, 1/3 bias.
  Within the basic timer BT, there are two bits to select one of four different frame frequencies.

• Segment signal outputs can be switched to an output port

• Display memory not used for segment information can be used as a normal memory.

• Operation via the basic timer with the auxiliary clock (ACLK).

• LCD+ Module only:
  Resistive network to supply the analog voltage levels for LCD drive
  One bit in the control register LCDCTL controls the switch through which the resistive network is connected with V1.

The frame frequency of the LCD lines is:

• Static method:  \( f_{\text{frame}} = \frac{1}{2} \times f_{\text{LCD}} \)

• 2MUX:  \( f_{\text{frame}} = \frac{1}{4} \times f_{\text{LCD}} \)

• 3MUX:  \( f_{\text{frame}} = \frac{1}{6} \times f_{\text{LCD}} \)

• 4MUX:  \( f_{\text{frame}} = \frac{1}{8} \times f_{\text{LCD}} \)
**LCD+ Module:**

The analog voltage is generated internally.

When the OSCOff bit in the status register is set, the power supply to the resistor network is switched off independently of the LCDM0 bit.

During static mode, the analog generator is switched to be inactive, since the static mode uses only V1 and V5 levels. Supply current consumption is reduced.

![Diagram of LCD+ Module](image)

**Figure 14.6:** Internal analog voltage generated by LCD+ Module
LCD Module:

The analog voltage is supplied externally, applied on pins R33**, R23, R13, R03**.

---

** Supply pins R33 and R03 are optional. Devices without R33 and R03 pins will have V1 tied to VCC and V5 tied to VSS. External resistor ladder should be connected to VCC and VSS.

---

* ≡ to the position of the switch

---

** Supply pins for V1 and V5 are optional. Devices without R33 and R03 pins will have V1 tied to VCC and V5 tied to VSS. External resistor ladder should be connected to VCC and VSS.

---

** Supply pins R33 and R03 are optional. Please see device data-sheet.
14.2.2 LCD Control & Mode Register

The content of the LCD control & mode register defines the different operating conditions. The LCD module is byte structured and should be accessed by byte instructions (suffix .B).

<table>
<thead>
<tr>
<th>LCDCTL</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCDM7</td>
<td>rw-0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LCDM6</td>
<td>rw-0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LCDM5</td>
<td>rw-0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LCDM4</td>
<td>rw-0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LCDM3</td>
<td>rw-0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LCDM2</td>
<td>rw-0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LCDM1</td>
<td>rw-0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LCDM0</td>
<td>rw-0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**LCDM0:**
- **LCDM0 = 0:** The timing generator is switched off. Common and segment lines are "L". Outputs selected for port output lines are not affected.
- **LCDM0 = 1:** Common and segment lines output the signal corresponding to the display memory. Outputs selected for port output lines are not affected.

**LCD+ Module:** Power supply to resistor network is off.

**LCDM0 = 1:** Common and segment lines output the signal corresponding to the display memory. Outputs selected for port output lines are not affected.

**LCD+ Module:** Power supply to resistor network is switched on at 2MUX, 3MUX and 4MUX not at static mode.

**LCDM1:** This bit selects the LCD drive magnitude, by selecting the internal resistance of the Analog Generator. It is only valid along with the LCD+ Module.
- **LCDM1 = 0:** High impedance of Analog Generator.
- **LCDM1 = 1:** Low impedance of Analog Generator.

**LCDM2,3,4:** These three bits select the display mode and can switch the segment output to non-selected level.

<table>
<thead>
<tr>
<th>LCDM4</th>
<th>LCDM3</th>
<th>LCDM2</th>
<th>Display mode</th>
<th>Bias, LCD+</th>
<th>Bias, LCD</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>0</td>
<td>Not affected, Display is off - all Segment signals are non-selected level. The port outputs remain stable</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Static mode</td>
<td>1/1</td>
<td>R33*, R03*</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>2MUX mode</td>
<td>1/2</td>
<td>R33*, R13, R03*</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>3MUX mode</td>
<td>1/3</td>
<td>R33*, R23, R13, R03*</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>4MUX mode</td>
<td>1/3</td>
<td>R33*, R23, R13, R03*</td>
</tr>
</tbody>
</table>

* optional pins

The signal LCDM2 disables (0) or enables (1) the segment lines. This is done with an AND combination with each individual segment information. It is located in the parallel serial conversion block between the output of the display memory and the segment output control. The segment information in the display memory remains.

The major purpose of this function is to support applications with flashing displays.
LCDM5,6,7: The information of the three bits selects groups of outputs to carry segment information or bit port information. The outputs selected for port function are driven with the state of the display memory bit, and are no longer part of the LCD segment lines.

<table>
<thead>
<tr>
<th>LCDM7</th>
<th>LCDM6</th>
<th>LCDM5</th>
<th>Group0</th>
<th>Group1</th>
<th>Group2</th>
<th>Group3</th>
<th>Group4</th>
<th>Group5</th>
<th>Group6</th>
<th>Group7</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>S0-S1</td>
<td>S0-S1</td>
<td>O2-S5</td>
<td>O6-S9</td>
<td>O10-O13</td>
<td>O14-O17</td>
<td>O18-O21</td>
<td>O22-O25</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>S0-S1</td>
<td>S2-S5</td>
<td>O6-O9</td>
<td>O10-O13</td>
<td>O14-O17</td>
<td>O18-O21</td>
<td>O22-O25</td>
<td>O26-O29</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>S0-S1</td>
<td>S2-S5</td>
<td>S6-S9</td>
<td>O10-O13</td>
<td>O14-O17</td>
<td>O18-O21</td>
<td>O22-O25</td>
<td>O26-O29</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>S0-S1</td>
<td>S2-S5</td>
<td>S6-S9</td>
<td>S10-S13</td>
<td>O14-O17</td>
<td>O18-O21</td>
<td>O22-O25</td>
<td>O26-O29</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>S0-S1</td>
<td>S2-S5</td>
<td>S6-S9</td>
<td>S10-S13</td>
<td>S14-S17</td>
<td>O18-O21</td>
<td>O22-O25</td>
<td>O26-O29</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>S0-S1</td>
<td>S2-S5</td>
<td>S6-S9</td>
<td>S10-S13</td>
<td>S14-S17</td>
<td>S18-S21</td>
<td>O22-O25</td>
<td>O26-O29</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>S0-S1</td>
<td>S2-S5</td>
<td>S6-S9</td>
<td>S10-S13</td>
<td>S14-S17</td>
<td>S18-S21</td>
<td>S22-S25</td>
<td>O26-O29</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>S0-S1</td>
<td>S2-S5</td>
<td>S6-S9</td>
<td>S10-S13</td>
<td>S14-S17</td>
<td>S18-S21</td>
<td>S22-S25</td>
<td>S26-S29</td>
</tr>
</tbody>
</table>

Note: LCD control bits
The control bits LCDM5 ... LCDM7 are reset with PUC.

Function Seg: The Sxx signals are part of the display driving signals, and carry modulated voltage levels according to the time frame of the common lines.

Function Port: The signals selected for 'port' function are static signals. They take two digital levels according to bits in the display memory. The logical state of the bits is taken from bit 0 to bit 3 for even S-lines (n=3,5,.....) and from bit 4 to bit 7 for odd S-lines (n=2,4,.....).

Figure 14.8: Information control
14.2.3 LC Display Memory

The LC Display Memory holds the information to be displayed during all operating and power down modes. The bits in the memory are directly attached to the segments of the liquid crystal display. The figures displayed at the LCD are decoded by the software from the BCD or binary representation to the segment/common combination of the individual display. The bit information in the memory matches with one common line and one segment line. The bit information in the memory corresponds to the selection of segments - a bit set in the memory is identical with segment selection 'on' and reverse.

One segment line carries the on/off state of one to four segments depending on the multiplex rate:

- Static drive  -> state of one segment/segment line
- 2MUX drive  -> state of two segment/segment line
- 3MUX drive  -> state of three segment/segment line
- 4MUX drive  -> state of four segment/segment line

The timing generator of the LCD controller/driver drives the conversion of the parallel information stored in the LC Display Memory into the serial information required for the segment line signal. The bits of the LC Display Memory are hard wired to the common lines:

- Static drive  -> COM0: Bit 0 to Sn, Bit 4 to Sn+1
- 2MUX drive  -> COM0: Bit 0 to Sn, Bit 4 to Sn+1, COM1: Bit 1 to Sn, Bit 5 to Sn+1
- 3MUX drive  -> COM0: Bit 0 to Sn, Bit 4 to Sn+1, COM1: Bit 1 to Sn, Bit 5 to Sn+1, COM2: Bit 2 to Sn, Bit 6 to Sn+1
- 4MUX drive  -> COM0: Bit 0 to Sn, Bit 4 to Sn+1, COM1: Bit 1 to Sn, Bit 5 to Sn+1, COM2: Bit 2 to Sn, Bit 6 to Sn+1, COM3: Bit 3 to Sn, Bit 7 to Sn+1

Figure 14.9: Bits of Display Memory attached to Segment lines
Display memory using the static driving method

The static driving method uses one common line. The active common line is COM0. In this mode BIT0 and BIT4 are used for segment information. The other bits can be used like any other memory.

The maximum number of segments is 30.

Figure 14.10: Use of Display Memory with the static driving method
Display memory using 2MUX, 1/2 bias driving method

The 2MUX driving method uses two common lines. The active common lines are COM0 and COM1. In this mode the BIT0, BIT1, BIT4 and BIT5 are used for segment information. The other bits can be used like any other memory.

The maximum number of segments is 60.

![Diagram of Display Memory with the 2MUX method]

**Figure 14.11:** Use of Display Memory with the 2MUX method
Display memory using 3MUX, 1/3 bias driving method

The 3MUX driving method uses three common lines. The active common lines are COM0, COM1 and COM2. In this mode BIT0, BIT1, BIT2, BIT4, BIT5 and BIT6 are used for segment information. The other bits can be used like any other memory.

The maximum number of segments is 90.

![Diagram of display memory with 3MUX method](image)

**Figure 14.12:** Use of Display Memory with the 3MUX method
Display memory using 4MUX, 1/3 bias driving method

The 4MUX driving method uses four common lines. The active common lines are COM0, COM1, COM2 and COM3. In this mode BIT0, BIT1, BIT2, BIT3, BIT4, BIT5, BIT6 and BIT7 are used for segment information.

The maximum number of segments is 120.

<table>
<thead>
<tr>
<th>MAB</th>
<th>BIT</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>03Fh</td>
<td>a</td>
<td>b</td>
<td>c</td>
<td>h</td>
<td>f</td>
<td>g</td>
<td>e</td>
<td>d</td>
<td></td>
</tr>
<tr>
<td>03Eh</td>
<td>a</td>
<td>b</td>
<td>c</td>
<td>h</td>
<td>f</td>
<td>g</td>
<td>e</td>
<td>d</td>
<td></td>
</tr>
<tr>
<td>03Dh</td>
<td>a</td>
<td>b</td>
<td>c</td>
<td>h</td>
<td>f</td>
<td>g</td>
<td>e</td>
<td>d</td>
<td></td>
</tr>
<tr>
<td>03Ch</td>
<td>a</td>
<td>b</td>
<td>c</td>
<td>h</td>
<td>f</td>
<td>g</td>
<td>e</td>
<td>d</td>
<td></td>
</tr>
<tr>
<td>03Bh</td>
<td>a</td>
<td>b</td>
<td>c</td>
<td>h</td>
<td>f</td>
<td>g</td>
<td>e</td>
<td>d</td>
<td></td>
</tr>
<tr>
<td>03Ah</td>
<td>a</td>
<td>b</td>
<td>c</td>
<td>h</td>
<td>f</td>
<td>g</td>
<td>e</td>
<td>d</td>
<td></td>
</tr>
<tr>
<td>039h</td>
<td>a</td>
<td>b</td>
<td>c</td>
<td>h</td>
<td>f</td>
<td>g</td>
<td>e</td>
<td>d</td>
<td></td>
</tr>
<tr>
<td>038h</td>
<td>a</td>
<td>b</td>
<td>c</td>
<td>h</td>
<td>f</td>
<td>g</td>
<td>e</td>
<td>d</td>
<td></td>
</tr>
<tr>
<td>037h</td>
<td>a</td>
<td>b</td>
<td>c</td>
<td>h</td>
<td>f</td>
<td>g</td>
<td>e</td>
<td>d</td>
<td></td>
</tr>
<tr>
<td>036h</td>
<td>a</td>
<td>b</td>
<td>c</td>
<td>h</td>
<td>f</td>
<td>g</td>
<td>e</td>
<td>d</td>
<td></td>
</tr>
<tr>
<td>035h</td>
<td>a</td>
<td>b</td>
<td>c</td>
<td>h</td>
<td>f</td>
<td>g</td>
<td>e</td>
<td>d</td>
<td></td>
</tr>
<tr>
<td>034h</td>
<td>a</td>
<td>b</td>
<td>c</td>
<td>h</td>
<td>f</td>
<td>g</td>
<td>e</td>
<td>d</td>
<td></td>
</tr>
<tr>
<td>033h</td>
<td>a</td>
<td>b</td>
<td>c</td>
<td>h</td>
<td>f</td>
<td>g</td>
<td>e</td>
<td>d</td>
<td></td>
</tr>
<tr>
<td>032h</td>
<td>a</td>
<td>b</td>
<td>c</td>
<td>h</td>
<td>f</td>
<td>g</td>
<td>e</td>
<td>d</td>
<td></td>
</tr>
<tr>
<td>031h</td>
<td>a</td>
<td>b</td>
<td>c</td>
<td>h</td>
<td>f</td>
<td>g</td>
<td>e</td>
<td>d</td>
<td></td>
</tr>
</tbody>
</table>

Figure 14.13: Use of Display Memory with the 4MUX method
14.2.4 Software Examples for LCD Operation

The examples in this paragraph demonstrate the software to display digits on the LCD. They used the standard nomenclature of 7-segment digits.

Software for 4MUX, 1/3 bias LCD

```assembly
.sect "lcd4mux",0f000h
; The 4MUX rate is the most easy-to-handle display rate. All eight segments of a digit
; are located in one display memory byte
;
.a .EQU 080h
.b .EQU 040h
.c .EQU 020h
.d .EQU 001h
.e .EQU 002h
.f .EQU 008h
.g .EQU 004h
.h .EQU 010h
;
; The LSDigit of register Rx (000m) should be displayed.
; The Table represents the 'on'-segments according to the content of Rx.
;
.LCD1 .EQU 00031h ; Address of LC Display Memory
...........
.LCD15 .EQU 0003Fh
...........
                      
;                      
; MOV.B Table(Rx),&LCD_n ; n = 1 ..... 15
; all eight segments are written to the
; display memory
;
;                      
; Table .BYTE a+b+c+d+e+f ; displays "0"
.BYTE b+c ; displays "1"
...........
...........
       .BYTE b+c+d+e+g ; displays "d"
.BYTE a+d+e+f+g ; displays "E"
.BYTE a+e+f+g ; displays "F"
```
Software for 3MUX, 1/3 bias LCD

; The 3MUX rate supports nine segments instead of eight segments for each digit.
; The nine segments of a digit are located in 1 ½ display memory bytes.

a .EQU 0040h
b .EQU 0400h
c .EQU 0200h
d .EQU 0010h
e .EQU 0001h
f .EQU 0002h
g .EQU 0020h
h .EQU 0100h
Y .EQU 0004h

; The LSDigit of register Rx (000m) should be displayed.
; The Table represents the 'on'-segments according to the LSDigit of register of Rx.
; The register Ry is used for temporary memory

LCD1 .EQU 00031h

............

LCD15 .EQU 0003Fh

............

ODDDIG RLA Rx

MOV Table(Rx),Ry ; Load segment information to temporary mem.

MOV.B Ry,&LCD n ; write 'a, b, c, d, e, f' of Digit n (LowByte)

SWPB Ry ; (Ry) = 0agd 0Yfe

BIC.B #07h,&LCD n+1 ; write 'b, c, h' of Digit n (HighByte)

BIS.B Ry,&LCD n+1.....

EVNDIG RLA Rx

MOV Table(Rx),Ry ; Load segment information to temporary mem.

RLA Ry ; (Ry) = 0000 bch0 agd0 Yfe0

RLA Ry ; (Ry) = 000b ch0a gd0Y fe00

RLA Ry ; (Ry) = 00bc h0ag d0Yf e000

RLA Ry ; (Ry) = 0bch 0agd 0Yfe 0000

BIC.B #070h,&LCD n+1 ; write 'Y, f, e' of Digit n+1 (LowByte)

BIS.B Ry,&LCD n+1.....

SWPB Ry ; (Ry) = 0Yfe 0000 bch0 0agd

MOV.B Ry,&LCD n+2 ; write 'b, c, h, a, g, d' of Digit n+1 (HighByte)
<table>
<thead>
<tr>
<th>Table</th>
<th>.WORD a+b+c+d+e+f ; displays &quot;0&quot;</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>.WORD b+c ; displays &quot;1&quot;</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>.WORD a+e+f+g ; displays &quot;F&quot;</td>
</tr>
</tbody>
</table>
Software for 2MUX, 1/2 bias LCD

.sect "lcd2mux",0f000h
; All eight segments of a digit are located in two display memory bytes with the
; 2MUX display rate
;
; a  .EQU 002h
b  .EQU 020h
c  .EQU 008h
d  .EQU 004h
e  .EQU 040h
f  .EQU 001h
g  .EQU 080h
h  .EQU 010h
;
; The register content of Rx (000m) should be displayed.
; The Table represents the 'on'-segments according to the content of Rx.
;
............
LCD1  .EQU 00031h
............
LCD15  .EQU 0003Fh
;

............
MOV.B  Table(Rx),Ry  ; Load segment information to
temporary mem.
MOV.B  Ry,&LCDn  ; (Ry) = 0000 0000 gebh cdaf
       ; Note:
       ; All bits of an LCD memory byte are
written
RRA  Ry  ; (Ry) = 0000 0000 0geb hcad
RRA  Ry  ; (Ry) = 0000 0000 00ge bhd
MOV.B  Ry,&LCDn+1  ; Note:
       ; All bits of an LCD memory byte are
written

............
Table  .BYTE a+b+c+d+e+f  ; displays "0"
............
      .BYTE a+b+c+d+e+f+g+h  ; displays "8"
............
............
............
............
Software for static LCD

.sect "lcd1mux",0f000h
; All eight segments of a digit are located in four display memory bytes with the
; static display method.
;
  a .EQU 001h
  b .EQU 010h
  c .EQU 002h
  d .EQU 020h
  e .EQU 004h
  f .EQU 040h
  g .EQU 008h
  h .EQU 080h
;
; The register content of Rx should be displayed.
; The Table represents the 'on'-segments according to the content of Rx.
;
...........

LCD1 .EQU 00031h
...........
...........
LCD15 .EQU 0003Fh
...........

............
MOV.B Table(Rx),Ry ; Load segment information to temporary
; mem.
; (Ry) = 0000 0000 hfdb geca
MOV.B Ry,&LCDn ; Note:
; All bits of an LCD memory byte are written
RRA Ry
; (Ry) = 0000 0000 0hfd bgec
MOV.B Ry,&LCDn+1 ; Note:
; All bits of an LCD memory byte are written
RRA Ry
; (Ry) = 0000 0000 00hf dbge
MOV.B Ry,&LCDn+2 ; Note:
; All bits of an LCD memory byte are written
RRA Ry
; (Ry) = 0000 0000 000h fdbg
MOV.B Ry,&LCDn+3 ; Note:
; All bits of an LCD memory byte are written
	
............
<table>
<thead>
<tr>
<th>Table</th>
<th>.BYTE</th>
<th>a+b+c+d+e+f ; displays &quot;0&quot;</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>.BYTE</td>
<td>b+c ; displays &quot;1&quot;</td>
</tr>
<tr>
<td></td>
<td>.......</td>
<td></td>
</tr>
<tr>
<td></td>
<td>.......</td>
<td></td>
</tr>
<tr>
<td></td>
<td>.BYTE</td>
<td></td>
</tr>
<tr>
<td></td>
<td>.......</td>
<td></td>
</tr>
</tbody>
</table>
14.3 LCD Port Function

The large number of LCD common and segment lines, together with the fixed number of pins of the package version, could limit the degree of integration. To support applications which require a reduced number of segments, the signals LCDM5 to LCDM7 can switch the function from segment lines to output lines in groups of four bits. These outputs can be used with the application for various functions. Bits in the display memory define the logical state of the signals. The output signals are digitally switched, either near to ground GND, or near to supply voltage VCC.

The nomenclature convention for signals used as segment lines is Sxx and as port functions is Oxx. A pin is identified equally with the same xx representation. The letter S or O states the function of that pin.

<table>
<thead>
<tr>
<th>LCDM7</th>
<th>LCDM6</th>
<th>LCDM5</th>
<th>Group0</th>
<th>Group1</th>
<th>Group2</th>
<th>Group3</th>
<th>Group4</th>
<th>Group5</th>
<th>Group6</th>
<th>Group7</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>S0-S1</td>
<td>O2-05</td>
<td>O6-09</td>
<td>O10-013</td>
<td>O14-017</td>
<td>O18-021</td>
<td>O22-025</td>
<td>O26-029</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>S0-S1</td>
<td>S2-S5</td>
<td>O6-09</td>
<td>O10-013</td>
<td>O14-017</td>
<td>O18-021</td>
<td>O22-025</td>
<td>O26-029</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>S0-S1</td>
<td>S2-S5</td>
<td>S6-S9</td>
<td>O10-013</td>
<td>O14-017</td>
<td>O18-021</td>
<td>O22-025</td>
<td>O26-029</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>S0-S1</td>
<td>S2-S5</td>
<td>S6-S9</td>
<td>S10-S13</td>
<td>O14-017</td>
<td>O18-021</td>
<td>O22-025</td>
<td>O26-029</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>S0-S1</td>
<td>S2-S5</td>
<td>S6-S9</td>
<td>S10-S13</td>
<td>S14-S17</td>
<td>O18-021</td>
<td>O22-025</td>
<td>O26-029</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>S0-S1</td>
<td>S2-S5</td>
<td>S6-S9</td>
<td>S10-S13</td>
<td>S14-S17</td>
<td>S18-21</td>
<td>S22-25</td>
<td>O26-029</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>S0-S1</td>
<td>S2-S5</td>
<td>S6-S9</td>
<td>S10-S13</td>
<td>S14-S17</td>
<td>S18-21</td>
<td>S22-25</td>
<td>S26-29</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>S0-S1</td>
<td>S2-S5</td>
<td>S6-S9</td>
<td>S10-S13</td>
<td>S14-S17</td>
<td>S18-21</td>
<td>S22-25</td>
<td>S26-29</td>
</tr>
</tbody>
</table>

Figure 14.14: Groups of Segment and Output Lines

**Note:** Control bits

The control bits LCDM5 ... LCDM7 are reset with PUC.

The segment signals Sxx are part of the display driving signals and carry modulated voltage levels according to the time frame of the common lines.

The output signals Oxx selected for 'port' function are static signals. They take two digital level according to bits in the display memory. The logical state of the bits is taken from bit 0 to bit 3* for odd S-lines (n=3,5,.....) and from bit 4 to bit 7* for even S-lines (n=2,4,.....).

* Bits taken are dependent on the MUX rate.
Figure 14.15: Segment Line or Output Line

The logical information of an output Oxx is defined in the display memory. Its location is either bit0 to bit3 or bit4 to bit7, depending on whether an odd or even assignment:

- $$xx = 2, 4, \ldots, 28$$: Oxx is defined with bit0 to bit3
- $$xx = 3, 5, \ldots, 29$$: Oxx is defined with bit4 to bit7
14.4 Application Example showing mixed LCD and Port Mode

The example uses the mixed mode: 4MUX LCD drive for 13 digits and one port group with four digital outputs.

![Diagram of LCD display and port connections]

**Note:** LCD port output

Any LCD port output is defined with four bits. All four bits of the group should have the same logical level, otherwise the output is not static. Assume O28 should be 'H', all the bit0 to bit3 are 'H'.

**Software example to set O28, O29 should be unchanged**

```
LCD15 .EQU 0003Fh
BIS.B 00Fh,&LCD15
```