Scratch(es), probe marks, etc... in the bonding pad area that expose underlying passivation or substrate and leaves < 75% of the unglassivated metallization area undisturbed.
Voids

Metallization Void rejection criteria:

(A void is any defect in the metallization where underlying metal or passivation is visible and is not caused by a scratch.)

Void(s) in the metallization that leaves < 50% of the original metal width undisturbed.

Void(s) in the metallization over a passivation step that leaves < 75% of the original metal width at the step undisturbed.

NOTE: (Does not apply to CMOS) Above criteria can be excluded for the last 25% of linear length of the contact cut and all metal beyond on the termination end(s) of metallization runs. In these cases there shall be at least 50% of the contact opening area covered by metallization.

Void(s) in the metallization over the gate oxide bridge that leaves < 75% of the metallization length (L) or width (W) between source and drain diffusion undisturbed.

Void(s) that leave < 60% of the metallization area over the gate oxide undisturbed.

Void(s) that leave < 75% of the metallization width coincident with the source and drain diffusion junction lines undisturbed.

Void(s) in the bonding pad area that leaves < 75% of its original unglassivated metallization area undisturbed.

Void(s) in the bonding pad or fillet area that reduces the metallization path width connecting the bond to the interconnecting metallization to < 50% of the narrowest entering interconnect metallization stripe width. If two or more stripes enter a bonding pad, each shall be considered separately.

Void(s) in the metallization of a thin film capacitor that reduces the metallization area >75%

Four sided peripheral metal or metal that is the same potential as the die, is rejectable when it exhibits a void that reduces the metal to < 50% of its original width and a second defect that totally isolates a contact from the remainder of the peripheral metal.

Alignment

Metallization Alignment rejection criteria: (all products except CMOS):

Contact window or via that has < 50% of its area covered by metallization

Contact window that has < 40% of its perimeter covered by metallization.
Contact window that has < 75% of its perimeter on two adjacent sides covered by metallization (applicable to MOS structures).

A metallization path not intended to cover a contact window that is not separated from the contact window by a line of separation.

Any exposure of the gate oxide from the source to drain diffusion (applicable to MOS structures).

Gate metallization not coincident with or extending over the diffused guard ring. This applies to MOS structures containing a diffused guard ring. MOS devices that do not contain a diffused guard ring shall have gate metallization extending not < 0.1 mil beyond the gate oxide bridge.

Below is an example of gross misalignment in which the contact window has < 50% of its area and < 40% of its perimeter covered by metal. This photograph shows the same product from a different wafer and is acceptably aligned.

General Metallization rejection criteria:

Metallization corrosion: any metallization corrosion is rejectable.

Metallization corrosion can have various colorations associated with it but is characterized by the "pitting" of the affected metal.
Metallization adherence: Any metallization lifting, peeling, or blistering is rejectable.

At right is an example of lifting metal.

Any metallization bridging where the separation between any two metallization paths is reduced to $< 0.1$ mil, unless by design.