Technology Day Montreal – May 10, 2011

Time	Session	Track 1 MCU and Wireless	Track 2 Embedded Processing	Track 3 Signal Chain	Track 4 Power
8:30 to 9 a.m.	**Registration**				
9 to 10 a.m.	1	MSP430™ MCU Value Line	How to Select the ARM® Core for Your Design	Introduction to Touch-Screen and Haptic Technologies	There's More to Linear Regulators Than You Think
10 to 10:15 a.m.	**Break**				
10:15 to 11:15 a.m.	2	Embedded Web Server-Enabled Design Made Easy with Stellaris® MCUs	Enabling and Accelerating Android on Sitara™, Integra™ and DaVinci™ Devices	Clocking to Maximize High-Speed Signal-Chain Performance	Achieving Better Transient Response with Less Output Capacitance from Your DC/DC Power Designs
11:15 to 12:30 p.m.	**Lunch**				
12:30 to 1:30 p.m.	3	Fundamentals of Antenna Design *by LSR*	Linux Development on ARM®-Based Microprocessors	High-Performance Differential ADC Input Interface Design	Managing and Sequencing Many Power Rails in a System
1:30 to 1:45 p.m.	**Break**				
1:45 to 2:45 p.m.	4	Energy Harvesting, Wireless Charging and Zero Power Devices *by Cymbet*	Video Capture and Processing with the TMS320DM8127	TI High-Speed Solutions for Wireless Infrastructure	Power Stage, Power Block and NexFET™ Technology Drive Higher Levels of Efficiency and Power Density for Power-Supply Design
2:45 to 3 p.m.	**Break**				
3 to 4 p.m.	5	FRAM for Ultra-Low Power	Adding Wi-Fi and *Bluetooth*® to TI Embedded Processors (MCUs and MPUs)	Combating Losses in High Speed Interface Standards (PCIe, SATA, SAS, USB 3.0) with Simple Signal Conditioners	High-Switching Frequency Barriers to Wide-Input-Voltage (Up to 60 V) DC/DC Converters

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Session Titles and Abstracts

Track and Course	Abstracts
Track 1 – MCU and Wireless	
MSP430™ MCU Value Line	The Value Line is the perfect gateway into the MSP430™ family of microcontrollers. No sacrifices are made on these G2xx1/2/3 series. The G2xxx Value Line provides a 16-bit architecture, high-performance analog integration, new features such as CapTouch (G2xx2) and extended I/O ports (G2xx3) while holding the title for ultra-low power. With volume pricing starting at $0.25 and 100 new devices to choose from, learn more to see how the Value Line can help your project get up and running quickly, without breaking the bank.
Embedded Web Server-Enabled Design Made Easy with Stellaris® MCUs	This presentation will cover the Stellaris® LM3S6965 Ethernet evaluation kit with Code Red Technologies' Red Suite tools to set up embedded Web solutions for a remote control application. The Stellaris LM3S6965 is an ARM Cortex™-M3 microcontroller with integrated 10/100 Ethernet MAC+PHY. The Stellaris LM3S6965 Ethernet evaluation kit features several different implementations of embedded Web servers. The fully functional Red Suite evaluation tools also feature real-time code and interrupt trace capability with the Red Trace feature. The Web server application will demonstrate how the provided royalty-free Stellaris libraries make it painless to have networking up and running in minutes, whether using an RTOS or not. Attendees will get a good understanding of how they can start building even the most advanced applications with Stellaris microcontrollers quickly and easily.
Fundamentals of Antenna Design *by LSR*	Antenna design is one of the most intimidating and important parts of any RF design. It is critical to understand the key factors involved when choosing an antenna topology, as well as what tools are needed for design, simulation and characterization. Designs must account for the effects of the enclosure material, the available space, the required radiation patterns, EMC compliance rules and regulations. This presentation discusses the fundamentals of antenna design for short-range devices, as well as the trade-offs between size, cost and performance. An antenna that is properly designed and optimized will enhance the overall performance of any radio.
Energy Harvesting, Wireless Charging and Zero Power Devices *by Cymbet*	New techniques and technologies are now available to create self-powered devices by harvesting ambient energy. Actual energy harvesting (EH)-based designs will be reviewed that use photovoltaic, piezoelectric, thermoelectric and electromagnetic EH transducers. New technologies in the areas of ultra-low-power MSP430™ MCUs, CC430 combined MCU/integrated radios, wireless charging and communications using the TI passive low-frequency interface (PaLFI) device, energy processors, solid-state batteries, and solar energy harvesting for the TI MSP430 LaunchPad kit will be detailed. The last portion of this session will include hands-on lab demos of various EH implementations.
FRAM for Ultra-Low Power	Ferroelectric random access memory (FRAM) is the next-generation non-volatile memory technology for ultra-low-power embedded microcontrollers. Its fast write capability (like DRAM), practically unlimited write endurance (>1,014 cycles) and ultra-low power consumption benefits developers and end users alike. This presentation will describe the new MSP430FR57xx FRAM family and the capabilities behind this newly integrated memory technology to enable ultra-low power applications. FRAM's ability to function as universal memory helps ease the life of developers, reducing development time (faster time to market) and costs. In addition, FRAM enables several new, exciting ultra-low-power applications such as batteryless intelligent sensors.

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Track and Course	Abstracts
Track 2 – Embedded Processing	
How to Select the ARM® Core for Your Design	You know you need a CPU in your system, and you're pretty sure you want to go with some form of an ARM® core. But what form does that CPU take? Should it be a mainstream microprocessor, a DSP, an ASIC, an FPGA, a configurable core or something else? What are the advantages and disadvantages of each of the ARM options? What if you've already selected your OS? How does that affect the choice of CPU? How do you ensure that you're getting the maximum performance from yourCPU? These are just some of the questions/issues we'll tackle in this session. Choosing the best ARM processor for your design can be a difficult decision. In this session, developers will gain insight into trade-offs between varying ARM-based processors, including TI's Stellaris® Cortex™-M3 based microcontrollers and Sitara™ Cortex-A8- and ARM9-based microprocessors. The session will address key design considerations, including power, interface, software support and performance requirements. The presenter will illustrate processor selection tips and tricks through industrial automation and human interface application examples.
Enabling and Accelerating Android on Sitara™, Integra™ and DaVinci™ Devices	With the availability of Android for TI's Cortex™-A8-based devices, developers are now able to use the unique power of the Andoid application framework to create new, compelling designs. Attend this session to learn about Android fundamentals, including key benefits, architecture review, how Android can benefit different end equipments and applications (including voice/video applications), and the TI/Android roadmap.
Linux Development on ARM®-Based Microprocessors	Linux development on ARM®-based microprocessors can be a daunting task. The purpose of this session is to introduce the Texas Instruments Sitara™ Linux software development kit (SDK). The SDK provides customers with a unique out-of-the-box experience and a quick path to application development by providing example applications for key high-touch IP and peripherals. This session will also discuss Matrix, a Qt/E Web kit-based HMI and application launcher; the SDK installer; and Code Composer Studio™ software v5, an Eclipse-based IDE for Linux application development and debugging.
Video Capture and Processing with the TMS320DM8127	TI provides a range of video encoding and processing solutions. The DM8127 is TI's latest DaVinci™ media processor. We will describe the advanced video capabilities of the DM8127 processor and present a camera reference platform for the DM8127 that enables video capture, encoding, display and streaming. An in-depth discussion of the features of the camera reference design will include how TI's complementary products enable a complete camera solution.
Adding Wi-Fi and *Bluetooth*® to TI Embedded Processors (MCUs and MPUs)	Quickly and easily add Wi-Fi and/or *Bluetooth*® technology to systems using TI MPUs (AM/DM37x, AM18x) and MCUs (MSP430™, Stellaris®). In this session, we will start with an overview of the WL1271-TiWi 802.11b/g/n + *Bluetooth*® transceiver and CC2560-PAN1325 *Bluetooth*® transceiver, and then go into the details of the platform. The platform provides complete system integration of all components including WLAN and *Bluetooth*® hardware, host hardware, Linux WLAN drivers, supplicant, TCP/IP integration, *Bluetooth*® stack, profiles, example code for configuration, and sample source applications. We will demonstrate how to establish a Wi-Fi and *Bluetooth*® connection by showing a sample application running on an AM/DM37x EVM.

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Track 3 – Signal Chain	
Introduction to Touch-Screen and Haptic Technologies	This session will discuss the fundamentals of operation and key design considerations when choosing between resistive and capacitive touch-screen technologies. No longer is multitouch a capacitive-only feature. Making multitouch affordable, we'll introduce the TI TSC2020 resistive multitouch controller. We'll also delve into the need for greater tactile response from touch-screens and the haptic options available to create a more immersive user experience.
Clocking to Maximize High-Speed Signal-Chain Performance	Selecting a clock driver for a high-performance sampling system involving high-speed data converters is a hard task and often underestimated. Designers must first understand the fundamentals of the analog-to-digital converter (ADC) to design a clock solution that does not degrade performance of the entire signal chain. Clocking solutions range from simple fanout buffers to sophisticated clock generators with the ability to control output frequencies, shape noise and control skew. As the input bandwidth of the ADC increases, the keystone of overall system performance can rely heavily on the jitter performance of the clock. This is particularly true for SNR and SRDR. This presentation will address sampling clock dependencies on ADC performance metrics (namely SNR and SFDR), explain methods to calculate required sampling clock jitter, introduce TI high-performance synthesizers/jitter cleaners, and show demonstrations of achieving best possible SNR (and SFDR) with cost-effective yet high-performance clocking devices.
High-Performance Differential ADC Input Interface Design	High-performance ADCs used in high-speed data acquisition systems like test and measurement, wireless infrastructure, medical, and military applications (to name a few) require high-performance differential input drive circuits. Designing the drive circuit for optimum SFDR and SNR from the ADC is a challenge for design engineers. This presentation will provide an overview of how ADCs are characterized and show how SFDR and SNR can be combined with the amplifier drive circuit to estimate overall system performance. Different circuit architectures will be presented along with their strengths and weaknesses. To show achievable results, we will show four example application circuits and performance: THS4521 interface to ADS1278 (24-bit, lower frequency, very high resolution, first Nyquist zone application); OPA695 interface to ADS5500 (14-bit, higher frequency, first Nyquist zone application); THS4509 interface to ADS6148 (14-bit, narrowband IF second Nyquist zone undersampling); and THS770006 interface to ADS5493 (16-bit, narrowband IF second Nyquist zone undersampling).
TI High-Speed Solutions for Wireless Infrastructure	This session will provide an overview of TI's signal chain devices targeting cellular wireless infrastructure (3G/4G/MC-GSM) applications. Solutions for radio architectures including direct conversion (quadrature) receive and transmit solutions as well as super-heterodyne architectures will be presented. Example radio diagrams will be given using high-speed ADC/DACs, RF, clocking, amplifier and digital radio blocks.
Combating Losses in High Speed Interface Standards (PCIe, SATA, SAS, USB 3.0) with Simple Signal Conditioners	Latest generation high speed serial communication signals based on popular standards like SATA, USB, PCIe, Display Port, when used in low cost and lossy computing and consumer platforms face signal degradation due to high frequency losses. System designers have couple of options to handle this signal integrity issue. Limit the distance high speed signal has to travel, upgrade to lower loss higher grade/cost PCB materials or use signal conditioners that use analog signal processing solutions like Pre-Emphasis and Equalization to compensate for the signal distortion while continuing to use conventional PCBs. The goal of this presentation is to discuss key electrical specs for loss and jitter in these high speed serial standards. We will then show how channel loss manifests itself in low cost consumer and computer platform PCB design. We will use two practical examples to high light the issue; one will be eSATA connector used for external SATA HDD connectivity in notebook PCs and another will be USB 3.0 connector in desktop PCs. We will introduce simple signal conditioning devices popularly known as redrivers that are increasingly being used in these platforms to compensate for signal dispersion that could lead to biterror failure. Redrivers specs as it applies to counteract channel loss and adherence to PCIe/SATA/USB3 protocol will also be discussed.

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Track 4 – Power	
There's More to Linear Regulators Than You Think	There is a lot more to linear regulators than three pins and heat generation. This is an in-depth look at linear regulators, covering topics such as the basic building blocks of an LDO, how the pass element transistor selection changes performance, the difference between an LDO and a standard linear regulator, stability, quiescent current trade-offs, what PSRR and output noise are, and thermal performance.
Achieving Better Transient Response with Less Output Capacitance from Your DC/DC Power Designs	The TPS54225, TPS54226, TPS54235 and TPS54326 are new product offerings in the switchers with integrated FETs (SWIFT™) power product line. They represent a significant addition to the product line with a totally different control mode from other SWIFT devices. They are very low cost and require a minimum number of external components to target cost-sensitive consumer or other applications. These devices use a proprietary DCAP2™ control mode that exhibits some very high-performance characteristics not normally found in low-cost devices, while also eliminating that bothersome external compensation. Transient response is extremely fast and the TPS54226 and TPS54326 feature a power-saving auto-skip mode. This presentation fully explains the DCAP2 control mode, shows it advantages and high-performance features, and provides competitive analysis with both TI and competitor products.
Managing and Sequencing Many Power Rails in a System	Have you ever wondered how to manage 10-16 power rails in a system design? There are many ways to do this with respect to discrete approaches or integrated designs. This session will show how the TI portfolio of power-supply rail sequencers and monitors will prevent designers from having to design a complex hardware and/or software solution. In this discussion, you will learn that TI devices can manage as many as 16 rails sequencing and monitoring. Learn about the configurable GUI to ease set up and design with respect to these features: watchdog timers, voltage margining, internal temp sensors, non-volatile fault-logging, multiphase clock generators and more. This session will leave you with a solutions-based idea of which sequencers/monitors to choose for a specific design and why.
Power Stage, Power Block and NexFET™ Technology Drive Higher Levels of Efficiency and Power Density for Power-Supply Design	The TI power stage product line is continuing to develop advanced technologies to drive efficiency and power density for switching power-supply designs. This presentation will highlight the latest advancements in both the discrete and multichip module approaches. Our discussion will also focus on advancements in power-stage circuitry from TI such as NexFET™ technology, controller/driver ICs and packaging. Specific attention will be given to technology that reduces power loss and enables high frequency. This allows designers to improve their power density and reduce cost. Comparisons will be made that demonstrate advantages over current state-of-the-art solutions.
High-Switching Frequency Barriers to Wide-Input-Voltage (Up to 60 V) DC/DC Converters	A DC/DC converter switching at 1 or 2 MHz sounds like a great idea, but there is more to understand about the impact to the power-supply system than size and efficiency. Several design examples will be shown revealing benefits and obstacles when switching at faster frequencies.