



Technology Day Ottawa November 17, 2011

Time	Session	Signal Chain	Embedded Processing	Power
8:30 to 9 a.m.	Registration			
9 to 10 a.m.	1	Clocking to Maximize High-Speed Signal Chain Performance	Introduction to the Stellaris® ARM Cortex-M4F Family	There's More to Linear Regulators Than You Think
10 to 10:15 a.m.	Break			
10:15 to 11:15 a.m.	2	How to Get the Best Performance Out of Your High-Speed Data Converter	Getting the Most Out of Your Ultra-Low-Power MSP430™ Design	Achieving Better Transient Response with Less Output Capacitance from Your DC/DC Power Designs
11:15 a.m. to 12:30	Lunch			
12:30 to 1:30 p.m.	3	Combating Losses in High-Speed Interface Standards (PCIe, SATA, SAS, USB 3.0) with Simple Signal Conditioners	Linux Development on ARM-Based Microprocessors	Managing and Sequencing Many Power Rails in a System
1:30 to 1:45p.m.	Break			
1:45 to 2:45 p.m.	4	TINA-TI™ Software v9: A New Simulation Solution for 2011	Video Processing with the TMS320DM816	How TI NexFET™ Power Block and Power Stage Technology Enables the Highest Efficiency and Power Density in Low- to Medium-Input-Voltage Power Systems
2:45 to 3 p.m.	Break			
3 to 4 p.m.	5	SuperSpeed USB and Thunderbolt: Overview and Comparison	Industry's First 10-GHz Cumulative Floating- and Fixed-Point Multicore DSP	DC/DC Converters 101

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Track and Course	Abstracts
Track 1 – Signal Chain	
Clocking to Maximize High-Speed Signal Chain Performance	<p>Selecting a clock driver for a high-performance sampling system involving high-speed data converters is a hard task and often underestimated. Designers must first understand the fundamentals of the analog-to-digital converter to design a clock solution that does not degrade performance of the entire signal chain. Clocking solutions range from simple fanout buffers to sophisticated clock generators with the ability to control output frequencies, shape noise and control skew. As the input bandwidth of the ADC increases, the keystone of overall system performance can rely heavily on the jitter performance of the clock. This is particularly true for SNR and SRDR. This presentation will address sampling clock dependencies on the ADC performance metrics (namely SNR and SFDR), explain methods to calculate required sampling clock jitter, introduce TI high-performance synthesizers/jitter cleaners, and show demonstrations of achieving best possible SNR (and SFDR) with cost-effective yet high-performance clocking devices.</p>
How to Get the Best Performance Out of Your High-Speed Data Converter	<p>This session deals with some of the common issues that haunt the proper application of high-speed ADCs. This is meant for engineers that have a working understanding of data conversion fundamentals already. We will treat subjects such as clocking and jitter, driving the analog input, driving/capturing digital data effectively and layout considerations. The session will focus more on real-world practical issues and their solutions and less on theoretical or mathematical derivations.</p>
Combating Losses in High-Speed Interface Standards (PCIe, SATA, SAS, USB 3.0) with Simple Signal Conditioners	<p>The latest generation of high-speed serial communication signals – based on popular standards like SATA, USB, PCIe and Display Port – face signal degradation due to high-frequency losses when used in low-cost and lossy computing and consumer platforms. System designers have a couple of options to handle this signal integrity issue: limit the distance the high-speed signal has to travel; upgrade to lower-loss, higher-grade/cost PCB materials; or use signal conditioners that use analog signal-processing solutions like pre-emphasis and equalization to compensate for the signal distortion while continuing to use conventional PCBs. The goal of this presentation is to discuss key electrical specs for loss and jitter in these high-speed serial standards. We will then show how channel loss manifests itself in low-cost consumer and computer platform PCB designs. We will use two practical examples to highlight the issue: an eSATA connector used for external SATA HDD connectivity in notebook PCs and a USB 3.0 connector in desktop PCs. We will introduce simple signal-conditioning devices, popularly known as redrivers, that are increasingly being used in these platforms to compensate for signal dispersion that could lead to bit error failure. Redriver specs</p>
TINA-TI™ Software v9: A New Simulation Solution for 2011	<p>TINA-TI™ software has been TI's free circuit simulator for five years. During that time, TI has released hundreds of macromodels and reference designs that can be simulated. This capability allows you to quickly evaluate parts, validate designs to ensure first-pass success, and, if necessary, debug problems. This session will provide an introduction to TINA-TI software, with an emphasis on new features in version 9. We will cover topics such as modifying EVM schematics to meet your needs, importing third-party models, running simulations, visualization/analysis of simulation output, and using parametric sweeping to improve your design.</p>
SuperSpeed USB and Thunderbolt: Overview and Comparison	<p>SuperSpeed USB has shown significant growth since the first certified products became available in early 2010. Yet many customers are still asking what it is, and what they can do with it. In addition to the Intel/Apple announcement of Thunderbolt, many in the market have become even more confused about what each technology is intended for and when it should be used. The first part of this session will present a brief overview of SuperSpeed USB, followed by a brief overview of Thunderbolt and a discussion of whether Thunderbolt and USB are competing or complementary. The second part will review TI's SuperSpeed USB products and plans.</p>



Texas Instruments
Technology Day: Ottawa – Nov. 17, 2011
Session Titles and Abstracts

Track and Course	Abstracts
Track 2 – Embedded Processing	
Introduction to the Stellaris® ARM Cortex-M4F Family	In this session, we will take an in-depth look at the new Stellaris® ARM Cortex-M4F family.
Getting the Most Out of Your Ultra-Low-Power MSP430™ Design	Realizing a low-power system design when every microampere counts is rarely an easy task to achieve. Such an effort requires detailed knowledge of everything your MCU offers in the way of enabling ULP, as well as the features of any external components. This course gives practical instructions of how to realize an ultra-low-power application using the MSP430™ family. Special focus is given to specific ULP features, how to select components for ULP applications, and coding techniques that reduce the power consumption of your embedded application.
Linux Development on ARM-Based Microprocessors	Linux development on ARM-based microprocessors can be a daunting task. The purpose of this session is to introduce the Texas Instruments Sitara™ Linux software development kit (SDK). The SDK provides customers with a unique out-of-the-box experience and a quick path to their application development. The Sitara Linux SDK accomplishes this by providing example applications for key, high-touch IP and peripherals. This session will also discuss Matrix, a Qt/E Webkit-based HMI and application launcher; the SDK installer; and Code Composer Studio™ software v5, an Eclipse-based IDE for Linux application development and debugging.
Video Processing with the TMS320DM816	TI provides a range of video encoding and processing solutions. The DM8168 is TI's latest DaVinci™ media processor. We will describe the advanced video capabilities of the DM8168 processor and the reference platform that enables video capture, encoding, decoding and display.
Industry's First 10-GHz Cumulative Floating- and Fixed-Point Multicore DSP	This session will review key aspects of TI's latest DSP core and family of C667x devices. With its ability to choose between fixed-point and floating-point instructions on a cycle-per-cycle basis, combined with 1.25-GHz performance on multiple cores, the C667x DSP allows designers to bring down system complexity and take advantage of the natural parallelism in various high-performance applications. Through improved SIMD functionality, numerous memory enhancements, and new peripherals and accelerators, C667x devices provide the ideal solution for demanding applications with a scalable option.



Track and Course	Abstracts
Track 3 – Power	
There's More to Linear Regulators Than You Think	There is a lot more to linear regulators than three pins and heat generation. This is an in-depth look at linear regulators, covering topics such as the basic building blocks of an LDO, how pass element transistor selection changes performance, the difference between an LDO and a standard linear regulator, stability, quiescent current trade-offs, what is PSRR, what is output noise, and thermal performance.
Achieving Better Transient Response with Less Output Capacitance from Your DC/DC Power Designs	The TPS54225, TPS54226, TPS54235 and TPS54326 are new product offerings in the switchers with integrated FETs (SWIFT™) power product line. They represent a significant addition to the product line with a totally different control mode from other SWIFT devices. They are very low cost and require a minimum number of external components to target cost-sensitive consumer or other applications. These devices use a proprietary DCAP2™ Mode control scheme that exhibits some very high performance characteristics not normally found in low-cost devices, while also eliminating bothersome external compensation. Transient response is extremely fast and the TPS54226 and TPS54326 feature a power saving auto-skip mode. This presentation fully explains the DCAP2 Mode control scheme, shows its advantages and high-performance features, and provides competitive analysis with both TI and competitor products.
Managing and Sequencing Many Power Rails in a System	Have you ever wondered how to manage 10 to 16 power rails in a system design? There can be many ways to do this with respect to discrete approaches or integrated designs. This session will show the TI portfolio of power supply rail sequencers and monitors, which can keep designers from having to design a complex hardware and/or software solution. In this discussion, you will learn that TI devices can manage up to 16 rails sequencing and monitoring. You'll also learn about the configurable GUI to ease setup and design with respect to these features: watchdog timers, voltage margining, internal temp sensors, nonvolatile fault logging, multiphase clock generators and more. This session will leave you with a "solutions-based" idea of which sequencers/monitors to choose for a specific design, and why.
How TI NexFET™ Power Block and Power Stage Technology Enables the Highest Efficiency and Power Density in Low- to Medium-Input-Voltage Power Systems	Switching power supply FET technology is ever-advancing. TI's NexFET™ Power Block and Power Stage technology enable ~92 percent efficiency at output currents >100 A, and meet the ever-increasing power density and efficiency demands in line and portable power systems. You will come away with a complete understanding of the system approach TI NexFET technology facilitates in TI power-management solutions, and will understand TI's NexFET power MOSFET technology's competitive advantages in the marketplace.
DC/DC Converters 101	This presentation is an introduction to power supplies for non-power supply engineers. If you are an engineer that works on systems that require power but you don't design the actual power supply, this presentation is for you. We will define and explain some of the terminology surrounding power supplies and explain why you might use one topology over another; for example, efficiency considerations and how they relate to the differences between synchronous and nonsynchronous converters. We will also explain many terms you may have heard but not fully understood, such as split rail, PSRR, converter vs. controller, LDO vs. linear regulator, buck vs. boost, etc. This presentation will not show you how to design a power supply, but it will help you to understand what power-supply designers are talking about.

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