PROJECT TITLE: *Low photon CCD sensor for security applications*

TEAM MEMBERS: *Mark Haslehurst (markhaslehurst@gmail.com). James Mills (jm5068@bristol.ac.uk)*

ADVISING PROFESSOR: *Naim Dahnoun (Naim.Dahnoun@bristol.ac.uk)*

UNIVERSITY: *University of Bristol*

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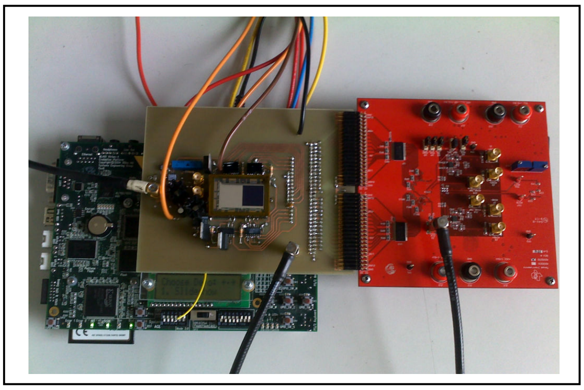
TI PARTS USED IN PROJECT: *ADS5232 (1), THS4503(2), SN74AVC16244 (2)*



PROJECT ABSTRACT (250 words maximum)

Digital imaging systems are ubiquitous in the modern world, with much of the security surveillance required taking place in low light levels. With digital imaging sensors suffering from significant dark current, resulting in poor low light performance, the CCD201-20 promises to outperform other sensors in this field. However, the cost of such devices has been prohibitive in their operation being investigated. As such, the required circuitry for operation is not openly documented.

This project therefore aims to investigate the implementation of hardware and firmware for the successful operation of such a device. Furthermore, this project encompassed the successful implementation of an image processing algorithm on an FPGA based platform.

Hardware was designed around an FPGA evaluation platform to provide the necessary interface for the sensor. After building and testing the circuits associated with this task, the FPGA was utilised to process a series of video frames, from which it must extract objects of interest. The system was used to successfully demonstrate the Mixture of Gaussians background subtraction algorithm running on the FPGA. This is capable of compiling a model of the video background and identifying moving objects in the current frame. The final implementation of this algorithm is capable of running in real time and is heavily optimised to make use of FPGA architectural features.

In order to operate under low light conditions, the effects of noise must be reduced where possible and this is enabled by making use of the TI ADS5232 device for sampling the sensor output.

Introduction

In the modern world, camera technology is a part of everyday life. It is used by consumers, businesses, governments and hobbyists for a wide range of applications under a variety of light conditions. Many of the applications where this technology is applied require performance in low to very low light levels. In recent years, the need for high quality surveillance equipment for national security has been proven, with much surveillance taking place at night.

Another trend in recent years has been to implement a digital solution to a given problem, and with good reason. A digital video surveillance system, for example, could allow integrated image processing therefore leading to higher levels of automation and hence lowering long term costs. In addition, the storage requirements are simpler in applications where many hours of footage must be stored. Instead of requiring a room of archived video footage, a single hard drive may now serve the same purpose.

However, the image quality obtained from conventional digital imaging sensors suffers greatly in low light conditions, where noise begins to become significant. Fortunately, there are new technologies emerging which promise to assist with this problem. Such a sensor which claims to outperform standard digital camera systems in low light conditions is the CCD201-20, from e2v.

Unfortunately, the interface for such devices is poorly specified and the hardware required to operate such a sensor is not common place. The aims of this project were therefore to design and build the hardware required to operate the sensor, sample the output and perform processing on the signals received.

Motivation for project

The potential applications for an optical sensor with enhanced low light level performance are vast, but the obvious fields where this could be put to use would be for military or security surveillance. This could be particularly beneficial when combined with the image processing techniques enabled by implementing a digital solution.

Further applications include astronomy and space imaging, where extremely low light levels are available. Similarly, deep sea exploration presents great challenges where light is unable to penetrate significant distances due to the water pressures encountered at depth.

Another application where such sensor technology can be applied is in healthcare, where it may be used to capture x-ray images. Due to the sensitivity of such a device, much lower levels of radiation may be used to create an image. This has clear health benefits over high dosage solutions. With the low levels of radiation enabled by these devices, full body scanning using this technique is a possibility.

However, the cost of such sensors is prohibitive to their use on a wide scale. A complete system is more costly still and this limits the applications of these devices. By providing a well documented basis for the design of such systems, this project hopes to enable their uses for a wider range of consumers.

Theoretical background

The sensor used in this project has a resolution of 1024 by 1024 pixels. It supports a maximum readout rate of 15MHz, allowing for a frame rate of close to 15 frames per second. Faster frame rates may be achieved by interlacing rows using the 'dump gate' pin to discard unwanted rows without reading. The images produced by this sensor are greyscale and so do not contain colour information, only the brightness of each pixel.

This is a frame transfer device, negating the need for an external shutter and also maximising image integration time. This requires half the silicon area to be covered by an opaque mask, allowing for the image to be quickly transferred from the active image area to the covered region. From here, it may be stored and protected from smearing effects while being read.

This device further enables operation under low light conditions by multiplying the charge captured by every pixel so that even a few photons may be detected under optimum conditions. This requires an additional gain register before the output amplifier, although this requires a higher than usual voltage signal which is used to generate a strong electric field, sufficient to cause impact ionisation at each stage of the register.

Such an electron-multiplying CCD device is able to reduce readout noise present in the output amplifier, relative to the signal by multiplying the pixel value before reaching the output amplifier.

Since readout noise is generally the dominant noise component in CCD sensors, the overall SNR is therefore greatly improved.

Another significant source of noise in this device is dark current, thermally generated noise inherent in the operation of the CCD sensor. Another common issue with CCD sensors is shot noise, caused by the random arrival of photons, however there is little to be done about this besides prolonged exposure. These main sources of noise combine as shown in equation 1.

$$Noise_{total} = \sqrt{(Read\ Noise)^2 + (Shot\ Noise)^2 + (Dark\ Current)^2} \quad (1)$$

The effects of dark noise may be reduced by employing correlated double sampling (CDS). This technique involves sampling the output twice, as shown in Figure 1. Here, the output of the sensor is sampled after being reset to a reference, providing a reference value for the noise. The output is sampled again once the pixel charge has been transferred. The reference (noise) value may be subtracted from the pixel measurement in order to obtain a final pixel value.

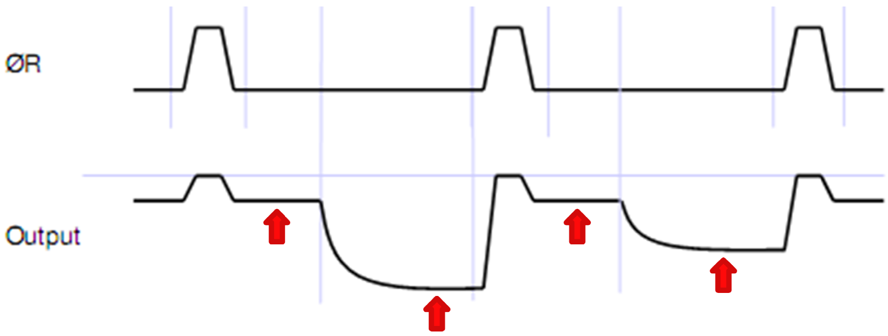


Figure 1: Correlated double sampling (CDS)

The use of the selected TI ADC device enables the use of such a technique to reduce image noise by sampling at up to 65MSPS.

Implementation

The system implemented and being described in this report encompasses all three elements of the high level system flow shown in Figure 2.

Figure 2: High level system flow

The system presented in this report is based around an FPGA evaluation platform for several reasons. While FPGAs are becoming increasingly competitive when applied to DSP tasks, they also have several other advantages. In being able to perform additional processing or tasks simultaneously, an FPGA is able to control the complete system from one device, whether providing direct feedback from the processing or performing unrelated tasks. Furthermore, the cost of such devices is also becoming increasingly competitive. The use of an FPGA device for this project has enabled the optimisation of DSP code to enjoy the benefits of parallel operation.

The capture process may be further described by Figure 3, which shows how the FPGA is able to interface with the sensor through the necessary hardware elements.

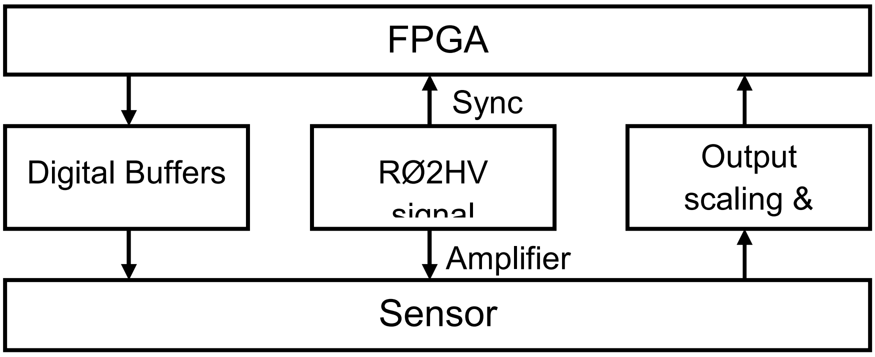


Figure 3: Image capture process

The requirements for all hardware elements of this project were assessed before possible solutions were considered. Circuits were then designed, simulated and prototyped before constructing the final system. By following this procedure, it was possible to ensure that every individual element behaved as expected before being combined.

The RØ2HV high voltage signal was a challenge to amplify, given the frequency and scale of the signal required. The final solution makes use of two discrete BJT devices to form a two stage amplifier capable of providing a 40 volt, 10MHz sine wave. The digital signals required were generated using a digital line driver to provide the required voltages, with calibration taking palce on the FPGA device.

With the device requiring 9 different bias voltages, in addition to the other signal supply rails, many voltage regulators were also employed in order to reduce the power supply requirements of the system.

Once the system was successfully generating an output, it was necessary to sample the output using an ADC. This was controlled by the FPGA to sample at the correct moment.

As previously described, the system implements correlated double sampling to reduce signal noise. With a readout frequency of 10MHz, a sampling frequency of 20MHz was used. The signal from the device was scaled before sampling, using a THS4503 amplifier, which also converted the differential amplifier into a differential signal for the amplifier.

The sensor provides two separate output signals, one amplified and the other unamplified. Since the ADS5232 provides two channels, both outputs may be sampled and then the desired signal may be selected on the FPGA, without changing the hardware configurations. This was one factor in the selection of this device, along with the sampling frequency.

In order to ensure correct operation, a SN74AVC16244DGG buffer was used on each ADC output. This was placed close to the device to avoid clock skew problems and ensure the correct reading of values.

Since it was not possible in the given time frame to build a lens to focus an image onto the sensor, the remainder of the project was tested using previously generated footage. The FPGA was used to process some typical security footage to detect and isolate foreground objects. This was done using a Mixture of Gaussians algorithm, heavily optimised to make use of the parallel FPGA architecture. The FPGA architecture also allowed the design to be pipelined efficiently, after being split into stages. This process required an entire rethink of the conventional DSP code to remove loops and exploit potential speed improvements. Even when running at 240MHz, this core is able to process the footage generated by the sensor in real time. This makes use of the DSP48 slices present in the Xilinx FPGA used for fast arithmetic. Coefficients for this algorithm were stored on local memory devices, whose interface was written for this purpose. Figure 4 shows a block diagram of the VHDL entities written for this project.

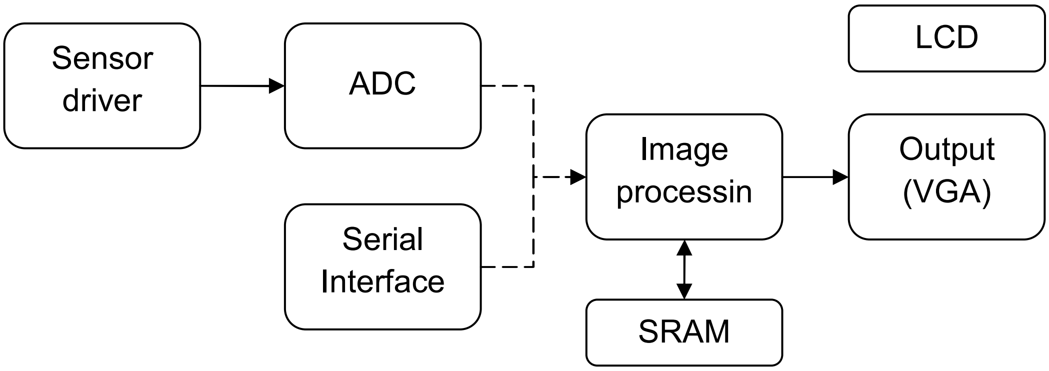


Figure 4: Structure of VHDL entities

After processing, the results were output through a VGA interface for visual confirmation.

Experimental results

The hardware built successfully operates the CCD201 sensor and provides an output signal. This can be clearly seen to vary with light conditions as expected. One of the digital sensor signals can be seen in Figure 5: (a) Output register after calibration (b) Output signalFigure 5, falling as the sinusoidal multiplication register clock peaks. The second image shows the output signal varying with time.

The ADC used is able to successfully sample the output signals into the FPGA, employing CDS to reduce the impact of noise.

The firmware generated is able to generate the signals required for the sensor, including calibration as shown in Figure 5 (a). The signal processing core works successfully, having been tested both mathematically and visually.

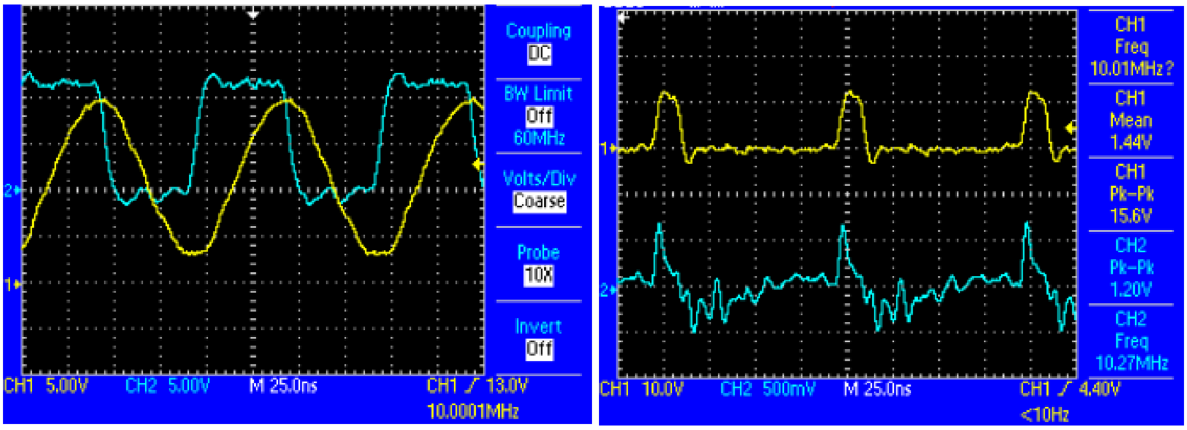


Figure 5: (a) Output register after calibration (b) Output signal

Figure 6 shows the system output, with added text overlay. This illustrates the successful aplication of Mixture of Gaussians to the footage used. Here, the parking space from which the car has just reversed is shown as foreground, but this is a problem due to the algorithm rather than the implementation.

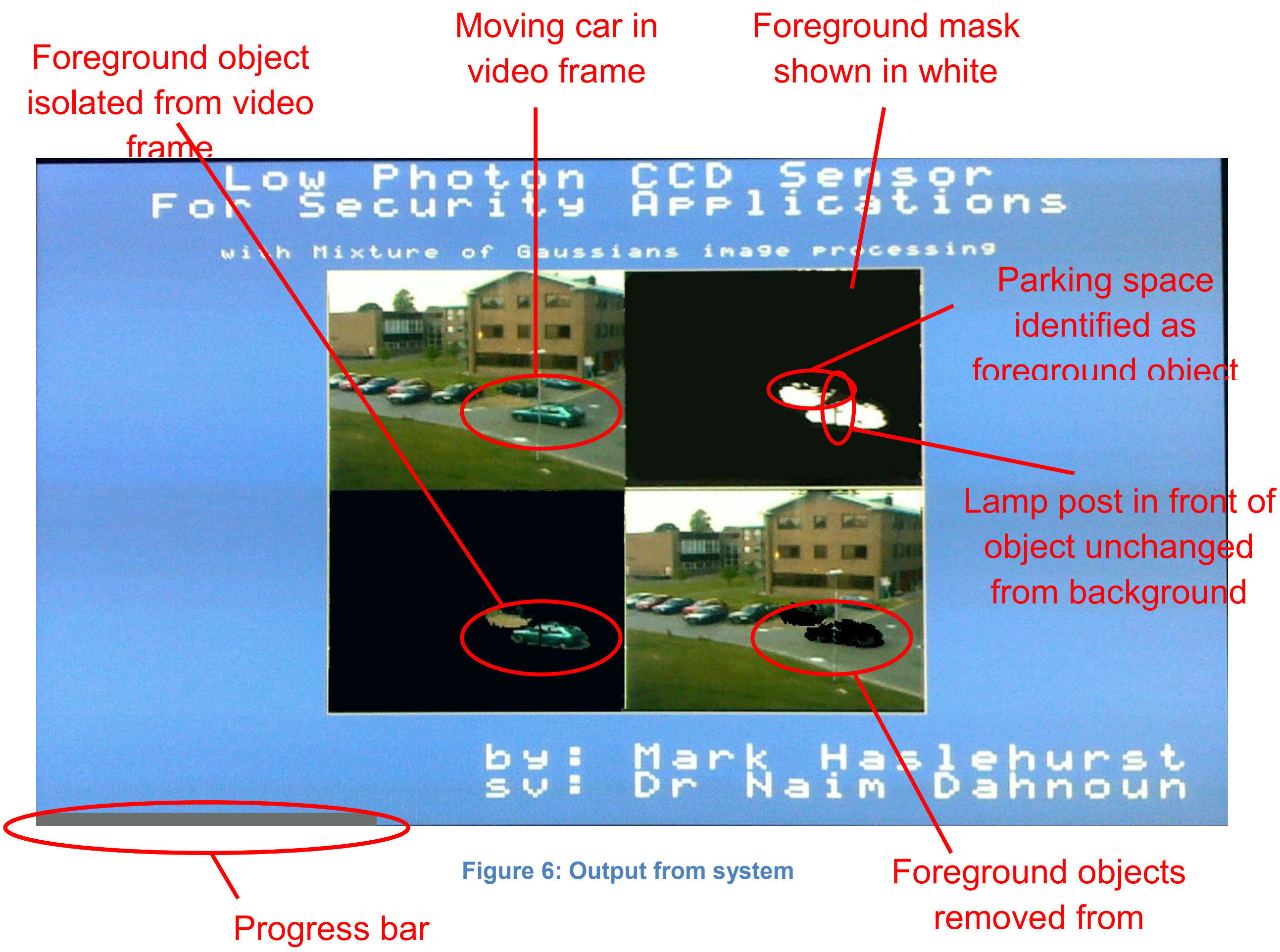


Figure 6: Output from system

Conclusions

This project has been successful in its aim of developing a successful CCD201 system, complete with image processing. The hardware provided many challenges, as did the very tight timing specifications of the CCD sensor, however all problems encountered were addressed and overcome successfully. The ADS5232 was pivotal in the successful sampling of the sensor output and for this purpose, it was perfect – with a sampling frequency to enable CDS and a sufficiently high resolution to provide a high quality digital representation of the signal being sampled. In addition, the second channel makes its application to a real system more beneficial, since both sensor outputs may be utilised without requiring another ADC device. The THS4503 was suitably applied for the amplification of the input signal and for converting into differential signal, for which both the data sheet and technical notes were excellent. The SN74AVC16244DGG buffer, was used as recommended in the ADS5232 datasheet to ensure correct operation, although operation without this device in the design was not tested. However, as a low cost buffer this also served its purpose well.

Were this project to be completed again, I would perhaps address the problem of generating the high voltage, high frequency RØ2HV signal differently, perhaps using a tuned transformer. However, the firmware used needs no further improvements other than perhaps the addition of further image processing such as perhaps object tracking.

Future plans

For future development of this project, I would recommend the investigation of more DSP algorithms being added to the system, perhaps to further filter noise from the sensor and to optimise the current algorithm for low light conditions. Unfortunately, this was beyond the timescale of this project.

Furthermore, the hardware could be developed further to reduce power consumption in the class A amplifier. The use of a tuned transformer amplifier, as described above, could help with this.