

# Powering the AM1705 and AM1707 With the TPS650061

Daniel Acevedo

Battery Power Applications

## ABSTRACT

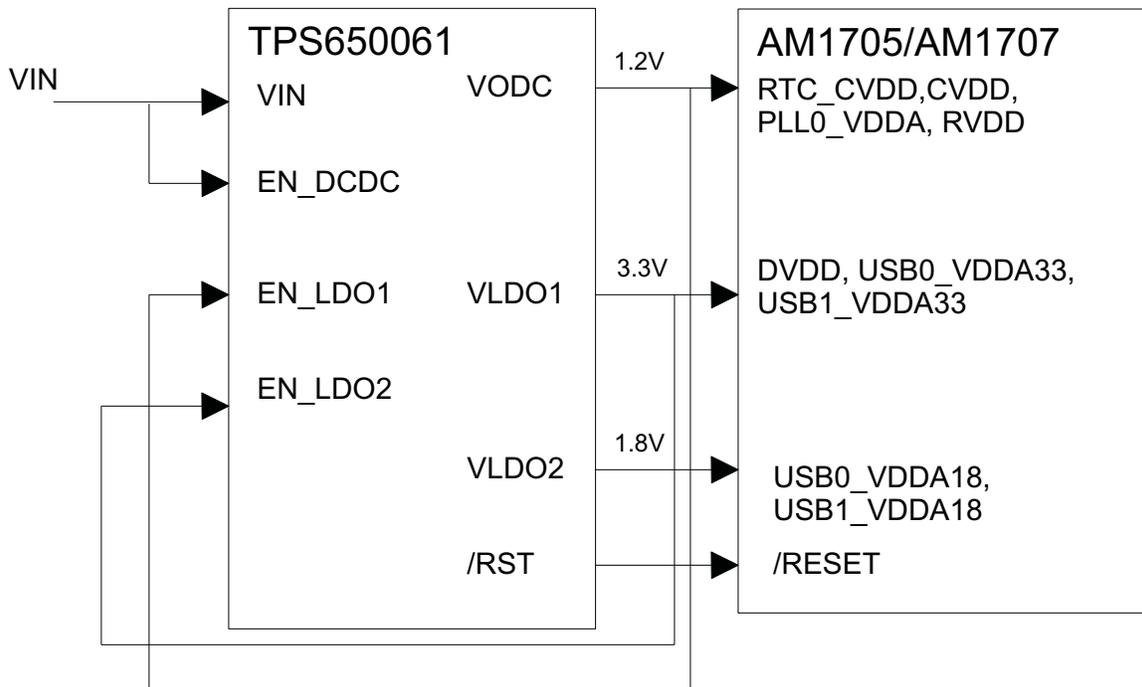
This document details the design considerations of a power solution for the AM1705 and AM1707 (AM1705/07) low-power application processor with a TPS650061, three-rail, Power Management Unit (PMU) or Power Management Integrated Circuit (PMIC).

Portable application solution size demands a high level of integration and the AM1705/07 requires at least three different voltage rails with specific sequencing and reset requirements. The TPS650061 is a highly integrated power solution that can provide the 1.2-V, 1.8-V, and 3.3-V rails and  $\overline{\text{RESET}}$  signal required by the AM1705/07. The TPS650061 has a single, step-down converter, two low-dropout regulators, and a voltage supervisor.

Included in this document is a power solution for the AM1705/07. Power requirements, illustrated schematic, operation waveforms, and bill of materials are detailed.

## 1 Power Requirements

Figure 1 presents the block diagram for the TPS650061 and AM1705/07.



**Figure 1. TPS650061 and AM1705/07 Simplified Block Diagram**

The AM1705/07 power requirements are listed in [Table 1](#).

**Table 1. AM1705/07 Power Requirements**

Rail Name	Voltage (V)	I <sub>max</sub> (mA)	Tolerance (%)
RTC_CVDD, CVDD, PLL0_VDDA, RVDD	1.2	435	-5, +10
USB0_VDDA18, USB1_VDDA18	1.8	50	±5
DVDD, USB0_VDDA33, USB1_VDDA33	3.3	115	±5

The TPS650061 meets these power requirements with its single, step-down converter, two low-dropout (LDO) regulators, and voltage supervisor.

## 1.1 Power-On Sequence

To meet the AM1705/07 power-on requirements, the 1.2-V rail must power on first, then the 1.8-V rail and the 3.3-V rail in any order. After all three rails are up, the RESET may be released. To ensure this power-up sequence, the 1.2-V enable is connected to VIN and the output is connected to EN\_LDO1. The output of the first LDO regulator, VLDO1, is connected to EN\_LDO2. To assert the reset only after all three supplies are up,  $\overline{RST}$  is pulled up to VLDO1, and RSTSNS is connected to VLDO2 with a resistor divider. The proper connections for this power-on sequencing are shown in [Figure 1](#).

Consider the following when selecting components for the circuit:

- VODC must be targeted above 1.2 V at full load to be used as enable for other supplies.
  - VIH for the TPS650061 is rated at a minimum of 1.2 V which ensures that the device recognizes an input as HIGH if it is at or above 1.2 V.
    - The AM1705/07 RTC\_CVDD, CVDD, PLL0\_VDDA, and RVDD tolerance of -5%, +10% makes targeting at or above 1.2 V at full load possible while remaining within the AM1705/07 recommended operating conditions.
- The resistor divider on RSTSNS is such that if VLDO2 goes below 1.8 V - 5% (1.71 V), reset becomes active.
  - Because  $\overline{RST}$  is pulled up to VLDO1, it only goes high if VLDO1 and VLDO2 are present.

Per the excerpt from the AM1705/07 data sheet, the device must be powered on in the following order:

- 1) RTC (RTC\_CVDD) may be powered from an external device (such as a battery) prior to all other supplies being applied or powered up at the same time as CVDD. If the RTC is not used, RTC\_CVD must be connected to CVDD.
- 2a) CVDD core logic supply
- 2b) Other 1.2-V logic supplies (RVDD, PLL0\_VDDA). Groups 2a) and 2b) may be powered up together or 2a) first followed by 2b). Groups 1 and 2 may be powered up together if the real-time clock is only needed when the core is powered.
- 3) All 1.8-V I/O supplies (USB0\_VDDA18).
- 4) All digital I/O and analog 3.3-V PHY supplies (DVDD, USB0\_VDDA33). USB0\_VDDA33 is not required if USB0 is not used and may be left unconnected.

Group 3) and Group 4) may be powered on in either order [3 then 4, or 4 then 3] but group 4) must be powered on after the core logic supplies.

No specific voltage ramp rate is required for any of the supplies.  $\overline{RESET}$  must be maintained active only after all power supplies have reached their nominal values.

## 1.2 Power-Off Sequence

For the AM1705/07, the power supplies can be powered off in any order. The AM1707 has the additional requirement that the 3.3-V supplies do not remain powered with the other supplies unpowered.

## 2 Schematic, Waveforms, and Bill of Materials

### 2.1 Schematic

Figure 2 is the schematic of the power solution for the AM1705/07.

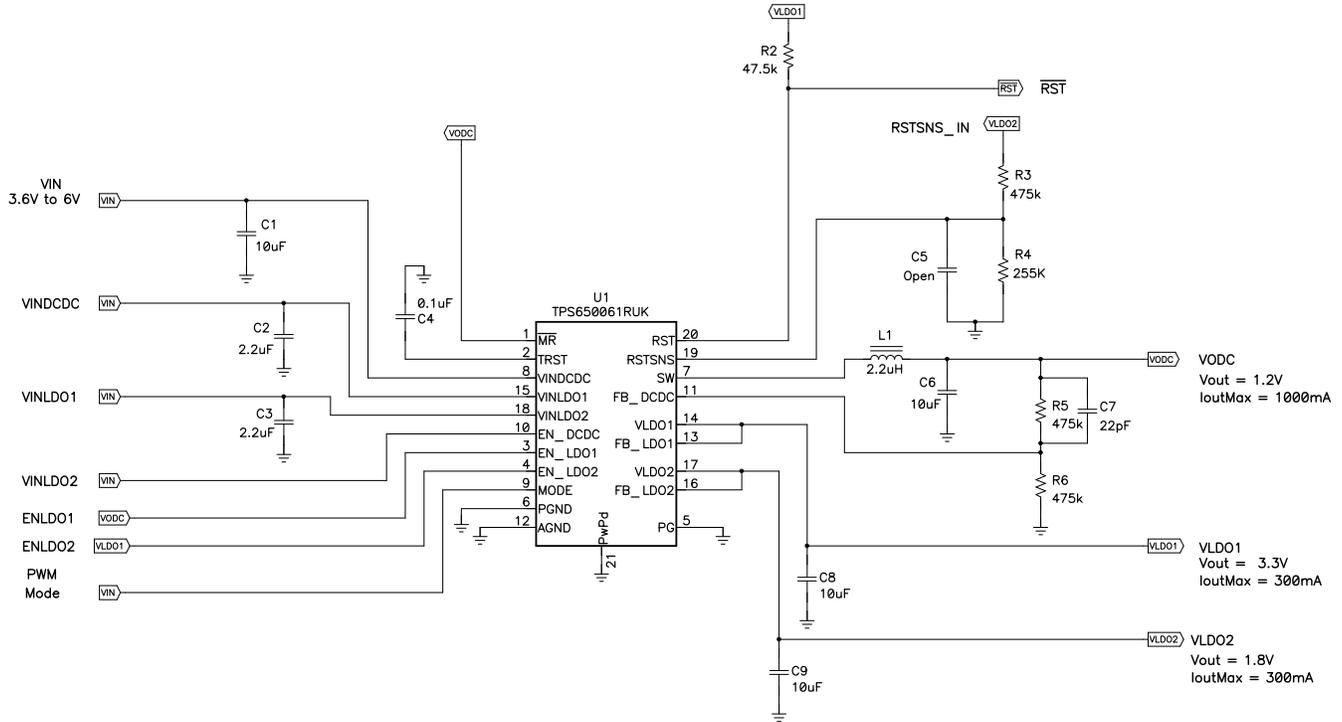


Figure 2. TPS650061 Schematic Diagram

### 2.2 Waveforms

The following waveforms demonstrate the start-up sequence and the reset of the TPS650061 as required by the AM1705/07. Figure 3, shows the TPS650061 power-on sequence of 1.2 V, then 3.3 V and 1.8 V. Figure 4 shows the reset pin,  $\overline{RST}$ , being released after the voltage on RSTNS rises above the threshold and after the reset recovery time,  $t_{RST}$ , is exceeded.

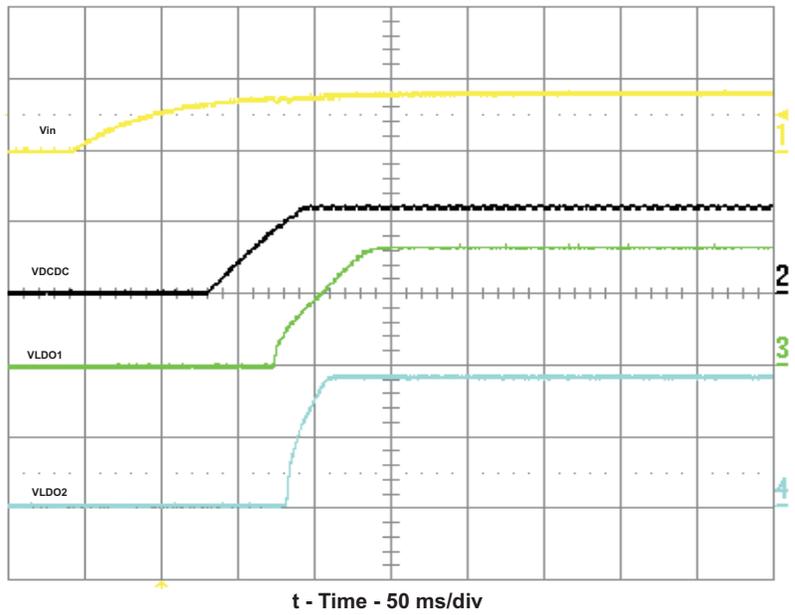


Figure 3. TPS650061 Power Up – Ch1-Vin, 5 V/div; Ch2-VDCDC, 1 V/div; Ch3-VLDO1, 2 V/div; and Ch4-VLDO2, 1 V/div

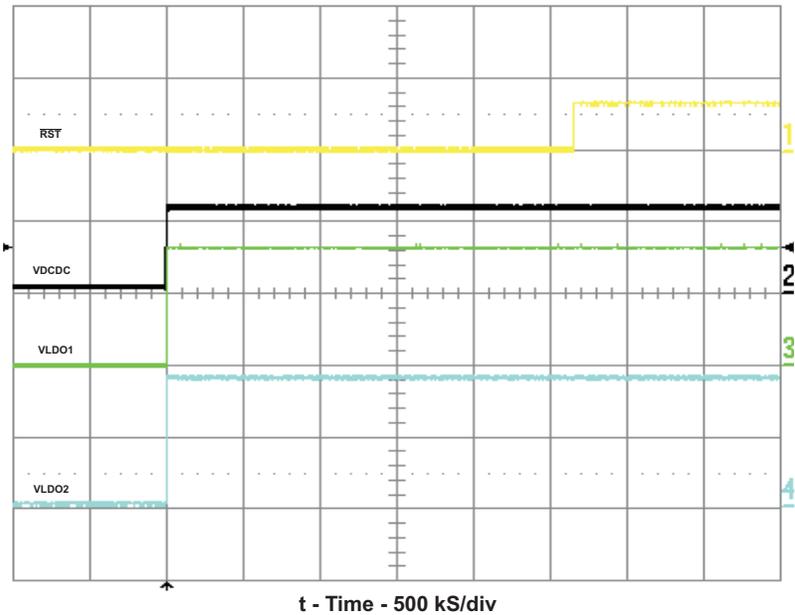


Figure 4. TPS650061 Power Up and Reset – Ch1-/RST, 5 V/div; Ch2-VDCDC, 1 V/div; Ch3-VLDO1, 2 V/div; and Ch4-VLDO2, 1 V/div

### 2.3 Bill of Materials

The bill of materials is displayed in [Table 2](#).

Table 2. Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
4	C1, C6, C8, C9	10uF	Capacitor, Ceramic, 10V, X5R, 10%	0805	Std	Std

**Table 2. Bill of Materials (continued)**

Count	RefDes	Value	Description	Size	Part Number	MFR
2	C2, C3	2.2uF	Capacitor, Ceramic, 10V, X5R, 10%	0603	Std	Std
2	C4	0.1uF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
1	C7	22pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	Std	Std
1	L1	2.2uH	Inductor, SMT, 2.0A, 110milliohm	0.118 x 0.118 inch	LPS3015-222ML	Coilcraft
3	R1, R2,	47.5k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
3	R3, R5, R6	475k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	232K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	U1	TPS650061RUK	IC, 2.25 MHz Step Down Converter with Dual LDOs and SVS	QFN	TPS650061RUK	TI

### 3 Conclusion

The TPS650061 provides a low-cost, comprehensive power solution for the AM1705/07. A 1.2-V rail (capable of supplying 1 A) is powered on, followed by a 3.3-V rail (300 mA), then a 1.8-V rail (300 mA); once all three supplies have reached minimum regulation,  $\overline{\text{RESET}}$  goes high (i.e., rises to its pullup voltage). This meets the power requirements of the AM1705/07.

### 4 References

1. *TPS650061, 2.25 MHz Step Down Converter with Dual LDOs and SVS* data sheet ([SLVS810](#))
2. *AM1705 ARM Microprocessor* data sheet ([SPRS657](#))
3. *AM1707 ARM Microprocessor* data sheet ([SPRS637](#))

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2021, Texas Instruments Incorporated