

# TI Designs: Verified Design

## Extending Rail-to-Rail Output Range for Fully Differential Amplifiers to Include True Zero Volts



### TI Designs

TI Designs Reference designs are analog solutions created by TI's analog experts. Verified Designs offer the theory, part selection, simulation, complete PCB schematic & layout, bill of materials, and measured performance of useful circuits. Circuit modifications that help to meet alternate design goals are also discussed.

### Design Resources

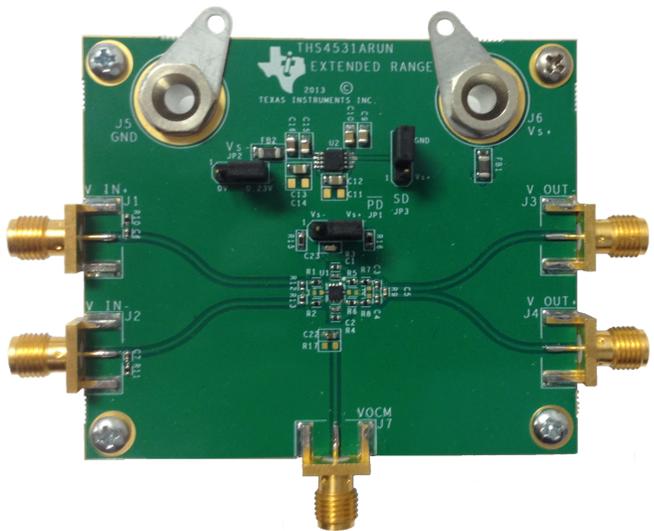
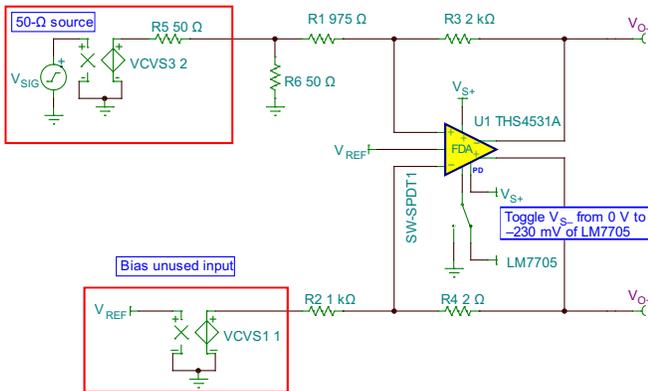
<a href="#">Design Files</a>	Simulations, PCB, Gerber, BOM
<a href="#">TINA-TI™</a>	SPICE Simulator
<a href="#">ADS8321EVM</a>	Tool Folder
<a href="#">ADS8321</a>	Product Folder
<a href="#">LM7705</a>	Product Folder
<a href="#">THS4531A</a>	Product Folder

### Design Features

The rail-to-rail output extension board is designed to overcome amplifier saturation and provide optimal performance in a single-supply environment.

- Single supply 3 V to 5 V
- Extends Differential Amplifier Output to Include 0 V
- Single-Ended or Differential Input
- Filtering and Noise Gain Configurations
- Low Power (2 mW at 5 V)
- Performance Demonstrated with ADS8321

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## 1 Introduction

Operational amplifiers (op amps) are frequently used in signal-conditioning circuits and measurement systems. An op amp that has an output spanning from a negative to a positive supply rail is generally referred to as a rail-to-rail output (RRO) op amp. These devices have been used increasingly in portable systems to drive analog-to-digital converters (ADCs) where a key concern is reducing power consumption without sacrificing dynamic range. While the task calls for the lowest power RRO op amps, circuit designers are discovering that the output is actually limited to a couple hundred millivolts short of the rail depending on the loading. Thus an input signal truly spanning to one or both of the rails will not be rail-to-rail at the output. This problem is known as headroom and is the result of the RRO architecture. This reference design focuses on using a low-power RRO fully-differential op amp (THS4531A) and low-noise negative-bias generator (LM7705) to achieve true zero volts in a ground-referenced single-supply system.

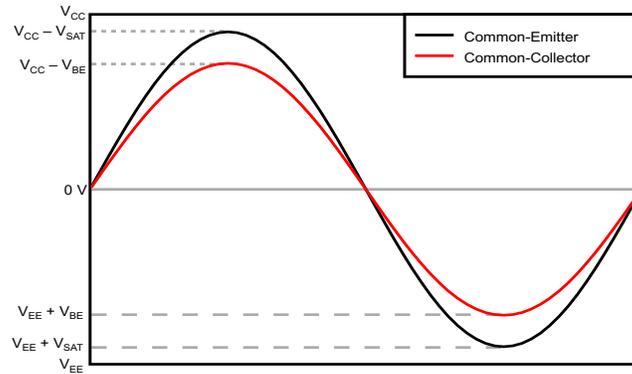
## 2 Rail-to-Rail Output Architecture

There are many different types of RRO amplifiers that vary with technology and topology. In high-speed applications bipolar-junction transistors (BJTs) are a good option because these transistors feature large transconductance gain ( $g_m$ ) over a wide bandwidth. Whereas in precision applications MOS transistors have an advantage with almost zero bias current affecting DC offsets and large input impedance for buffering. As the line between high speed and precision begins to blur, especially as precision ADCs become available with faster conversion speeds, RRO op amps using BJTs offer a very competitive solution.

A simplified amplifier-output stage can be thought of as a pair of complementary BJTs in either a common-collector or common-emitter structure shown in [Figure 1](#). The traditional method for constructing the output stage uses a common-collector architecture ([Figure 1 A.](#)) which is very simple to implement but results in a base-emitter voltage ( $V_{BE}$ ) drop between 0.7 V to 1 V on either end of the range. Because of this, it is not considered to be RRO. In wide-supply applications, this drop in  $V_{BE}$  can generally be tolerated, but in portable systems where battery-powered single supplies are typically less than 5 V, this drop may not be acceptable. A more effective approach is to use the common-emitter structure ([Figure 1 B.](#)) which allows outputs that can swing within tens of millivolts of the rail and thus for many applications can be considered to be RRO. This approach can be slightly more difficult to implement because the output drop is not constant and is based on the loading and saturation voltage ( $V_{SAT}$ ) of each transistor. Also the common-emitter topology does not achieve a bandwidth as high as the common-collector, but the benefits of being able to swing closer to the rail ([Figure 2](#)) make it very appealing for single supply applications.



Figure 1. Simplified Output Stages



D001

Figure 2. Common-Emitter and Common-Collector Saturation Voltages

Both architectures face a limitation that is generally referred to in device data sheets as *output saturation voltage: high/low* or *output voltage low/high*. Figure 3 shows an example of this limitation.

OUTPUT					
Linear output voltage: low	$T_A = +25^\circ\text{C}$	$V_{S-} + 0.1$	$V_{S-} + 0.2$	V	A
	$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	$V_{S-} + 0.1$	$V_{S-} + 0.2$		B
Linear output voltage: high	$T_A = +25^\circ\text{C}$	$V_{S+} - 0.25$	$V_{S+} - 0.12$	V	A
	$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	$V_{S+} - 0.25$	$V_{S+} - 0.12$		B
Output saturation voltage: high/low			120/100	mV	C

Figure 3. Output Saturation of the THS4531A

**NOTE:** The op amp can still function in this region, but the performance begins to degrade rapidly; therefore, it is best to avoid operation in this condition. Consequently, the wider range of the common-emitter structure is better suited for low-supply applications.

### 3 Driving the ADC

Interfacing to an ADC generally requires a driving amplifier for optimal performance. Whether the driving amplifier is used to buffer the signal or increase the gain in the signal path, there are a number of reasons to use an op-amp front end. Some filtering is also typically required to improve signal integrity. Figure 4 shows a typical simplified diagram.

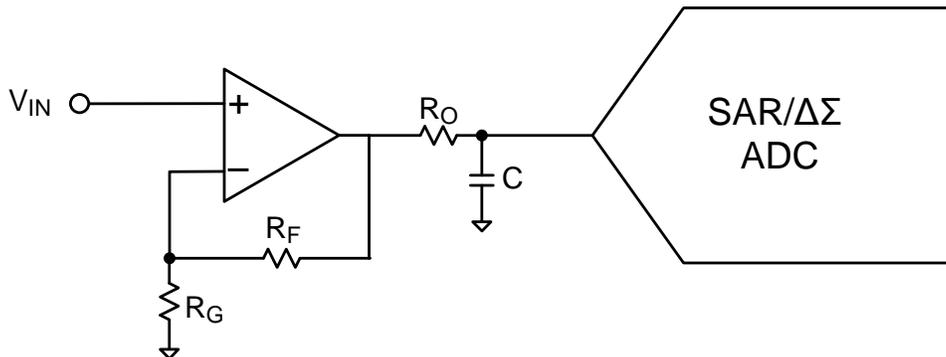
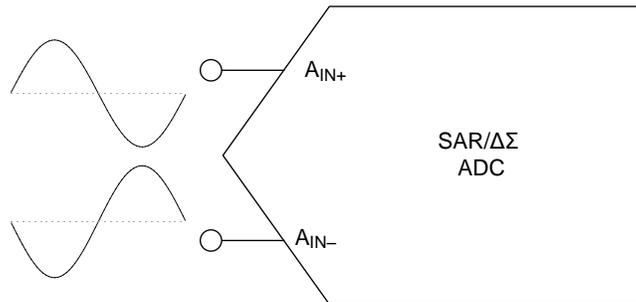


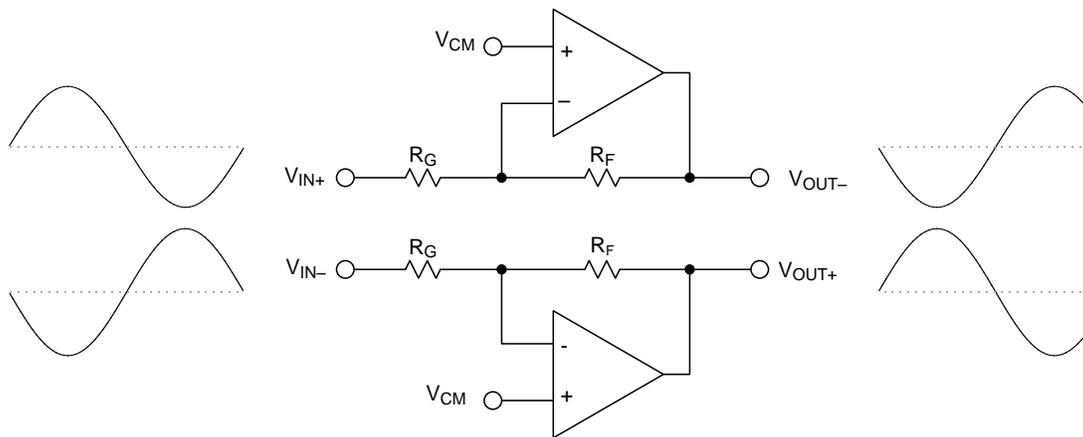
Figure 4. Typical ADC Driver Circuit

Modern ADCs tend to have a differential input structure which effectively doubles the dynamic range and can add an additional 6-dB improvement to the signal-to-noise ratio (SNR) at full scale.

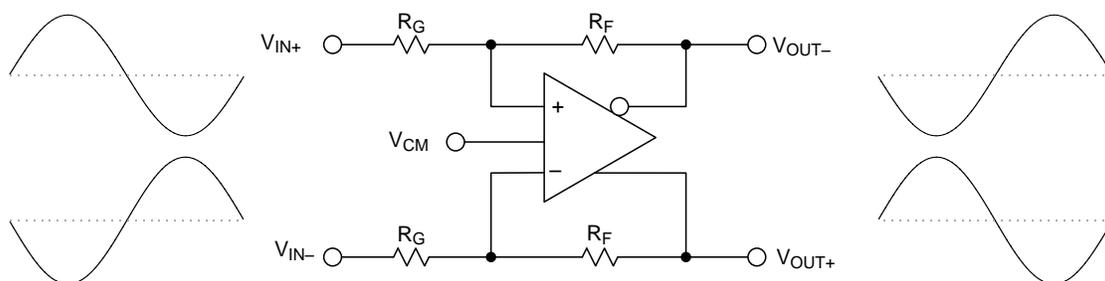


**Figure 5. Differential Input ADC**

Driving a fully-differential ADC is achieved by using a dual op amp shown in [Figure 6](#) or a fully-differential amplifier (FDA) [\[1\]](#) shown in [Figure 7](#).



**Figure 6. Differential-to-Differential Using a Dual Amplifier**



**Figure 7. Differential-to-Differential Using a Fully Differential Amplifier**

The benefit of using an FDA is that it tends to use less power and have better internal matching. This matching improves the even-order harmonics generated by the amplifier. Additionally, most FDAs have a pin ( $V_{CM}$  or  $V_{OCM}$ ) that controls the output common mode voltage, simplifying the task of matching the input common mode of the ADC.

The FDA can also convert single ended signals to differential with proper biasing on the unused input. The input signal can be bipolar or unipolar as is the case for single supply applications [\[2\]](#) [\[3\]](#) [\[4\]](#).

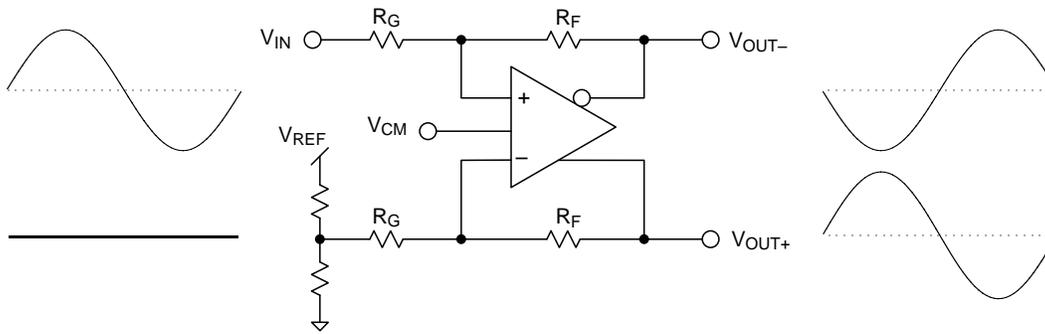


Figure 8. Single-Ended-to-Differential Using a Fully Differential Amplifier

#### 4 Extending the Range

The ADC input range is defined by a reference voltage ( $V_{REF}$ ).

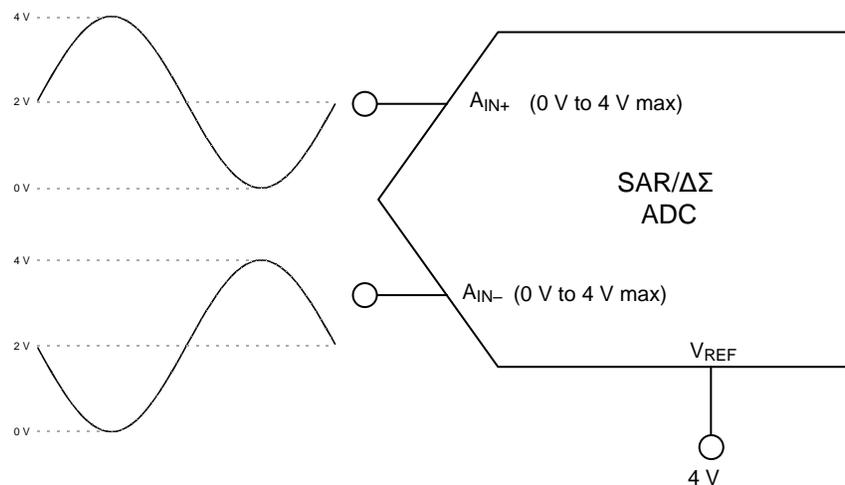
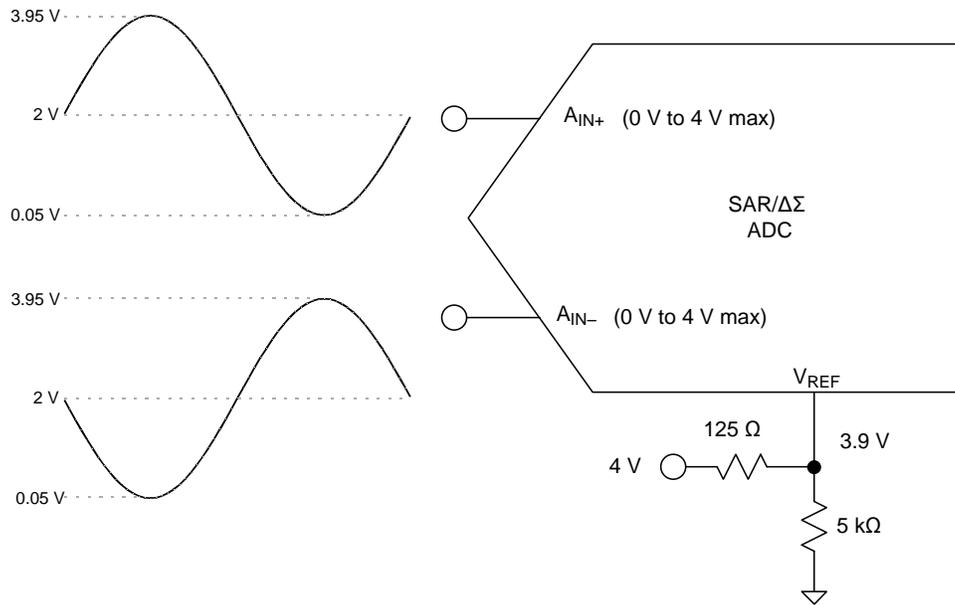


Figure 9. ADC Input Range Defined by  $V_{REF}$

The common mode range can vary from 0 V to  $V_{CC}$  (or close to  $V_{CC}$ ), but the differential input signal must not be greater than  $\pm V_{REF}$  as measured from positive input to negative input. For the maximum input swing,  $V_{REF}$  is set to the limit and the common mode voltage is set to  $V_{REF} / 2$  which includes 0 V for a full scale input. Note that using a larger  $V_{REF}$  results in an increased dynamic range which improves the signal-to-noise ratio (SNR) and reduces the impacts of noise on the system. Some applications may require reducing  $V_{REF}$  to give finer resolution in each step, but for portable applications reducing noise is more important and so an increased  $V_{REF}$  is better suited.

Often the driving amplifier will have a larger supply than the ADC which may allow a full scale output but at a common mode voltage too high for the ADC. The  $V_{OCM}$  pin of the FDA can be used to lower the common mode to a level that matches the ADC. In single supply systems reducing the output common mode too much may saturate the output stage of the amplifier for signals that approach 0 V. One solution is to reduce the amplifier gain to avoid saturation and reduce  $V_{REF}$  to avoid wasting codes shown in Figure 10.

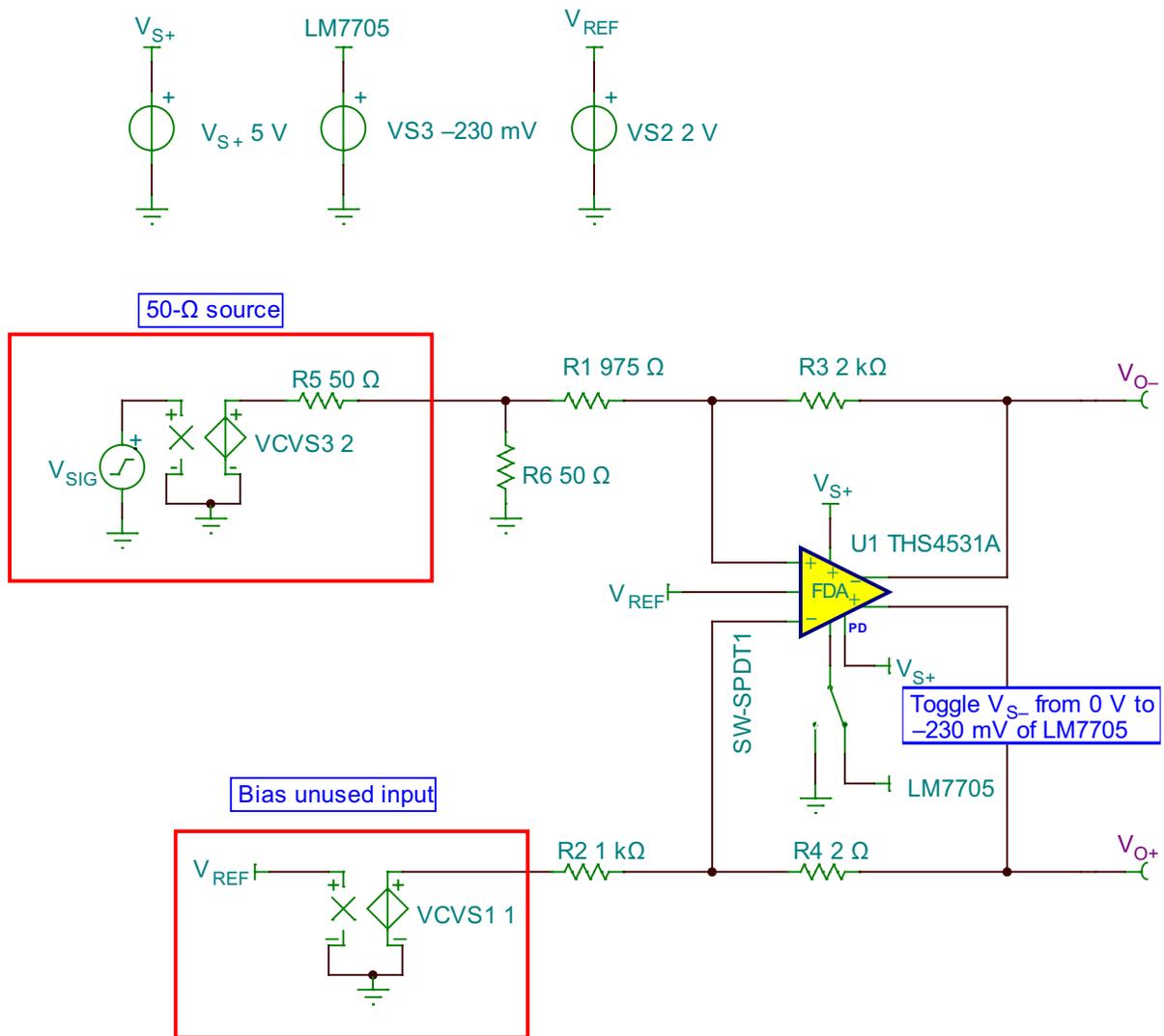


**Figure 10.  $V_{REF}$  Reduced to Avoid Saturation**

Although reducing the gain and  $V_{REF}$  is a common workaround, it results in a loss of SNR and thus a loss of accuracy for the ADC. Rather than connecting 0 V to the negative supply of the amplifier, for the purpose of this design, connect a negative voltage that is large enough to compensate for the headroom loss but not so large as to exceed the absolute maximum power supply ratings. The resulting effect is an extended linear range and an output that includes zero volts.

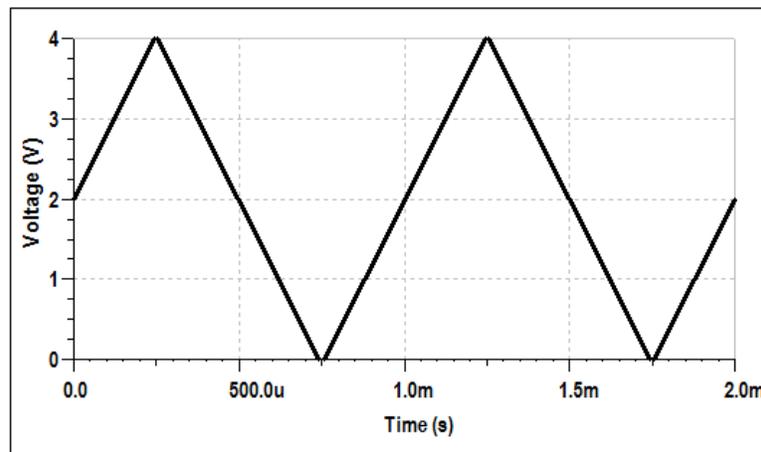
To test this theory, the THS4531A device which is an ultra low power RRO FDA with 36 MHz of bandwidth is used. The THS4531A device can operate on a single supply of 5 V with an absolute maximum rating of 5.5 V. The device also has an output saturation low of 100 mV. In order to compensate for the saturation without exceeding the absolute maximum ratings, a voltage between  $-100$  mV and  $-500$  mV can be added to the negative supply. It is important that additional supply does not introduce a lot of noise to the system, which is a common drawback among switching regulators. The LM7705 device was selected for this design because it is a very low-noise negative-bias generator that runs on a single 3 V to 5.25 V supply and outputs a regulated  $-230$  mV with good tolerance. The addition of  $-230$  mV results in a total op-amp supply of 5.23 V which is still within the maximum ratings for the device. A 5 V  $\pm 5\%$  or better power supply should also be used to ensure that the supply is kept within the absolute maximum ratings.

To simulate the desired effect, TI's SPICE-based Analog Simulation Program, [TINA](#), can be used. The LM7705 is represented as a DC voltage of  $-230$  mV and THS4531A device is represented by the THS4531A model. A TINA SPICE model for the THS4531A is provided online (see the [THS4531A product folder](#)).



**Figure 11. Schematic to Test the Impact of a Negative Supply**

To test the saturation, the output must swing to the negative rail. Set the THS4531A device with a gain of 2 V/V and use an input signal of 2 V<sub>pp</sub> with a 2-V offset and a frequency of 1 kHz as shown in Figure 12.


**Figure 12. Input Signal**

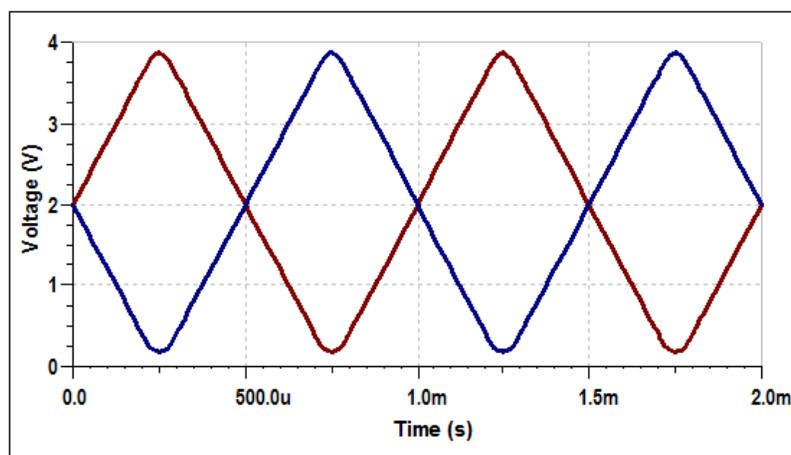
If the  $V_{OCM}$  terminal is connected to 2 V, each output is expected to swing from 0 V to 4 V resulting in a differential output of 8  $V_{PP}$ .

The negative supply can be configured to 0 V or  $-230$  mV by switching SW-SPDT1 (see [Figure 11](#)). [Figure 13](#) shows that with the negative supply connected to ground the output begins to saturate at about 200 mV on the low end.

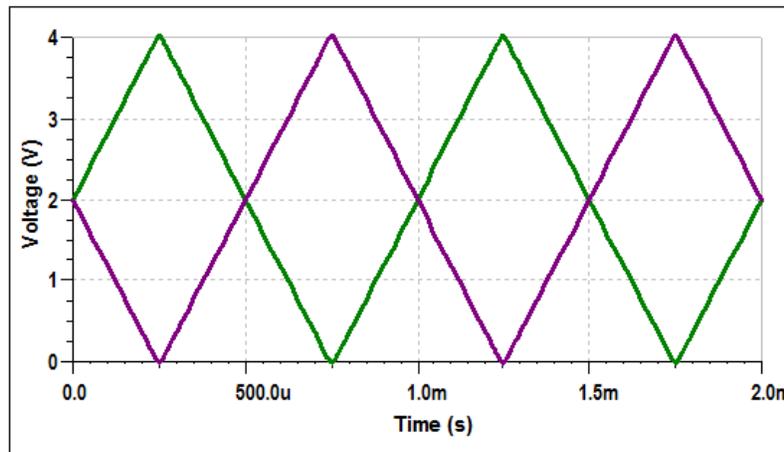
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**NOTE:** Because of the differential nature of the THS4531A device, the opposite output attempts to follow the saturated output in order to keep the input error as low as possible. In a real system, when one output begins to saturate, the linearity of the amplifier begins to degrade and the opposite output may not follow the saturated output very closely.

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**Figure 13. Saturated Output with Negative Supply Connected to Ground**

With the switch connected to the opposite side, the negative supply is set to  $-230$  mV. [Figure 14](#) shows that the output now has enough margin to swing down to true zero volts.



**Figure 14. Unclipped Output with Negative Supply Connected to LM7705**

## 5 Building a Prototype

Using the results from TINA, a prototype can be built to test on the bench. The schematic shown in [Figure 15](#) was drawn using the OrCAD Capture [5] in a similar configuration to the TINA schematic shown in [Figure 11](#). Jumper JP2 can switch the negative supply of the THS4531A device between the signal ground of 0 V and the LM7705 output of  $-230$  mV thus acting like the switch SW-SPDT1 shown in [Figure 11](#). To reduce any impact of switching noise caused by the LM7705 device, place bypass capacitors (C15 and C16) close to the output of the LM7705 device as well as a series ferrite bead (FB2). Other board population options are added to allow testing in a variety of applications. These options include power-down jumpers (JP1 and JP3), noise-gain boost for improved stability (R14 and C8), filtering, and single-ended-to-differential inputs or differential-to-differential inputs.

\*For optimal performance refer to the table below

	C1	C2	R5	R6	R3	R4
No Filtering	2 kΩ	2 kΩ	0 Ω	0 Ω	DNP	DNP
Feedback Filter Configuration	1 nF	1 nF	40.2 Ω	40.2 Ω	2 kΩ	2 kΩ

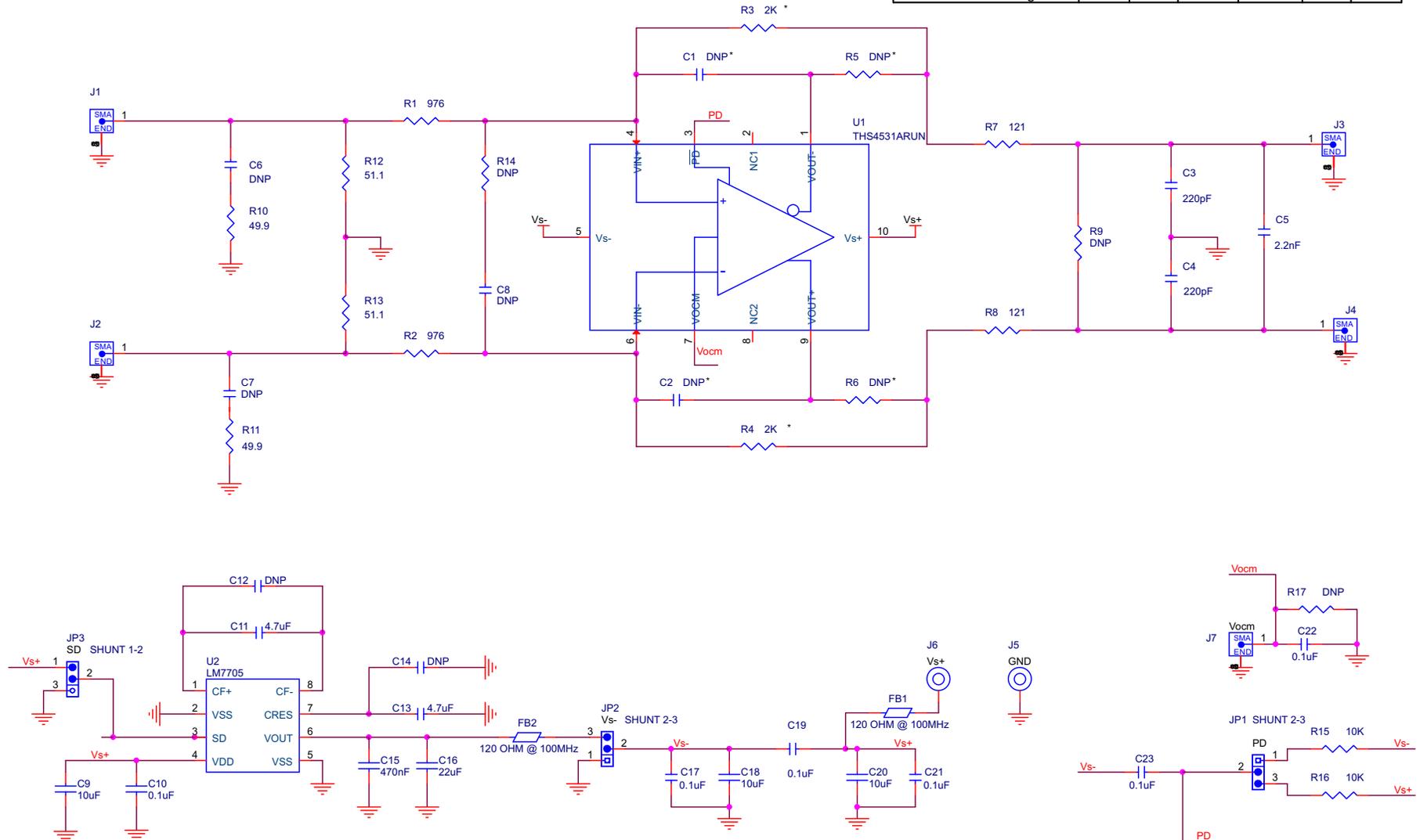
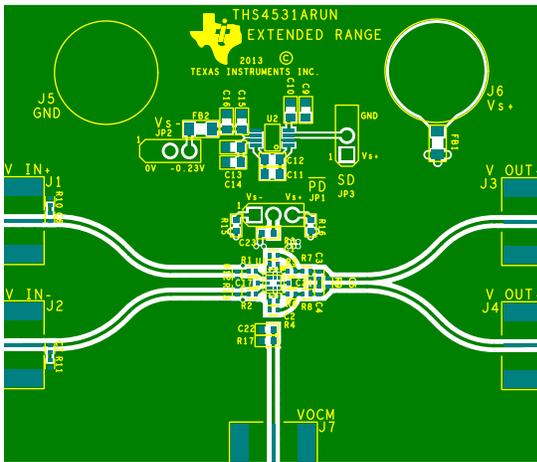
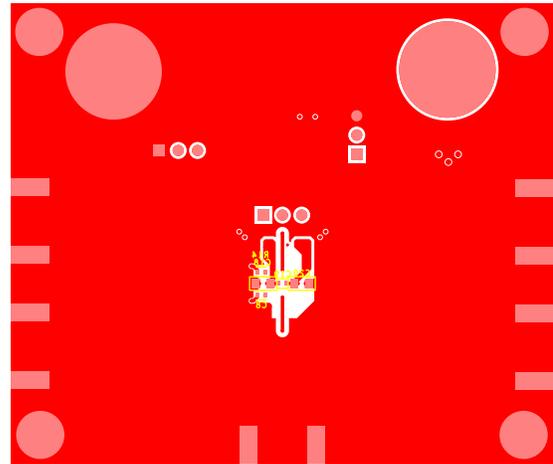


Figure 15. Test Board Schematic

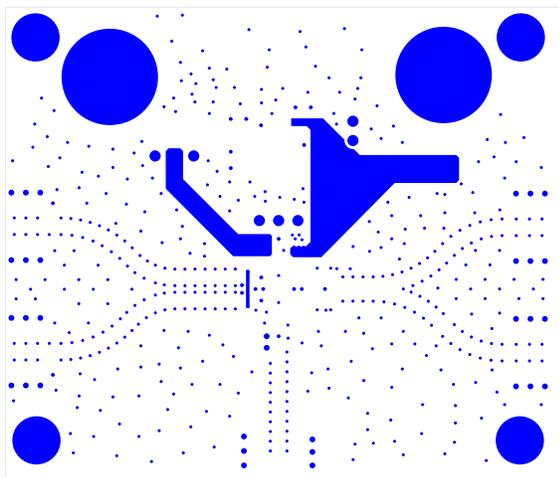
The Allegro PCB Designer [6] was used to build the layout as shown in Figure 16. This layout was built using good design techniques for high speed layout [7].



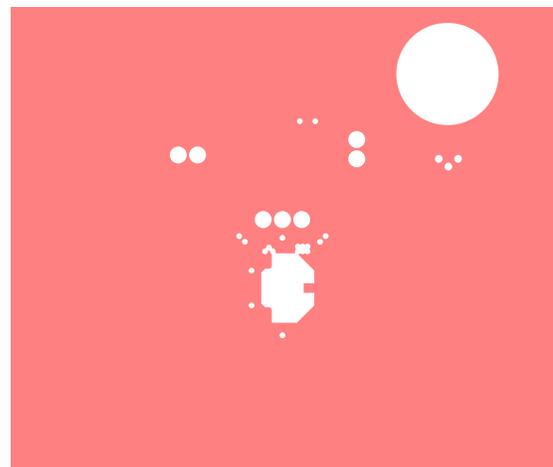
**Figure 16. PCB Layout Top View**



**Figure 17. PCB Layout Bottom View**



**Figure 18. PCB Layout Power View**



**Figure 19. PCB Layout Layer Ground View**

After the completion of the schematic and layout, a prototype was built and assembled for bench testing as shown in Figure 20.

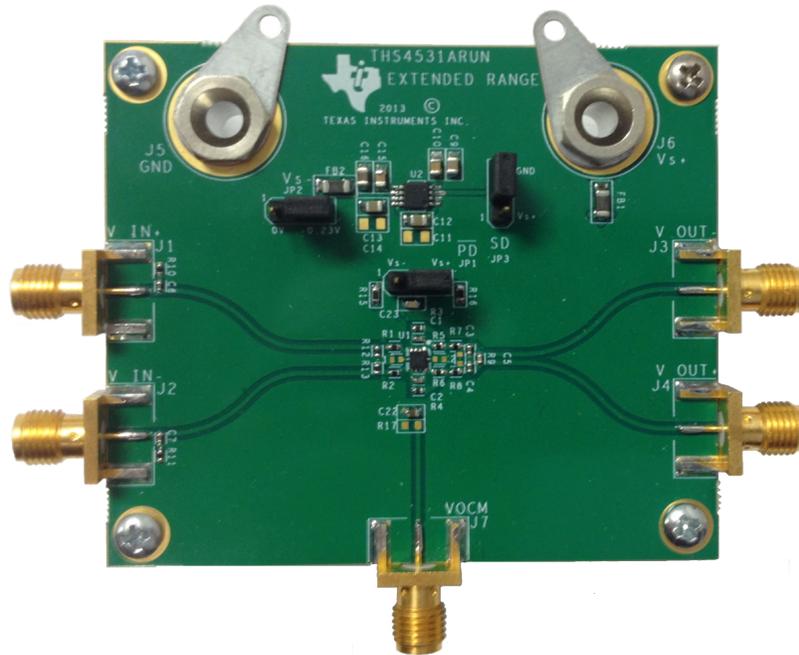


Figure 20. Assembled Test Board Top View

The board was populated using the same schematic configuration as shown in Figure 11 in order to verify the simulation results on the bench. Using a 1-kHz triangle wave with a 2.1-V<sub>PP</sub> amplitude and 2-V DC offset as the input signal, each output is expected to swing from -0.1 V to 4.1 V resulting in an 8.4-V<sub>PP</sub> differential signal. With JP2 (see Figure 15) in position 2-1, the THS4531A negative supply is connected to 0 V. Figure 21 shows that the output saturates when it approaches 0 V.

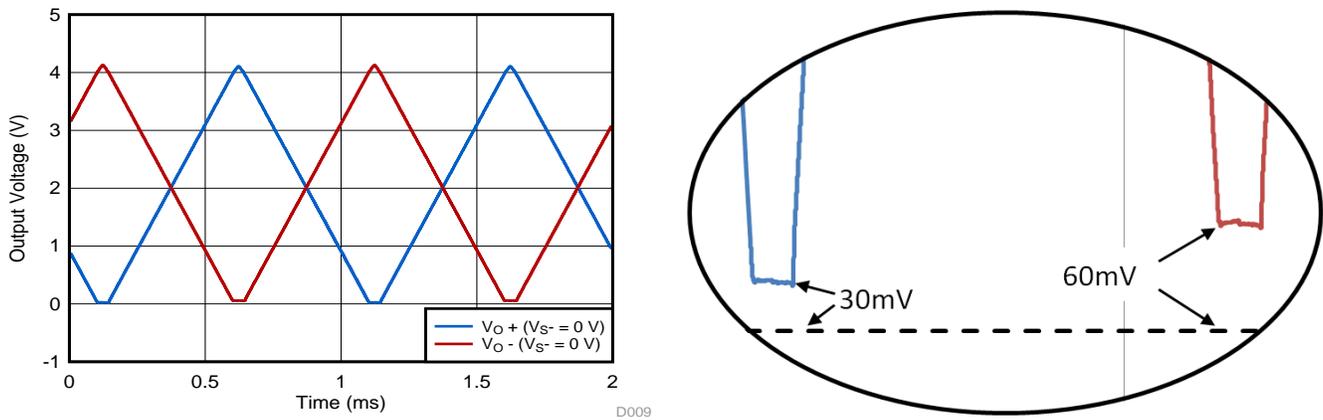
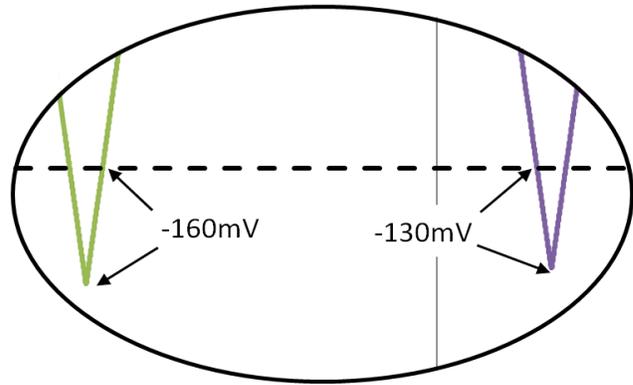
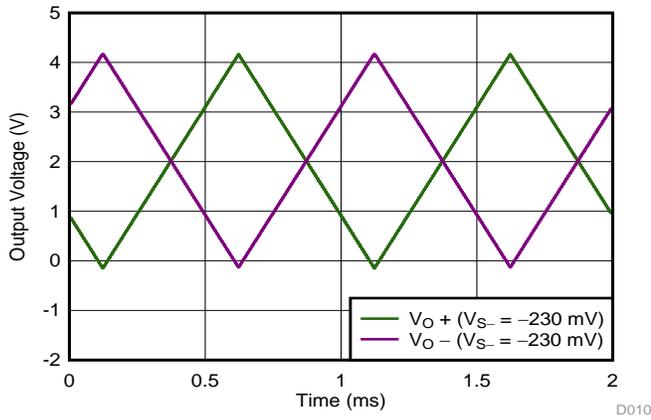


Figure 21. Measured Data with Negative Supply Connected to Ground

The positive output and negative output can only reach 30 mV and 60 mV respectively. This result is closer to the negative rail than what was previously simulated which can be expected because the TINA models are simplified and do not predict perfectly what happens at or near saturation.

With the JP2 in position 2-3, the negative supply of the THS4531A device is connected to the -230 mV output of the LM7705 device. Figure 22 shows that the THS4531A device is no longer saturating and can swing below 0 V.



**Figure 22. Measured Data with Negative Supply Connected to LM7705**

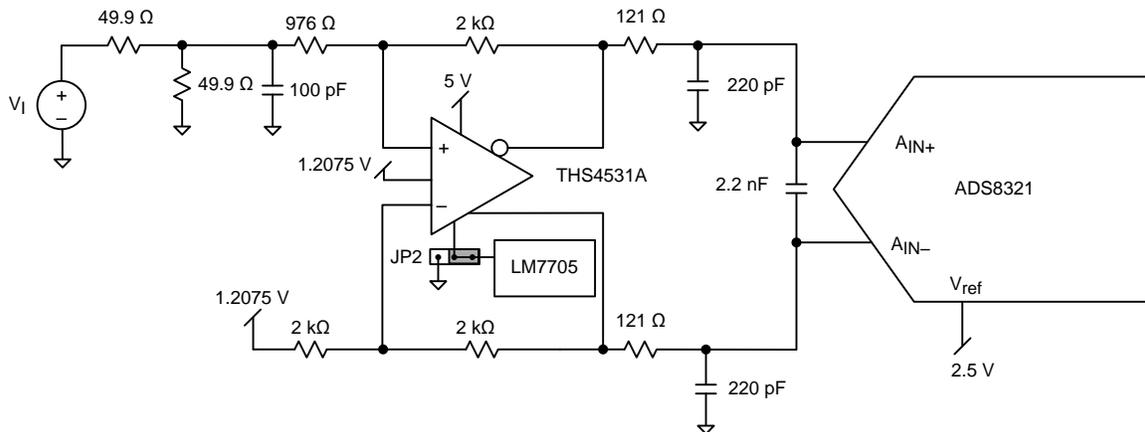
As shown in [Figure 22](#), the positive output and negative output swing are  $-160\text{ mV}$  and  $-130\text{ mV}$ , respectively. The added range allows the THS4531A to drive to  $0\text{ V}$  and will also improve the linearity in this region.

## 6 Testing in a Typical Application

The THS4531A device is a very good low-power driver for many differential data converters. This technique can be used to drive the ADS8321 device which is a high performance differential SAR ADC with 16 bits of resolution, a 100-kHz sampling rate, and typical 87 dB of SNR (see the ADS8321 data sheet, [SBAS123](#) for more information).

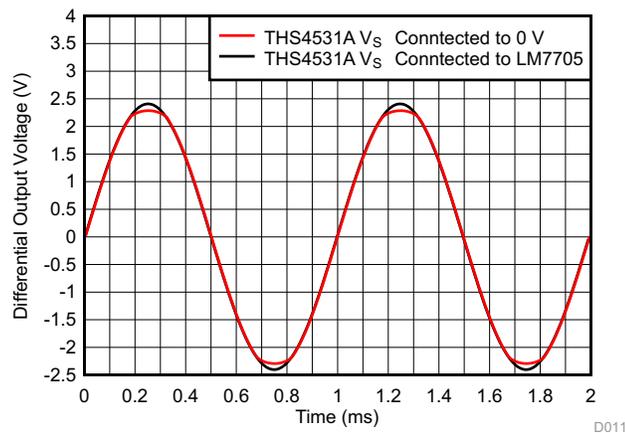
The ADS8321 device has an analog supply of 5 V and a full-scale differential voltage range of  $\pm V_{REF}$ . In this example  $V_{REF}$  is connected to 2.5 V which results in a maximum input voltage range of  $5 V_{PP}$  differential.

The ADS8321 device has an available EVM which is used to evaluate the ADS8321 device (see the ADS8321EVM User's Guide, [SBAU140](#)). Configure the test board and make the connection to the ADS8321EVM as shown in [Figure 23](#) to evaluate the THS4531A device in a full signal chain.



**Figure 23. Driving ADS8321 With THS4531A**

When a single-ended sinusoidal input signal of  $2.415 V_{PP}$  is used and the  $V_{OCM}$  terminal is connected to 1.2075 V, each single-ended output is expected to swing from 0 V to  $2.415 V$  resulting in a differential voltage of  $4.83 V_{PP}$  or a  $-0.3$ -dBFS signal that includes 0 V. JP2 can be configured to connect the negative supply of the THS4531A to either signal ground of 0 V or the LM7705 output of  $-230$  mV. [Figure 24](#) shows what this looks like in the time domain using a 1-kHz input signal.

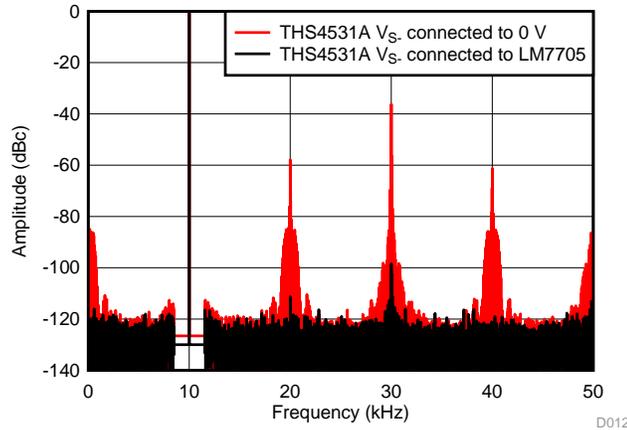


$$V_{IN} = 2.415 V_{PP} \quad f_{IN} = 1 \text{ kHz} \quad V_{OUT\_DIFF} = -0.3 \text{ dBFS}$$

$$V_{OCM} = 1.2075 \text{ V} \quad f_s = 100 \text{ kHz}$$

**Figure 24. Time-Domain Capture of 1kHz Sine Wave using THS4531A and ADS8321 With and Without LM7705**

With the negative supply of the THS4531A connected to 0 V, the output saturates similar to the previous bench results. Connecting the negative supply of the THS4531A to the LM7705 output remedies this problem and allows a full unclipped sine wave of  $\pm 2.415 V_{PP}$  differential that includes 0 V.



16 384 Point FFT       $f_{IN} = 10 \text{ kHz}, -0.3 \text{ dBFS}$        $f_S = 100 \text{ kHz}$   
 $V_{OCM} = 1.2075 \text{ V}$

Figure 25. FFT of 10 kHz Sine Wave Using THS4531A and ADS8321 With and Without LM7705

Figure 25 shows an FFT performed on an input signal of 10 kHz. Because of the sampling clock of the ADS8321 being generated onboard, providing a clean external clock source with coherent sampling is not possible. Therefore the input signal was tuned as close as possible to coherency for 16 384 samples and  $\pm 250$  bins around the fundamental were notched and replaced with the RMS noise power. Figure 25 shows the dramatic effect that saturation has on the frequency spectrum. When connected to the LM7705 device, a clean and stable spectrum was produced. Table 1 lists a comparison of the results against the typical values in the ADS8321 datasheet.

Table 1. Performance Versus the ADS8321 Data Sheet

CONFIGURATION	$V_{S-}$ OF THS4531A	$V_{OCM}$ OF THS4531A (V)	TONE (kHz)	SIGNAL (dBFS)	SNR (dBC)	THD (dBC)	SINAD (dBC)	SFDR (dBC)
ADS8321 with THS4531A	0 V	1.2075	10	-0.3	37.5	-36	33.6	36
ADS8321 with THS4531A and LM7705	-230 mV	1.2075	10	-0.3	88.4	-97.7	88	98
ADS8321 (typical)	-	-	10	-0.3	87	-86	84	86

## 7 Conclusion

This reference design has described a simple and straight forward approach to extending the range of a RRO op amp using TI's THS4531A low-power RRO FDA and LM7705 low-noise negative-bias generator. Use the information provided in this report to rebuild this circuit and adjust it according to the given requirements. This circuit was also designed with multiple configurable options so that the circuit can be repurposed to include filtering, single ended or differential inputs, and a way to adjust the noise gain for improved stability. Note that the THS4531A device is pin-for-pin compatible with the THS4541 and THS4521 device family which provides a good starting place for fully differential SAR-ADC drivers.

## 8 References

1. *Fully-Differential Amplifiers*, Karki 2002, [SLOA054](#)
2. *Using fully differential op amps as attenuators, Part 1: Differential bipolar input signals*, Karki 2009, [SLYT336](#)
3. *Using fully differential op amps as attenuators, Part 2: Single-ended bipolar input signals*, Karki 2009, [SLYT341](#)
4. *Using fully differential op amps as attenuators, Part 3: Single-ended unipolar input signals*, Karki 2009, [SLYT359](#)
5. Cadence OrCAD Capture, [http://www.cadence.com/products/orcad/orcad\\_capture](http://www.cadence.com/products/orcad/orcad_capture)
6. Allegro PCB Designer, [http://www.cadence.com/products/pcb/pcb\\_design](http://www.cadence.com/products/pcb/pcb_design)
7. *PCB Layout for Low Distortion High-Speed ADC Drivers*, Ramus 2004, [SBAA113](#)

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