

Design Considerations for TIDA-00356

CC2541:

Versatile, well documented, low power, easy implementation, Automotive qualified

- This design utilizes the SAT0016 BLE module which is a complete design including crystals and PCB antenna, which greatly simplifies layout and design considerations. Primary layout considerations for the main board include minimizing distance to power capacitors and avoiding any excess metal or ground planes within close proximity to the module antenna.
- To prolong battery life, each input is configured to operate as an interrupt input rather than polling the switches periodically.
- The I2C pins are configurable as GPIOs, but interrupts are not available on the I2C pins. As such these pins were allocated to the two outputs in the design – PWM and module LED.
- Pins 0 and 1 on Port 1 of the CC2541 do not have internal pull-downs, requiring external 10kΩ resistors for this design.
- Each switch has a debounce capacitor, and for the debugging lines these capacitors can interfere with programming and debugging. For this design, the switches and debounce capacitors can be isolated from the module when the debugger is present via jumpers J5 and J7.

TPS79801Q:

Wide voltage input, connects directly to car battery, reverse input protection

- The LDO is configured for 3V output via resistors R5 and R6.

TPS92638Q:

Wide voltage input, connects directly to car battery, 8 Channel output, low component count.

- For this application all PWM channels are tied together to a single GPIO. The LED driver is not operational off the Li-Ion battery, and the current in each channel is limited to 20mA via the reference resistor R11.
- Running the LED driver at the limited current for extended periods of time can generate significant amounts of heat, and as such special layout considerations should be observed to ensure appropriate thermal dissipation.

TPD4E001Q:

Multiple channels with small footprint, simple integration

- These TPD devices require very little configuration and are capable of protecting the CC2541 from Level 4 Contact Discharge on each of the tactile switches.

Design Improvements:

This design utilizes all GPIOs available on the SAT0016 module. Multiplexing GPIOs or using a matrix keypad for user input would greatly simplify the design. Placing PWM on the I2C line requires software PWM to operate, should be moved to a pin with a hardware timer as per Table 7-1 in the CC2541 user guide:

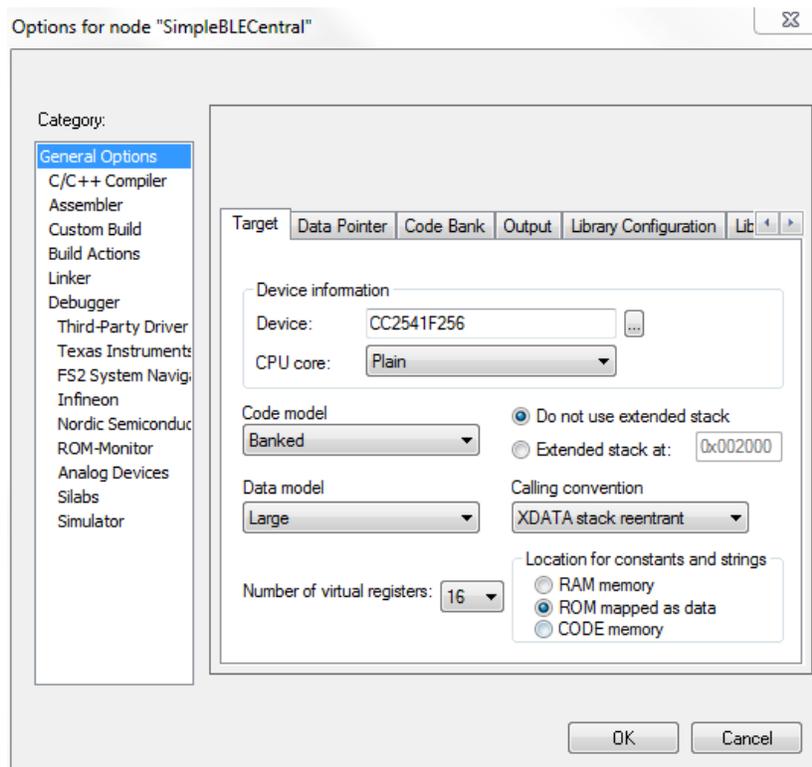
Table 7-1. Peripheral I/O Pin Mapping

Periphery/ Function	P0								P1								P2				
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	4	3	2	1	0
ADC	A7	A6	A5	A4	A3	A2	A1	A0													T
Operational amplifier						O	-	+													
Analog comparator			+	-																	
USART 0 SPI			C	SS	MO	MI															
Alt. 2											MO	MI	C	SS							
USART 0 UART			RT	CT	TX	RX															
Alt. 2											TX	RX	RT	CT							
USART 1 SPI			MI	MO	C	SS															
Alt. 2									MI	MO	C	SS									
USART 1 UART			RX	TX	RT	CT															
Alt. 2									RX	TX	RT	CT									
TIMER 1		4	3	2	1	0															
Alt. 2	3	4												0	1	2					
TIMER 3												1	0								
Alt. 2									1	0											
TIMER 4															1	0					
Alt. 2																		1			0
32-kHz XOSC																	Q1	Q2			
DEBUG																			DC	DD	
OBSSEL											5	4	3	2	1	0					

SOFTWARE DESIGN CONSIDERATIONS:

Shunts present on jumpers J5 and J7 can cause errors and warnings during programming. Removing these shunts disconnects debounce capacitors from the Debug Data and Debug Clock lines and should eliminate many errors that only occur when attempting to debug or program the device.

General IAR compiler warnings and errors: As this code had been built off of existing workspaces, many of the compiler options and settings have been pre-set. If however the code is being utilized as a reference, then special care should be taken to ensure that proper workspace options have been set. The following contains the full list of settings as of this document for **IAR version 8.20**, and serves only as a point of reference for future development and debugging. Some of these settings have been modified for debugging purposes and may not be required, and using these settings does not guarantee correct operation of the IAR compiler or software. For use with IAR version 8.30, know issues can arise with association to the linker file configuration.



Options for node "SimpleBLECentral"



Category:

- General Options
- C/C++ Compiler
- Assembler
- Custom Build
- Build Actions
- Linker
- Debugger
 - Third-Party Driver
 - Texas Instruments
 - FS2 System Navig
 - Infineon
 - Nordic Semiconduc
 - ROM-Monitor
 - Analog Devices
 - Silabs
 - Simulator

Target | Data Pointer | Code Bank | Output | Library Configuration | Lib

Number of DPTRs: 1

Size

16 bit

24 bit

DPTR select

Select register: 0x92

Toggle using INC

Set using XOR/AND

Mask: 0xFF

Page register address

Bit 8-15: 0x93

Bit 16-23:

DPTR addresses

Shadowed

Separate

Configure ...

OK Cancel

Options for node "SimpleBLECentral"



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Target | Data Pointer | Code Bank | Output | Library Configuration | Lib

Number of banks: 0x07

Register address: 0x9F

Register mask: 0xFF

Bank start: 0x8000

Bank end: 0xFFFF

OK Cancel

Options for node "SimpleBLECentral"

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Library Configuration | Library options | Stack/Heap | MISRA-C:2004

Stack sizes	Heap sizes
IDATA: 0xC0	XDATA: 0xFF
PDATA: 0x00	Far: 0xFFF
XDATA: 0x280	Far22: 0xFFF
Extended: 0x3FF	Huge: 0xFFF

OK Cancel

Options for node "SimpleBLECentral"

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Factory Settings

Multi-file Compilation
 Discard Unused Publics

Optimizations | Output | List | Preprocessor | Diagnostics | Extra Opt

Ignore standard include directories

Additional include directories: (one per line)

```

$PROJ_DIRS\..\..\common
$PROJ_DIRS\..\Source
$PROJ_DIRS\..\..\..\Components\hal\include
$PROJ_DIRS\..\..\..\Components\hal\target\CC2540EB
$PROJ_DIRS\..\..\..\Components\osal\include

```

Preinclude file:

Defined symbols: (one per line)

```

INT_HEAP_LEN=3072
HALNODEBUG
OSAL_CBTIMER_NUM_TASK
HAL_AES_DMA=TRUE

```

Preprocessor output to file
 Preserve comments
 Generate #line directives

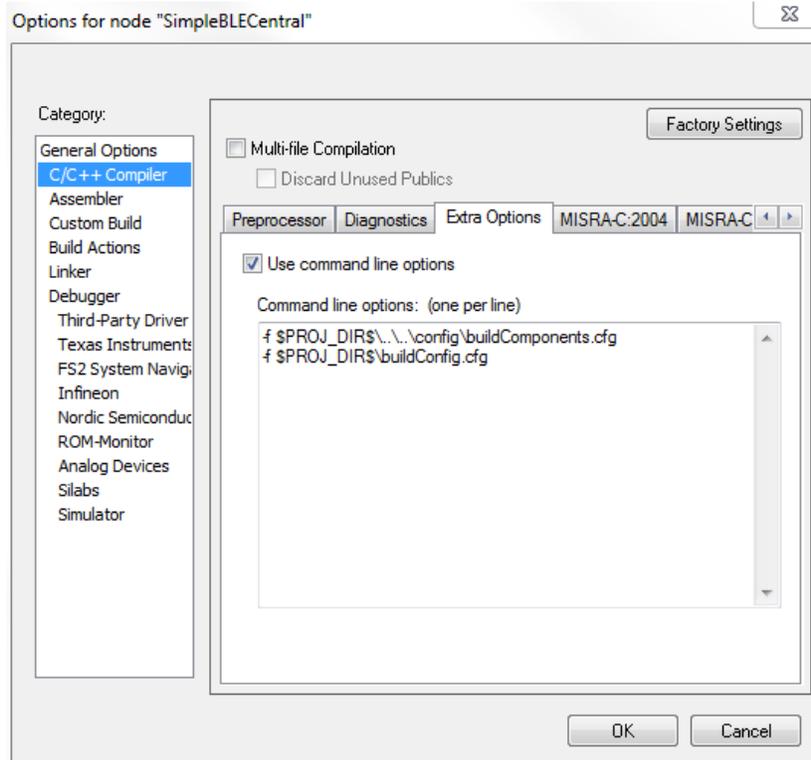
OK Cancel

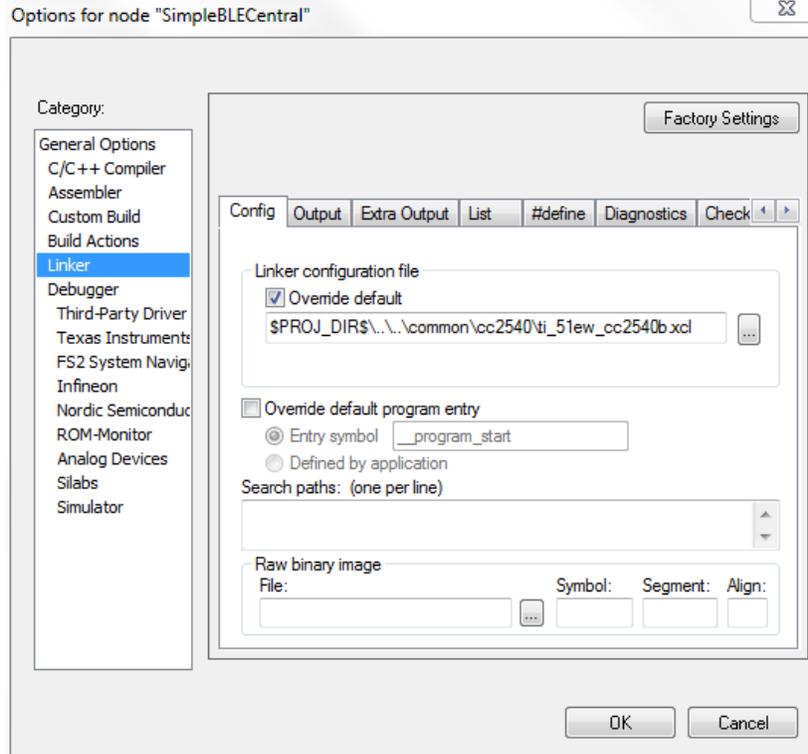
Additional Directories

```
$PROJ_DIR$\\..\..\common  
$PROJ_DIR$\\..\Source  
$PROJ_DIR$\\..\..\..\Components\hal\include  
$PROJ_DIR$\\..\..\..\Components\hal\target\CC2540EB  
$PROJ_DIR$\\..\..\..\Components\osal\include  
$PROJ_DIR$\\..\..\..\Components\services\saddr  
$PROJ_DIR$\\..\..\..\Components\ble\include  
$PROJ_DIR$\\..\..\..\Components\ble\controller\phy  
$PROJ_DIR$\\..\..\..\Components\ble\controller\include  
$PROJ_DIR$\\..\..\..\Components\ble\hci  
$PROJ_DIR$\\..\..\..\Components\ble\host  
$PROJ_DIR$\\..\..\common\cc2540  
$PROJ_DIR$\\..\..\common\npi\npi_np  
$PROJ_DIR$\\..\..\Include  
$PROJ_DIR$\\..\..\Profiles\Roles  
$PROJ_DIR$\\..\..\Profiles\SimpleProfile
```

Defined Symbols

```
INT_HEAP_LEN=3072  
HALNODEBUG  
OSAL_CBTIMER_NUM_TASKS=1  
HAL_AES_DMA=TRUE  
HAL_DMA=TRUE  
POWER_SAVING  
HAL_LCD=FALSE  
HAL_LED=FALSE
```





If there are linker issues while using IAR version 8.30:

- Go to C:\Texas Instruments\BLE-CC254x-1.4.0\Projects\ble\common\cc2540\ti_51ew_cc2540b.xcl
- Change the line "-Z(DATA)VREG+_NR_OF_VIRTUAL_REGISTERS=08-7F" to "-Z(DATA)VREG=08-7F"

Note: IAR changed the way virtual registers are handled and placed. Therefore the linker configuration files must be updated

For more information on software development, including estimating memory size and debugging in IAR, please refer to document [SWRU271](#) on the Texas Instruments website.

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