

TI Designs

Low Noise Power Solution Reference Design for Clock Generators



TI Designs

TI Designs provide the foundation that you need including methodology, testing and design files to quickly evaluate and customize the system. TI Designs help **you** accelerate your time to market.

Design Resources

[TIDA-00597](#)

Design Folder

[LP3878-ADJ](#)

Product Folder

[LMK03806BEVAL](#)

Product Folder



[Ask The Analog Experts](#)
[WEBENCH® Design Center](#)

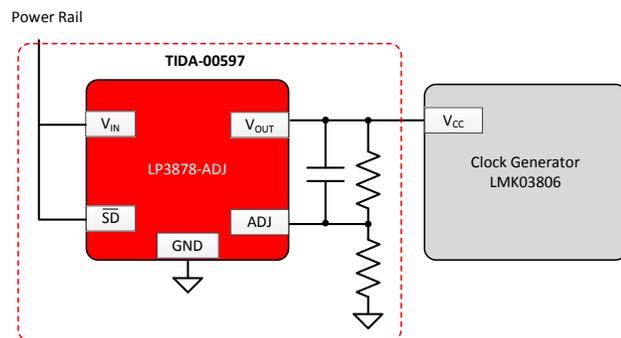
Design Features

- Low Noise for Clock Generator
- Up to 800-mA output current
- Output Voltage Enable and Disable

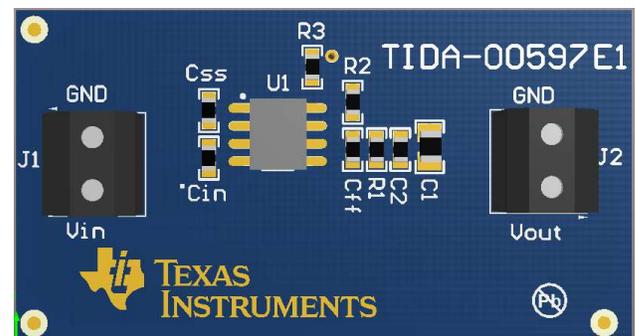
Featured Applications

- Clock Generator
- ASIC power supplies
- DSP and FPGA power supplies

Block Diagram



Board Image



1 System Description

Clock generator is widely used in many applications like Ethernet, Fiber Channel, PCIE and Network processors, among the characteristics, phase noise is a key parameter, which is required to meet strict requirement. If the clock phase noise is degraded, then both down-converted and up-converted signals are corrupted. Many factors degrade clock phase noise performance, and one among them is supply noise. In order to improve phase noise performance, LDO, linear regulator with low noise, is used for powering clock generator.

This design illustrates the clock phase noise degradation due to supply noise, and implements a low noise LDO to power clock generator. This design provides design files such as schematic, Gerber files, and test data.

1.1 Device Selection Considerations

In this design, the case of designing supply for the LMK03806 is depicted. LMK03806 is a high performance, multi-rate clock generator capable of synthesizing 8 different frequencies on 14 outputs. In the design, a low noise LDO with large output current like LP3878-ADJ is implemented as power supply for LMK03806.

Table 1 Design parameters

PARAMETERS	VALUES
V_{IN}	3.9V to 5V
V_{OUT}	3.3V
I_{LOAD}	800mA

2 Block Diagram

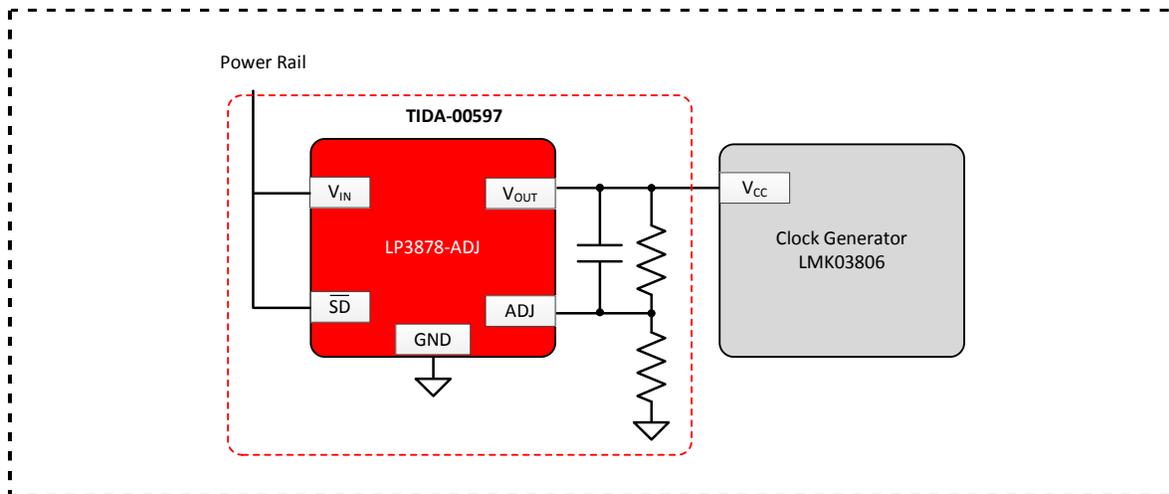


Figure 1 Block Diagram

Figure 1 gives a block diagram of the system. The red block represents the focus component of this document. The grey components are mentioned in this document and its power requirements is defined and taken into consideration to specify the system requirements and test parameters; however this component was not design into the TIDA-00597 and some of their application specific requirements are not mentioned, it is recommended to review its datasheet for additional application implementation requirements.

2.1 Component Selection

This design selects the following parts:

- [LP3878-ADJ](#): 800-mA Linear Regulators with Adjustable Output Stable with Ceramic Output Cap.
- [LMK03806](#): Ultra-low jitter clock generator with 14 outputs

2.1.1 LP3878-ADJ

The LP3878-ADJ is an 800 mA adjustable output voltage regulator designed to provide high performance and low noise in applications requiring output voltage as low as 1.0-V.

The LP3878-ADJ delivers superior performance:

- **Ground Pin Current:** Typically 5.5-mA @ 800-mA load and 180- μ A @ 100- μ A load.
- **Low Power Shutdown:** the LP3878-ADJ draws less than 10- μ A quiescent current when shutdown pin is pulled low.
- **Precision Output:** Ensured output voltage accuracy is 1% at room temperature.
- **Low Noise:** broadband output noise is only 18- μ V (typical) with 10-nF bypass capacitor.

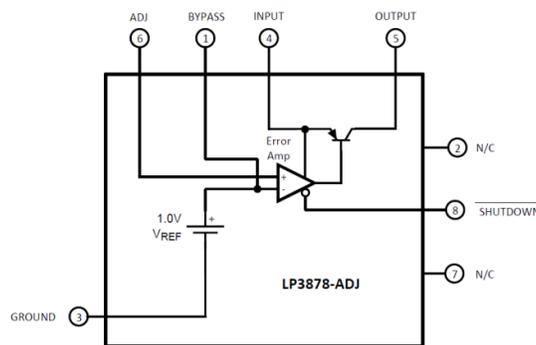


Figure 2 LP3878-ADJ Block Diagram

3 Design Considerations

This design provides the description of clock phase noise degradation due to supply noise, and provides test results. The clock generator of LMK03806 is not designed in this design. The test results are conducted on LMK03806BEVAL.

3.1 Supply Noise Impact on Phase Noise

Phase noise at the clock generator output is affected by supply noise mostly due to the following two significant reasons.

3.1.1 Ringing at V_{CC} Due to Change in Current Drawn by Clock Generator

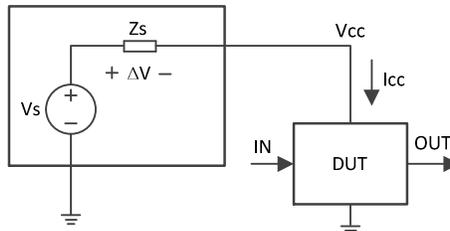


Figure 5 Simple Setup with Clock Generator and Supply

Figure 5 shows a simple block diagram with the clock generator, the device under test, (DUT) supplied by the V_{CC} and I_{CC}. The supply is considered to have source voltage, V_s, and source impedance, Z_s. This supply can either be considered as a laboratory supply or laboratory supplies + LDO. In an ideal case, Z_s = 0; however, in a non-ideal world, Z_s ≠ 0.

With the activity of clock generator, the supply current I_{CC} changes, and this changes the drop across Z_s, i.e., ΔV, this translates to change in the supply V_{CC} and is added as noise to clock generator phase noise. This noise can be minimized by using supplies with minimum Z_s, or the LDOs used must be robust against the changes in I_{CC}. Essentially, it is desirable that the ac output impedance be as low as possible. Most of the TI LDOs has low output impedance (and usually decoupling capacitors are added to minimize the ac output impedance), and thus the phase noise affected due to V_{CC} ringing is less.

3.1.2 Noise Generated by LDO

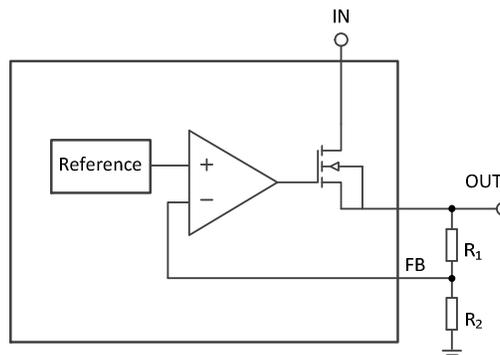


Figure 6 Simplified LDO Block Diagram

Figure 6 shows the simplified LDO block diagram. The LDO output is regulated with respect to the LDO band gap reference. Any noise on the LDO band-gap reference is translated at the LDO output. Considering the noise power generated at the band gap reference V_{NBG}, the noise power at the output from the band gap reference V_{NOUT} is as is given in Equation 1:

$$V_{NOUT} = V_{NBG} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

Along with the LDO band-gap reference, total output noise at the LDO output is the sum of noise generated by the error amplifier, noise from the pass transistor, and thermal or 4KTR noise from the

R_1 and R_2 resistor divider network. Noise from LDO band-gap reference is usually the dominant source. This design illustrates the importance of this noise, which effects phase noise. It is important to select low noise LDO to improve clock generator phase noise.

4 Design Implementation Guidelines

4.1 Input and Output Capacitor

Input and output capacitors eliminate high frequency noise and are necessary for loop stability. Consider the following recommendations:

- Utilize X7R or X5R ceramic capacitors to minimize tolerance and variation with temperature
- Capacitance ESR in the 50- to 200-kHz range must not exceed 25mΩ
- Input and output caps must be located less than 1 inch from the input and output pins
- Input minimum capacitance of 4.7-μF
- Output minimum capacitance of 10-μF
- Minimum of ±20% capacitance tolerance

4.2 Noise Bypass Capacitor

As mentioned in [section 3.1.2](#), noise from LDO band-gap reference is usually the dominant source. A 100-nF bypass capacitor on the BYPASS pin significantly reduces band-gap noise. The following recommendation must be taken into account:

- The bypass capacitor leakage must never exceed 100-nA.
- High-quality ceramic capacitors with either an NPO or COG dielectric typically have very low leakage.

4.3 Setting the Output Voltage

The output voltage is set by using an external resistor divider R_1 (upper-side resistor) and R_2 (lower-side resistor). The formula for output voltage is:

$$V_{OUT} = V_{ADJ} \times \left(1 + \frac{R_1}{R_2}\right) \quad (2)$$

R_2 must be less than 5 kΩ to ensure loop stability. To be compliant with the 5-kΩ rule, 866-Ω was chosen for R_2 , then 2-kΩ was chosen for R_1 to yield the expected voltage of 3.3-V.

4.4 Feedforward Capacitor

The feedforward capacitor C_{FF} is required to increase phase margin, ensure loop stability.

The C_{FF} forms both a pole and zero in the loop gain. The zero provides a beneficial phase lead (which increases phase margin), and the pole adds an undesirable phase lag that must be minimized.

The zero frequency is determined by the values of C_{FF} and R_1 :

$$F_Z = \frac{1}{2\pi C_{FF} \times R_1} \quad (3)$$

The pole frequency is determined by the value of C_{FF} and the parallel combination of R_1 and R_2 :

$$F_P = \frac{1}{2\pi C_{FF} \times \frac{R_1 \times R_2}{R_1 + R_2}} \quad (4)$$

For $V_{OUT} \geq 2.5$ -V, C_{FF} should be selected to set the zero frequency in the range of about 20-kHz to 100-kHz. The zero frequency is set to 36-kHz.

$$C_{FF} = \frac{1}{2\pi F_Z \times R_1} = \frac{1}{2\pi \times 36\text{kHz} \times 2\text{k}\Omega} = 2200 \text{ pF} \quad (5)$$

The feedforward capacitor C_{FF} can also help to reduce output noise. This capacitor forwards (bypasses) output noise around R_1 . This bypass or shorting action prevents the bandgap noise from being increased by the gain of error amplifier at frequencies higher than the resonant frequency, $f_{Resonant}$, of R_1 and C_{FF} , where,

$$F_{Resonant} = F_Z = \frac{1}{2\pi C_{FF} \times R_1} \quad (6)$$

The equation (1) becomes:

$$V_{NOUT} = V_{NBG} \times \left(1 + \frac{R_1 \parallel \frac{1}{2\pi \times f \times C_{FF}}}{R_2}\right) \quad (7)$$

5 Test Setup and Results

In order to show the advantage of selecting low noise LP3878-ADJ, below setups were made to quantify the benefits.

5.1 LP3878-ADJ vs DCDC Switching Supply

This setup used LP3878-ADJ and DCDC switching supply, and measure the clock phase noise.

Table 2 Test Equipment

Equipment	device number	Function
Lab linear supply	Agilent E3631A	Constant voltage supply
DCDC switching supply	TPS62203EVM	3.3V output for LMK03806BEVAL
Clock generation	LMK03806BEVAL	Clock generation
Signal source analyzer	N9020A	Used to measure phase noise

Figure 7 represents the test setup.

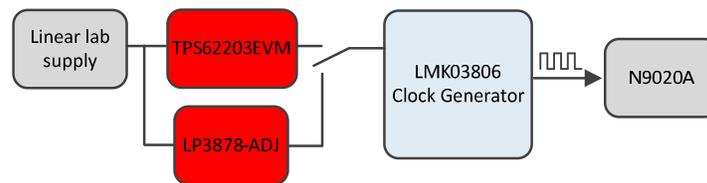


Figure 7 Test Setup of LP3878-ADJ vs DCDC Switching Supply

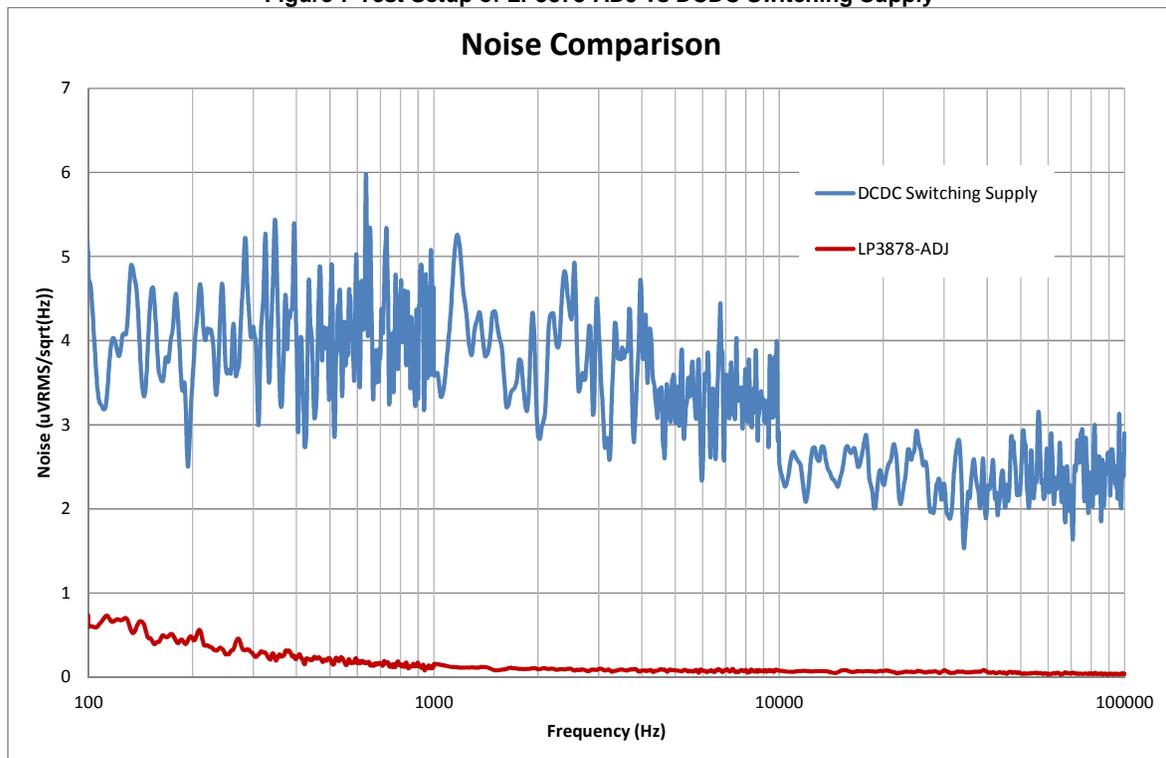


Figure 8 Output Noise Comparison between LP3878-ADJ and DCDC Switching Supply

Figure 8 shows the output noise of DCDC switching supply is higher than that of LP3878-ADJ. When using DCDC switching supply and LP3878-ADJ to power LMK03806, the clock phase noise is shown in Figure 9.

It can be seen that noise of DCDC switching supply is translated at the clock output and degrades the clock phase noise response.

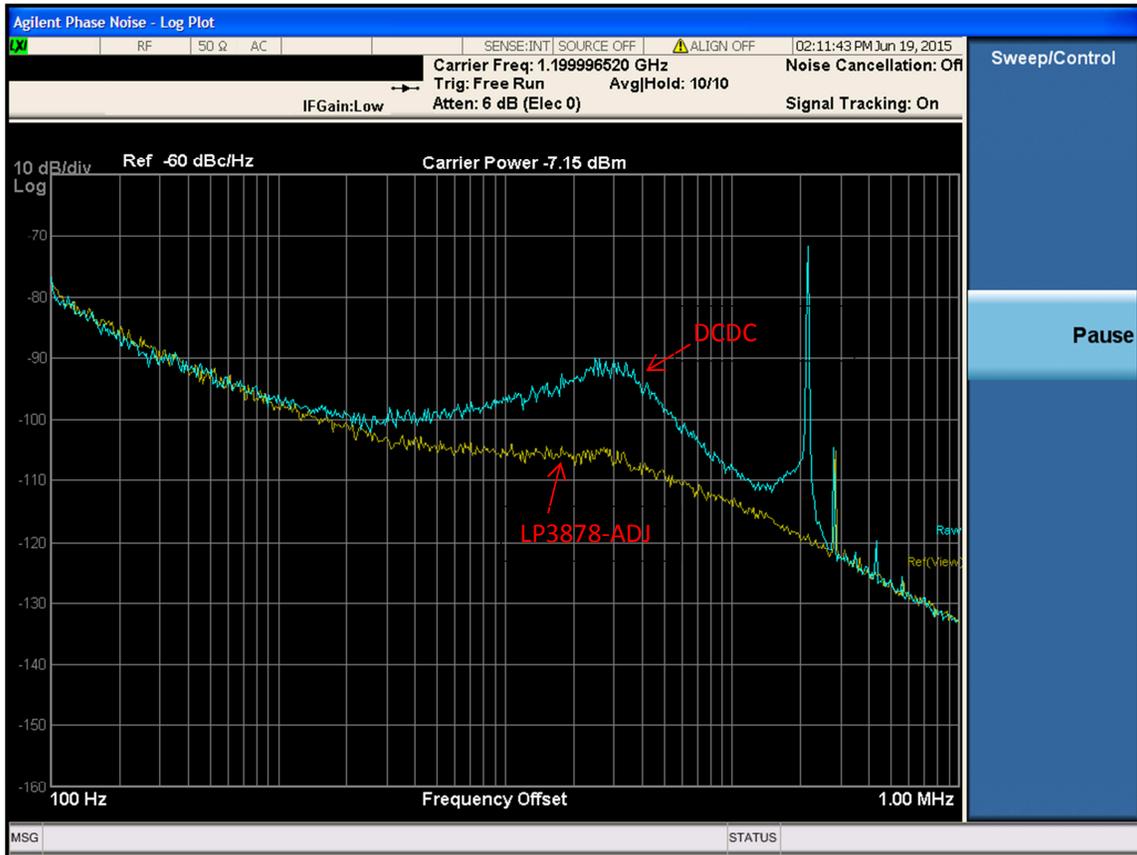


Figure 9 Clock Phase Noise Supplied by LP3878-ADJ and DCDC Switching Supply

5.2 LP3878-ADJ vs Lab Linear Power

This setup used LP3878-ADJ and lab linear power, and measures the clock phase noise.

Table 3 Test Equipment

Equipment	device number	Function
Lab linear supply	Agilent E3631A	Constant voltage supply
Clock generation	LMK03806BEVAL	Clock generation
Signal source analyzer	N9020A	Used to measure phase noise

Figure 10 represents the test setup.

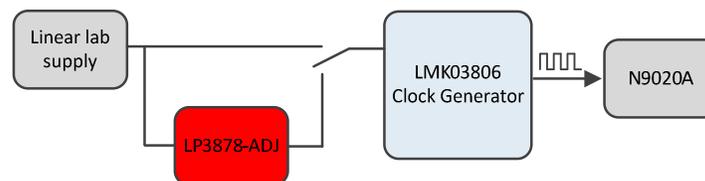


Figure 10 Test Setup of LP3878-ADJ vs DCDC Switching Supply

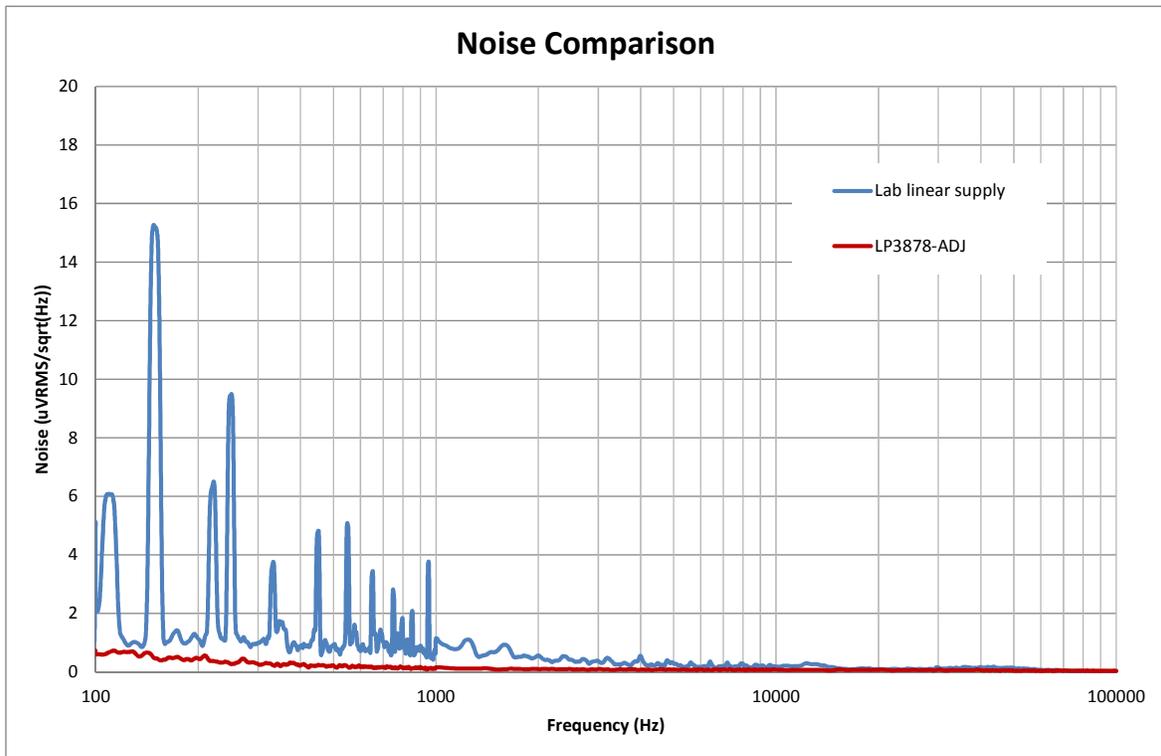


Figure 11 Output Noise Comparison between LP3878-ADJ and Noisy LDO

Figure 11 shows the output noise of lab linear power at lower frequency is much higher than that of LP3878-ADJ, at higher frequency, the output noise of lab linear power and LP3878-ADJ are almost the same.

When using lab linear power and LP3878-ADJ to power LMK03806, the clock phase noise is shown in Figure 12. It can be seen the phase noise response has difference at lower offset frequency and almost the same at higher offset frequency.

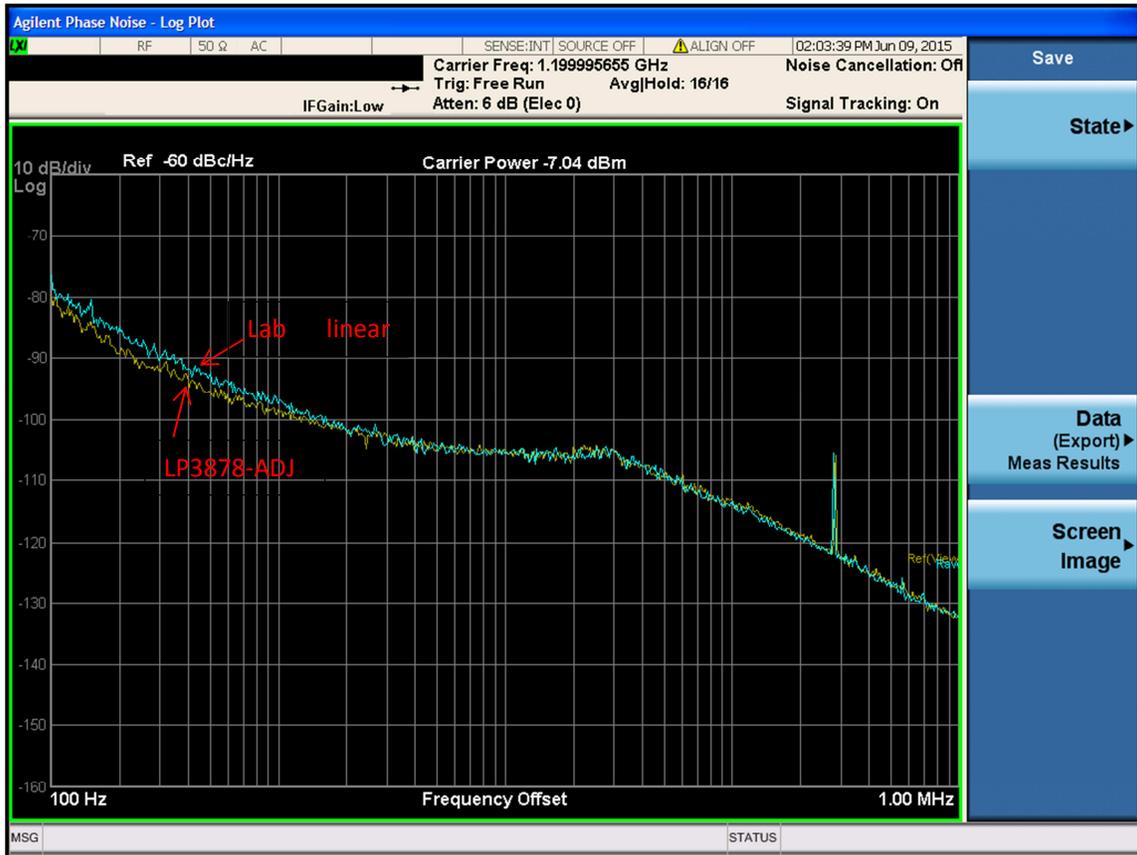


Figure 12 Clock Phase Noise Supplied by LP3878-ADJ and Lab Linear Power

5.3 Noise Impact on Different Supply Rail of Clock Generation

The clock generation of LMK03806 has many supply rails, these rails can be divided into two groups of V_{CC_Core} and V_{CC_CLK} . In order to check which rail with noise supply will affect clock phase noise, below setup is made. In this setup, each rail is supplied by noisy power while the remaining one continues to use LP3878-ADJ.

Figure 13 represents the test setup.

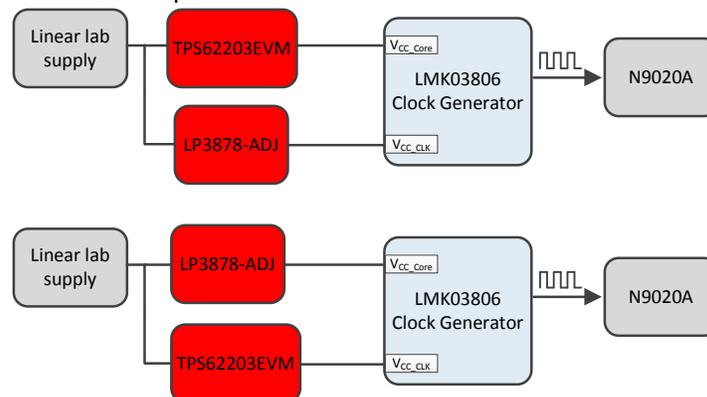


Figure 13 Test Setup of Powering Different Supply Rail

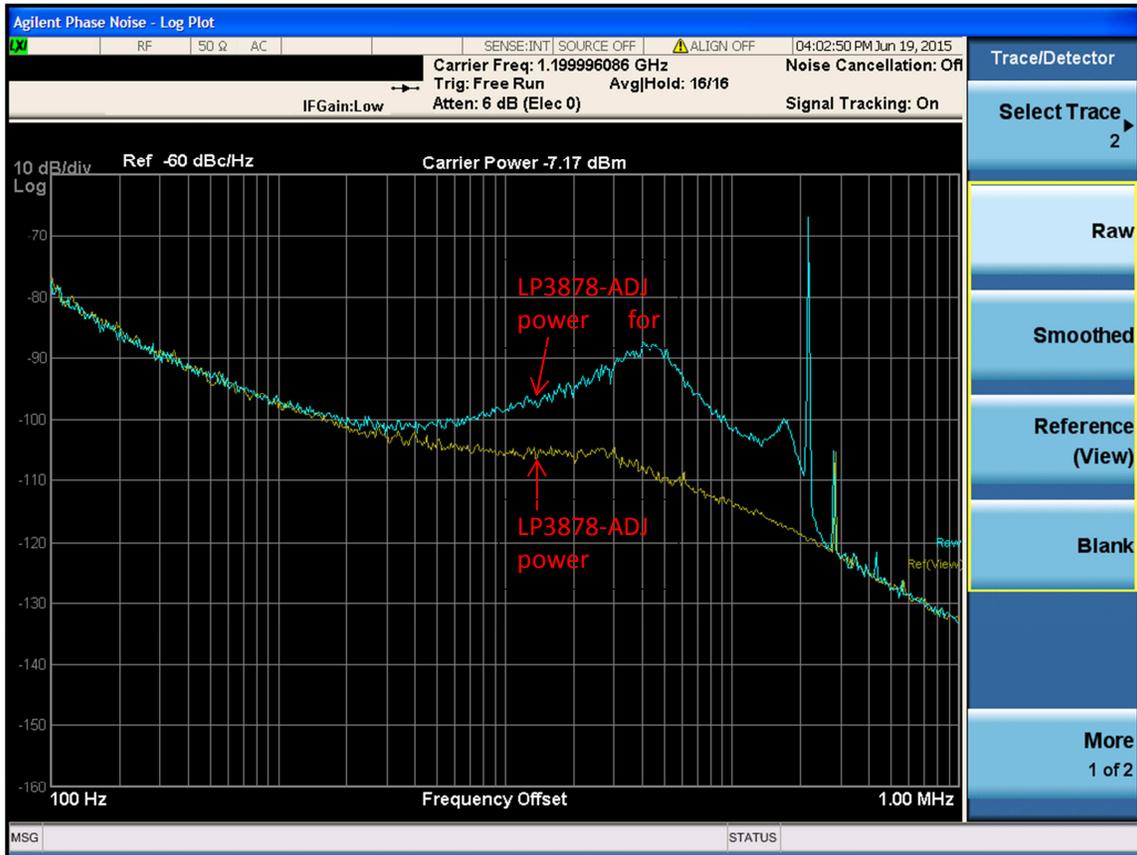


Figure 14 Clock Phase Noise of LP3878-ADJ Power CLK and DCDC Supply Power Core

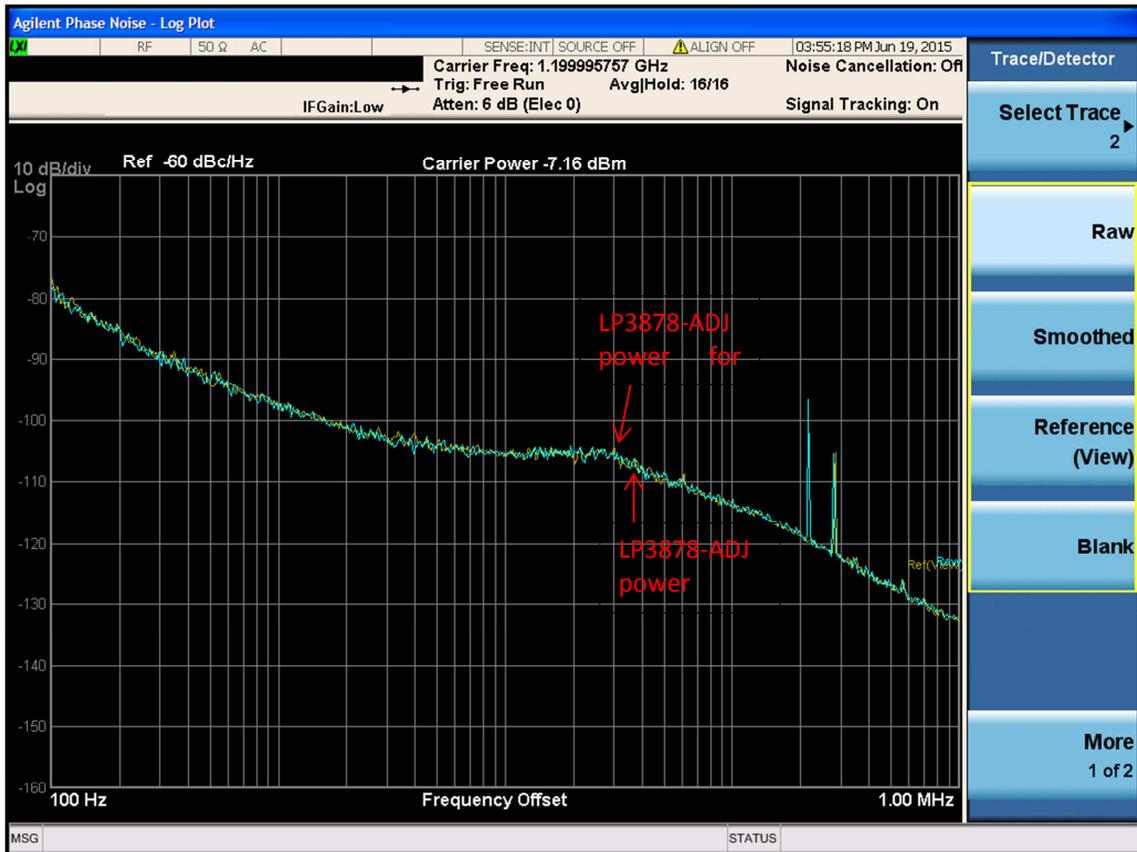


Figure 15 Clock Phase Noise of LP3878-ADJ Power Core and DCDC Supply Power CLK

From Figure 14 and 15, it can be seen that noise on V_{CC_Core} is translated at the clock output and degrades the clock phase noise response. If different rail needs different supplies, it is important to select quiet supply for core rail.

6 Design Files

6.1 Schematics

To download the Schematics for each board, see the design files at <http://www.ti.com/tool/TIDA-00597>

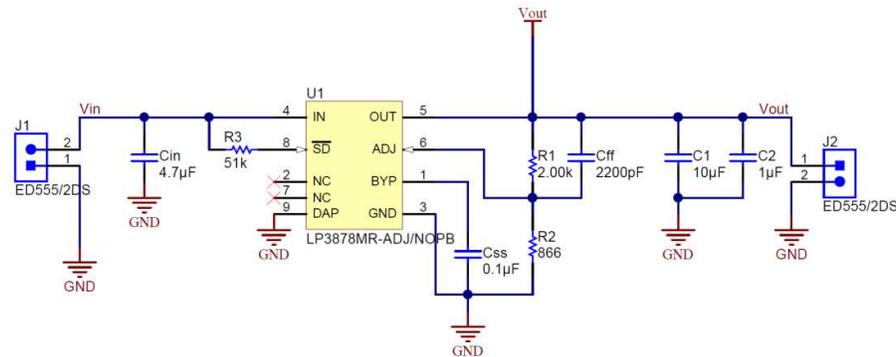


Figure 16 TIDA-00597 Schematic

6.2 PCB Layout Recommendations

6.2.1 Layout Guidelines

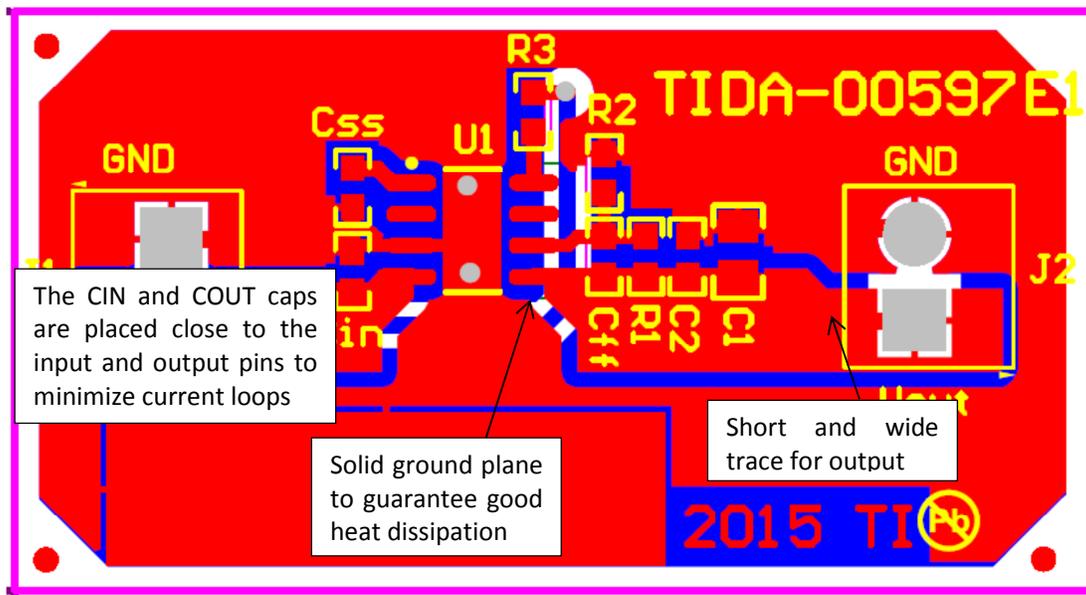


Figure 17 Layout Guidelines

6.2.2 Altium Project

To download the Altium project files for each board, see the design files at.

<http://www.ti.com/tool/TIDA-00597>

- Gerber and NC-drills
- Bill of Materials (BOM)
- Assembly Drawings

7 Terminology

TI Glossary: [SLYZ022](#) This glossary lists and explains terms, acronyms, and definitions.

8 About the Author

Hank Cao

Is a System Engineer at Texas Instruments on the mobile power devices RF power group at Texas Instruments. Hank earned his Masters of Power Electronics from Nanjing University of Aeronautics and Astronautics.

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers ("Buyers") who are developing systems that incorporate TI semiconductor products (also referred to herein as "components"). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer's systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER'S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer's safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have **not** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.