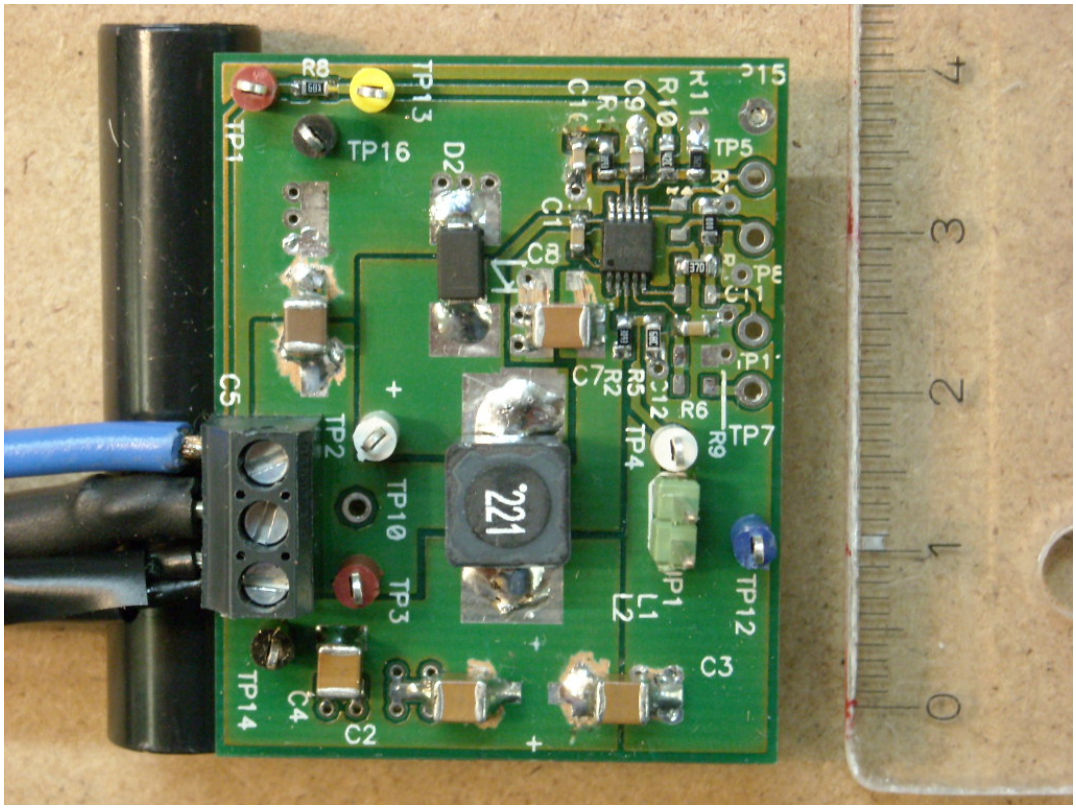
PMP10210RevB Test Results

Topology: inverting BuckBoost, built on buck PCB PMP2763 RevA
Device: TPS54060**A**

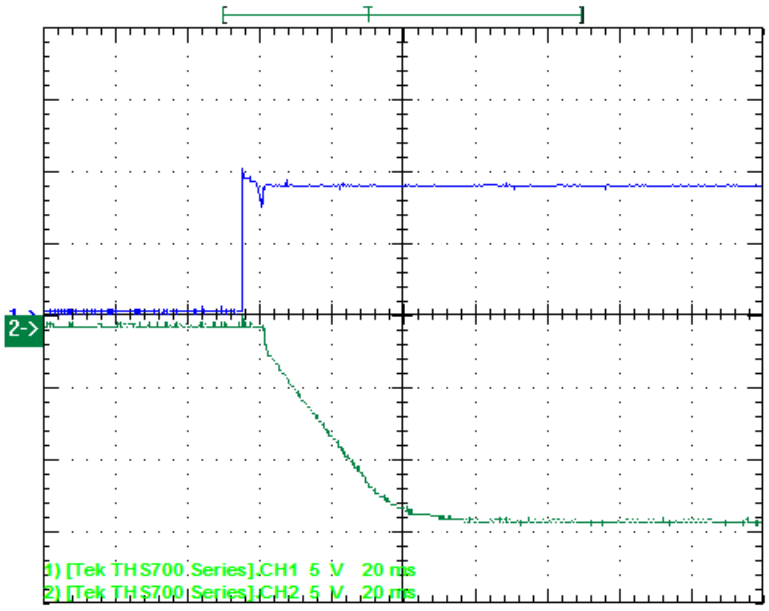
Unless otherwise mentioned, the measurements were done with 150mA output current

Static measurements:
ON @ 8.5V OK
Fsw 485kHz OK



1 Startup

The startup waveform is shown in the Figure 1. The input voltage was set at 9V:



Ch1=> input voltage 5V/div

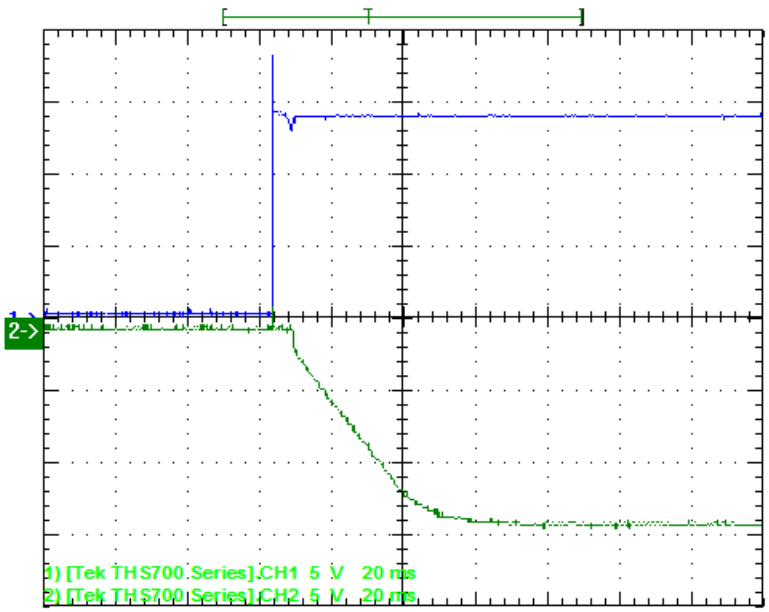
Ch2=> output voltage 5V/div

20ms/div

20MHz bw

Figure 1

The startup waveform is shown in the Figure 2. The input voltage was set at 14V:



Ch1=> input voltage 5V/div

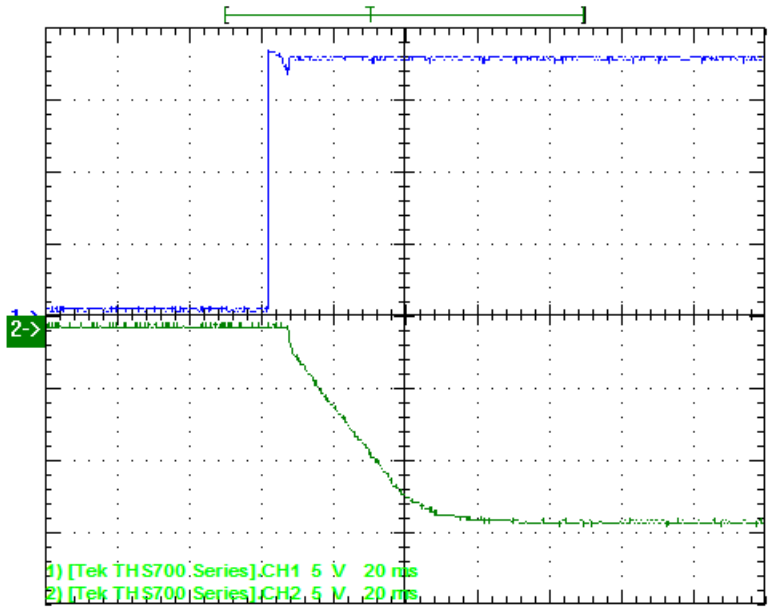
Ch2=> output voltage 5V/div

20ms/div

20MHz bw

Figure 2

The startup waveform is shown in the Figure 3. The input voltage was set at 18V:



Ch1=> input voltage 5V/div

Ch2=> output voltage 5V/div

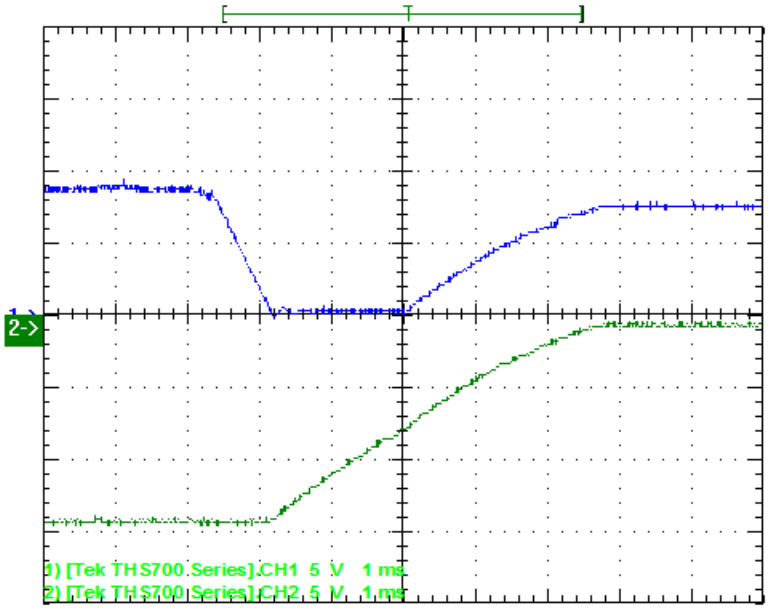
20ms/div

20MHz bw

Figure 3

2 Shutdown

The shutdown waveform is shown in the Figure 4. The input voltage was set at 9V.
The power supply was disconnected.



Ch1=> input voltage 5V/div

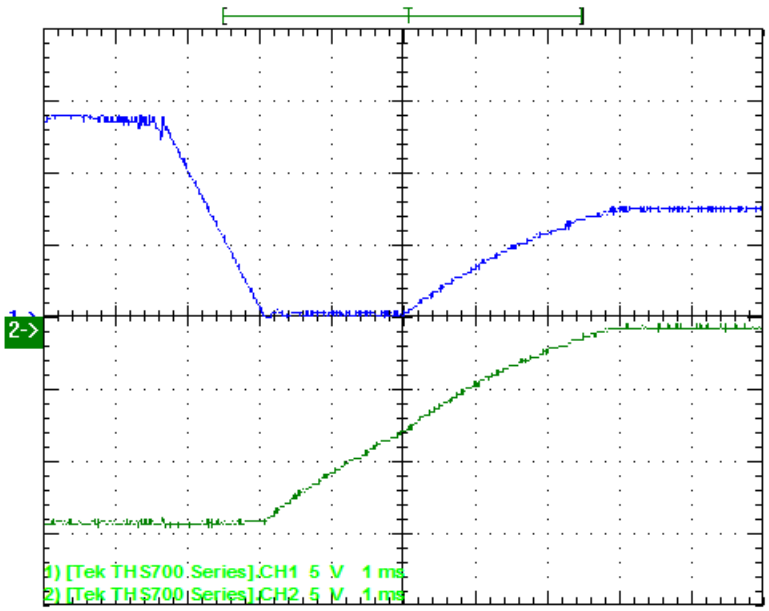
Ch2=> output voltage 5V/div

1ms/div

20MHz bw

Figure 4

The shutdown waveform is shown in the Figure 5. The input voltage was set at 14V.
The power supply was disconnected.



Ch1=> input voltage 5V/div

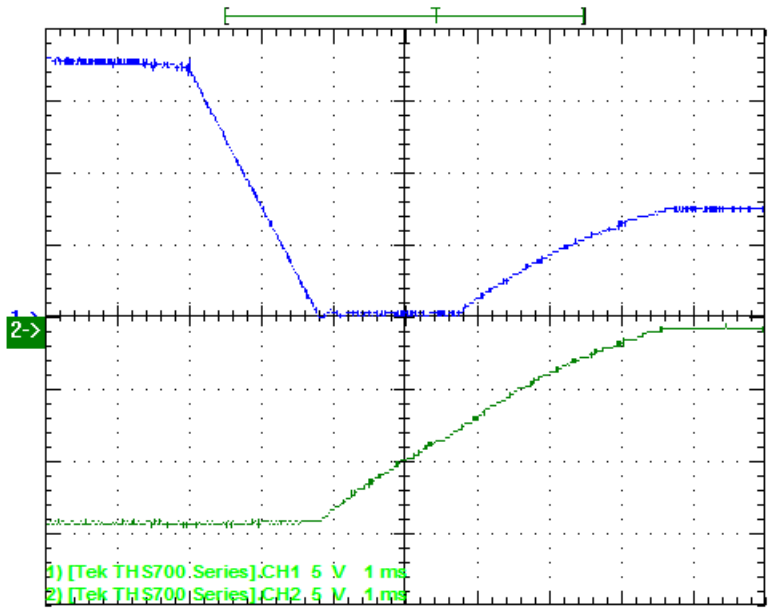
Ch2=> output voltage 2V/div

50µs/div

20MHz bw

Figure 5

The shutdown waveform is shown in the Figure 6. The input voltage was set at 18V.
The power supply was disconnected.



Ch1=> input voltage 5V/div

Ch2=> output voltage 5V/div

1ms/div

20MHz bw

Figure 6

3 Efficiency

The efficiency is shown in the Figure 7 below. The input voltage was set to 9V, 14V and 18V. Using inductor DR125-221-R will improve efficiency 1%..2% (size is 12.5mm x 12.5mm x 6mm)

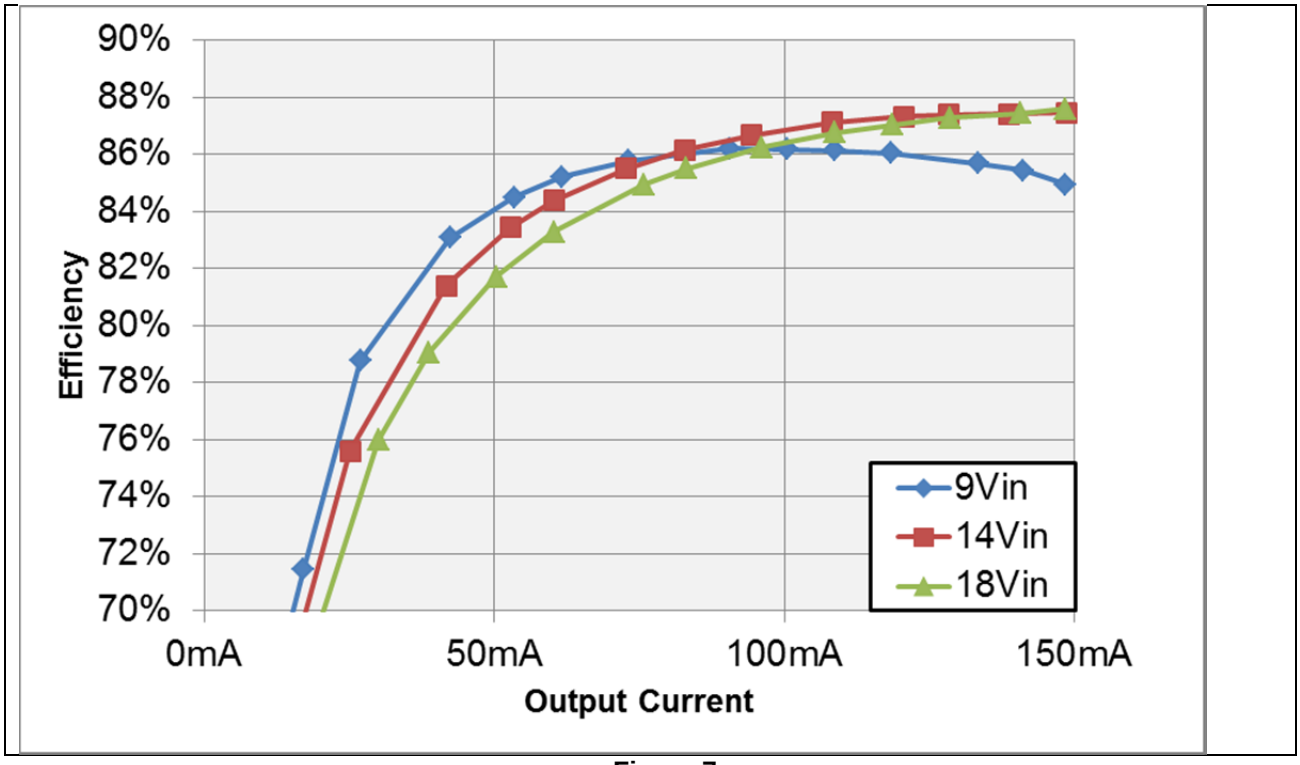


Figure 7

4 Load Regulation

The load regulation of the output is shown in the Figure 8 below.
The input voltage was set to 9V, 14V and 18V.

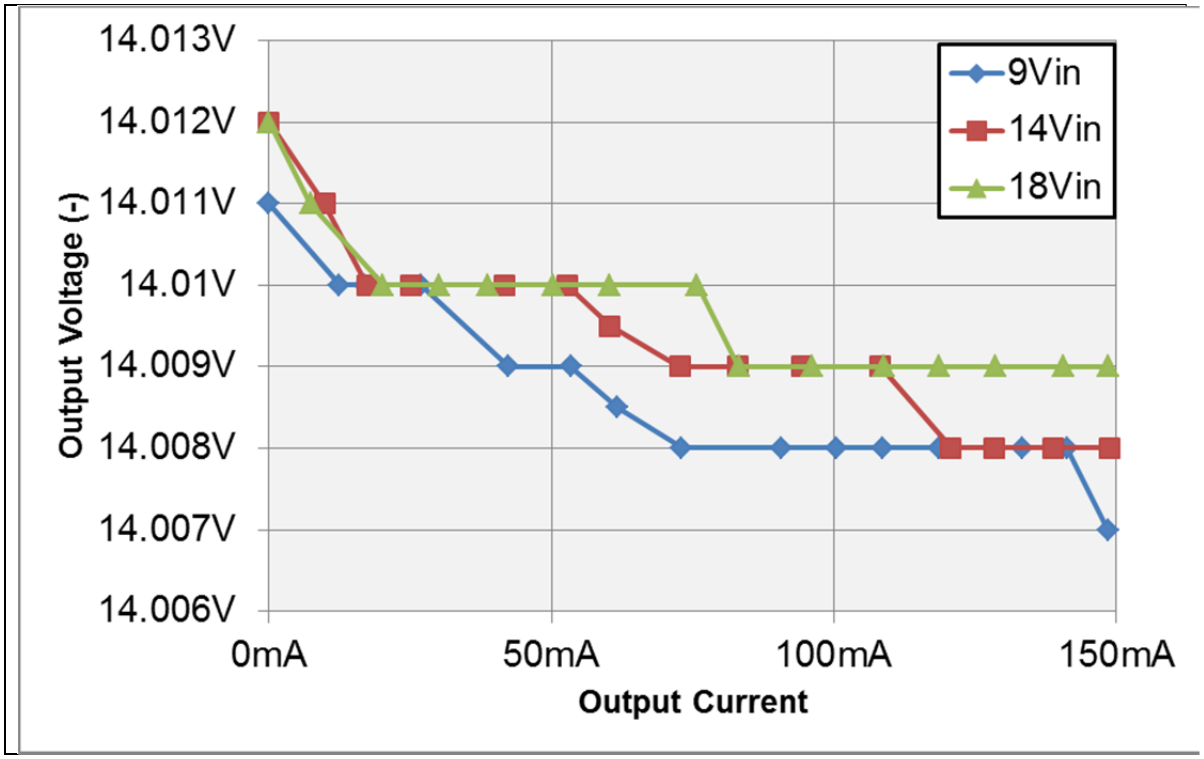


Figure 8

5 Line Regulation

The line regulation is shown in Figure 9.

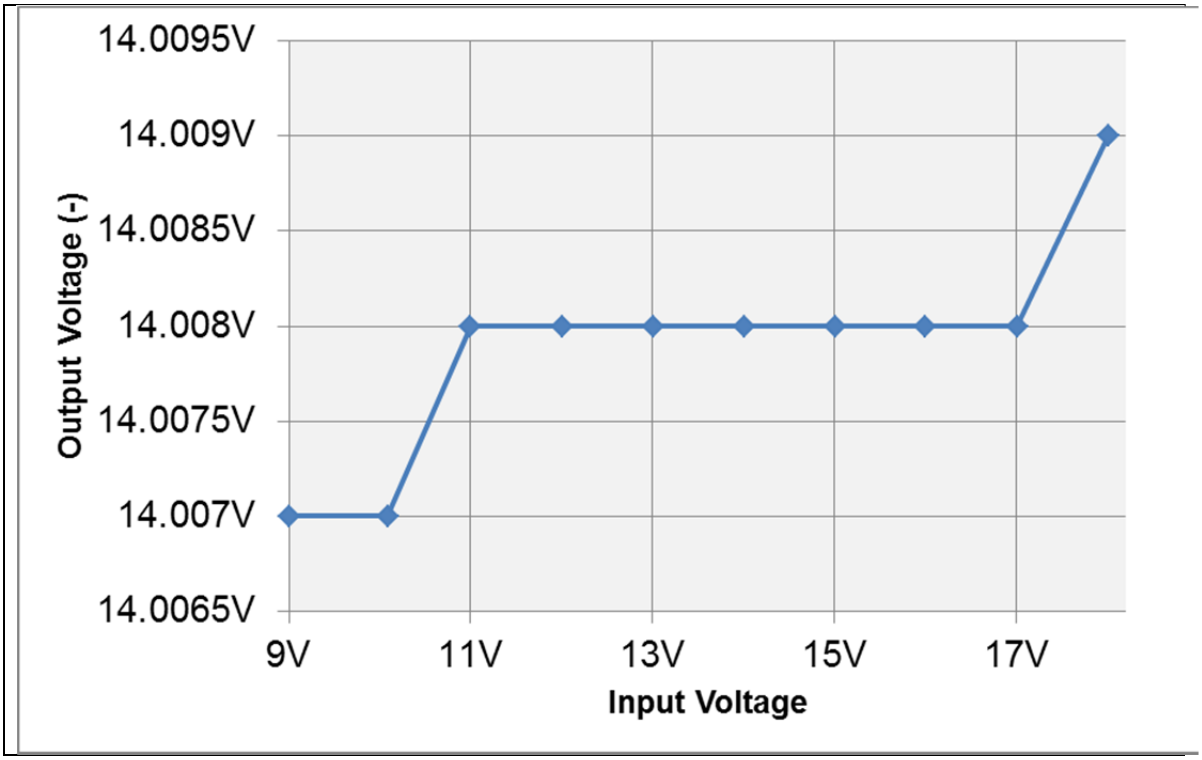


Figure 9

With the same setup the efficiencies are shown in Figure 10.

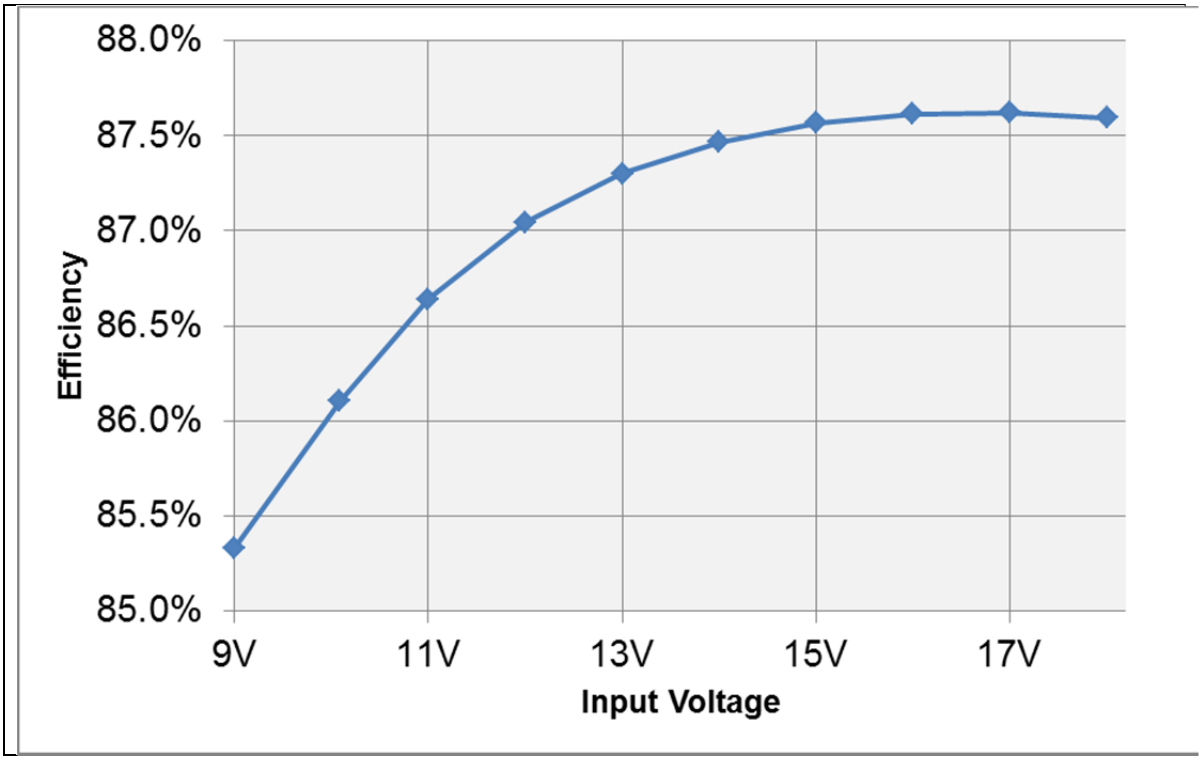
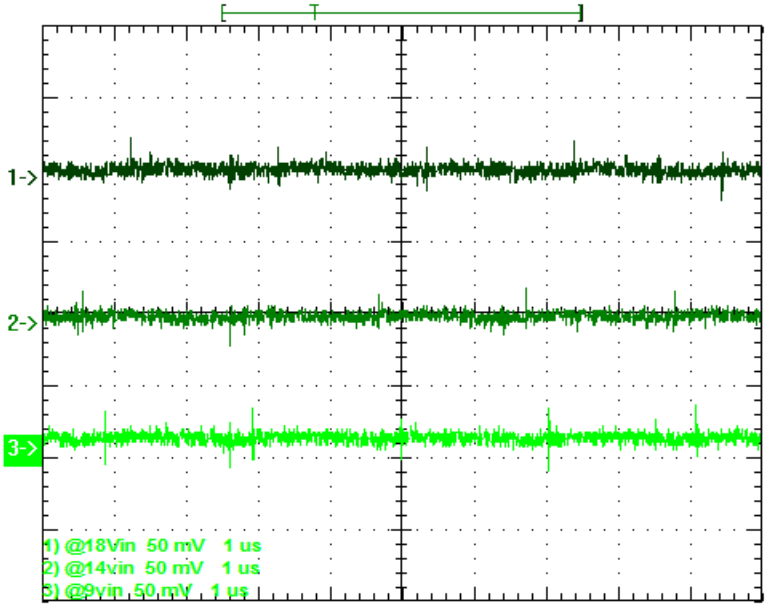


Figure 10

6 Output Ripple Voltage

The output ripple voltage is shown in Figure 11, ripple is below 50mVpp at bandwidth 200MHz



Ch1 => output voltage@18Vin

Ch2 => output voltage@14Vin

Ch3 => output voltage@9Vin

Vin 50mV/div

AC coupled

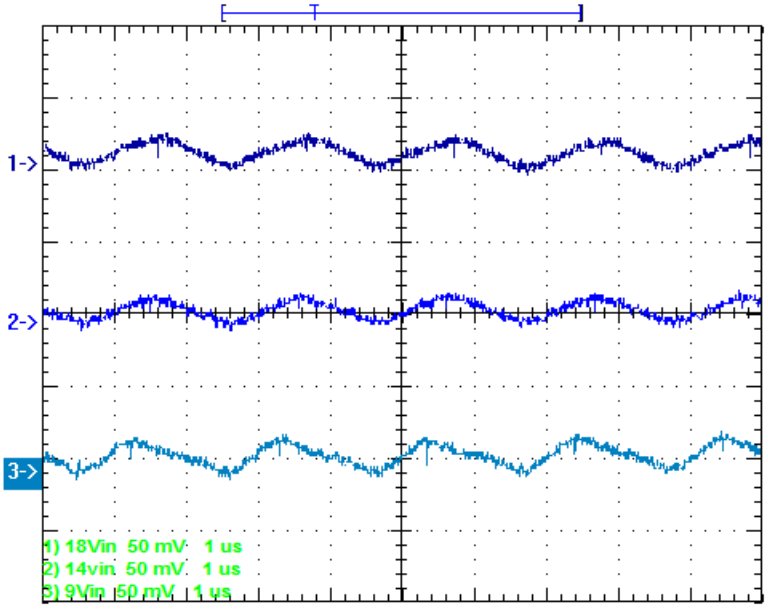
full bw

1µs/div

Figure 11

7 Input Ripple Voltage

The input ripple voltage is shown in Figure 12.



Ch1 => input voltage@18Vin

Ch2 => input voltage@14Vin

Ch3 => input voltage@9Vin

Vin 50mV/div

AC coupled

20MHz bw

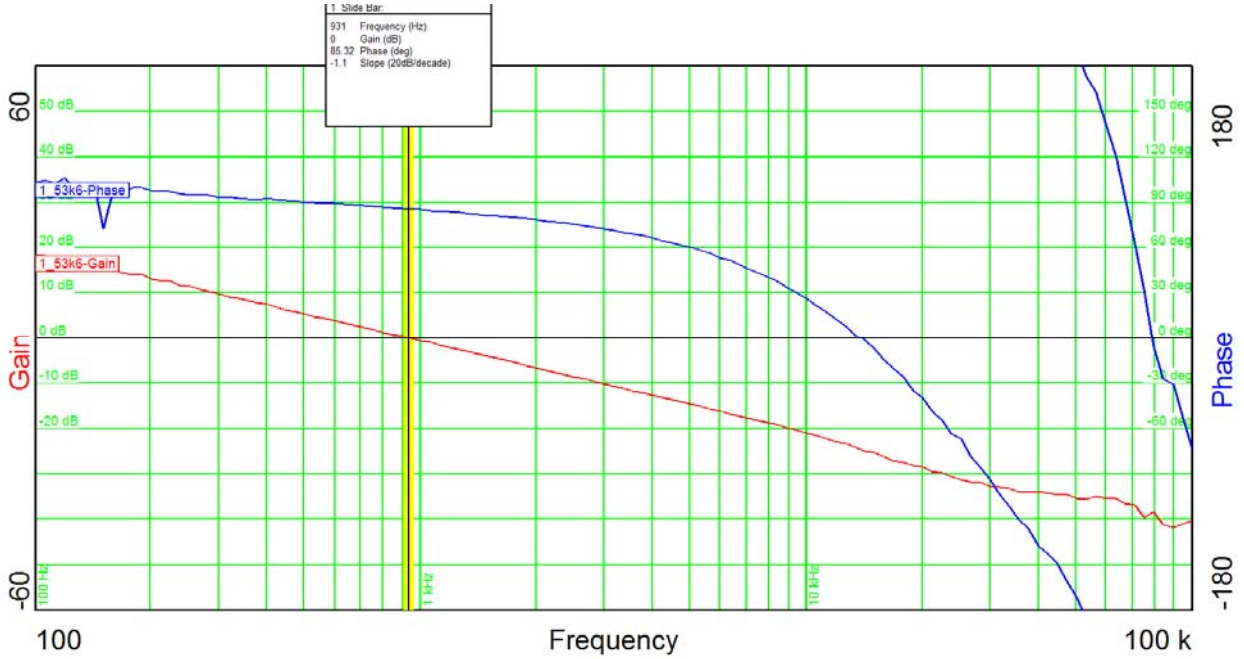
1µs/div

Figure 12

8 Loop Compensation & Transient Response

Revision A, calculated for Fco 1kHz,
compensation ZERO at load pole 30Hz
compensation POLE at 30kHz
R1 53k6 / C10 100nF / C9 100pF

Measured at min. Vin 9V (= max. duty = lowest RHPZ = worst case) and at full load 150mA

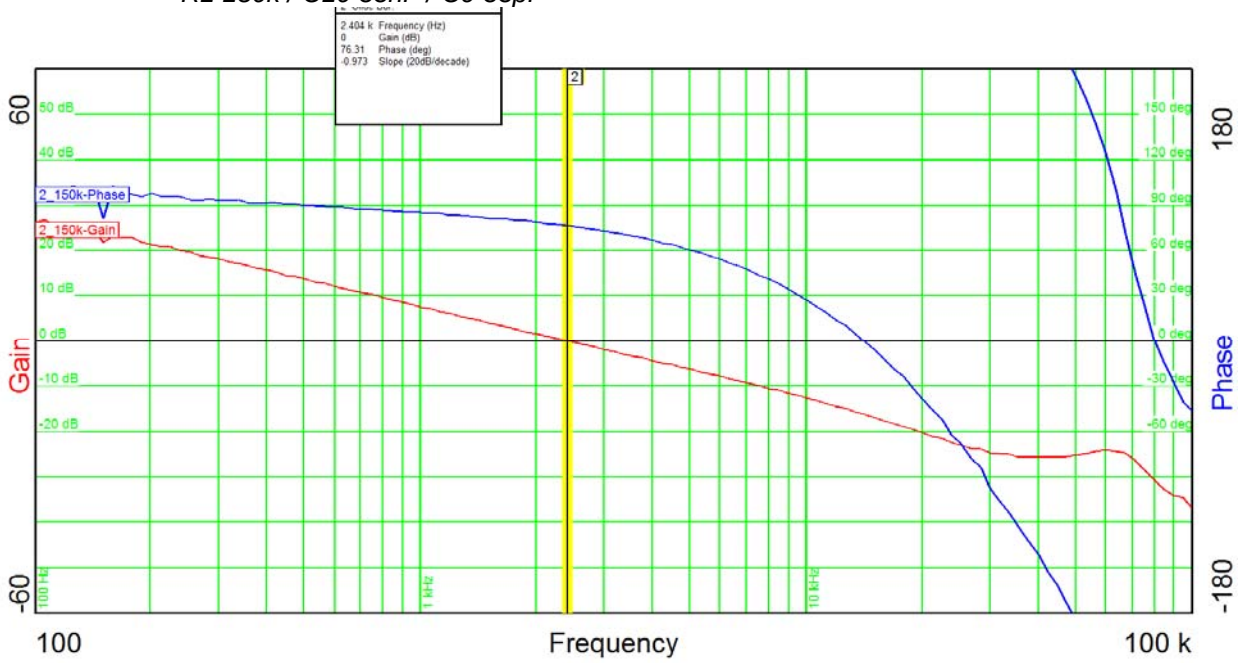


Loop compensation designed ultraconservative for flyback topology; high phase & gain margin.
Results correspond to calculations:

- *crossover frequency 931 Hz*
- *85 degs phase margin*
- *-25 dB gain margin*
- *slope -1.1 (roughly -20dB/decade)*

Next step is to increase gain by nearly x3 by keeping compensation pole and zero;
A shift in gain close to +9dB could be expected, crossover in the area 2 kHz to 3 kHz.

Revision A1, calculated for crossover frequency 2.5kHz,
compensation ZERO at load pole 30Hz
compensation POLE at 30kHz
R1 150k / C10 33nF / C9 33pF



crossover frequency 2.4 kHz, 76 degs phase margin, -16dB gain margin, slope -1, PERFECT Bode Plot is small signal analysis in frequency domain, now large signal analysis in time domain, the TRUE behavior of the power supply:

load transient 10mA <->150mA, **deviation 250mV = 1.8% of Vout -14V**:

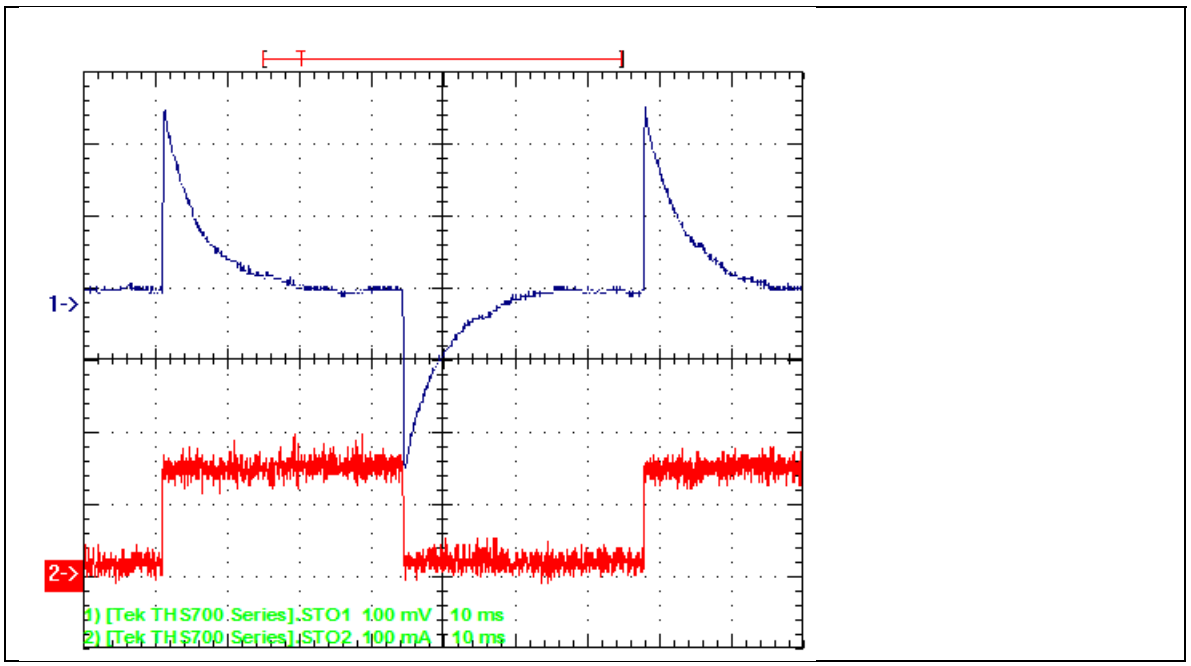
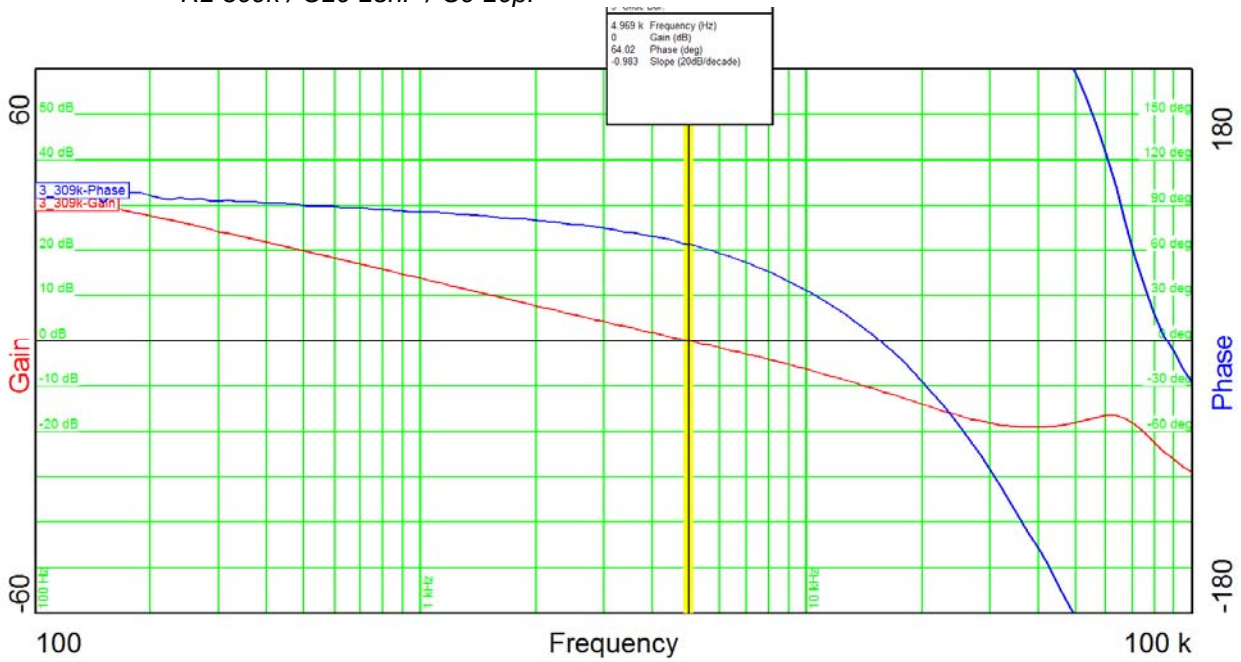


Figure 13 150k

Revision B, calculated for Fco 5kHz, twice the gain, +6dB, “pushing the edge”
compensation ZERO at load pole 30Hz
moved compensation POLE to 50kHz, a decade above crossover
R1 309k / C10 15nF / C9 10pF



crossover frequency 4.97 kHz, 64 phase margin, -12dB gain margin (!), slope -1

load transient 10mA <->150mA, **deviation 160mV = 1.1% of Vout -14V**:

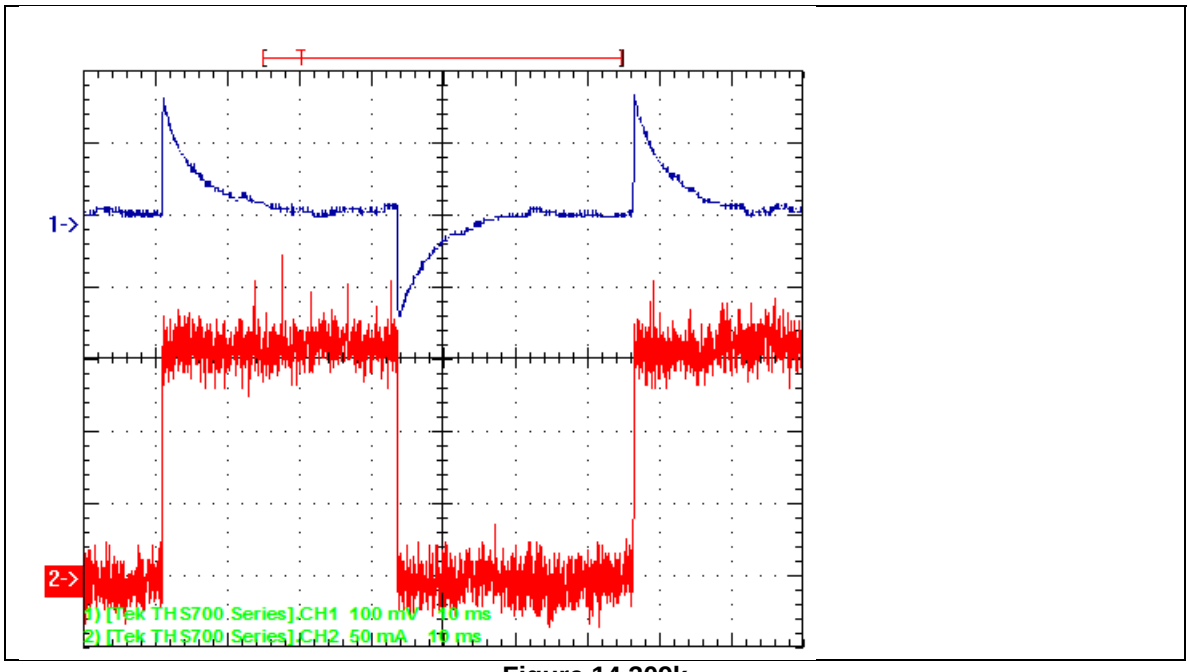


Figure 14 309k

9 Miscellaneous Waveforms

Switch to -VOUT

The waveform of the voltage on switchnode is shown in Figure 15. Input voltage was set to 9V.

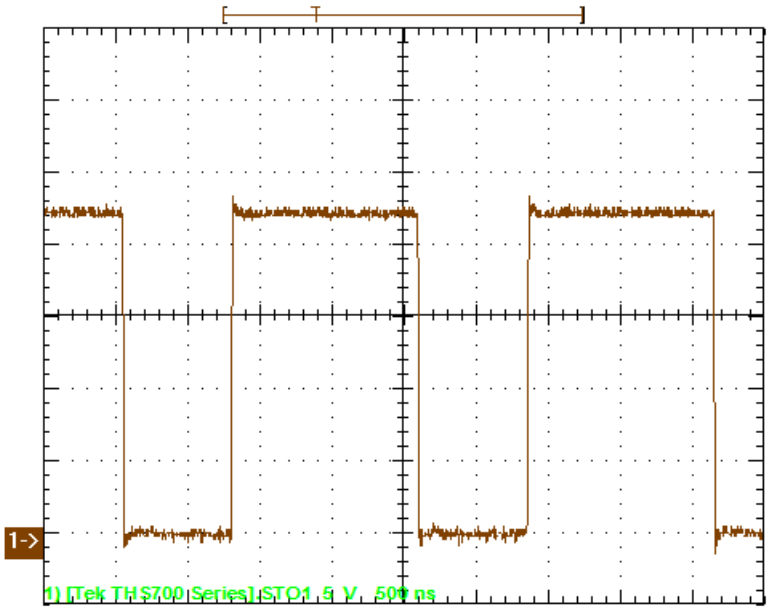
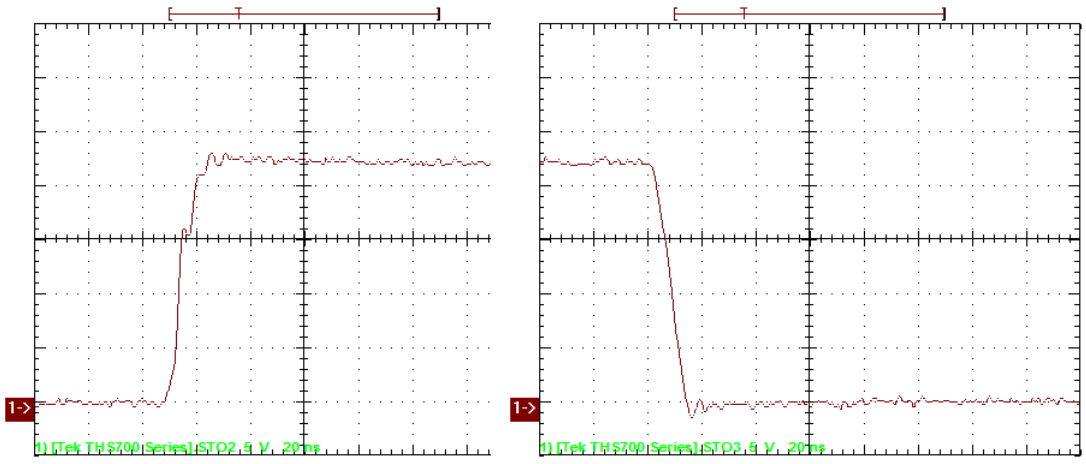
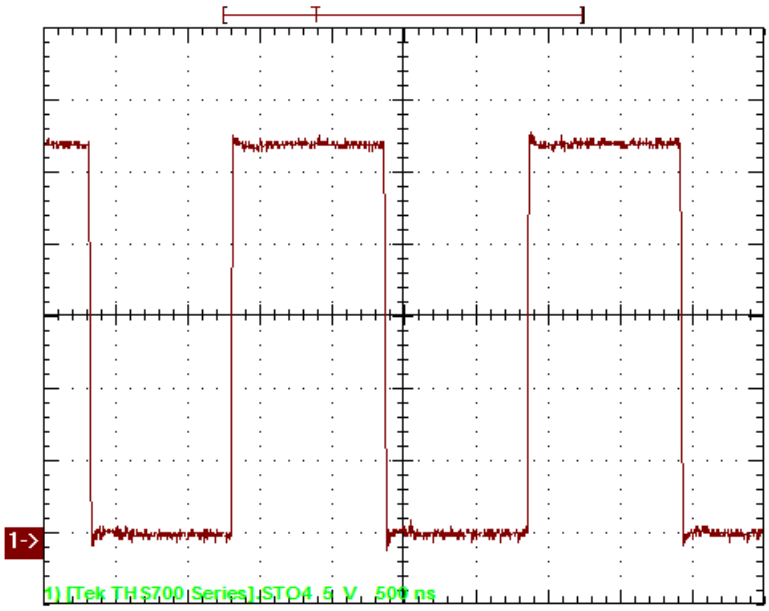
	Ch1 => 5V/div 500ns/div **full bandwidth**
	Ch1 => 5V/div 20ns/div

Figure 15

no ringing, no overshoot

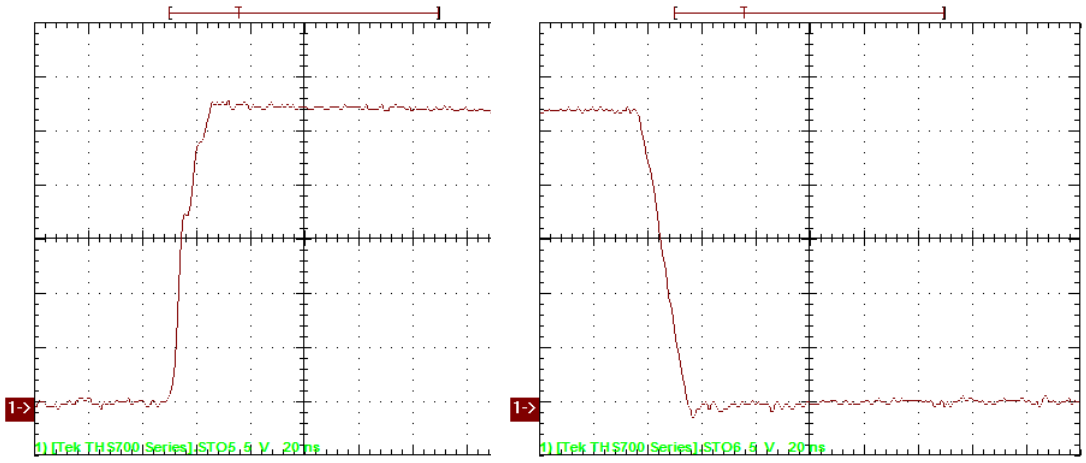
The waveform of the voltage on switchnode is shown in Figure 16. Input voltage was set to 14V.



Ch1 =>
5V/div

500ns/div

full bandwidth

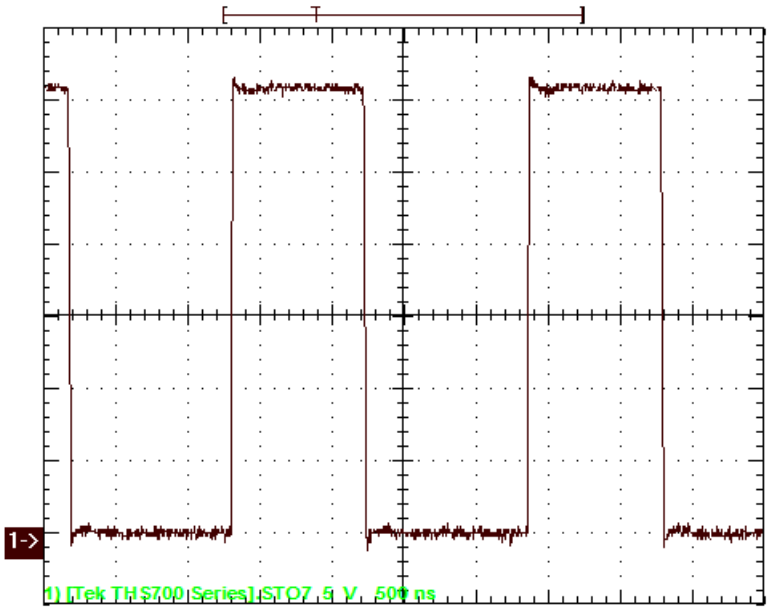


Ch1 =>
5V/div
20ns/div

Figure 16

no ringing, no overshoot

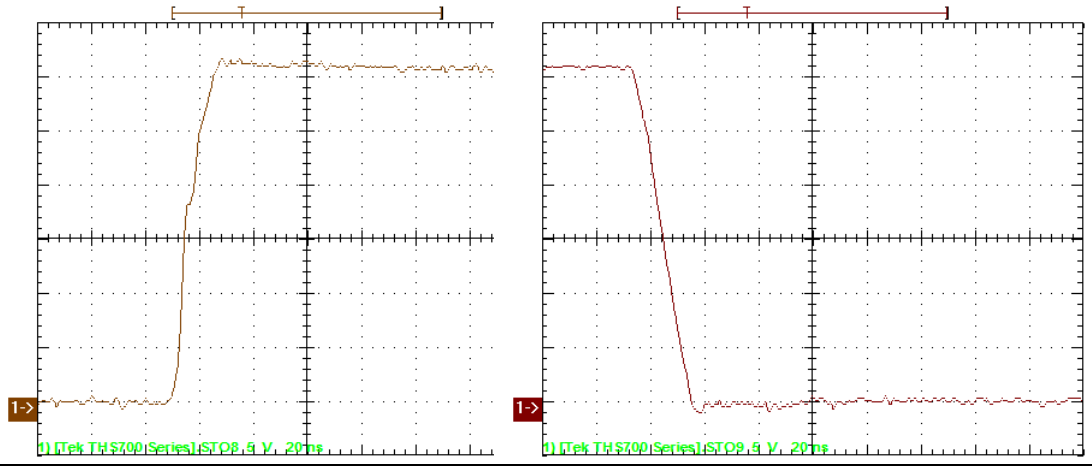
The waveform of the voltage on switchnode is shown in Figure 17. Input voltage was set to 18V.



Ch1 =>
5V/div

500ns/div

full bandwidth



Ch1 =>
5V/div
20ns/div

Figure 17

no ringing, no overshoot

10 Thermal Image

Figure 18 shows the thermal image at 14V input voltage and 200mA output current (=overload condition). The picture has been taken after one hour operation, NO FORCED COOLING, PCB horizontally:

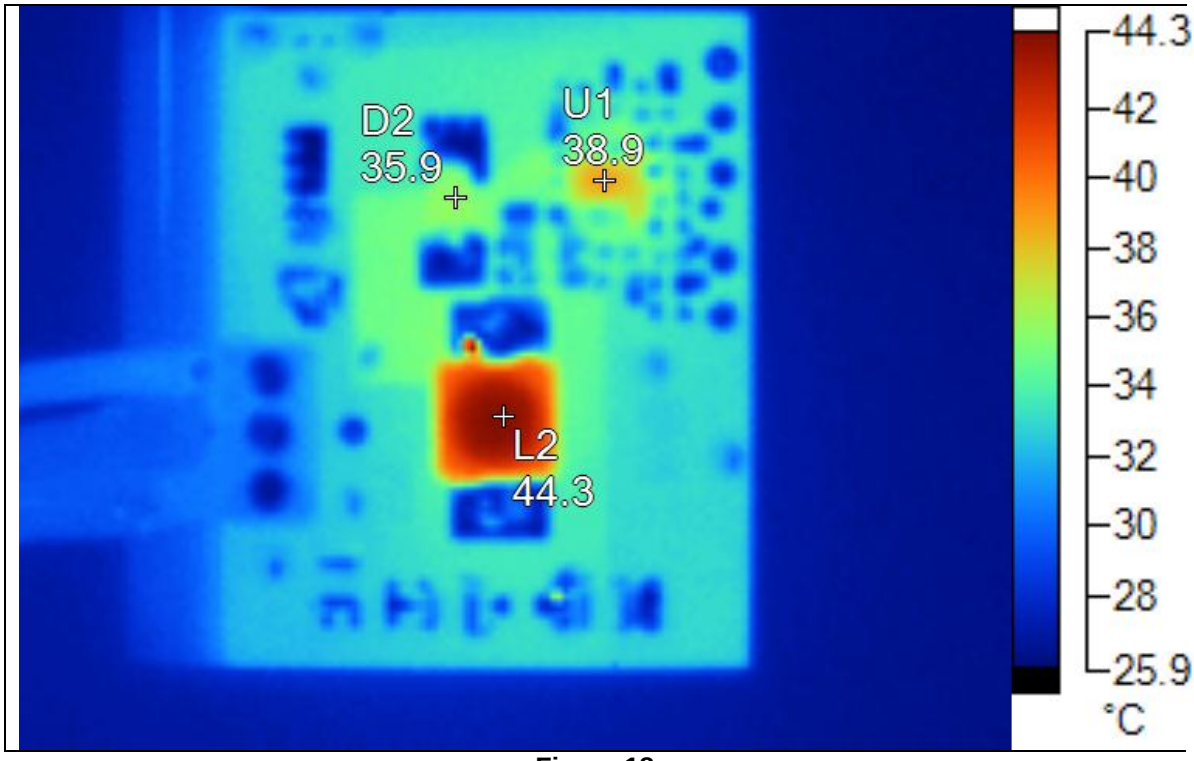


Figure 18

Temperature rise at inductor slightly more than 20K - silicon far below 20K;

Main Image Markers

Name	Temperature
L2	44.3°C
U1	38.9°C
D2	35.9°C

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265