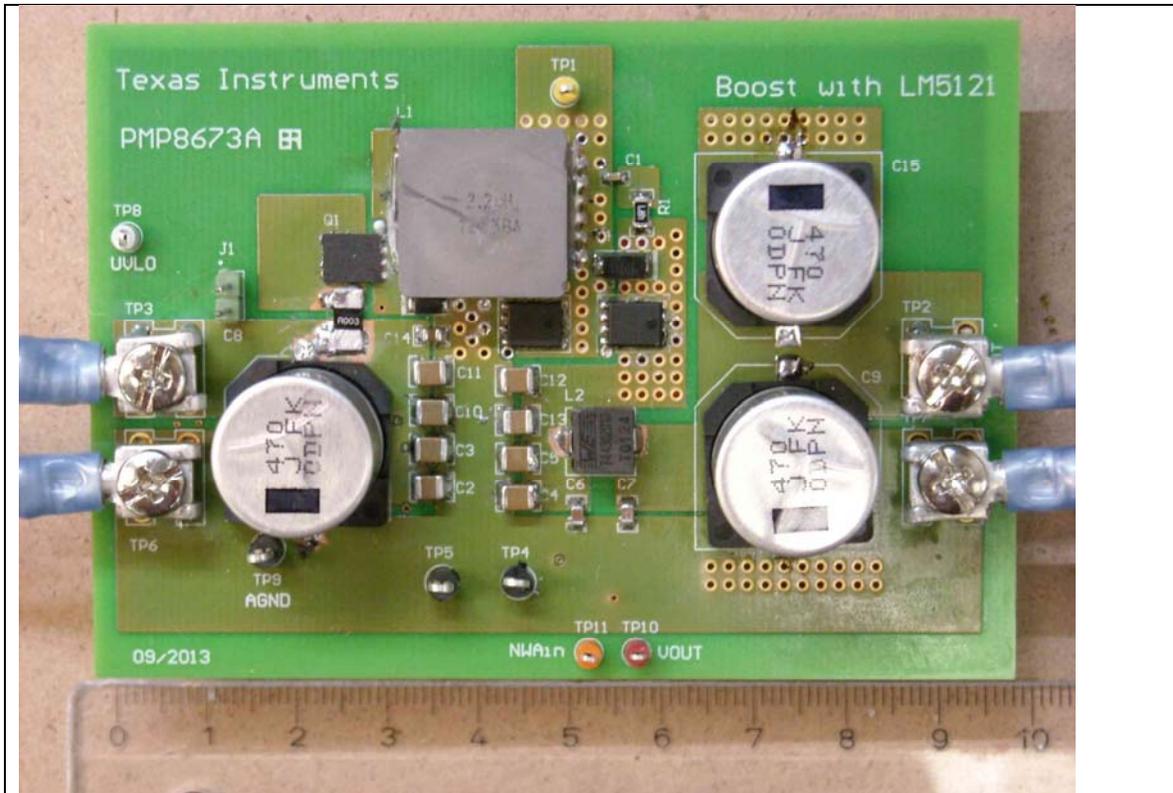


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Topology: Boost
Device: LM5121



The measurements were done with additional airflow at 3Vin unless otherwise mentioned;
The board is operational down to Vin 4.5V w/out bias power;
For operation at Vin 3V..4.5V a bias supply is needed to power Vcc in a range 9V..14V;
For this test purposes the design simply has been powered out of Vout, means:

- **startup needs input voltage >4.5V**
- **maximum input voltage <14V; at higher Vin the controller will be damaged**

Furthermore:

Full load operation at Vin 3V needs a source that is able to drive >25A_{dc}

Limit continuous full load operation <60secs or use forced cooling 1m/s (200lfm)

1 Startup

The startup waveform is shown in the Figure 1. The input voltage was set at 4.5V, with 7A load at the output. Power supply was connected.

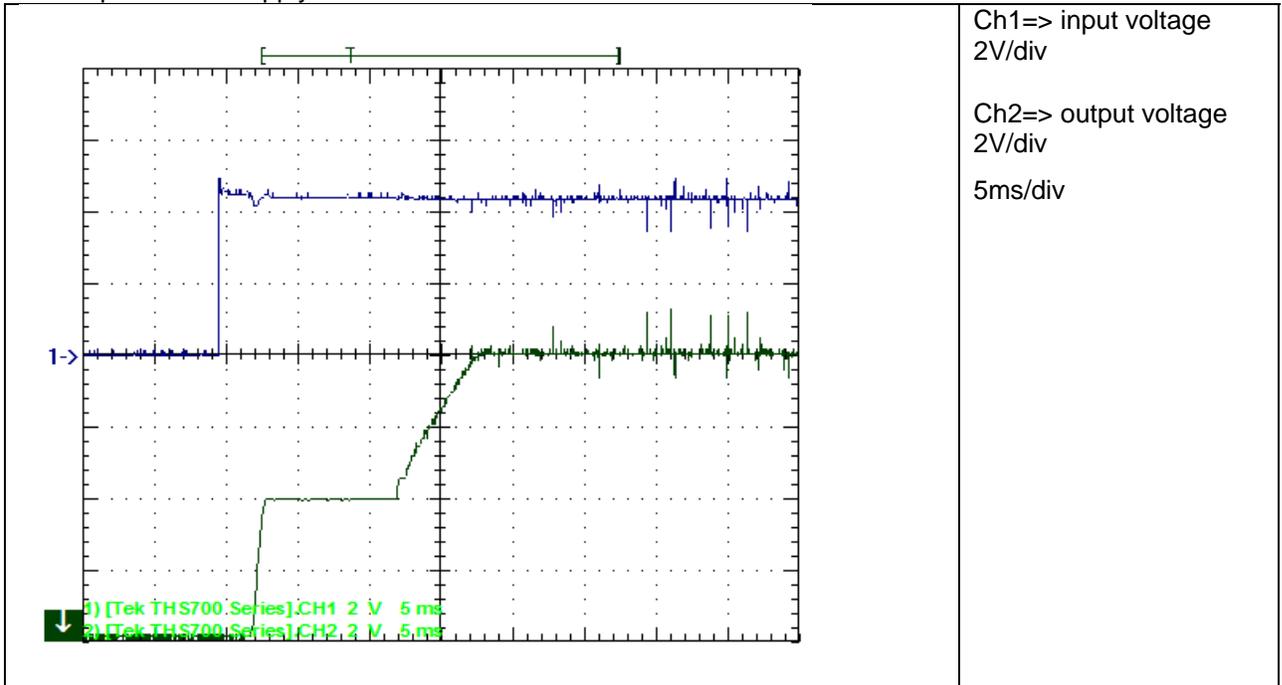


Figure 1

The startup waveform is shown in the Figure 2. The input voltage was set at 4.5V, with 7A load at the output. Power supply output enabled.

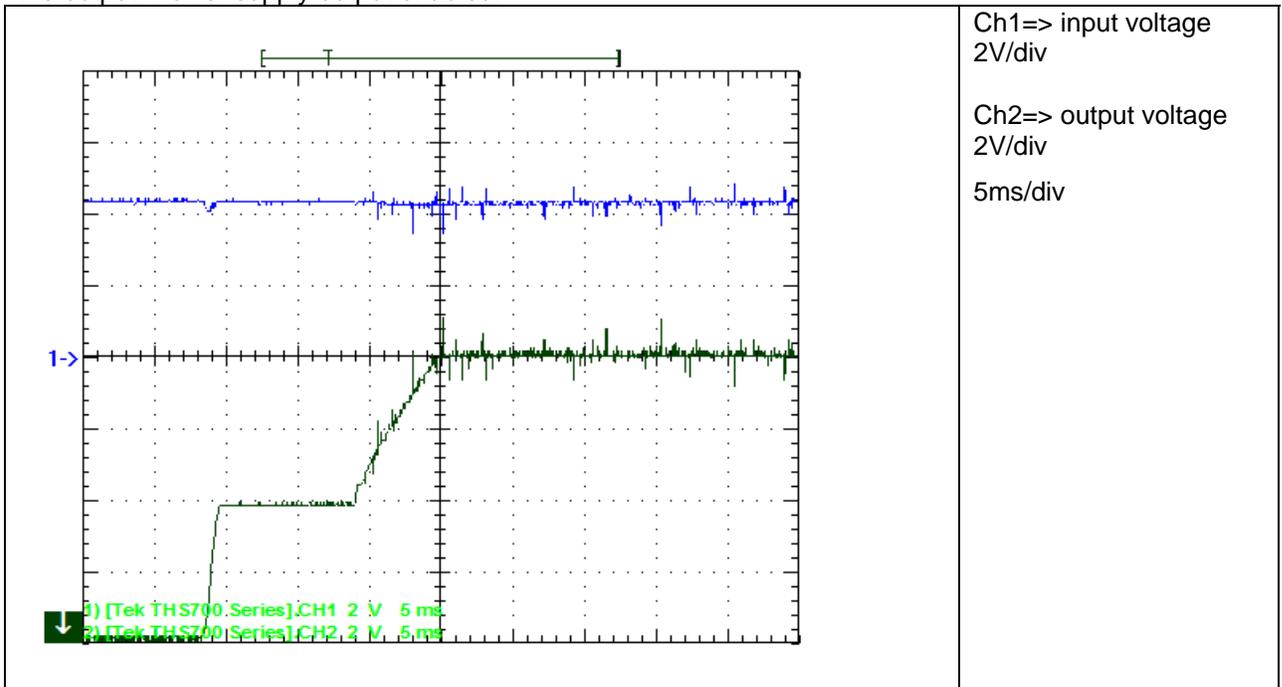


Figure 2

The startup waveform is shown in the Figure 3. The input voltage was set at 6V, with 7A load at the output. Power supply was connected.

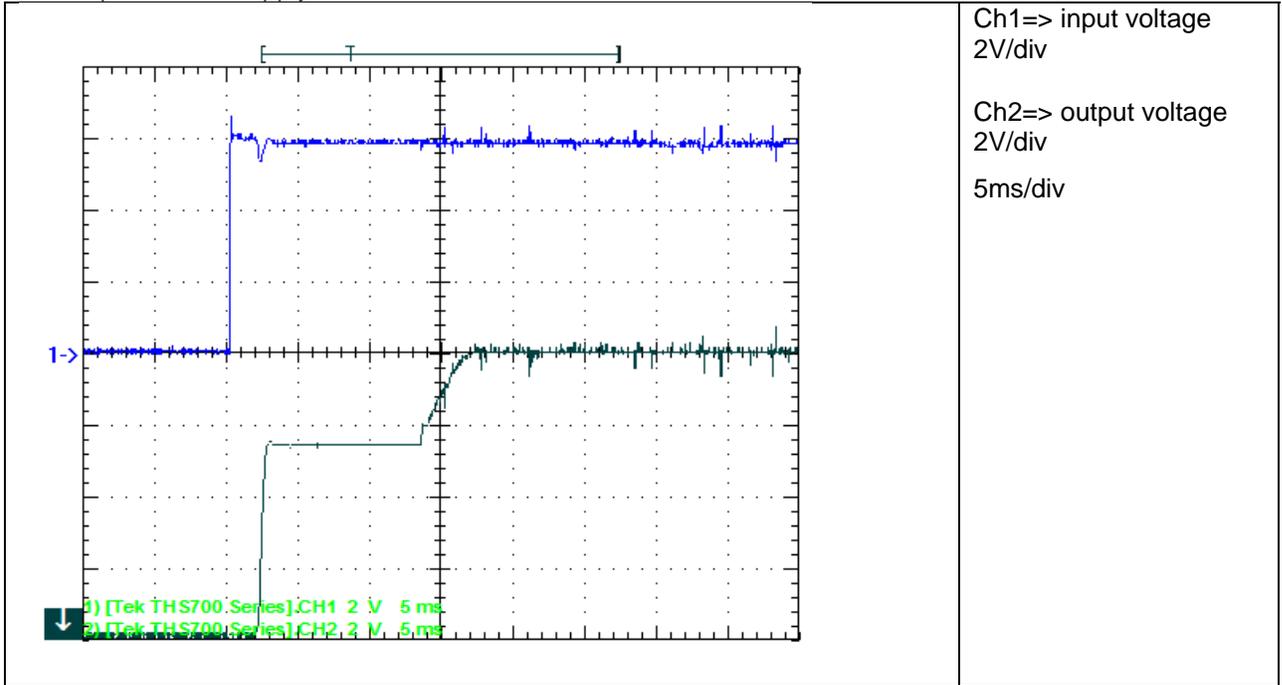


Figure 3

The startup waveform is shown in the Figure 3. The input voltage was set at 6V, with 7A load at the output. Power supply output enabled.

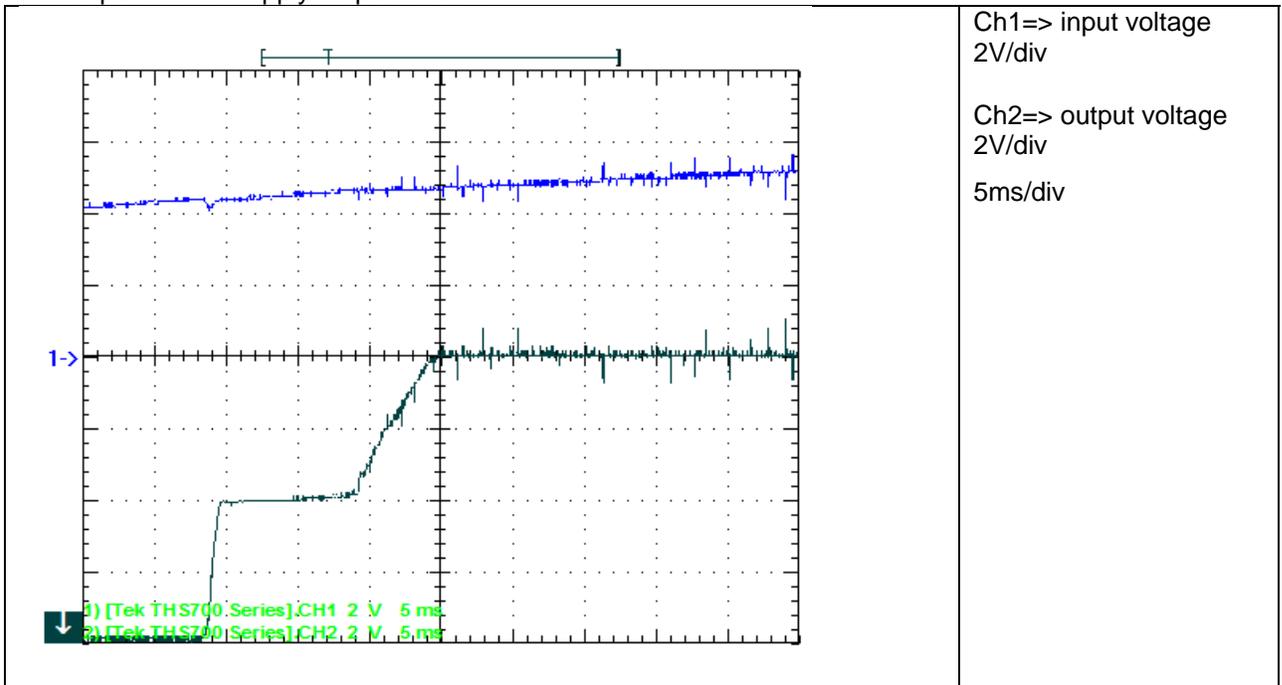


Figure 4

2 Shutdown

The shutdown waveform is shown in the Figure 5. The input voltage was set at 3V, with 7A load on the output. Power supply was disconnected.

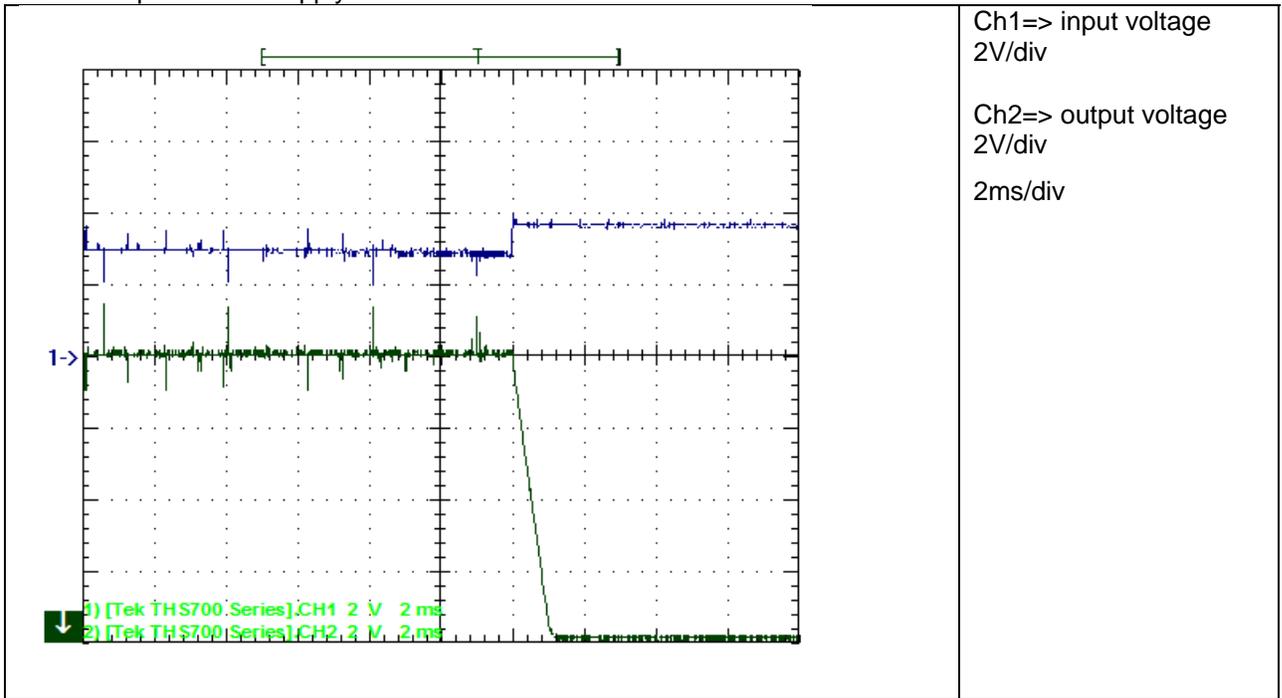


Figure 5

The shutdown waveform is shown in the Figure 6. The input voltage was set at 3V, with 7A load on the output. Power supply output disabled.

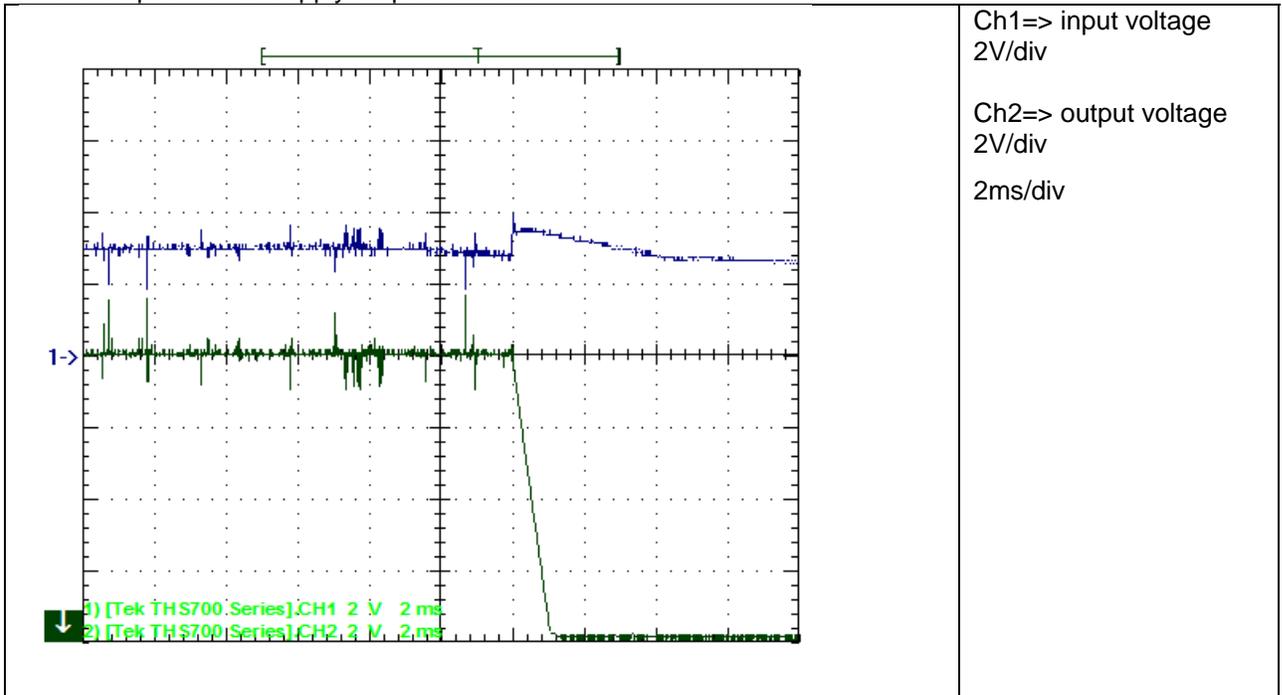


Figure 6

The shutdown waveform is shown in the Figure 7. The input voltage was set at 4.5V, with 7A load on the output. Power supply was disconnected.

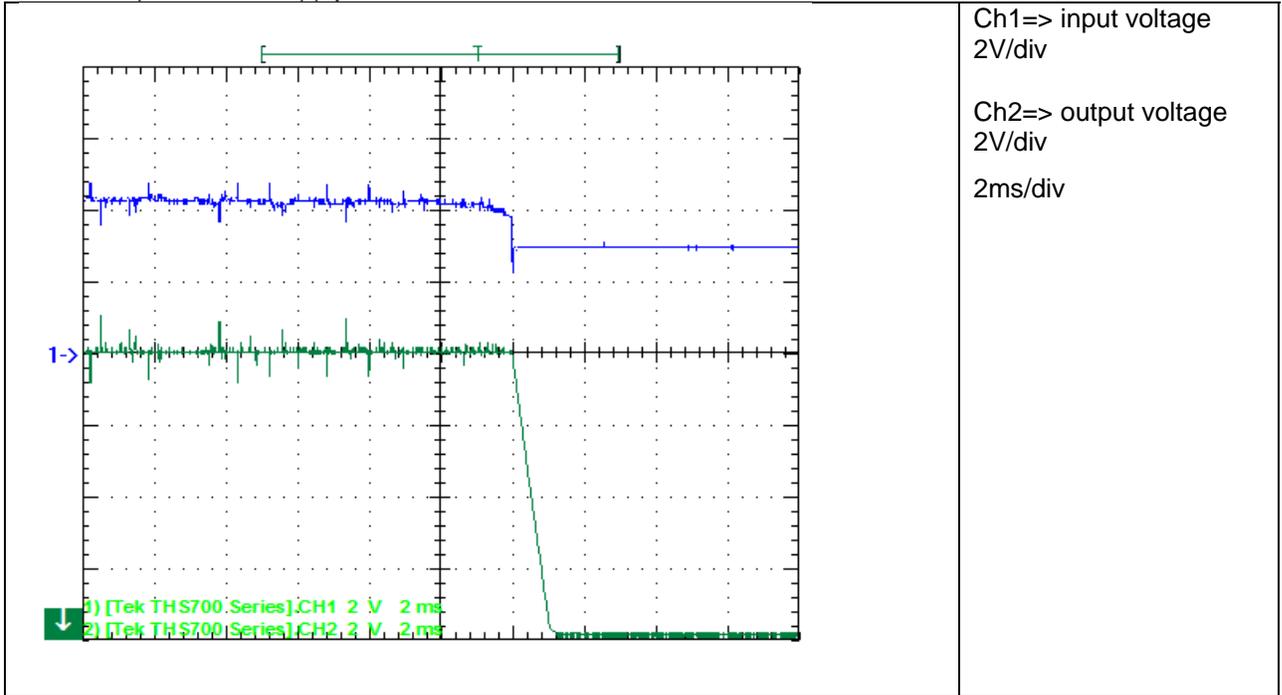


Figure 7

The shutdown waveform is shown in the Figure 8. The input voltage was set at 4.5V, with 7A load on the output. Power supply output disabled.

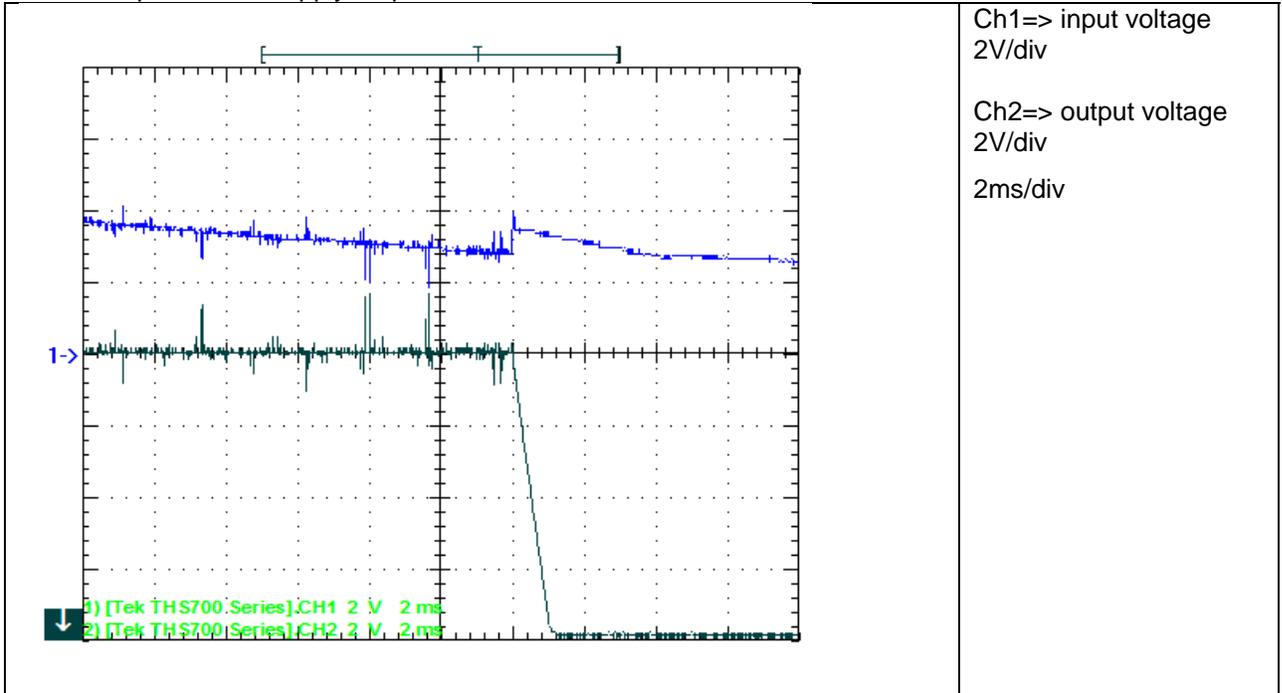


Figure 8

The shutdown waveform is shown in the Figure 9. The input voltage was set at 6V, with 7A load on the output. Power supply was disconnected.

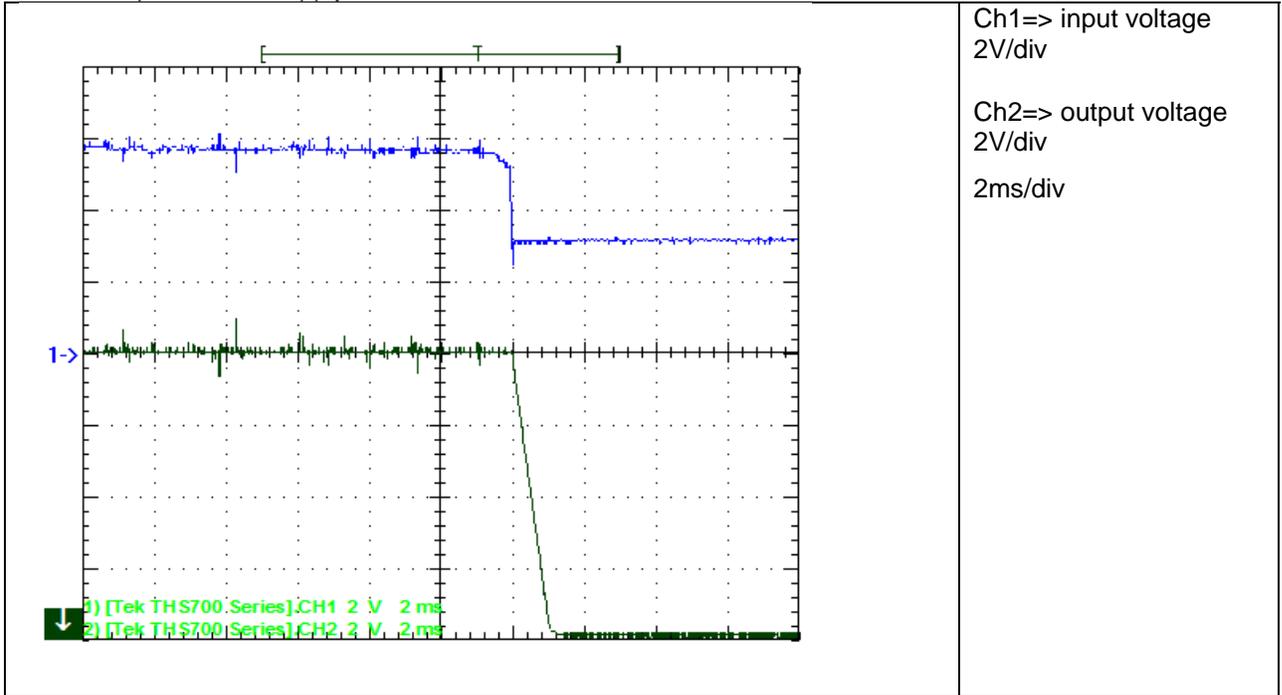


Figure 9

The shutdown waveform is shown in the Figure 10. The input voltage was set at 6V, with 7A load on the output. Power supply output disabled.

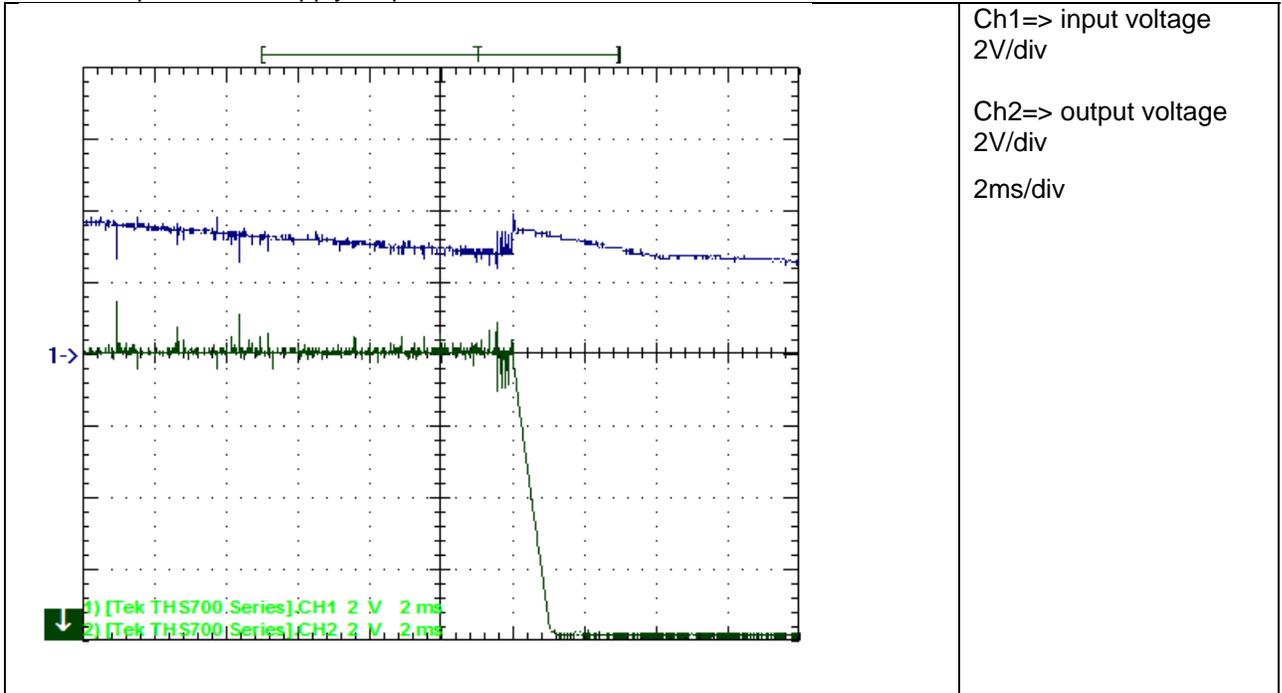


Figure 10

3 Efficiency

The efficiency is shown in the Figure 11 below.

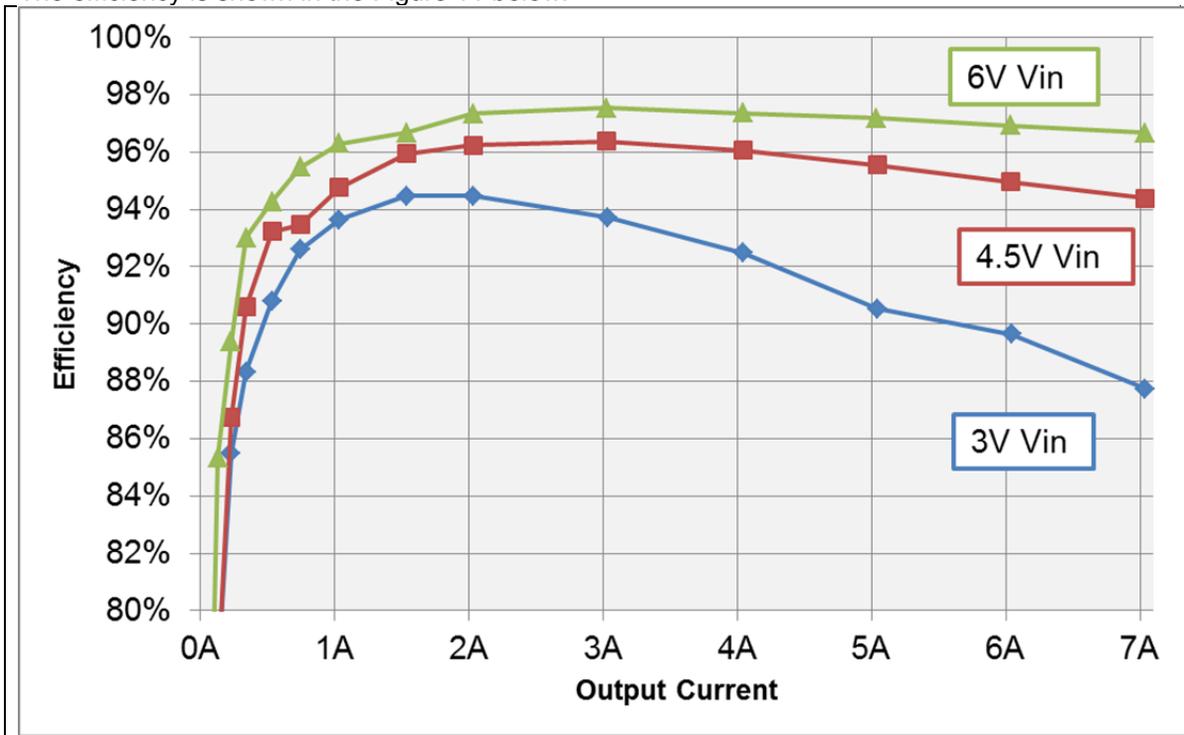


Figure 11

4 Load Regulation

The load regulation of the output is shown in the Figure 12 below.

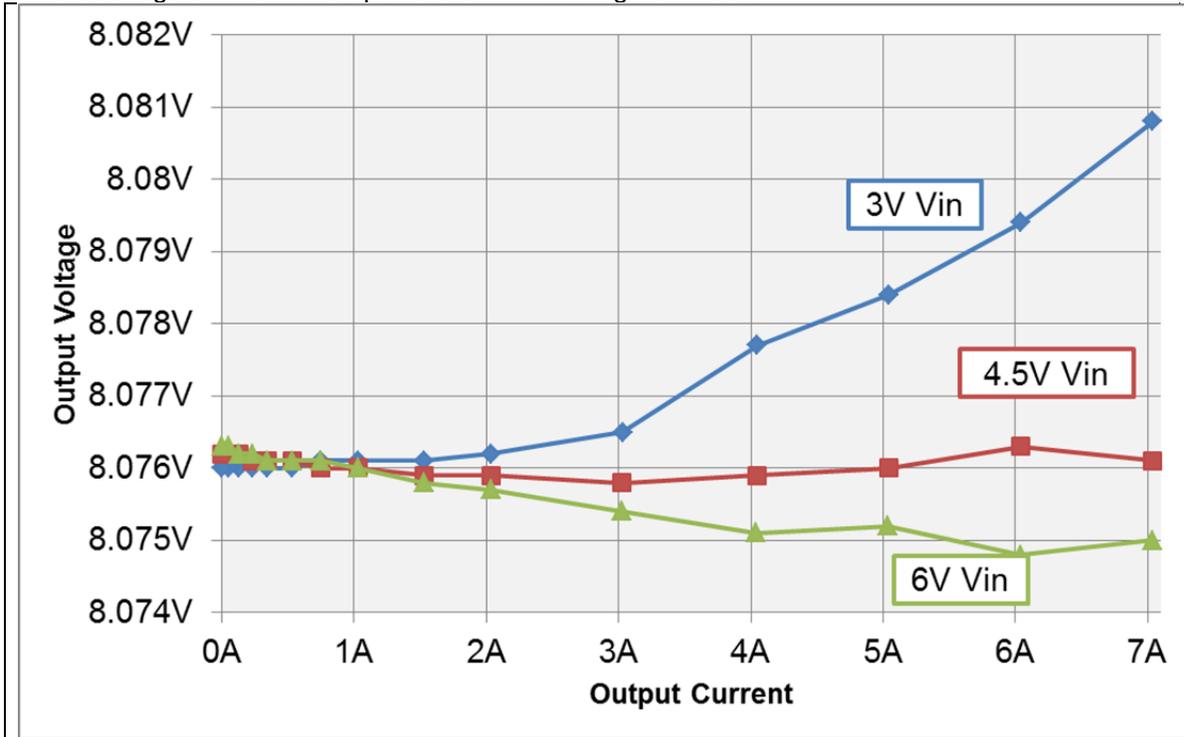


Figure 12

5 Line Regulation

Line regulation at 7A output current is shown in Figure 13

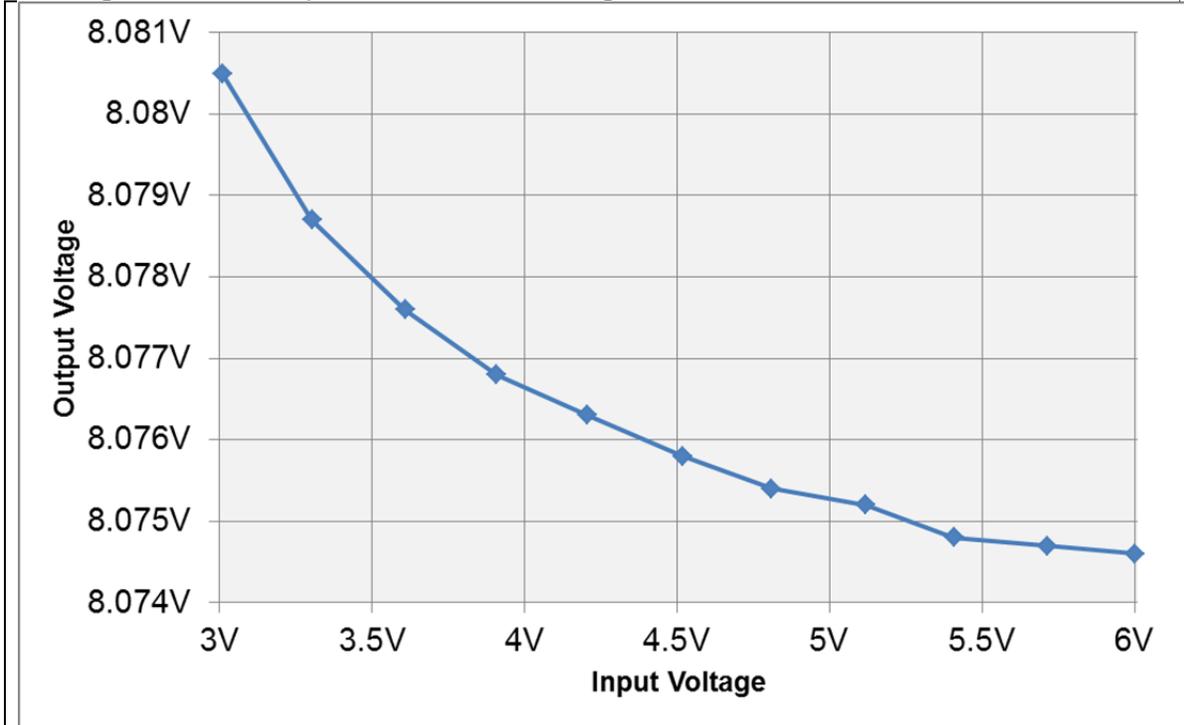


Figure 13

With the same measurement the full load efficiencies across input voltage were calculated

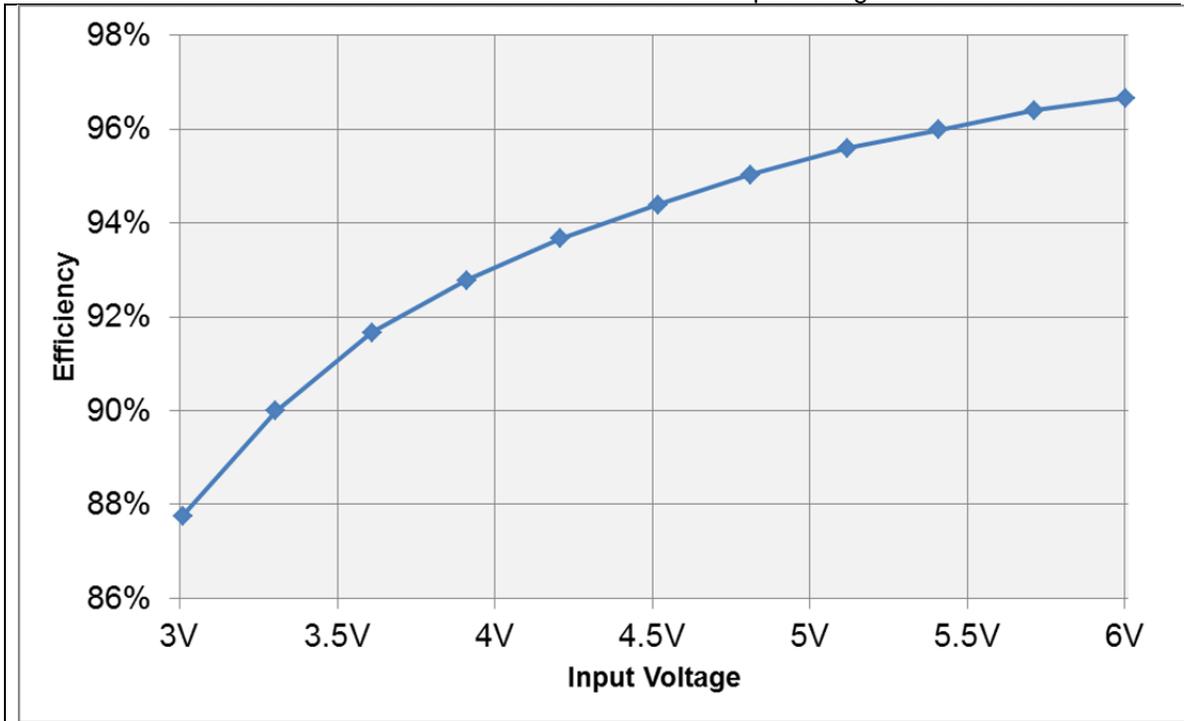


Figure 14

6 Ripple Voltage

6.1 Output

The output ripple voltage is shown in Figure 15. The image was taken with a 7A load and 3V, 4.5V and 6V at the input.

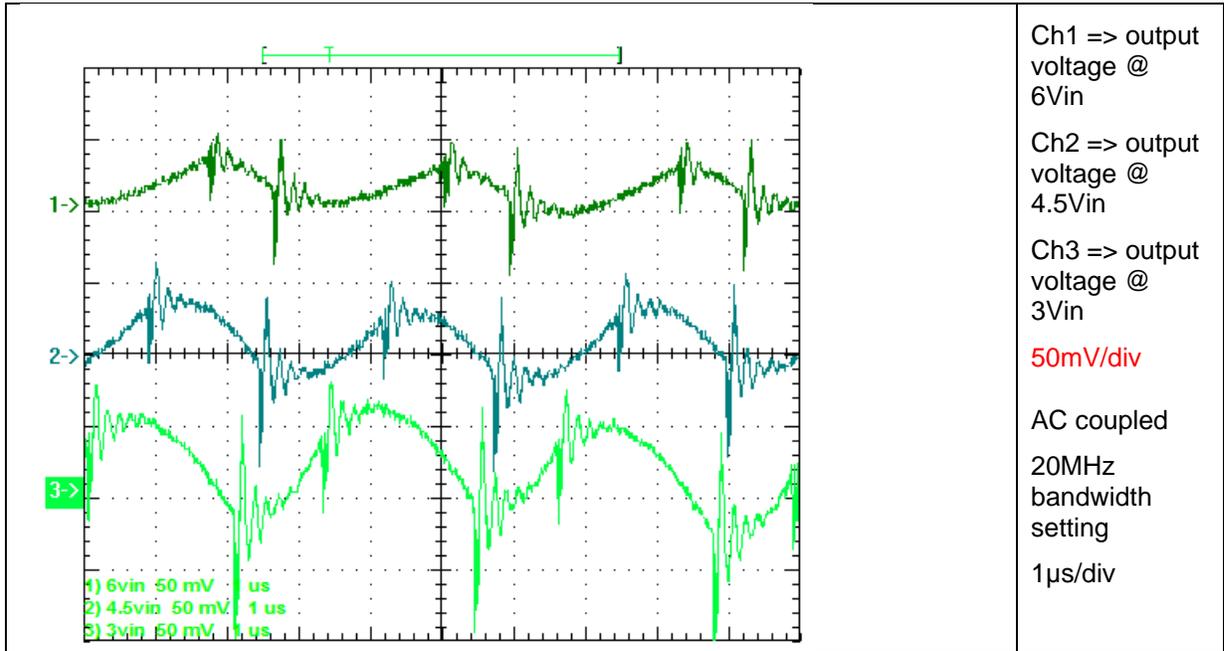


Figure 15

The output ripple voltage before filtering at L2 is shown in Figure 16. The image was taken with a 7A load 3V at the input.

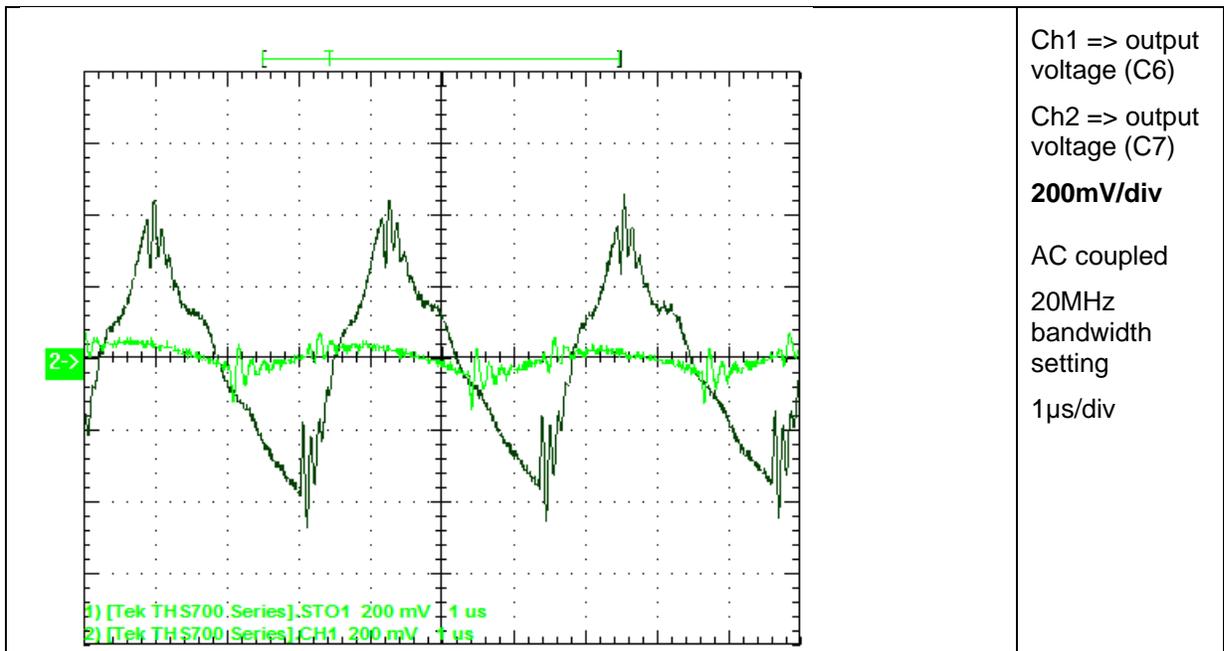


Figure 16

The output ripple voltage before filtering at L2 is shown in Figure 17. The image was taken with a 7A load 4.5V at the input.

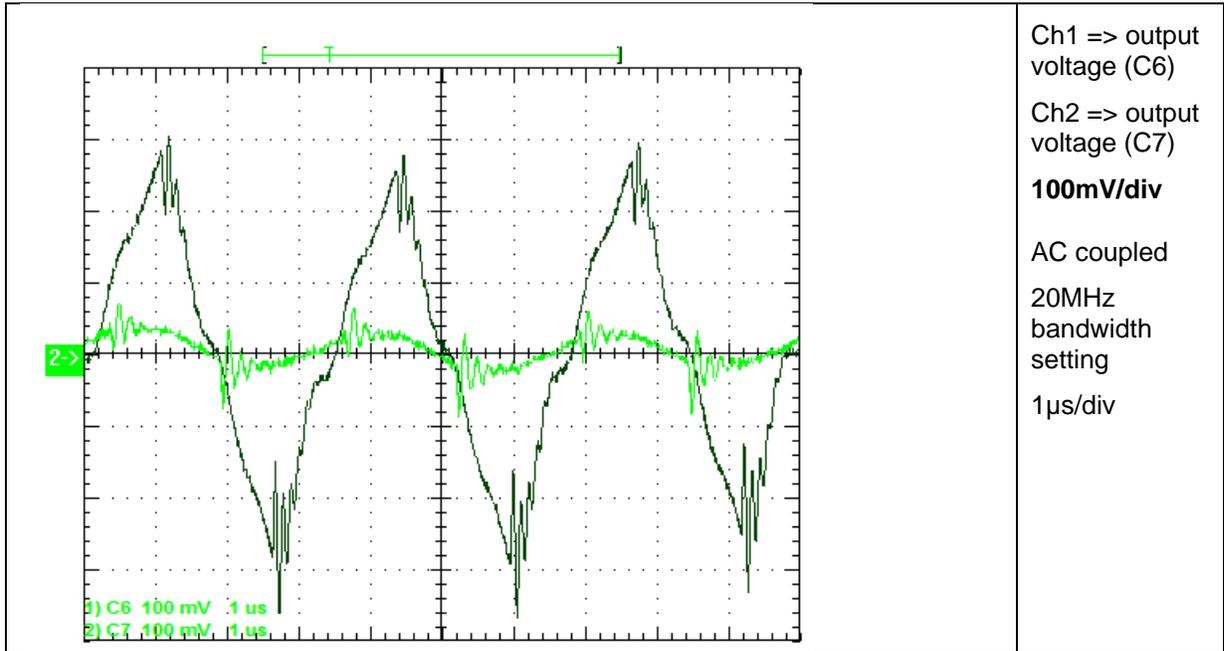


Figure 17

The output ripple voltage before filtering at L2 is shown in Figure 18. The image was taken with a 7A load 6V at the input.

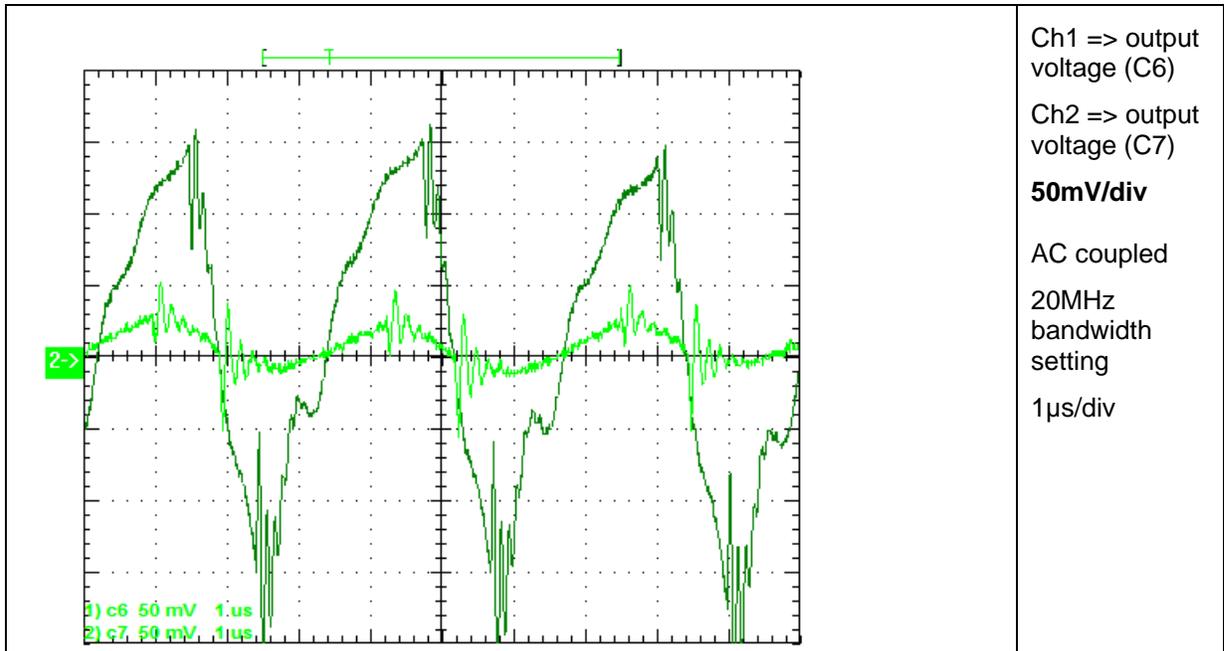


Figure 18

6.2 Input

The input ripple voltage is shown in Figure 19. The image was taken with a 7A load 35V at the input.

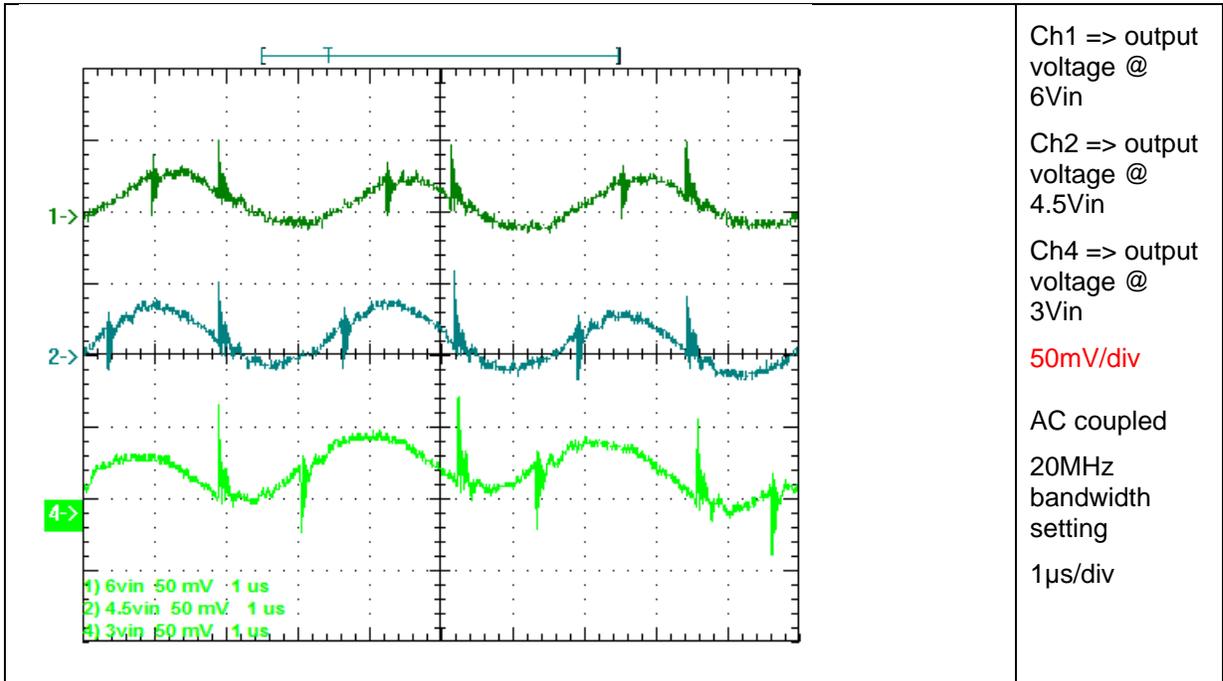


Figure 19

7 Control Loop Frequency Response

Figure 20 shows the loop response with 7A load and 3V input.

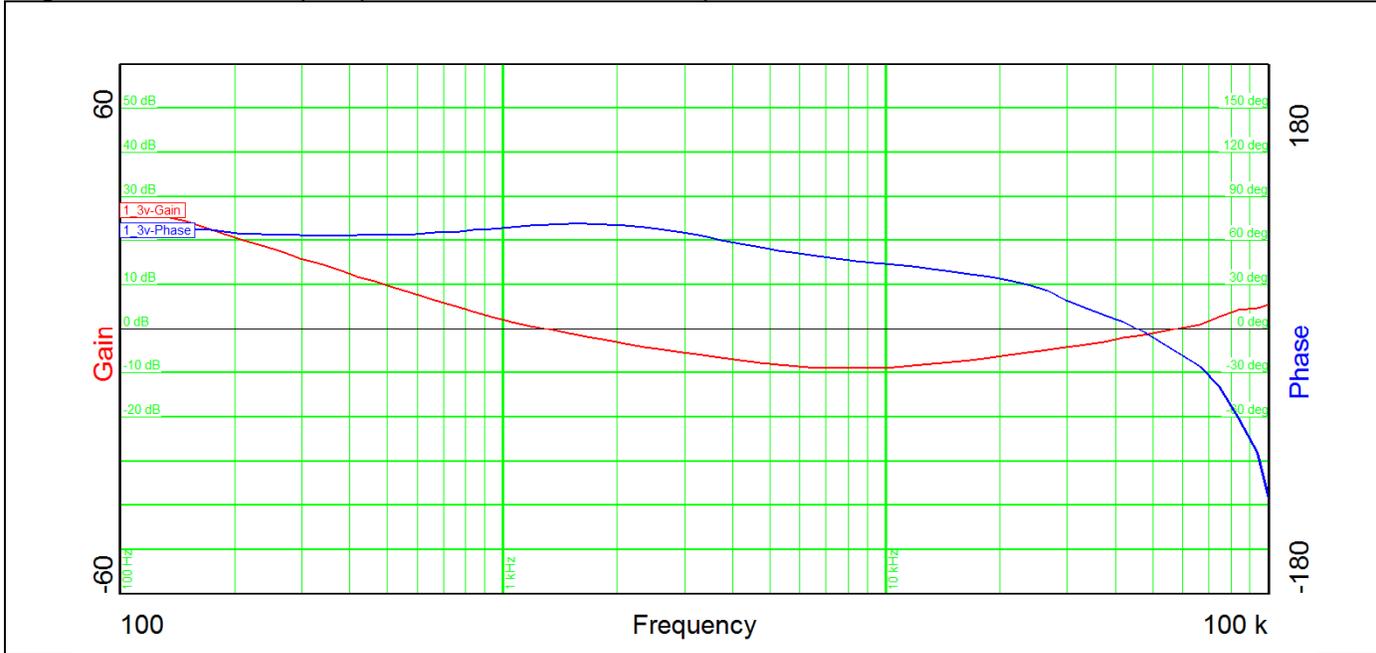


Figure 20

Figure 21 shows the loop response with 7A load and 4.5V input.

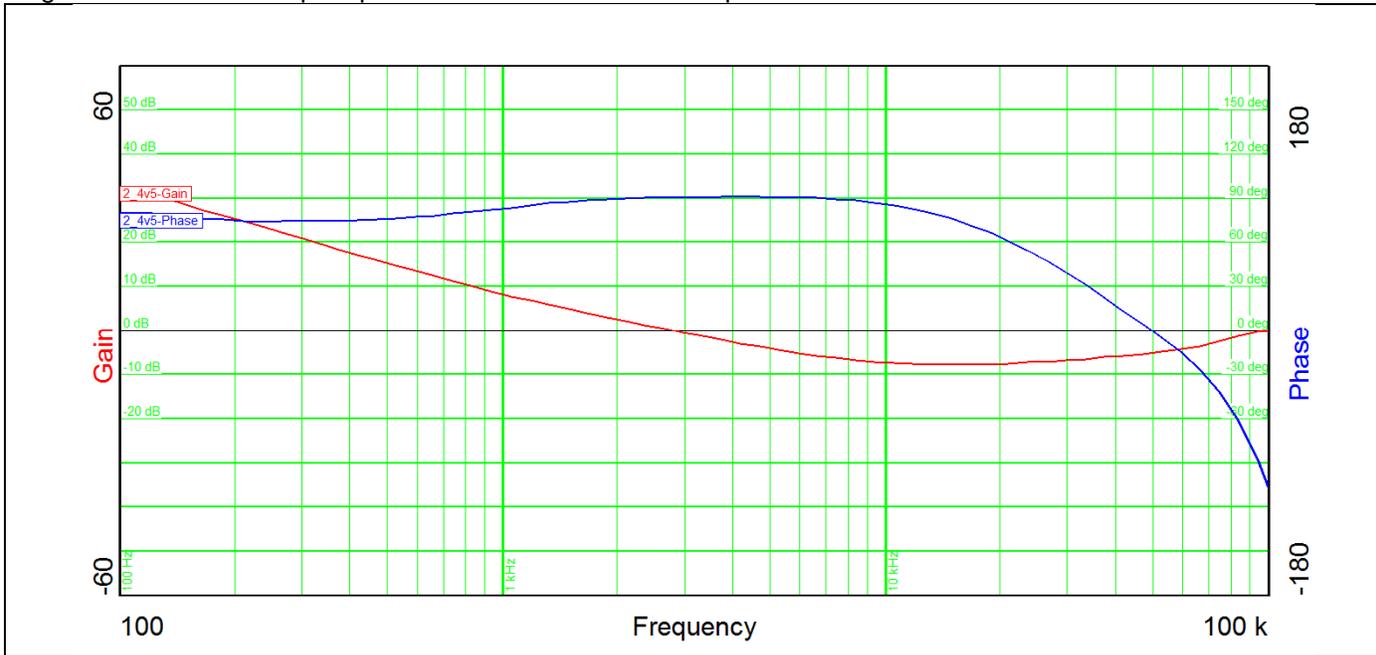


Figure 21

Figure 22 shows the loop response with 7A load and 6V input.

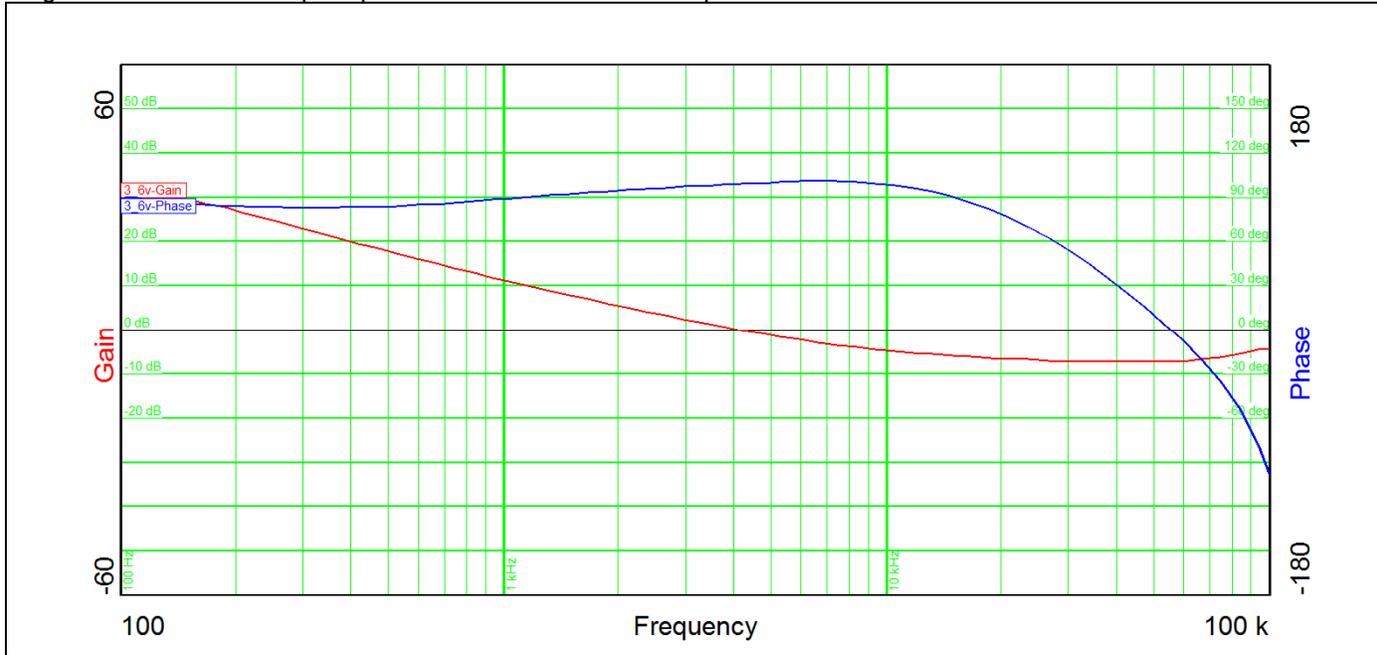


Figure 22

Table 1 summarizes the results

	3V	4.5V	6V
Bandwidth (kHz)	1.29	2.79	4.2
Phasemargin	71°	90°	99°
slope (20dB/decade)	-0.96	-0.87	-0.808
gain margin (dB)	-1.76	-5.29	-7.2
slope (20dB/decade)	+0.617	+0.486	+0.2
freq (kHz)	45.5	49.6	55

Table 1

Loop bandwidth drops by input voltage – see transient response:

8 Load Transients

The Figure 23 shows the response to load transients. The load is switching from 3.5A to 7A. The input voltage was set to 3.2V – the deviation is 3%

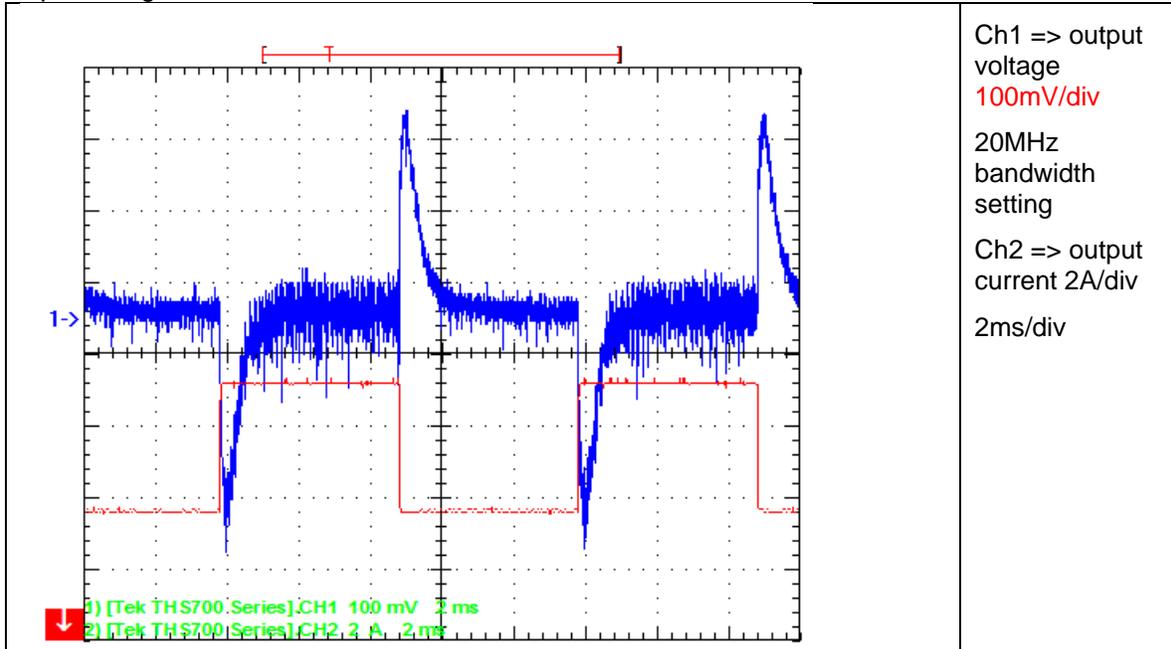


Figure 23

The Figure 24 shows the response to load transients. The load is switching from 3.5A to 7A. The input voltage was set to 4.5V – the deviation is below 3%

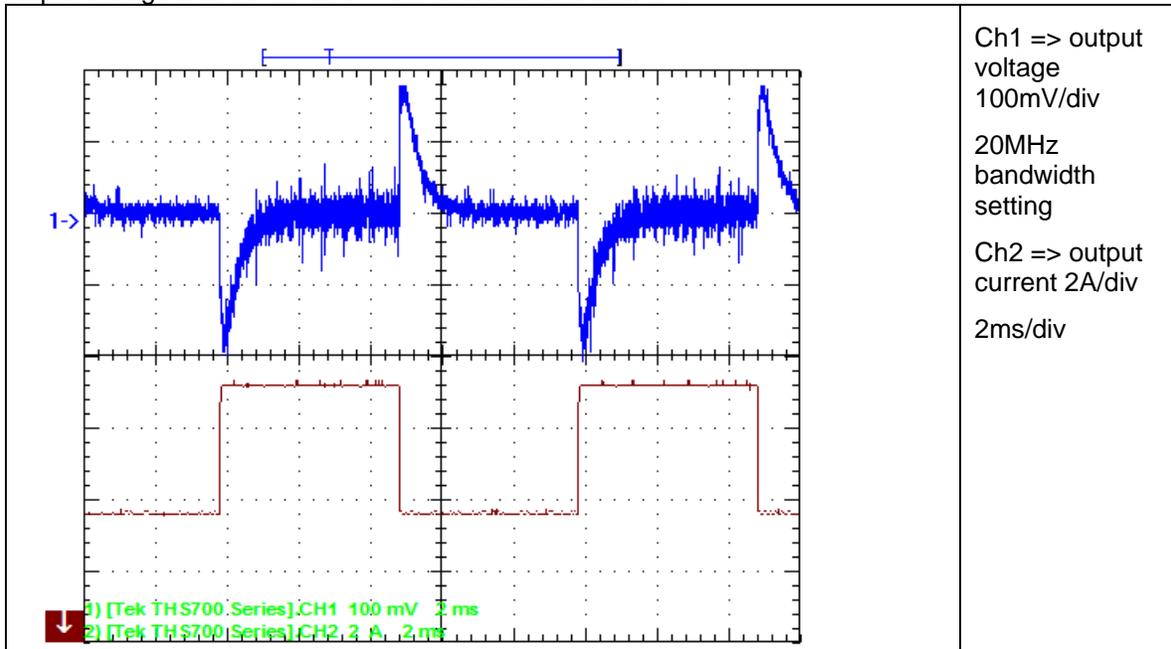


Figure 24

The Figure 25 shows the response to load transients. The load is switching from 3.5A to 7A. The input voltage was set to 6V

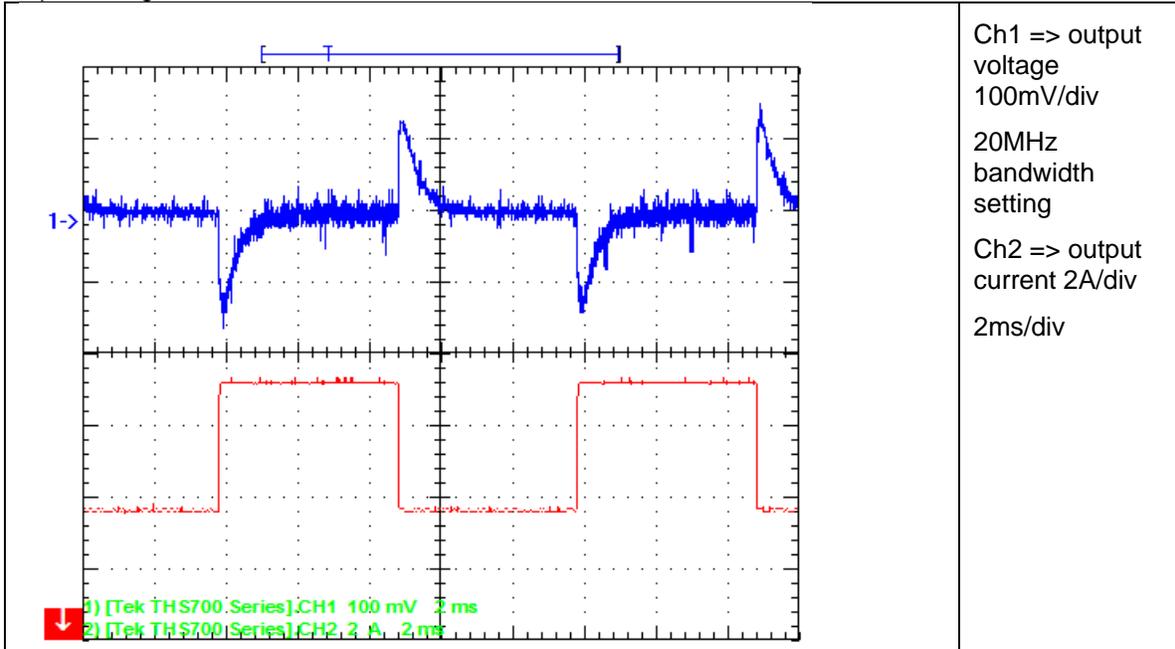


Figure 25

9 Miscellaneous Waveforms

9.1 3V Input

9.1.1 Switch node (Low Side FET)

With input voltage set to 3V and 7A lout results in the waveform shown in Figure 26

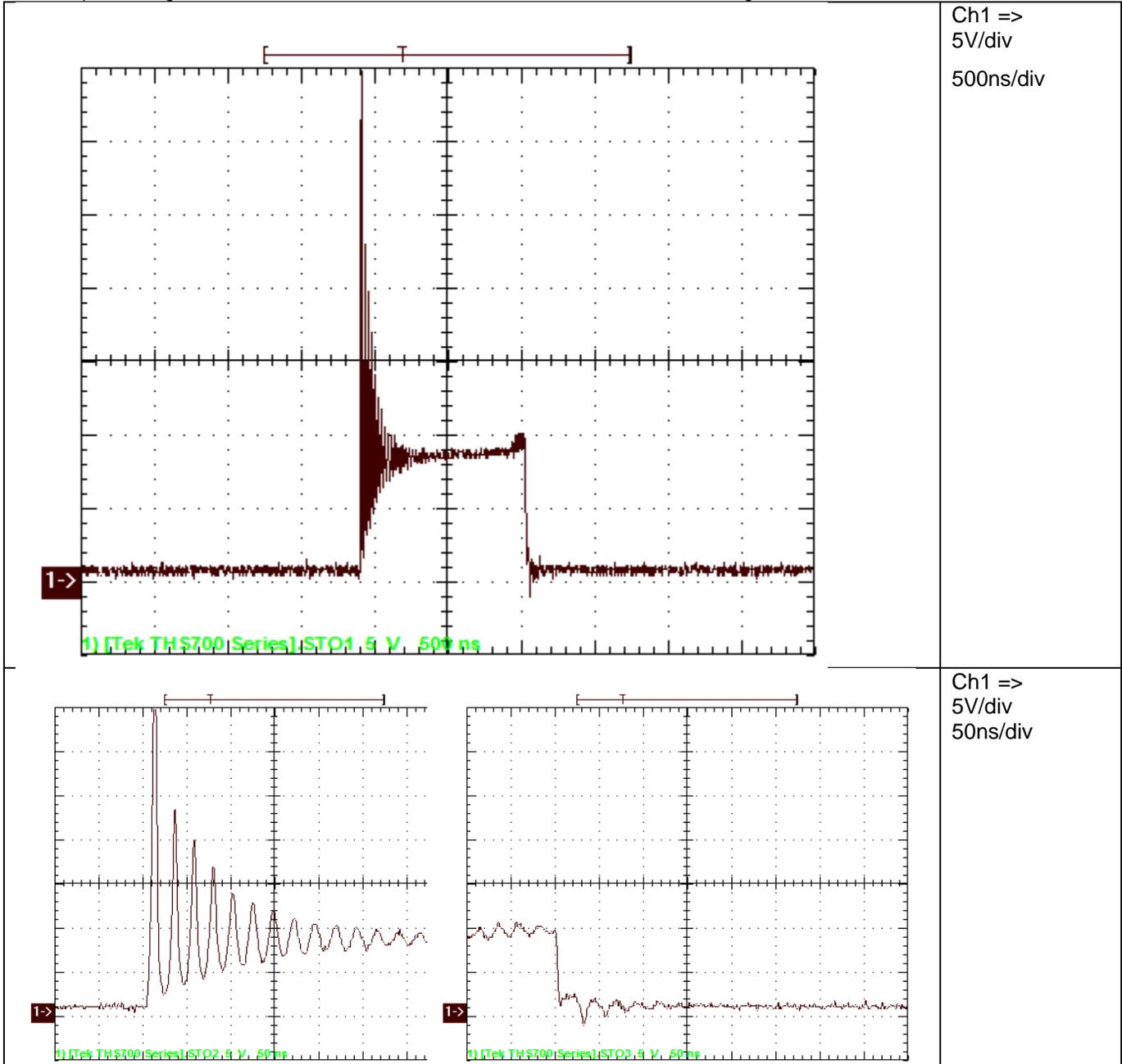


Figure 26

9.1.2 Gate of Low side MOS-FET

With input voltage set to 3V and 7A lout results in the waveform shown in Figure 27.

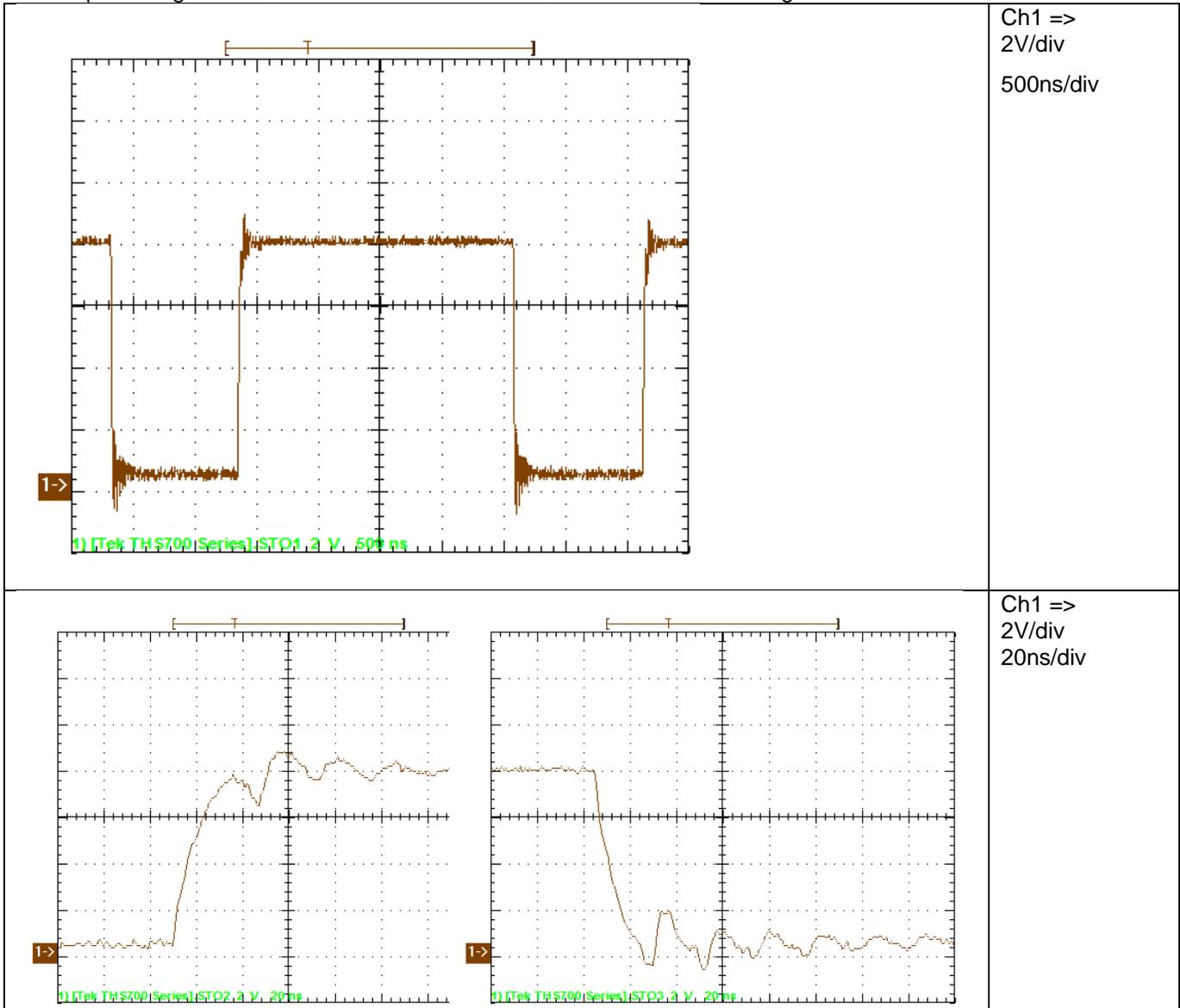


Figure 27

9.1.3 Hi Side MOS FET

The waveform is shown in **Figure 28**.(the same setup as above)

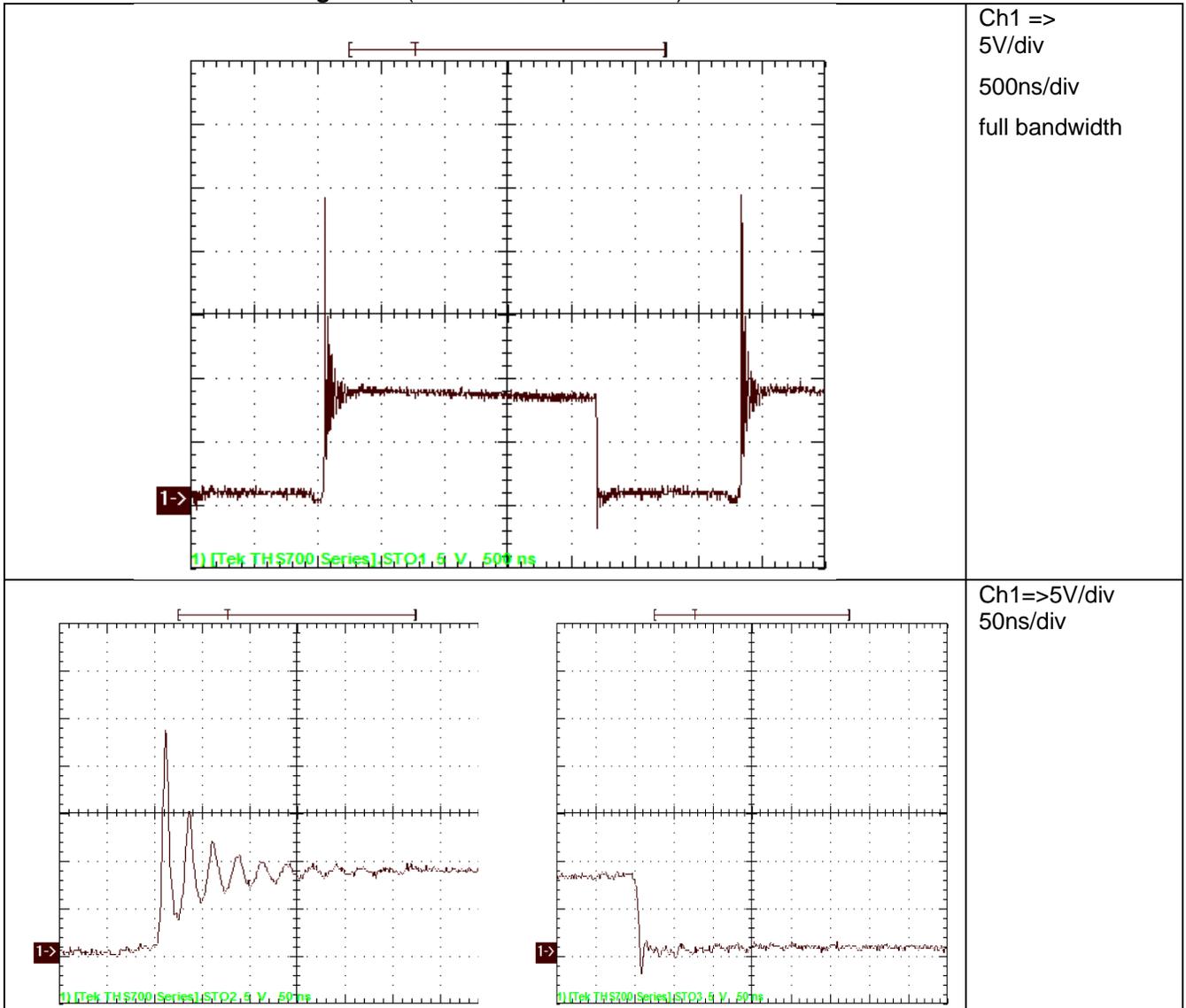


Figure 28

9.1.4 Hi Side MOS FET Gate

With input voltage set to 3V and 7A lout results in the waveform shown in Figure 29.

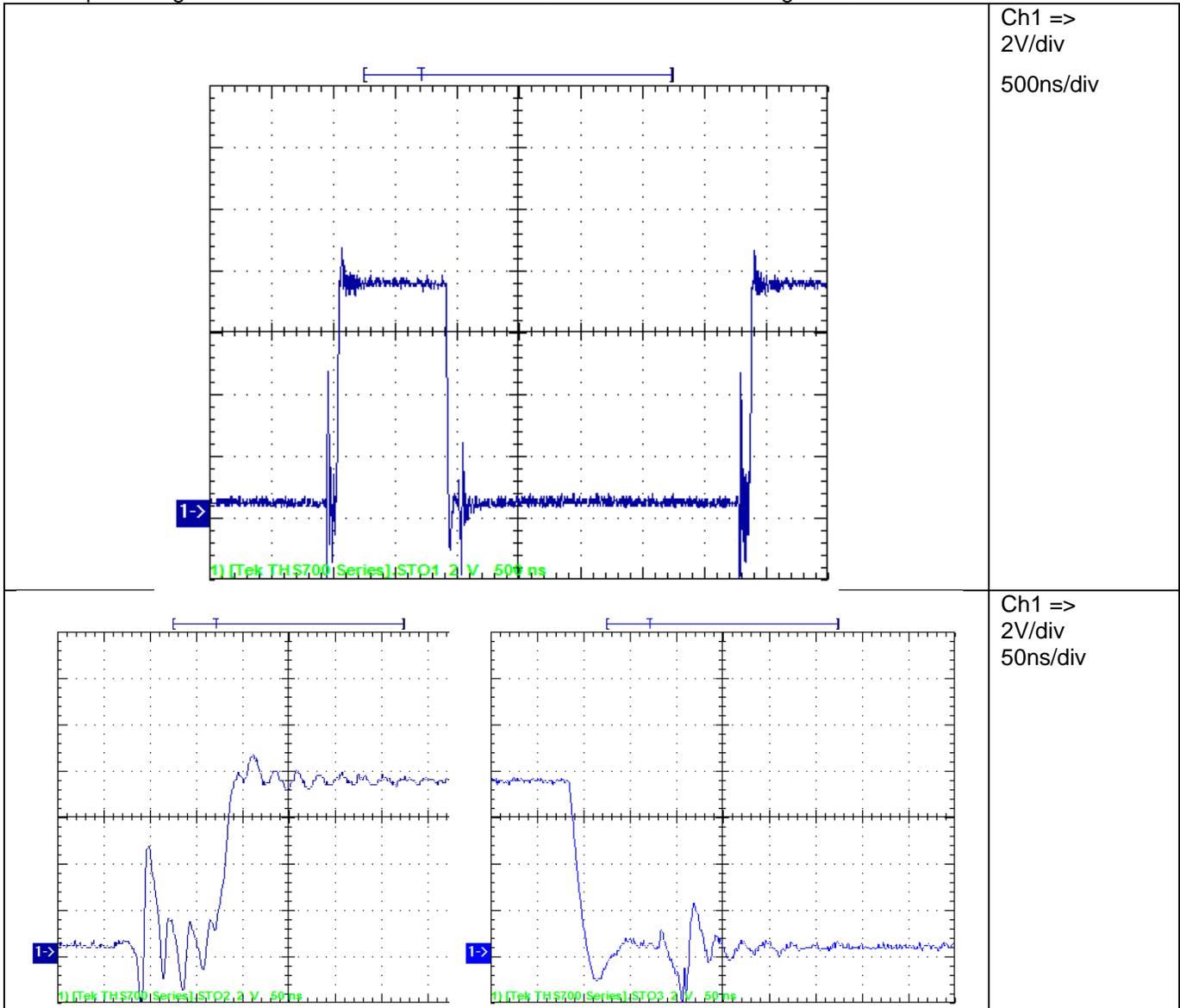


Figure 29

9.2 4.5V Input

9.2.1 Switch node (Low Side FET)

With input voltage set to 4.5V and 7A Iout results in the waveform shown in Figure 30

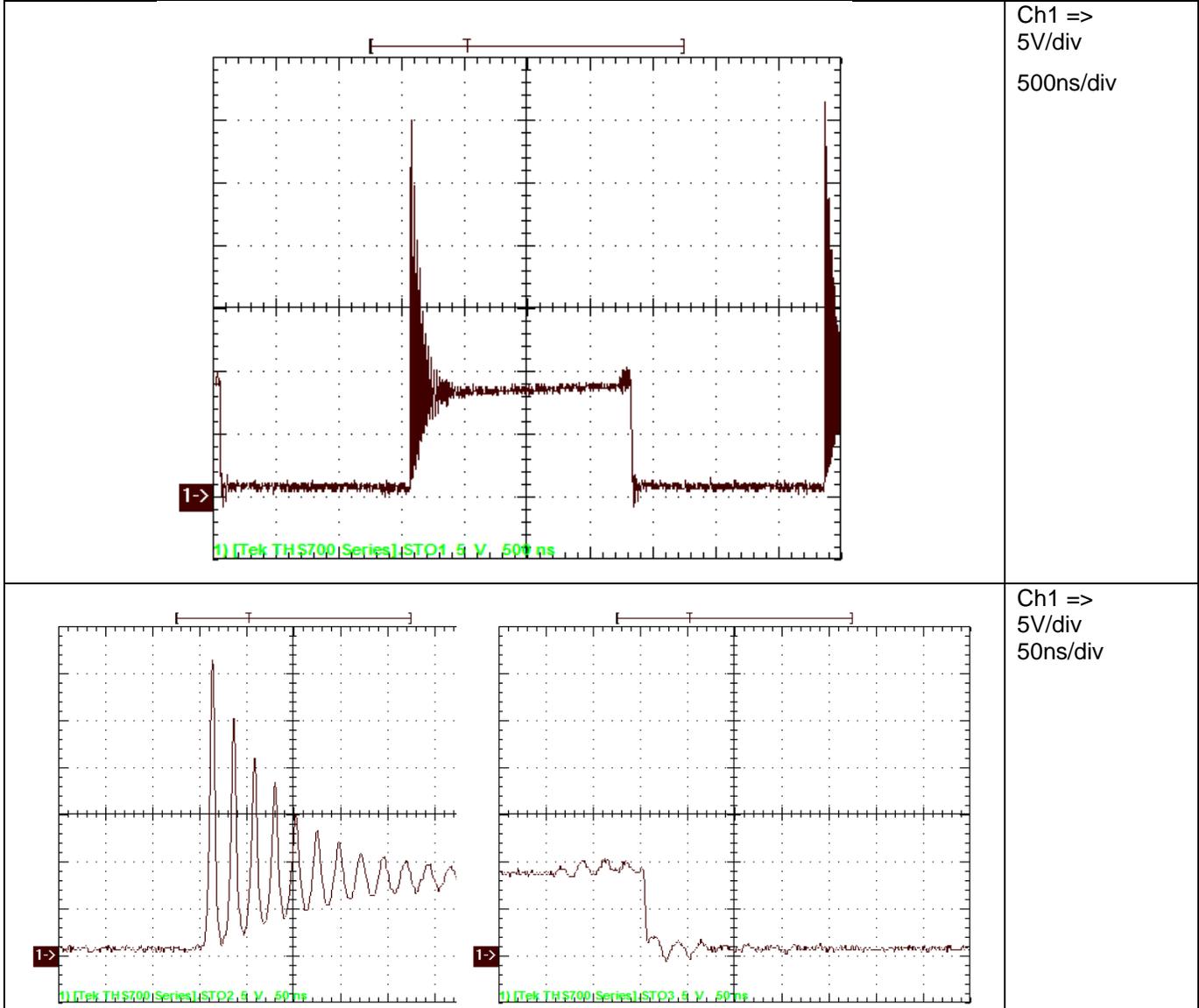


Figure 30

9.2.2 Gate of Low side MOS-FET

With input voltage set to 4.5V and 7A Iout results in the waveform shown in Figure 31.

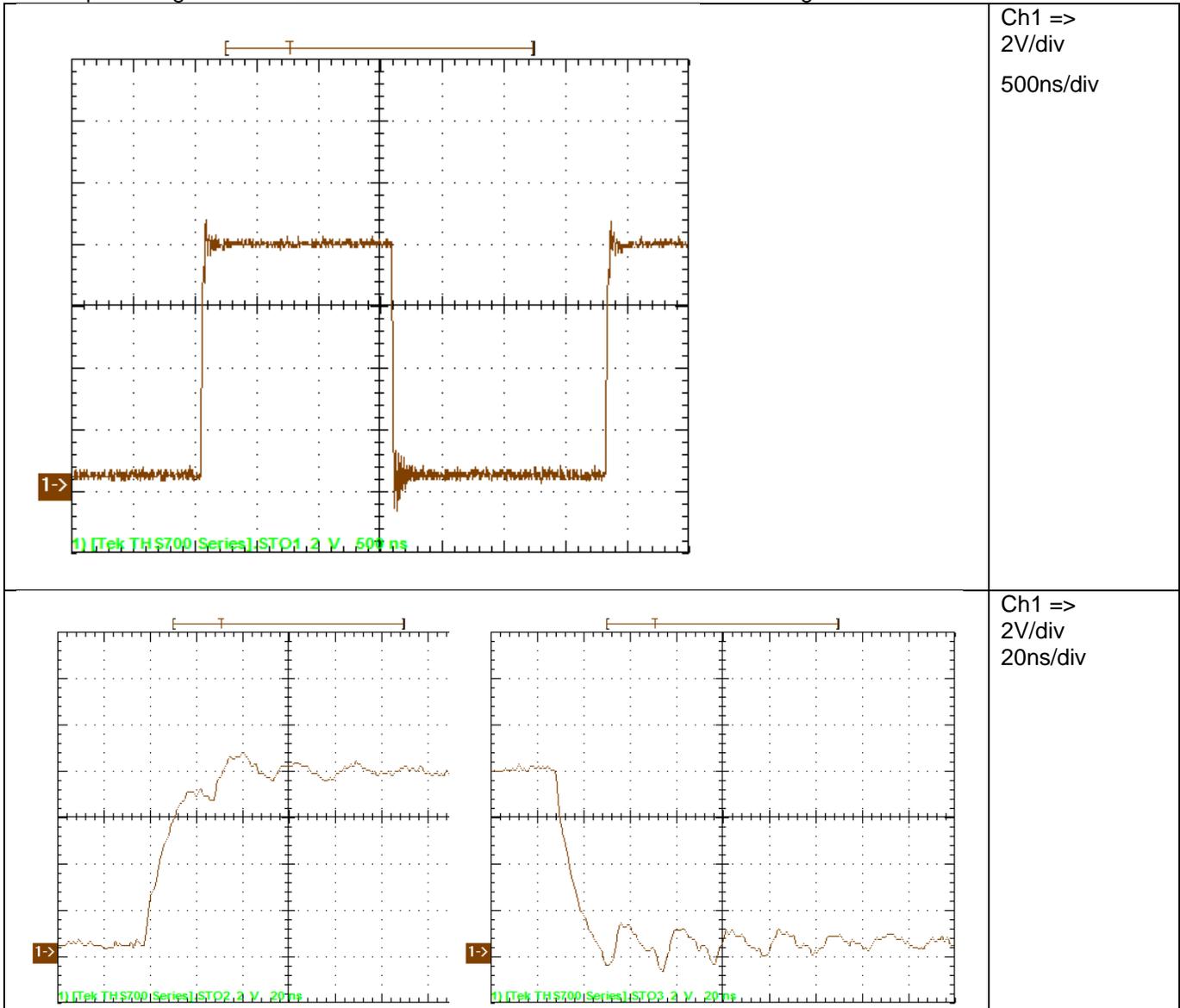


Figure 31

9.2.3 Hi Side MOS FET

The waveform is shown in **Figure 32**.(the same setup as above)

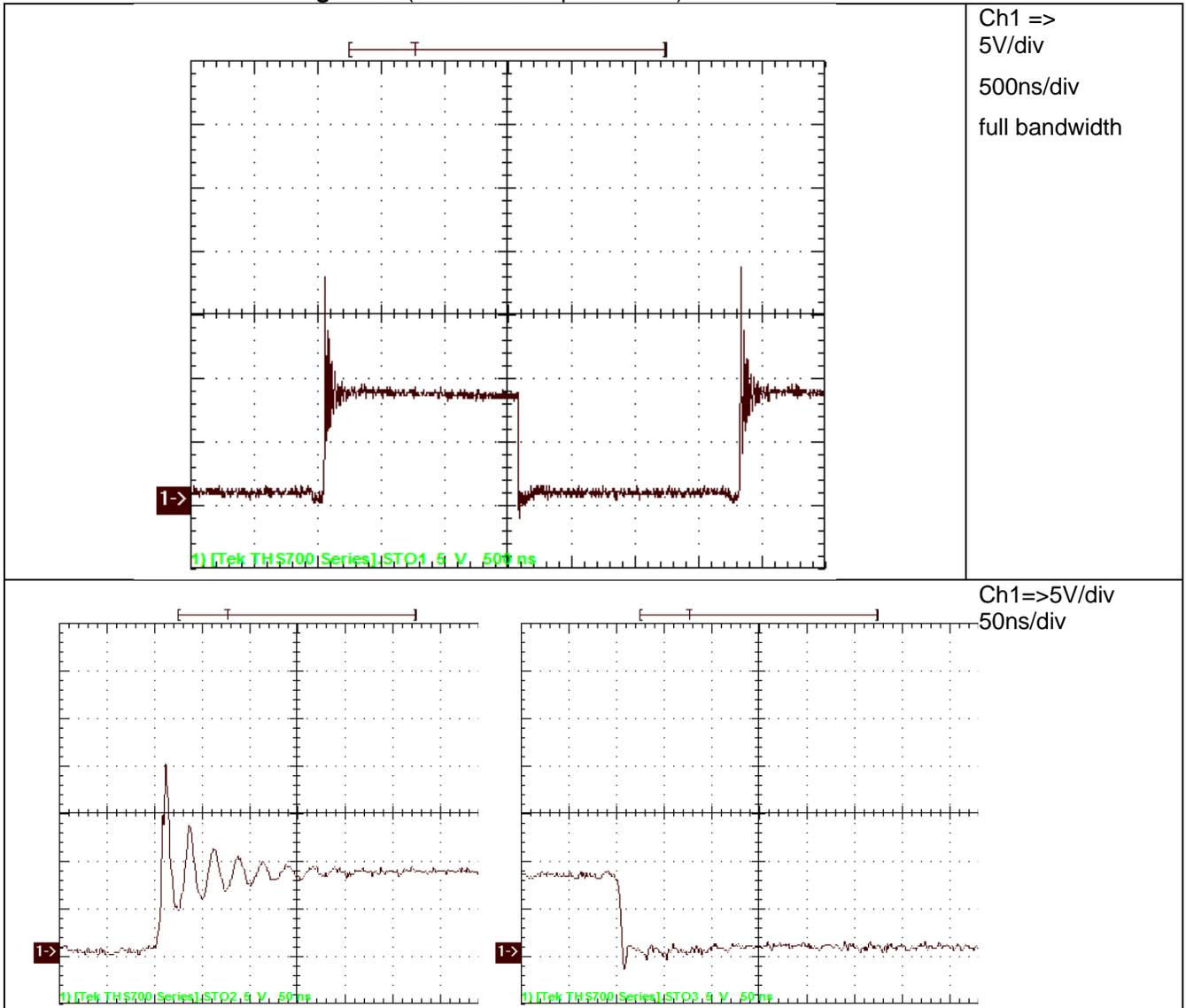


Figure 32

9.2.4 Hi Side MOS FET Gate

With input voltage set to 4.5V and 7A Iout results in the waveform shown in Figure 33.

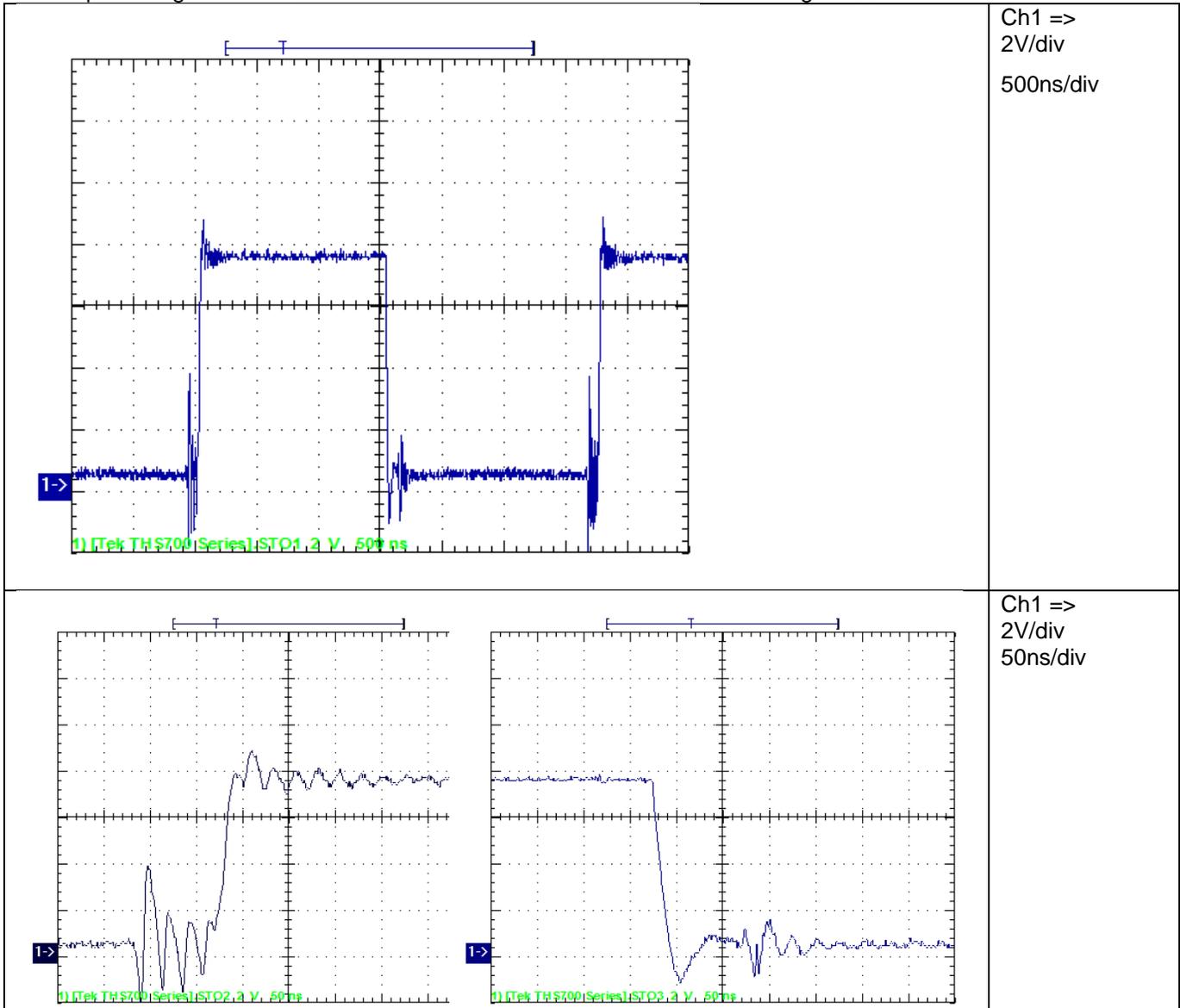


Figure 33

9.3 6V Input

9.3.1 Switch node (Low Side FET)

With input voltage set to 6V and 7A lout results in the waveform shown in Figure 34

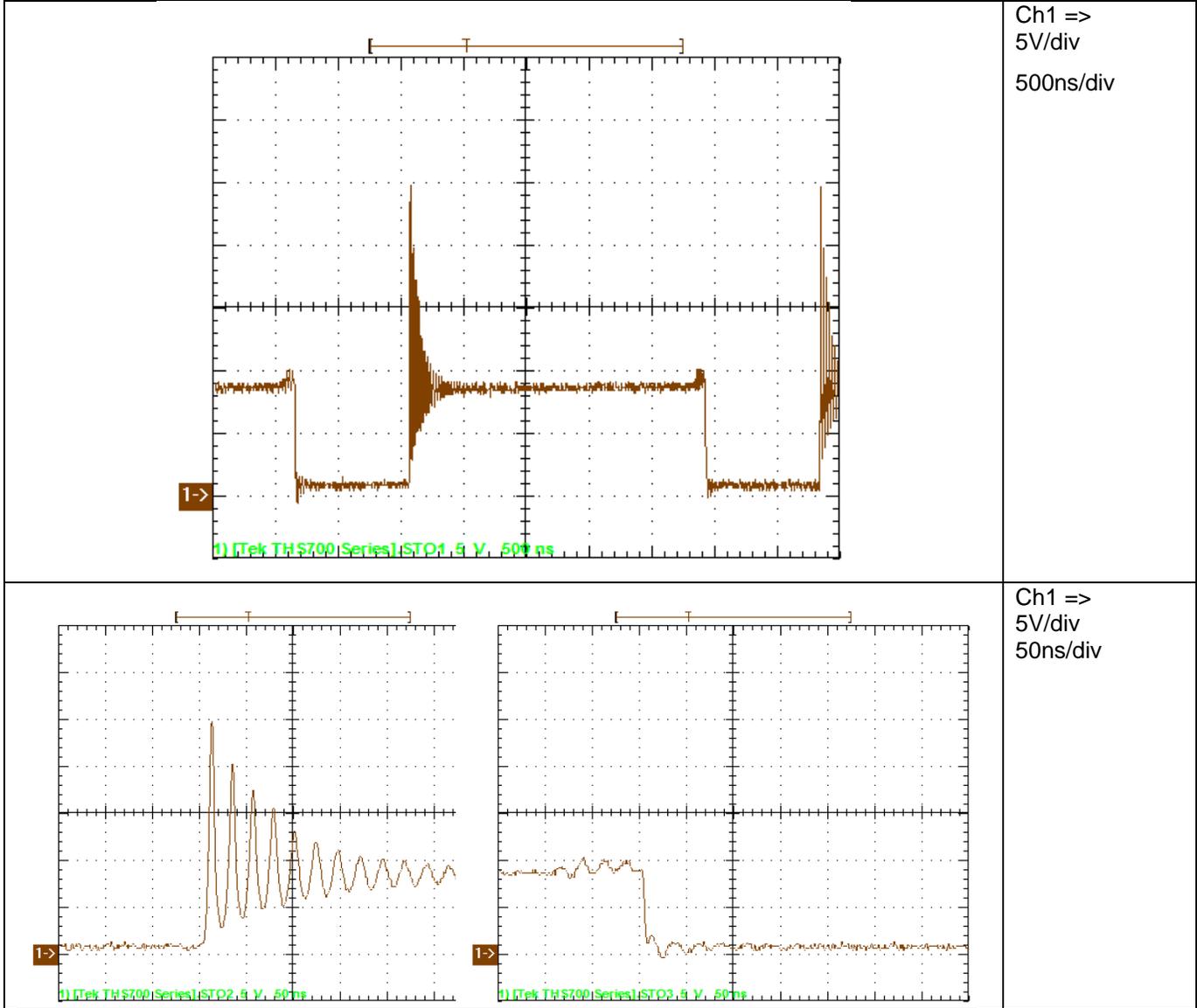


Figure 34

9.3.2 Gate of Low side MOS-FET

With input voltage set to 6V and 7A Iout results in the waveform shown in Figure 35.

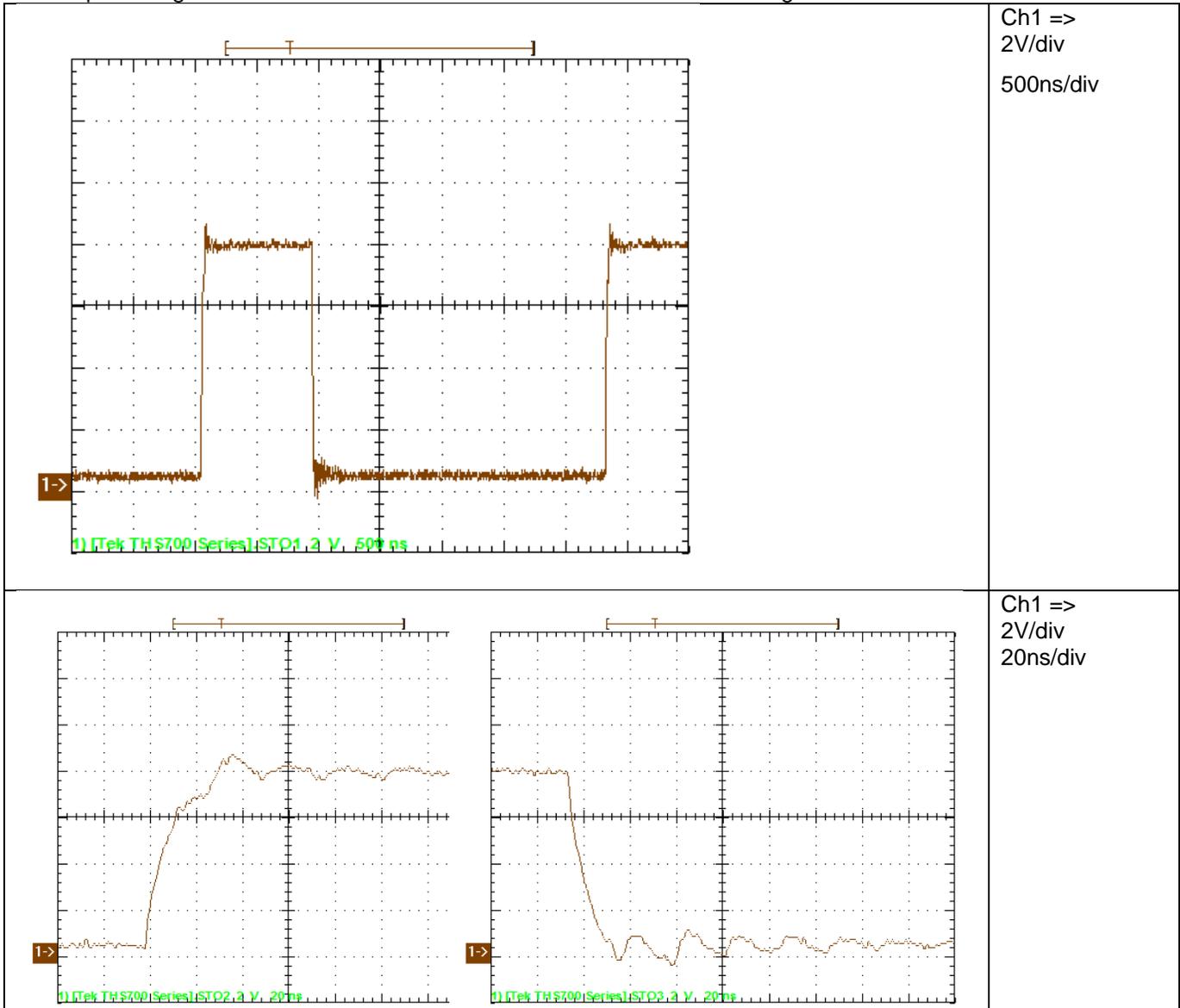


Figure 35

9.3.3 Hi Side MOS FET

The waveform is shown in **Figure 36** (the same setup as above)

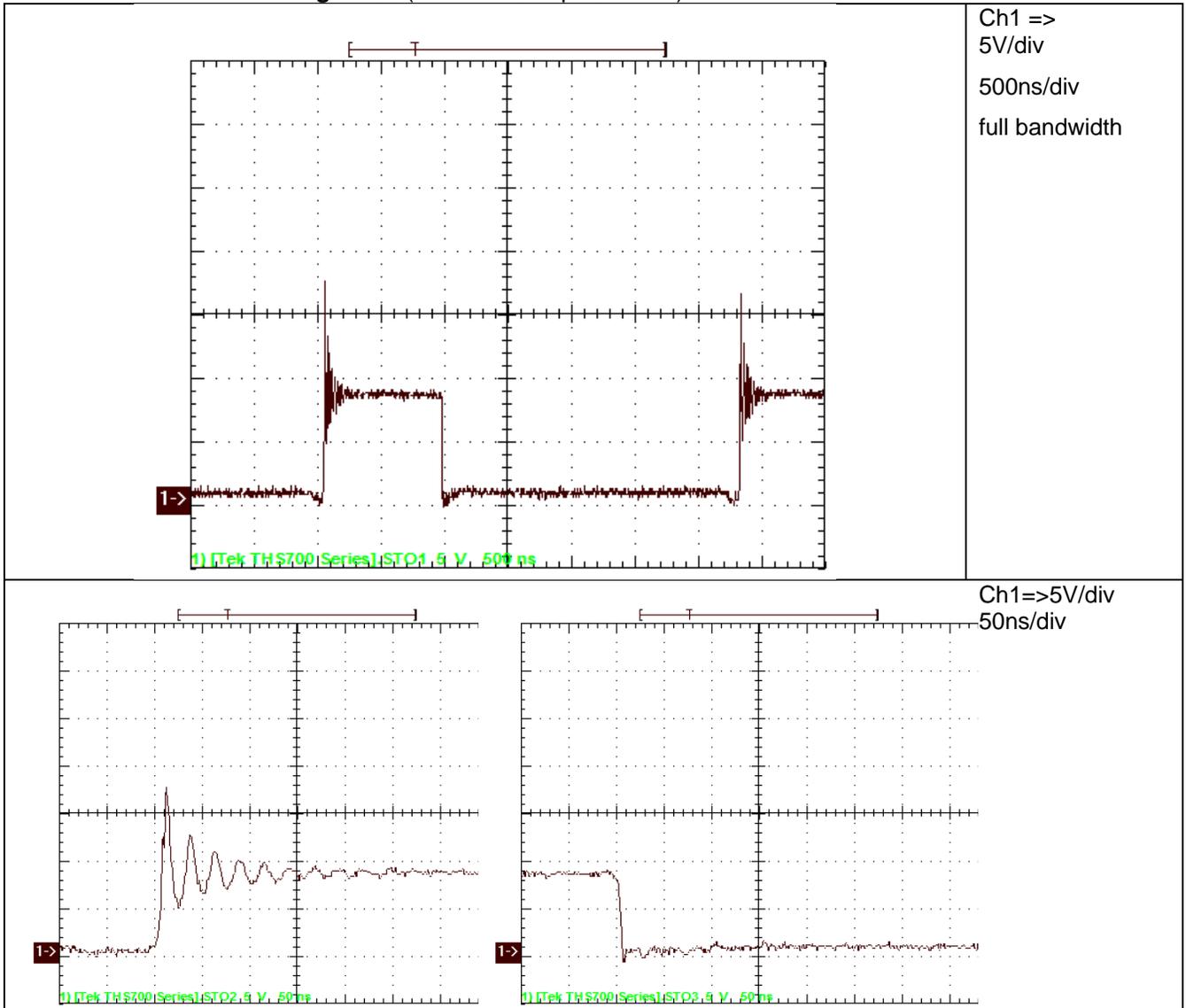


Figure 36

9.3.4 Hi Side MOS FET Gate

With input voltage set to 6V and 7A lout results in the waveform shown in Figure 37.

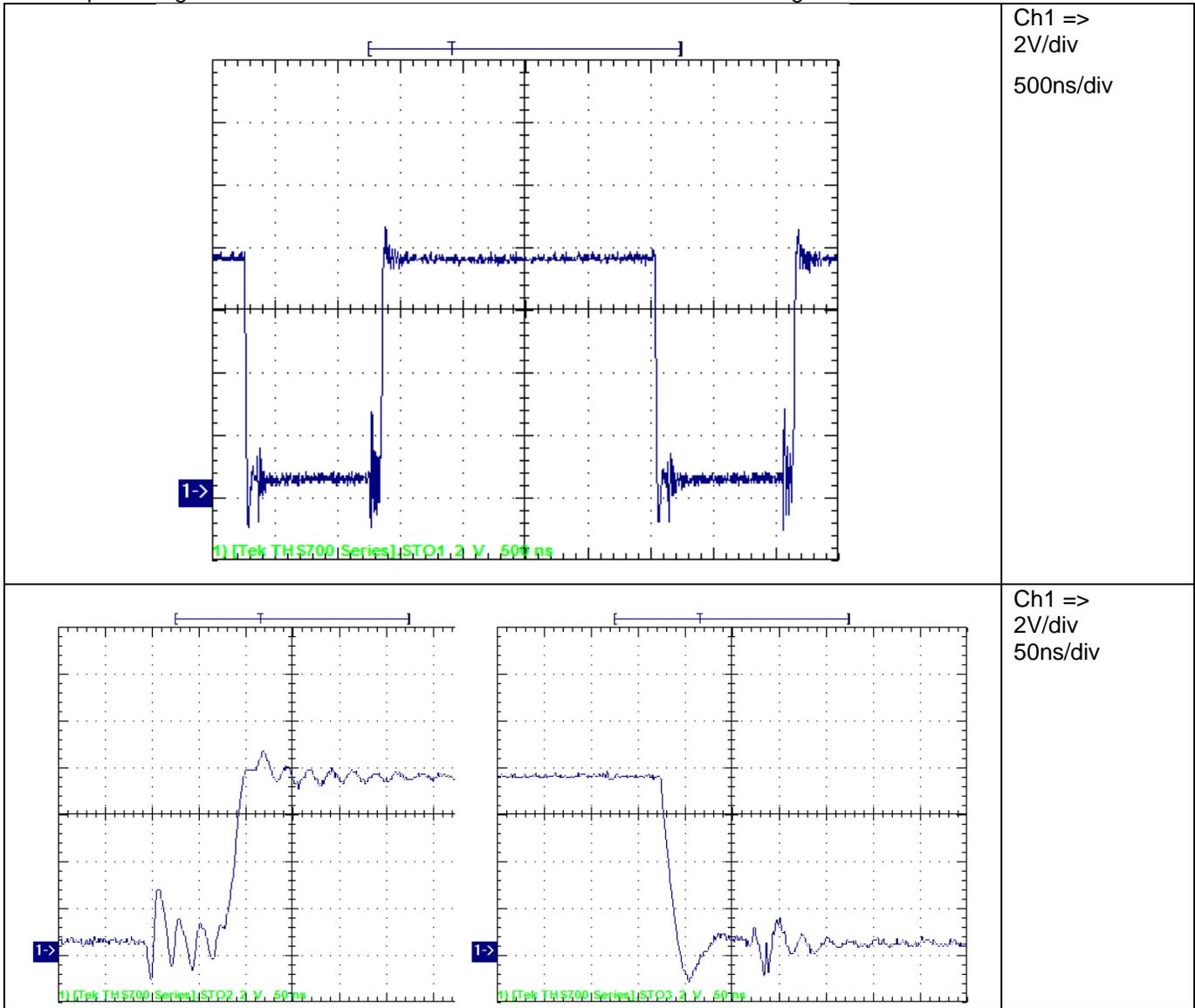


Figure 37

10 Thermal Image

Figure 38 shows the thermal image at 6V input and 7A output (no additional airflow)

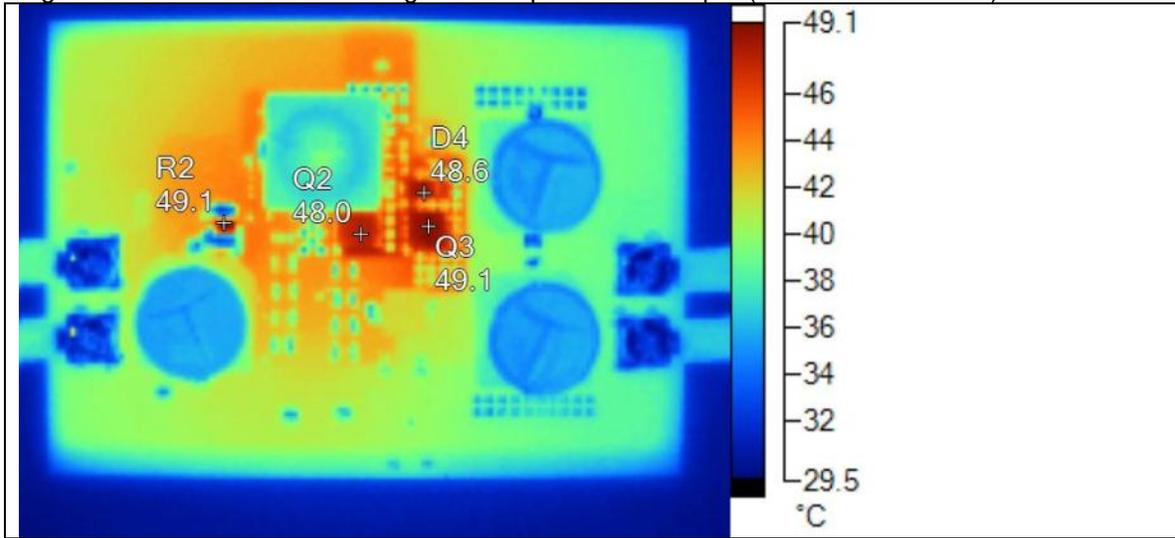


Figure 38

Name	Temperature
R2	49.1°C
Q2	48.0°C
Q3	49.1°C
D4	48.6°C

Table 2

Figure 39 shows the thermal image at 4.5V input and 7A output (no additional airflow)

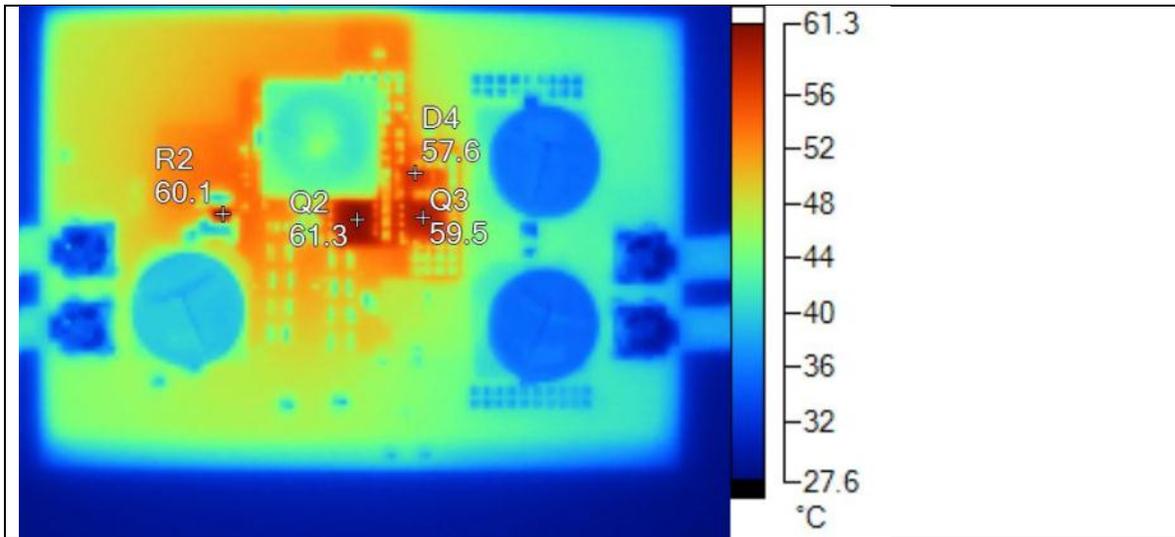


Figure 39

Name	Temperature
Q2	61.3°C
Q3	59.5°C
D4	57.6°C
R2	60.1°C

Table 3

Figure 40 shows the thermal image at 3V input and 7A output (no additional airflow)

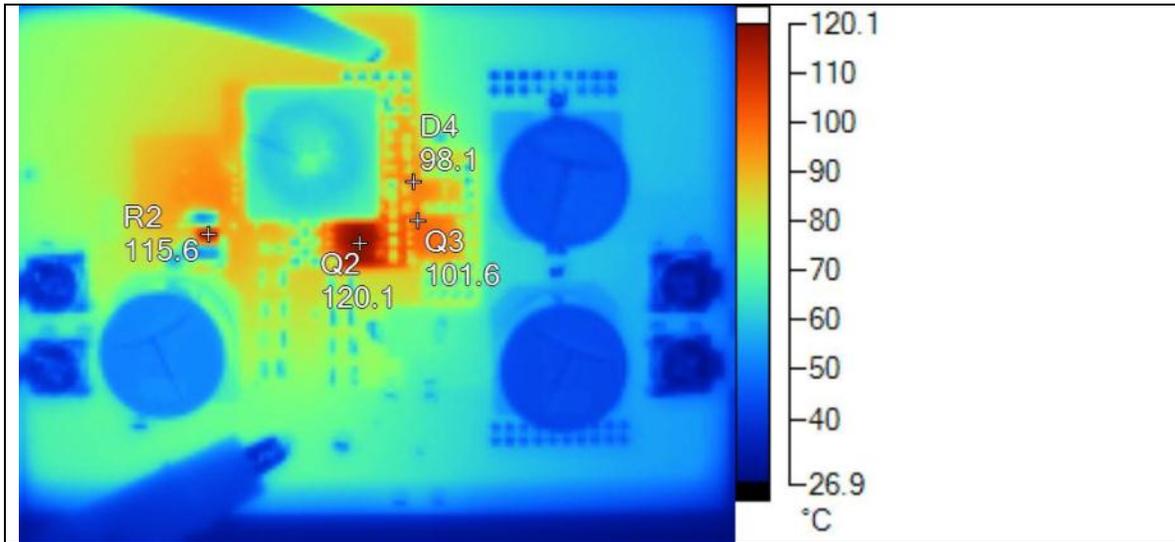


Figure 40

Name	Temperature
Q2	120.1°C
R2	115.6°C
Q3	101.6°C
D4	98.1°C

Table 4

Figure 40 shows the thermal image at 3V input and 7A output (with additional airflow)

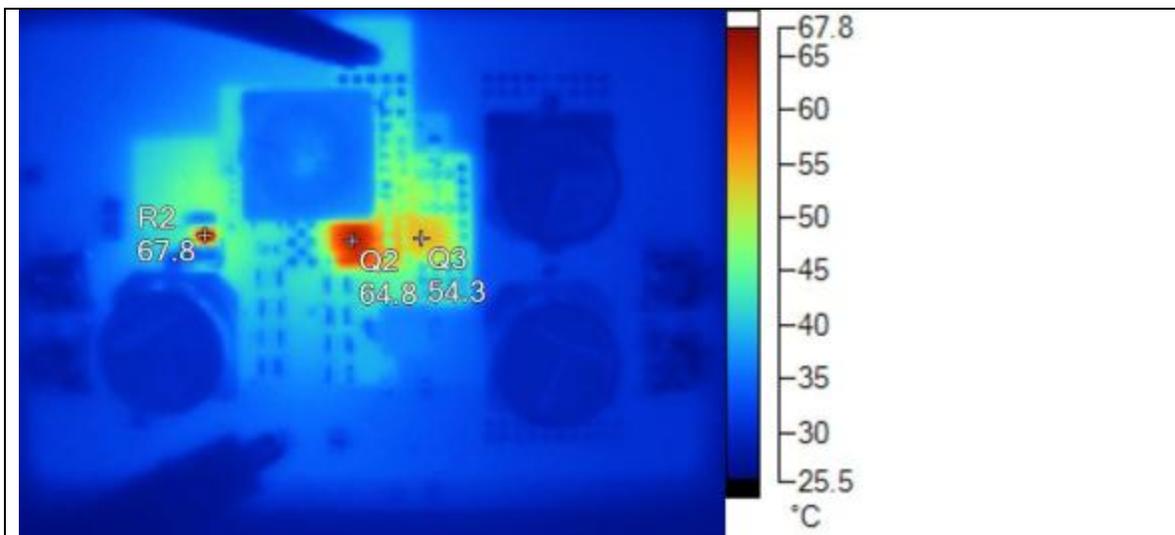


Figure 41

Name	Temperature
R2	67.8°C
Q2	64.8°C
Q3	54.3°C

Table 5

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