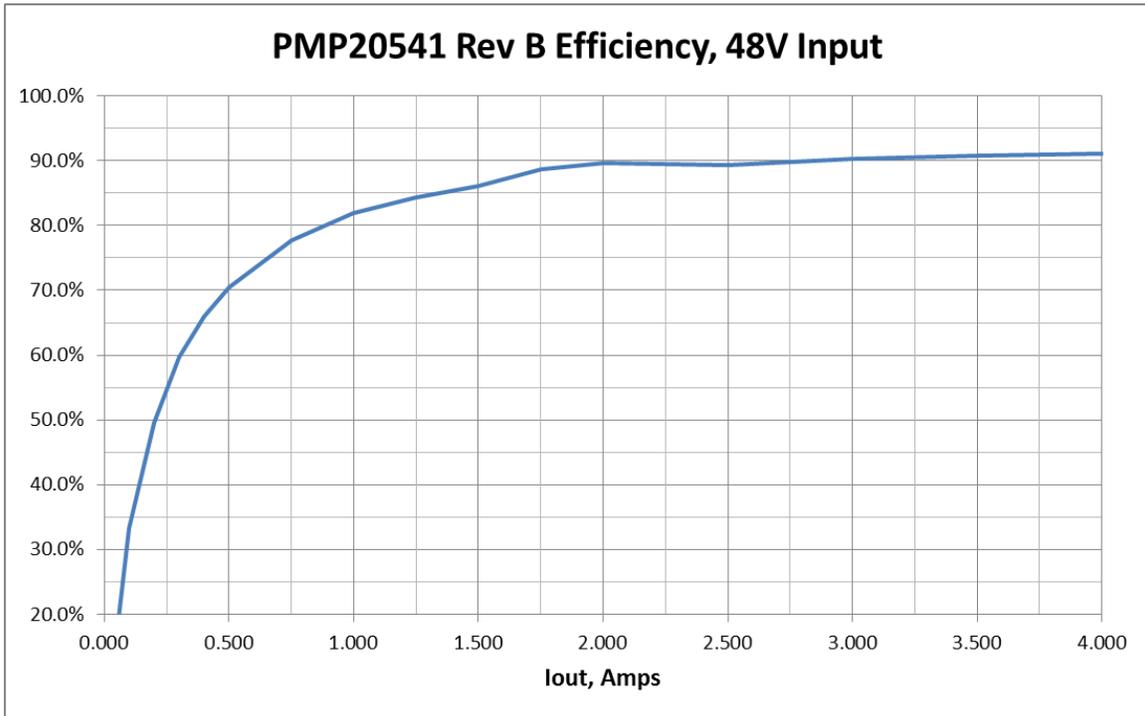


Testing performed with 54V input, 4A load and 20MHz bandwidth unless noted.

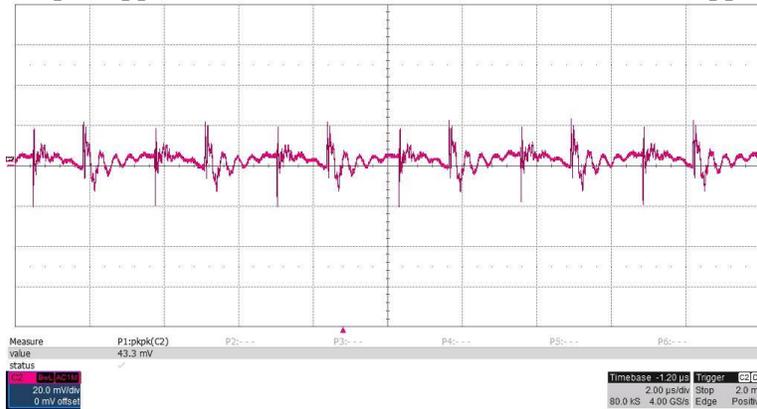
Efficiency

J2 I_{out}	J2 V_{out}	J1 I_{in}	J1 V_{in}	J1 Eff
0.000	12.030	0.044	54.00	0.0%
0.100	12.030	0.067	54.00	33.3%
0.200	12.030	0.090	54.00	49.5%
0.300	12.030	0.112	54.00	59.7%
0.400	12.029	0.135	54.00	66.0%
0.500	12.029	0.158	54.00	70.5%
0.750	12.028	0.215	54.00	77.7%
1.000	12.028	0.272	54.00	81.9%
1.250	12.027	0.330	54.00	84.4%
1.500	12.027	0.388	54.00	86.1%
1.750	12.206	0.446	54.00	88.7%
2.000	12.206	0.504	54.00	89.7%
2.500	12.024	0.623	54.00	89.4%
3.000	12.023	0.740	54.00	90.3%
3.500	12.021	0.859	54.00	90.7%
4.000	12.020	0.978	54.00	91.0%

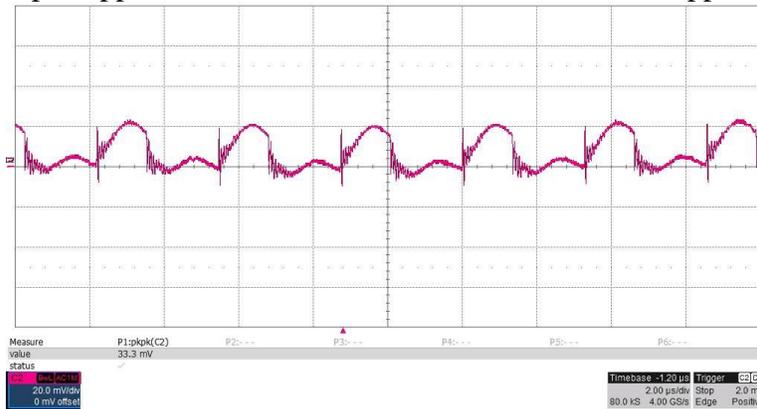


Ripple and Noise

Output ripple, 20mV/div, 2usec/div, measured 43.3mVpp across C14:

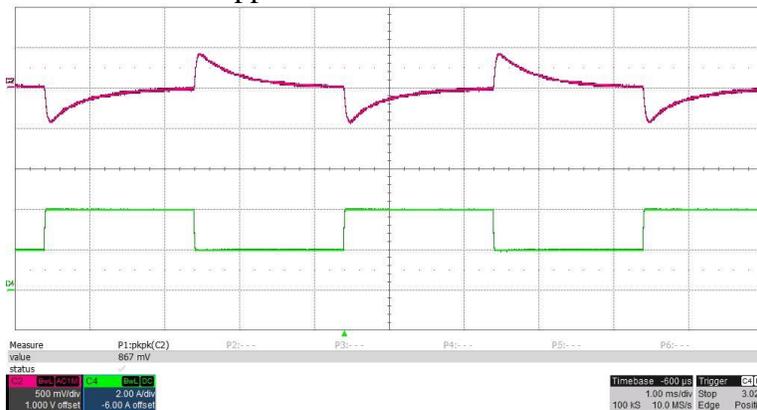


Input ripple, 20mV/div, 2usec/div, measured 33.3mVpp across C3:



Dynamic Loading

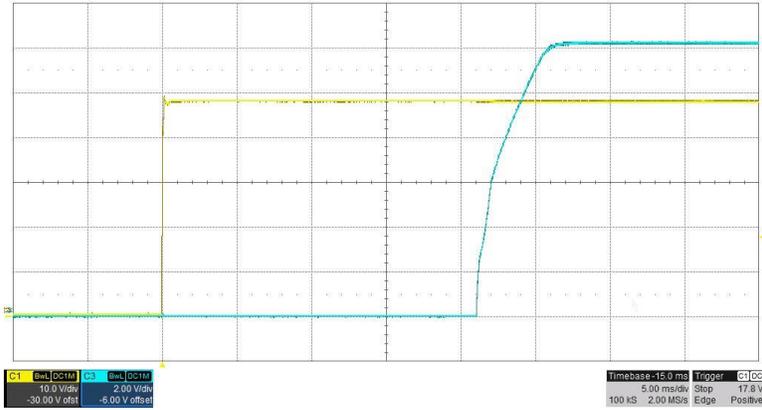
Output load step response, 2A to 4A load step
500mV/div, 2A/div, 1msec/div, slew rate = 400mA/usec
Measured 867mVpp across C14:



Turn On Response

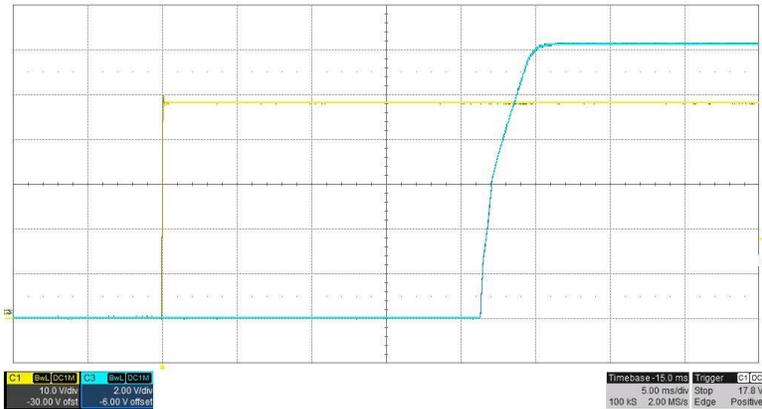
4A load, 5msec/div

CH1= Vin, 10V/div; CH2=Vout, 2V/div:



0A load, 5msec/div

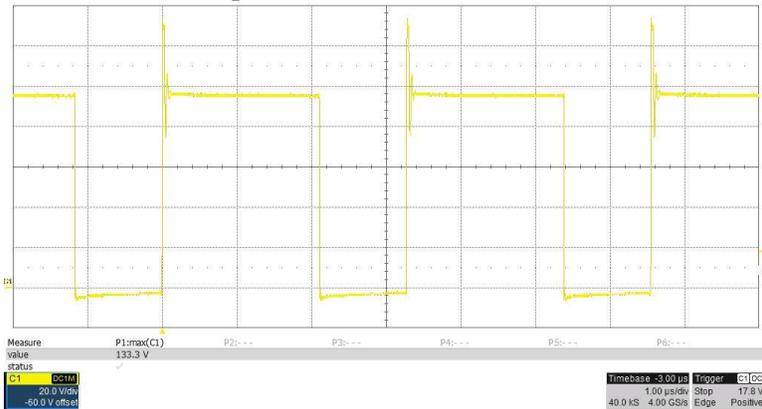
CH1= Vin, 10V/div; CH2=Vout, 2V/div:



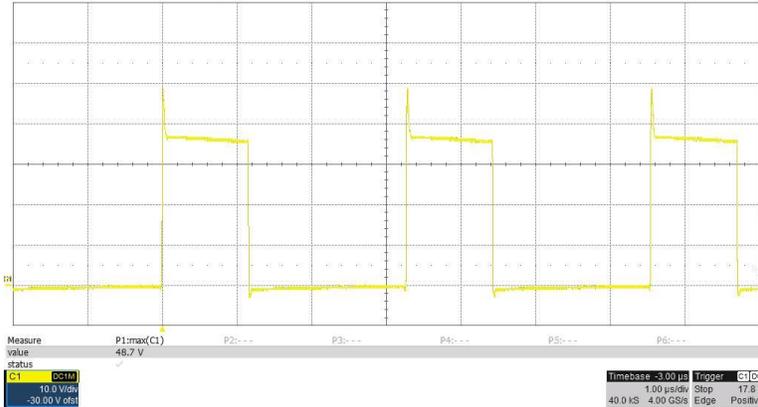
Waveforms

Vds, Q1, 20V/div, 1usec/div, 60Vdc input, 750MHz bandwidth

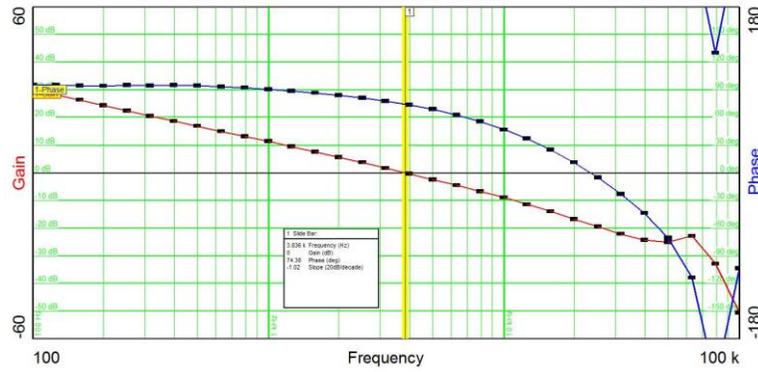
Measured 133.3Vpeak:



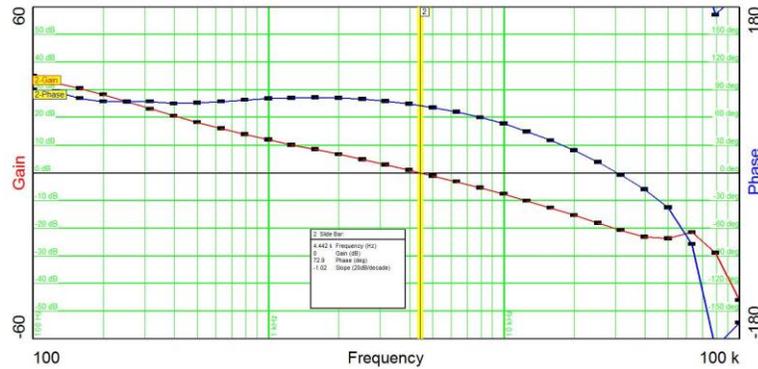
V_{ds}, Q3, 10V/div, 1usec/div, 60Vdc input, 750MHz bandwidth
 Measured 48.7Vpeak:



Loop Stability

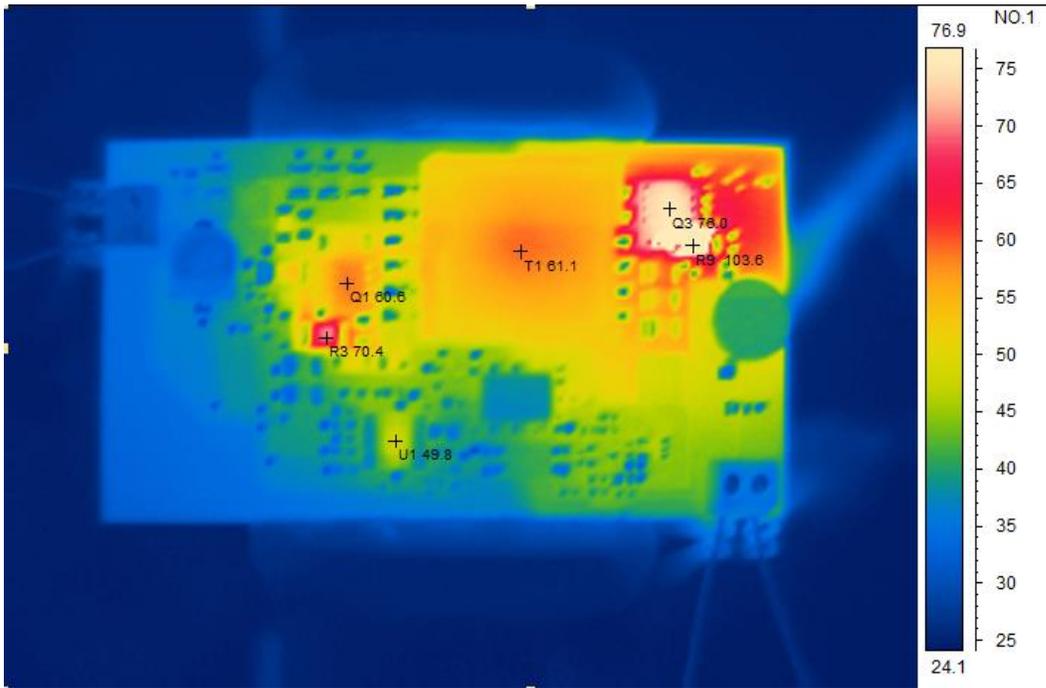


4A Load: Bandwidth= 3.8 kHz Phase Margin=74 degrees Gain Margin=18dB

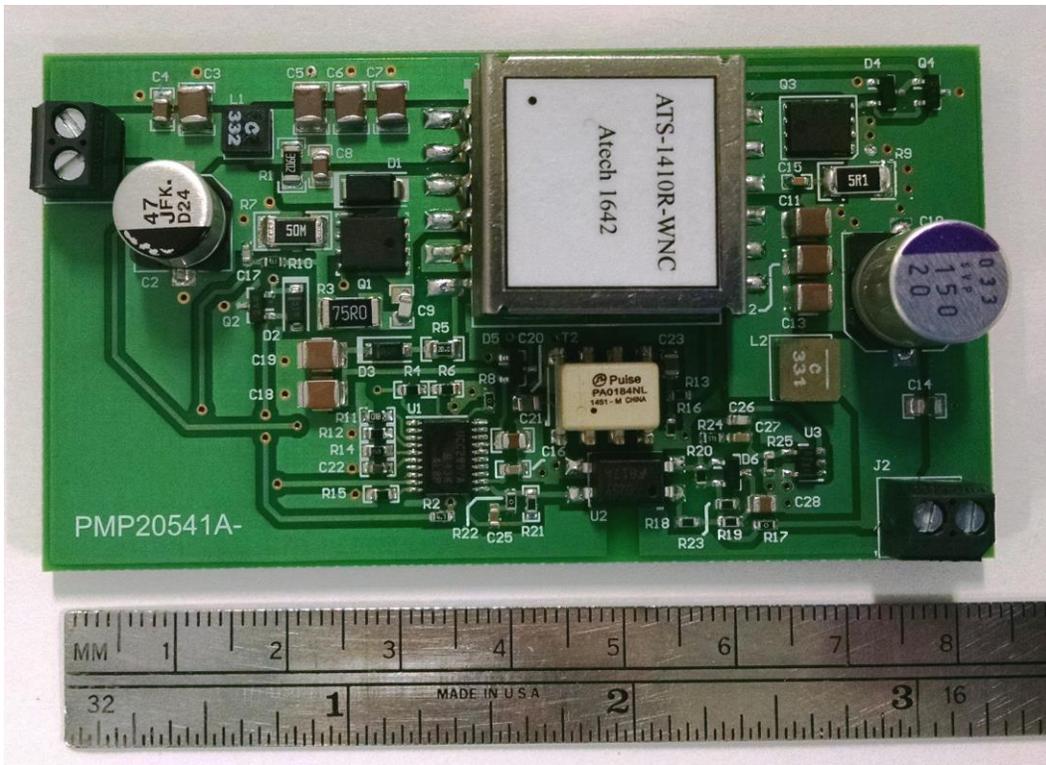


400mA Load: Bandwidth= 4.4 kHz Phase Margin=73 degrees Gain Margin=20dB

Thermal Plots



Photo



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