Design Guide: TIDA-010933

1.6-kW, Bidirectional Micro Inverter Based on GaN Reference Design

Description

This reference design implements a four-channel 1.6-kW single-phase bidirectional micro inverter based on GaN. The reference design supports four identical channels with up to 60 V and ±10 A on the DC side. These channels can be connected to photovoltaic (PV) panels or to 48-V Battery Energy Storage Systems (BESS). On the High-Voltage (HV) side, the reference design is connected to a single-phase AC grid. The reference design has Low-Voltage (LV) and HV sides isolated by means of a bidirectional fixed-frequency CLLLC converter. The control algorithm for the reference design is implemented in C2000™ MCU.

Features

- Four channels for PV or 48-V BESS connection
- High power density, up to 1 kW/L
- Bidirectional power flow capable and reactive power compensation
- Digital control implemented in single controller: TMS320F280039C
- Industrial temperature range (–40°C to +85°C)

Applications

- Micro inverter
- Power conversion system (PCS)

Resources

TIDA-010933	Design Folder
LMG2100R044, LMG3522R050	Product Folder
TMCS1123, AMC3330	Product Folder
AMC1311, ISO6741, UCC21540	Product Folder
TMDSCNCD280039C	Tool Folder

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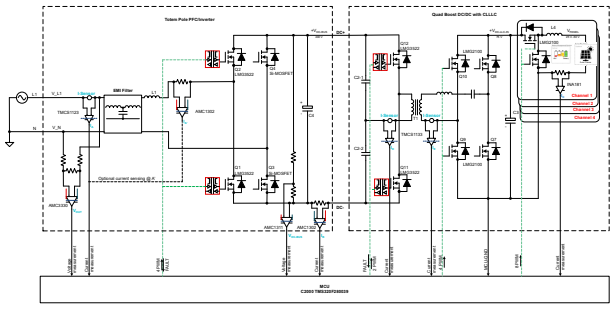
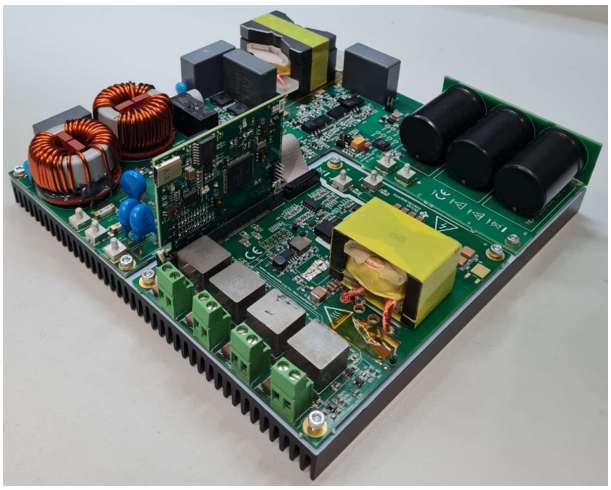




1 System Description

Energy sustainability and security are accelerating the demands for renewable energy as solar and energy storage systems. In residential use cases, micro inverters present a good trade-off in terms of costs and efficiency together with a simple end-user installation. Conversely, the energy storage system becomes a challenge in existing micro inverters due to the lack of a bidirectional converter in this end-equipment.

This reference design is intended to show a possible implementation of the 4-channel micro inverter with fully bidirectional power flow to combine PV input functionality with a 48-V BESS.

The design contains three main stages:

- PV or Battery input with DC/DC converter with individual MPPT functionality
- Isolated Capacitor-Inductor-Inductor-Inductor-Capacitor (CLLLC) converter
- Totem-pole DC/AC converter

Each stage is based on GaN technology to achieve high power density and efficiency.

The reference design is made with two boards split by functions.

The first board is called DC/DC board containing four input DC/DC converters and one isolated CLLLC converter. All the conversion stages in the board are based on top-cooled GaN devices from TI and are placed on the bottom side of the board. This enables dissipation of the power losses into the heat sink.

The second board is called DC/AC board and contains DC link electrolytic capacitors, a totem-pole DC/AC converter, pre-charging circuit and EMI filter. The high-frequency branch of the totem-pole DC/AC is based on top-cooled GaN devices from TI.

Both the boards are mounted above an aluminum heat sink which is connected by means of thermal interface materials to the GaN FETs. The heat sink in the design is supposed to work in static cooling condition and the size is 15 mm × 250 mm × 250 mm. Overall system dimension is 40 mm × 250 mm × 250 mm, thus leading to a volume of 1.6 liter. The calculated power density is equal to 1 kW/liter.

1.1 PV or Battery Input With DC/DC Converter

Each PV panel or battery connected to the micro inverter reference design can lead to different voltage across the inputs.

The design has four input stages, where each stage can independently operate as:

- DC/DC boost converter when transferring power from the input to the internal 75-V rail
- DC/DC buck converter when transferring power from the 75-V rail to the input

The stages control input voltage and current and can implement a Maximum Power Point Tracking (MPPT) algorithm for each PV panel. There are three possible use cases for each input:

- PV panel connection with individual MPPT
- Battery charging
- Battery discharging

Figure 1-1 illustrates the input channel block diagram.

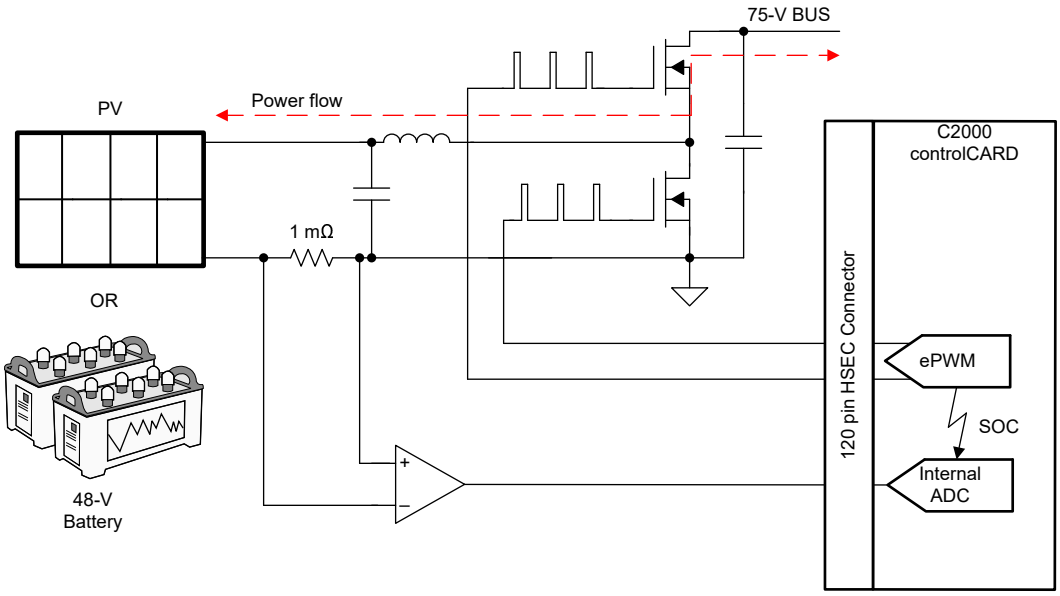


Figure 1-1. Input Channel Block Diagram

1.2 Isolation and CLLLC Converter

Micro inverters require isolation between PV panels and the AC grid because of a variety of reasons such as the following:

- Electrical safety
- Mitigation of common-mode currents flowing between the panels and the grid
- High input or output voltage ratio

From a safety point of view, PV panels can be touched by the end-user, thus isolation can mitigate the electrical shock hazard. The common-mode currents are a well-known challenge in PV applications due to PV surfaces exposed over grounded roofs or other surfaces in the proximity. This enormous quantity of surface leads to high parasitic capacitance between the panels and the ground (200 nF / kW). This parasitic capacitance can cause high common-mode current flowing into the system when common mode voltage of the converters is not mitigated enough. A common strategy to significantly reduce the parasitic currents flowing in the system is to add an isolation stage between the panels and the grid.

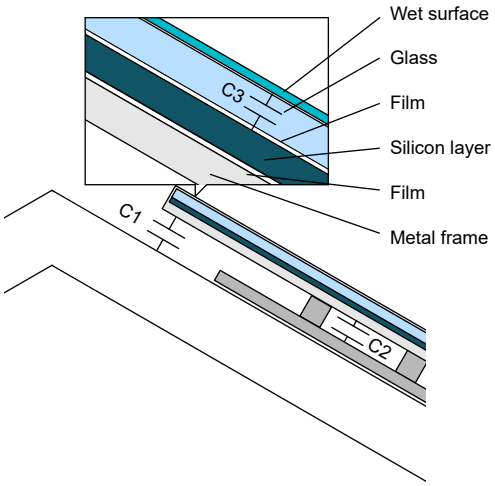


Figure 1-2. PV Panel Parasitic Capacitance

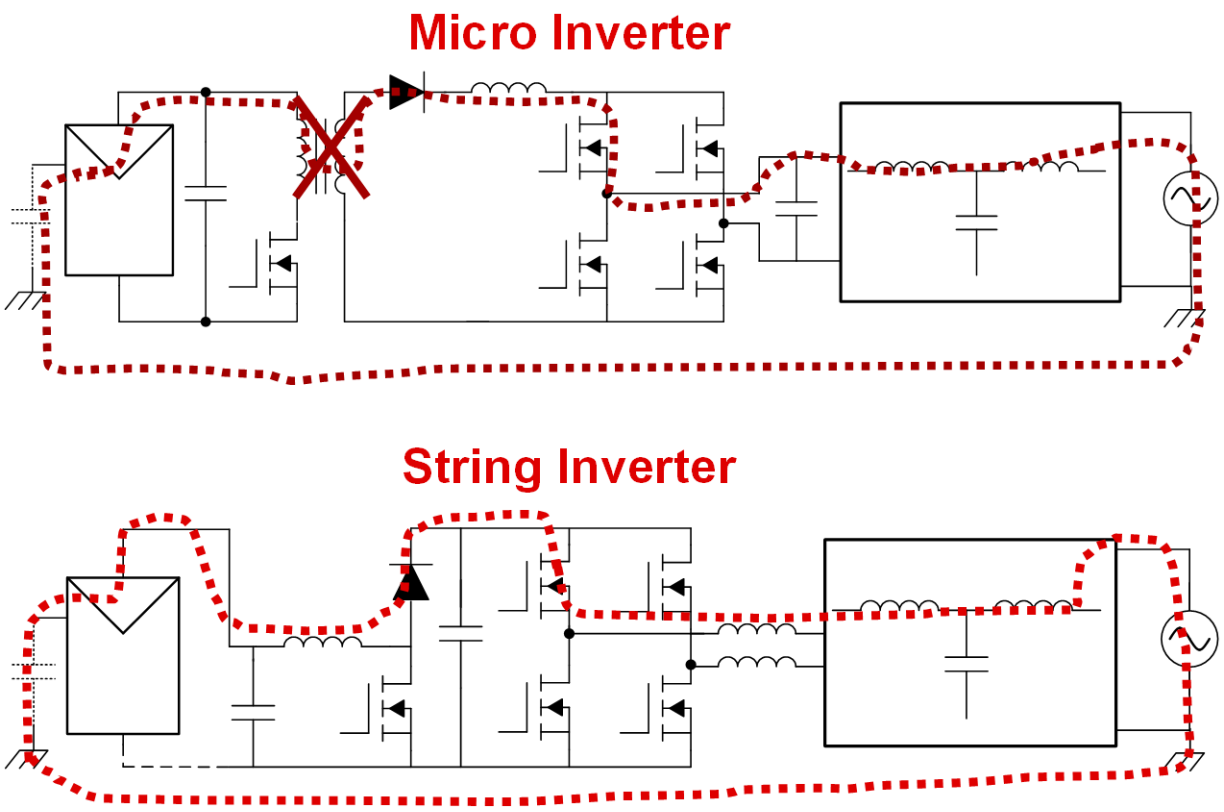


Figure 1-3. Blocking Common-Mode Noise

The third reason to use an isolated transformer is to efficiently convert power from 75 V to 400 V.

When converting from 75 V to 400 V, using non-isolated DC/DC, challenges like very short duty cycle and high losses in inductor and switches are found. To improve efficiency and thermal performance of the conversion stage, a transformer CLLLC was used.

The input and output voltage for the CLLLC converter is fixed and regulated by PV or battery inputs and DC/AC converter, respectively. This means that no voltage regulation is needed in this stage.

To address all these requirements, CLLLC topology with fixed-frequency was selected, thus leading to small magnetic size and high efficiency. This converter can be optimized to operate in the most favorable point and achieve Zero Voltage Switching (ZVS) in the entire load range.

To increase efficiency and provide bidirectional power flow, this design uses CLLLC topology with Synchronous Rectification (SR). When power flows from the LV to the HV, SR is implemented on the HV side. In reverse power flow, the excitation is on HV side and SR on the LV side.

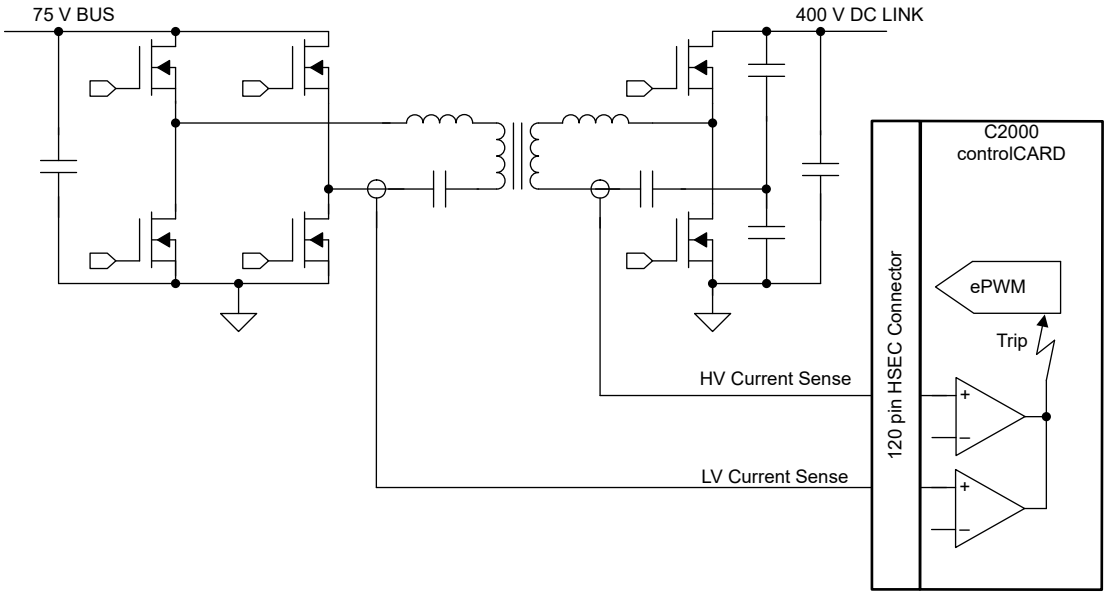


Figure 1-4. CLLLC Block Diagram

Driving the transformer in a CLLLC converter can be achieved with two possible configurations: full-bridge and half-bridge configurations. The full-bridge requires twice the amount of switches with respect to the half-bridge configuration. Conversely, half-bridge has 2 times more current with the same power level.

On the LV side current is higher, thus making the full-bridge converter the best option. The HV side has much higher voltage and lower current levels, thus making a half-bridge converter the optimum design.

1.3 DC/AC Converter

A totem-pole topology was selected in this micro inverter reference design. The totem-pole topology presents higher performance and lower cost with respect to other DC/AC topologies. A drawback of the totem-pole is the high-common mode noise with respect to other DC/AC topologies such as H-bridge, bipolar, or Highly Efficient and Reliable Inverter Concept (HERIC). Conversely, the isolation between panels and grid features significant reduction of the leakage current flowing from DC to AC. The totem pole is designed to operate in Continuous Conduction Mode (CCM). This allows for lower conduction losses and a better EMI picture versus Discontinuous Conduction Mode (DCM) because of lower peak-to-peak ripple current. Figure 1-5 shows a block diagram of this topology.

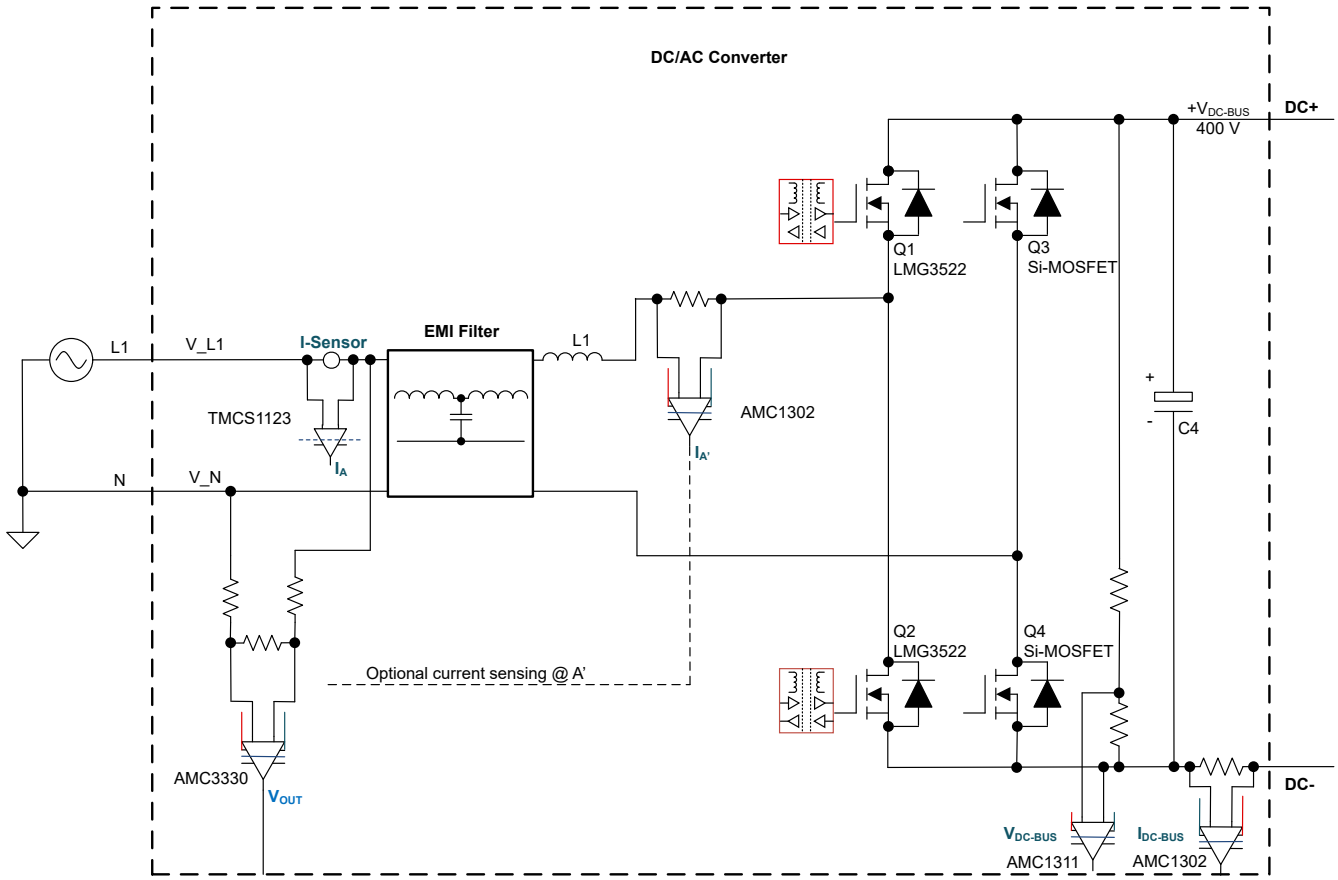


Figure 1-5. Totem-Pole DC/AC Block Diagram

In totem-pole DC/AC, there are two half-bridges. One is operating at high-frequency and another one at line frequency. The high-frequency switches are based on GaN technology to achieve 125-kHz switching frequency for sinusoidal grid current control.

Low-frequency switches are operating as a grid voltage rectifier. During the negative half-cycle switch Q4 is continuously on and Q3 is off, when the half-cycle is positive switch Q4 is off and switch Q3 is continuously on. Note that both of the half-bridges need to have a dead-time to avoid shoot-through.

The current in the grid is measured and then controlled by the MCU using Proportional Resonant (PR) controllers. High-accuracy measurement of the current flowing in the Point of Common Coupling (PCC) is required to control active and reactive power. The current control requires the implementation of a Phase Locked Loop (PLL) which is synchronized with the grid voltage. A DC link voltage control loop is used to control the amplitude of the active current sink or source from the grid.

1.4 Key System Specifications

Table 1-1 shows key specifications of the reference design.

Table 1-1. Key System Specifications

PARAMETER	SPECIFICATION	COMMENT
Input DC voltage range	30 V to 60 V	
Maximum input DC current	10 A	Limited by input inductor saturation current
DC/DC Boost converter switching frequency	250 kHz	
Number of input channels	4	
CLLLC switching frequency	500 kHz	

Table 1-1. Key System Specifications (continued)

PARAMETER	SPECIFICATION	COMMENT
Nominal output voltage	400 V	Output voltage is not regulated without the DC/AC board. Use with the DC/AC board or clamp output voltage with DC load.
Maximum output current	4 A	
Nominal Output AC voltage	230 VAC	LMG3522R030 required for 120-VAC operation
Output AC current	7 A	
DC/AC stage switching frequency	125 kHz	

CAUTION

Do not leave the design powered when unattended.

WARNING

High voltage! *Accessible high voltages are present on the board*. Electric shock is possible. The board operates at voltages and currents that can cause shock, fire, or injury if not properly handled. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property. For safety, use of isolated test equipment with overvoltage and overcurrent protection is highly recommended.

TI considers it the user's responsibility to confirm that the voltages and isolation requirements are identified and understood before energizing the board or simulation. *When energized, do not touch the design or components connected to the design*.

WARNING

Hot surface! Contact can cause burns. Do not touch!

Some components can reach high temperatures > 55°C when the board is powered on. Do not touch the board at any point during operation or immediately after operating, as high temperatures can be present.

WARNING

TI intends this reference design to be operated in a ***lab environment only and does not consider the design as a finished product*** for general consumer use. The design is intended to be run at ambient room temperature and is not tested for operation under other ambient temperatures.

TI intends this reference design to be used only by ***qualified engineers and technicians*** familiar with risks associated with handling high-voltage electrical and mechanical components, systems, and subsystems.

There are ***accessible high voltages present on the board***. The board operates at voltages and currents that can cause shock, fire, or injury if not properly handled or applied. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property.

2 System Design Theory

2.1 Boost Converter Design

The inductor is the most important component in power regulator design. There are three important inductor specifications: inductor value, saturation current, and DC resistance (DCR).

In a boost regulator, the inductor DC current can be calculated by Equation 1.

$$I_{L(DC)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (1)$$

where

- V_{OUT} is the output voltage of the boost converter
- I_{OUT} is the output current of the boost converter
- V_{IN} is the input voltage of the boost converter
- η is the power conversion efficiency, use 90% for most applications

The inductor ripple current is calculated using Equation 2.

$$\Delta I_{L(P-P)} = \frac{V_{IN} \times D}{L \times f_{SW}} \quad (2)$$

where

- D is the duty cycle
- L is the inductance value of the inductor
- f_{SW} is the switching frequency
- V_{IN} is the input voltage of the boost converter

Therefore, the inductor peak current is calculated with Equation 3.

$$I_{L(P)} = I_{L(DC)} + \frac{\Delta I_{L(P-P)}}{2} \quad (3)$$

Normally, it is advisable to work with an inductor peak-to-peak current of less than 40% of the average inductor current for maximum output current. A smaller ripple from a larger valued inductor reduces the magnetic hysteresis losses in the inductor and EMI. But in the same way, load transient response time is increased. The saturation current of the inductor must be higher than the calculated peak inductor current.

2.2 MPPT Operation

The power output from a PV panel depends on a few parameters, such as the irradiation received by the panel, panel voltage, panel temperature, and so forth. The power output also varies continuously throughout the day as the conditions affecting the change.

Figure 2-1 shows the I-V curve and the P-V curve of a solar panel. The I-V curve represents the relationship between the panel output current and the output voltage. As the I-V curve in the figure shows, the panel current is at the maximum when the terminals are shorted and is at the lowest when the terminals are open and unloaded.

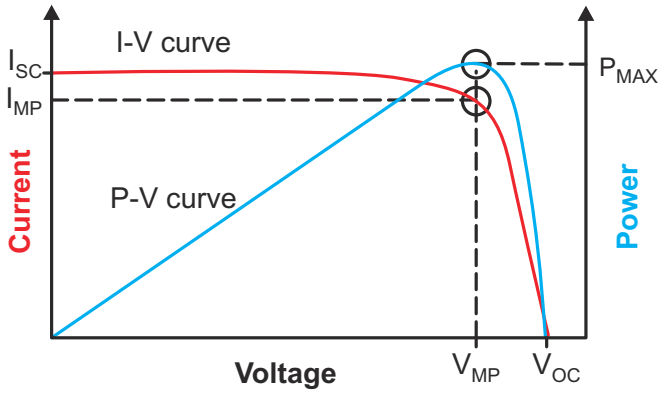


Figure 2-1. Solar Panel Characteristics I-V and P-V Curves

As shown, the maximum power obtained from the panel represented as P_{MAX} at a point when the product of the panel voltage and the panel current is at the maximum. This point is designated as the maximum power point (MPP).

The graphs below show examples of how each of the various parameters affect the output power from the solar panel. The graphs also show the variation in the power output of a solar panel as a function of irradiance. Observe in these graphs how the power output from a solar panel increases with the increase in irradiance and decreases with a decrease in irradiance. Also note that the panel voltage at which the MPP occurs also shifts with the change in irradiance.

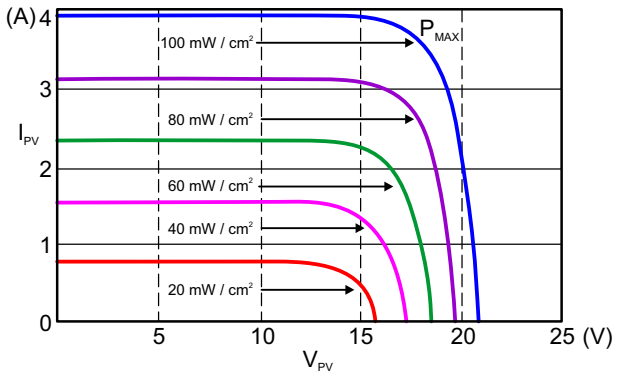


Figure 2-2. Solar Panel Output Power Variation Under Different Irradiation Conditions—Graph A

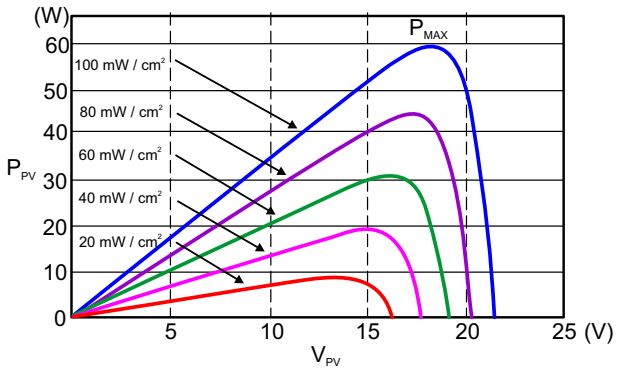


Figure 2-3. Solar Panel Output Power Variation Under Different Irradiation Conditions—Graph B

The challenge of automatically identifying the MPP of the panel is typically performed by employing MPPT algorithms in the system. The MPPT algorithm tries to operate the photovoltaic panel at the maximum power point and uses a switching power stage to supply the load with the power extracted from the panel.

Perturb and Observe (PO) is one of the most popular MPPT algorithms used. The fundamental principle behind this algorithm is simple and easy to implement in a microcontroller based system. The process involves slightly increasing or decreasing (perturbing) the operating voltage of a panel. Perturbing the panel voltage is accomplished by changing the duty cycle of the converter. Assuming that the panel voltage has been slightly increased and that this leads to an increase in the panel power, then another perturbation in the same direction is performed. If the increase in the panel voltage decreases the panel power, then a perturbation in the negative direction is done to slightly lower the panel voltage.

By performing the perturbations and observing the power output, the system begins to operate close to the MPP of the panel with slight oscillations around the MPP. The size of the perturbations determines how close the system is operating to the MPP. Occasionally this algorithm can become stuck in the local maxima instead of the global maxima, but this problem can be solved with minor tweaks to the algorithm.

The PO algorithm is easy to implement and effective, and was chosen for this design.

2.3 CLLLC Converter Design

In a CLLLC converter, a proper design of the resonant tank and transformer is needed to achieve high efficiency. The second goal is to have enough voltage gain over switching frequency range. In this CLLLC, input and output voltages are constant. This means that CLLLC converter can operate on fixed resonant frequency and achieve the lowest possible losses.

In resonant converters, the resonant tank is designed to have enough gain to cover full input and output voltages range. At the same time, design the tank to have inductive current in all load and frequency ranges. A more detailed procedure of designing resonant converters is available in *Designing an LLC Resonant Half-Bridge Power Converter*.

2.3.1 Achieving Zero Voltage Switching (ZVS)

Transformers for resonant converters need to be designed to have enough magnetizing current to discharge output capacitance of the switches on both the sides. There are two conditions to be met. Make the energy stored in magnetizing and resonant inductors bigger than energy stored in output capacitance of switches on both sides. Also, the magnetizing current needs to be big enough to discharge capacitance of switches within a given dead time.

$$\frac{(L_M + L_R) \times I_{M\_PEAK}^2}{2} \geq \frac{C_{EQ} \times V_{IN}^2}{2} \tag{4}$$

where

- I_{M_PEAK} is maximum peak current in transformer
- L_M is the magnetizing inductance of the transformer
- L_R is the resonant tank inductance
- V_{IN} is the input voltage of the CLLLC converter
- C_{EQ} is the equivalent capacitance of the switching node

$$L_M \leq \frac{T_{DT}}{4 \times C_{EQ} \times f_{sw}} \tag{5}$$

where

- T_{DT} is the duration of the dead time
- C_{EQ} is the equivalent capacitance of the switching node
- L_M is the magnetizing inductance of the transformer
- f_{SW} is the switching frequency of the CLLLC converter

The first condition (Equation 4) is the energy requirement and the second condition (Equation 5) is the slew rate requirement.

The peak magnetizing current is a half of the peak-to-peak value of magnetizing current.

$$I_{M_{PEAK}} = \frac{V}{4 \times (L_M + L_R) \times f_{sw}} \tag{6}$$

The equivalent capacitance is the sum of capacitance on the LV side plus capacitance of the HV side reflected to the LV side:

$$C_{EQ} = C_P + C_S' \tag{7}$$

where

- C_{EQ} is the equivalent capacitance of the switching node
- C_P is the capacitance of primary side switches
- C'_S is the capacitance of secondary side switches reflected to primary side

The reflected capacitance C'$_S$ can be calculated using transformer ratio:

$$C'_S = C_S \times \left(\frac{N_S}{N_P}\right)^2 \quad (8)$$

where

- C_S is the capacitance of secondary side switches
- N_S is the number of turns of the secondary winding
- N_P is the number of turns of the primary winding

The output capacitance of switches limit the maximum magnetizing inductance. Select switches as a trade-off between $R_{DS(on)}$ and C_{OSS}.

2.3.2 Resonant Tank Design

For resonant converters, the resonant tank needs to be designed to have enough voltage gain over frequency and load ranges. In a fixed frequency converter that operates at the resonant frequency, the gain is unity and not dependent from the load. This converter uses leakage inductance of the transformer as a resonant inductor, thus reducing system losses.

To design a resonant tank in a fixed frequency converter, the resonant frequency of the tank needs to match the switching frequency. The series resonant frequency can be calculated with the following formula.

$$f_0 = \frac{1}{2 \times \pi \times \sqrt{L_R \times C_R}} \quad (9)$$

With the given resonant inductance, the required series capacitance can be calculated using the following equation:

$$C_R = \frac{1}{4 \times \pi^2 \times f_0^2 \times L_R} \quad (10)$$

The resonant tank on the secondary side can be calculated by reflecting the resonant components to the HV side. The HV side leakage inductance is determined with the following equation:

$$L_{KS} = \frac{L_{KP}}{\left(\frac{N_S}{N_P}\right)^2} \quad (11)$$

The secondary side resonant capacitance is found with Equation 12:

$$C_{RS} = C_{RP} \times \left(\frac{N_S}{N_P}\right)^2 \quad (12)$$

2.4 DC/AC Converter Design

The inductor plays an important role in system efficiency, current ripple, and overall size. The inductance value is calculated based on the input voltage, output voltage, and worst-case ripple. The inductance value of a totem-pole DC/AC can be calculated with Equation 13:

$$L \geq \frac{D \times (1 - D)}{\Delta I_{pk-pk} \times f_{sw}} \times V_{OUT} \quad (13)$$

where

- D is the duty cycle
- f_{SW} is the switching frequency
- V_{OUT} is the DC link voltage
- I_{pk-pk} was calculated as shown in Equation 14

$$I_{pk-pk} = \frac{K_{ripple} \times P_{nom}}{V_{OUT}} \quad (14)$$

Worst-case current ripple is when the duty cycle is equal to 50%

DC link capacitor voltage ripple frequency is double the line frequency. The required DC link capacitance can be calculated as shown in Equation 15:

$$C_{OUT} \geq \frac{P_{OUT}}{2 \times V_{OUT} \times \pi \times f_{line} \times V_{ripple}} \quad (15)$$

where

- V_{OUT} is the DC link nominal voltage
- F_{line} is the frequency of the grid
- P_{OUT} is the maximum power
- V_{ripple} is the peak to peak voltage ripple.

3 System Overview

3.1 Block Diagram

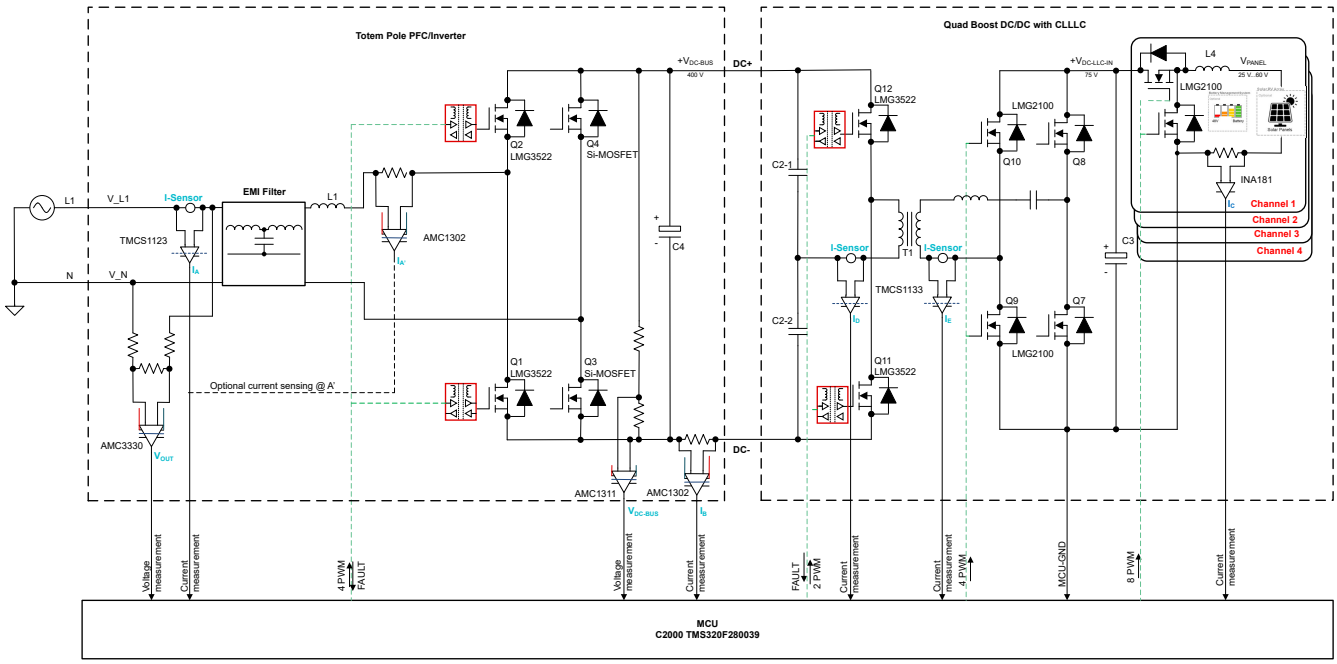


Figure 3-1. TIDA-010933 Block Diagram

3.2 Design Considerations

3.2.1 DC/DC Converter

The first stage of this reference design is the LV non-isolated DC/DC converter. The design has four identical channels having one common output rail. By boost converter nature, the output voltage during operation needs to be higher than input voltage. The voltage of the majority of PV panels are in 30- to 50-V range, a fully charged 48-V battery has 55 V to 60 V, so for a common bus the 75-V nominal voltage was chosen.

PARAMETERS	VALUES
Input voltage	30 V to 60 V
Output voltage	75 V
Input current	10 A
Input power	400 W
Efficiency	> 99 %

In this reference design, the DC/DC converter was designed to keep CCM mostly in all the voltage and current conditions. CCM operation can help to achieve high efficiency on medium and high loads and a better EMI footprint. However, for light loads CCM mode has lower efficiency due to higher conduction and core losses. On very light loads, the converter operates in Discontinuous Conduction Mode (DCM).

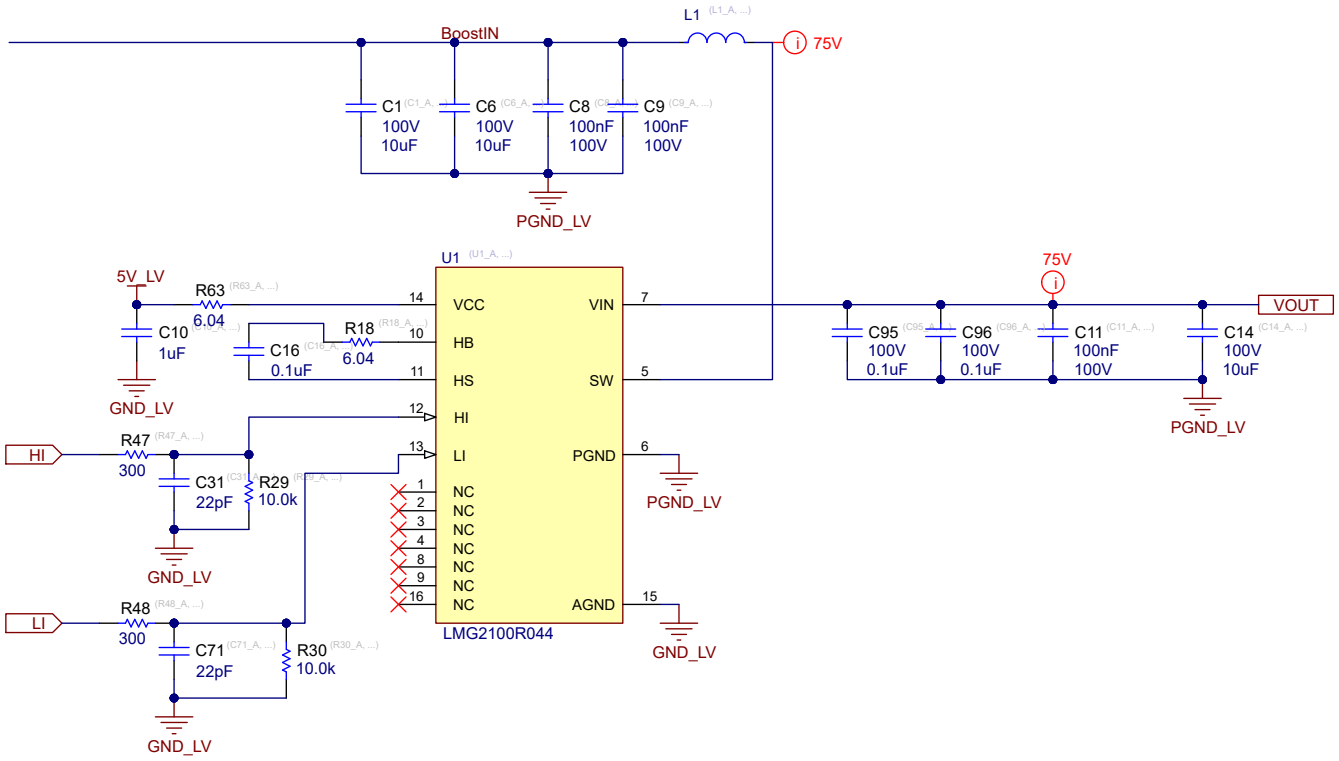


Figure 3-2. DC/DC Converter

LMG2100R044 is used for this stage. This device has high integration level and can be controlled by digital lines coming from the MCU. Simple filters are placed for noise rejection. High quality input and output ceramic capacitors are required to handle current ripple. LMG2100R044 has a very high switching performance and parasitic inductance and power loop is important. Special layout was used to reduce the effect of parasitic inductance, thus reducing voltage spike at the switching node. High-frequency ceramic capacitors are placed next to the VIN pin and the return path is routed on the next inner layer. This routing has a very small loop area in PCB layers and leads to small parasitic inductance. Two capacitors in parallel help to reduce Equivalent Series Inductance (ESL) by a factor of two. Layout of the LMG2100R044 is shown in Figure 3-3.

In Figure 3-3, the return path for current is on the inner layer (cyan) for low parasitic inductance.

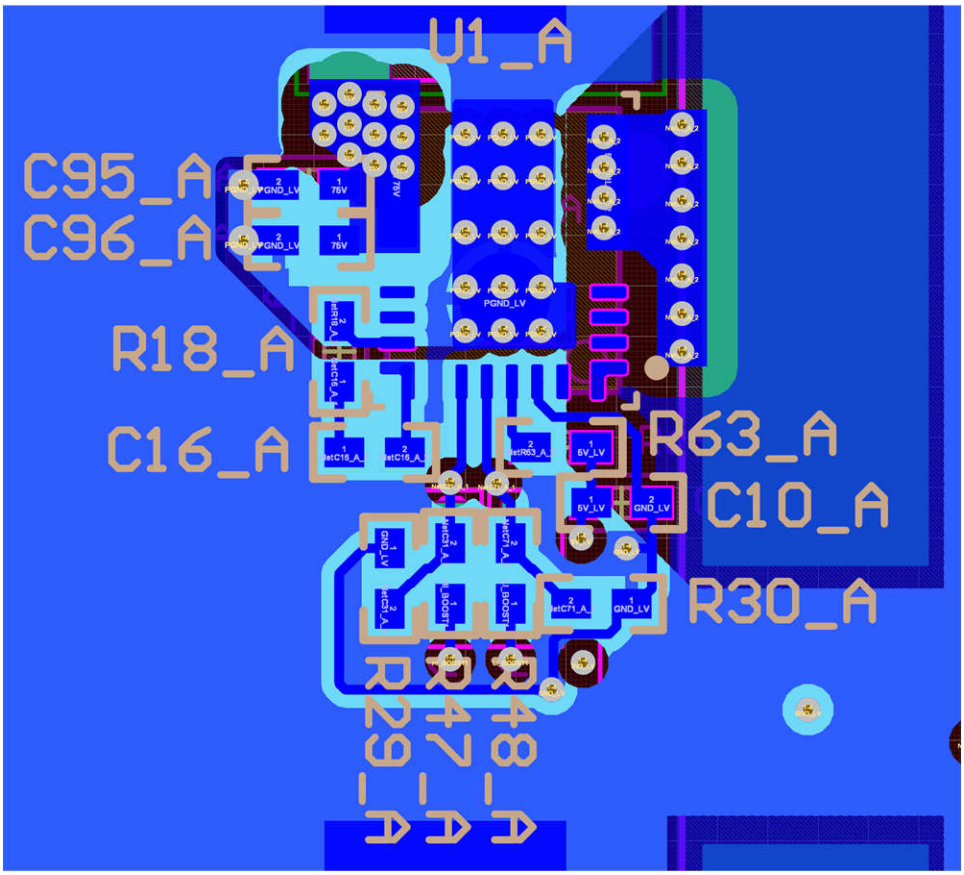


Figure 3-3. LMG2100R044 Layout

3.2.1.1 Input Current and Voltage Senses and MPPT

The PV panel requires a special control of the voltage and current to achieve maximum power (MPPT). MPPT is described in Section 2.2.

To enable MPPT operation, the design has voltage and current measurements of each input channel. Input channels are placed in the same potential as the MCU and do not need to be isolated. This enables the use of cost competitive non-isolated shunt-based current-sensing design based on the INA181 amplifier. INA181 is a bidirectional voltage output current-sense amplifier. The device has reference voltage input that is used to measure negative current during battery charging. INA181A3 has an internal gain set up to 100 V/V and a bandwidth of 150 kHz.

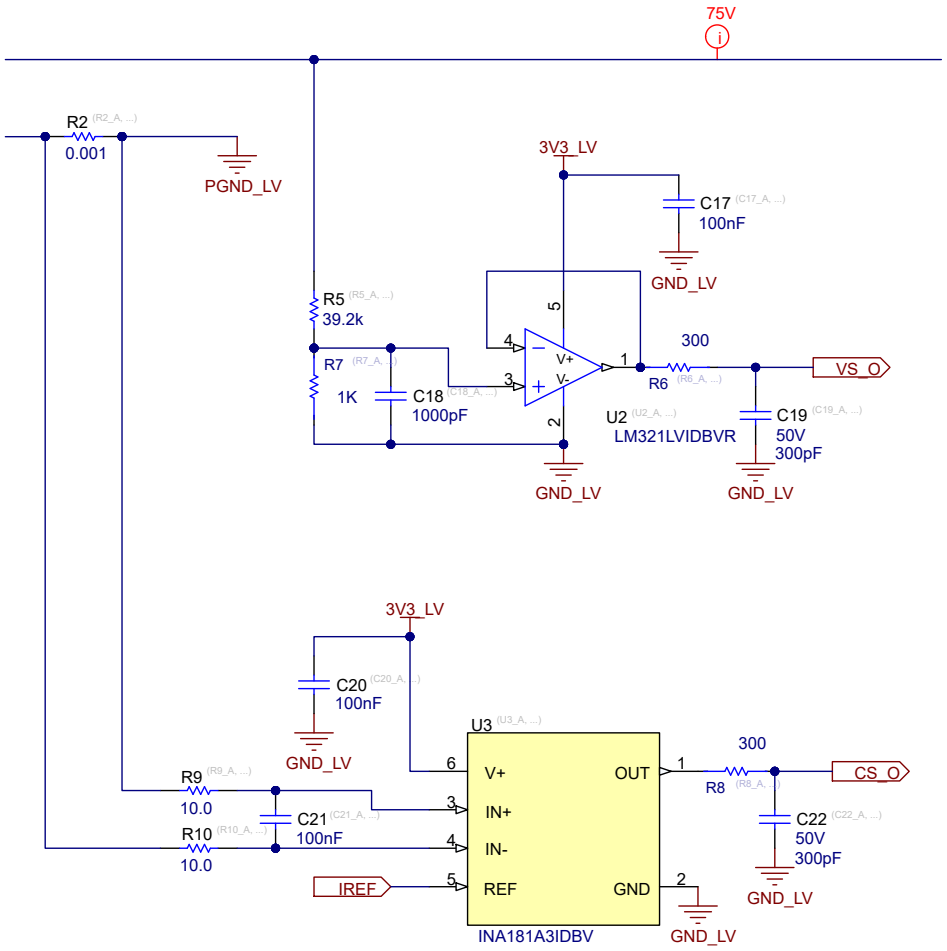


Figure 3-4. Input Current and Current Sensing

Voltage sense is implemented with a resistive divider and the low-voltage general purpose operation amplifier LM321LV configured as a voltage follower. The voltage follower circuit needs to decrease impedance of the sense line, increase noise immunity, and mitigate error from ADC input impedance.

3.2.1.2 Inrush Current Limit

Input channels can be connected to PV panels and to a 48-V battery. With the PV panel acting as current source, an inrush current is usually not a concern. However, batteries are acting as a very low-impedance voltage source. This means that inrush current can be high and can damage the board.

To limit the current, the following inrush current-limiting circuit was implemented:

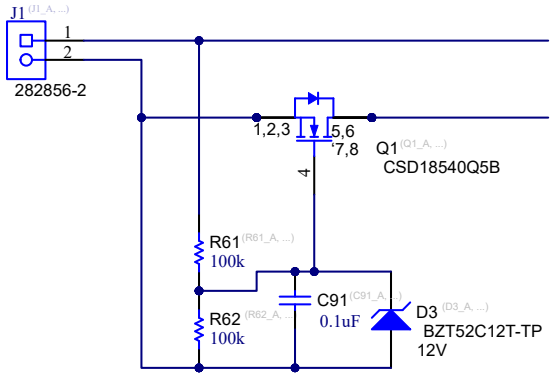


Figure 3-5. Input Inrush Current Limit

When the battery is connected to the input channel - the Q1 MOSFET is turned off. The battery slowly charges the gate of the MOSFET through R61. A Zener diode D3 is used to protect the gate of the MOSFET.

3.2.2 CLLLC Converter

For this CLLLC converter, a transformer with a turn ratio of 4:11 and leakage inductance of 140 nH is used. The HV side has switching stage in half-bridge configuration with voltage doubler. All switches are based on GaN technology on both LV and HV sides.

To achieve ZVS, the effective parasitic capacitance was derived to calculate the needed magnetizing inductance. The parasitic capacitance of both sides (HV and LV) need to be considered.

The parasitic equivalent capacitance was calculated using the equation from Section 2.3.1:

$$C_s' = (2 \times 0.26\ \text{nF}) \times \left(\frac{11}{4}\right)^2 = 3.9\ \text{nF} \quad (16)$$

$$C_{EQ} = (4 \times 0.501\ \text{nF}) + 3.9\ \text{nF} = 5.9\ \text{nF} \quad (17)$$

Based on Equation 5, the maximum L_M is 8.5 µH for 100-ns dead time. In this design L_M = 6 µH was selected (Bourns 145449, D6735).

An additional energy check is required to provide ZVS. Energy stored in the calculated inductance needs to be higher than the energy stored in the C_{OSS}.

$$I_{M_{PEAK}} = \frac{75}{4 \times (6\ \mu\text{H} + 0.14\ \mu\text{H}) \times 500\ \text{kHz}} = 6.1\ \text{A} \quad (18)$$

$$\frac{(6\ \mu\text{H} + 0.14\ \mu\text{H}) \times (6.1\ A)^2}{2} \geq \frac{5.9\ nF \times 75^2}{2} \quad (19)$$

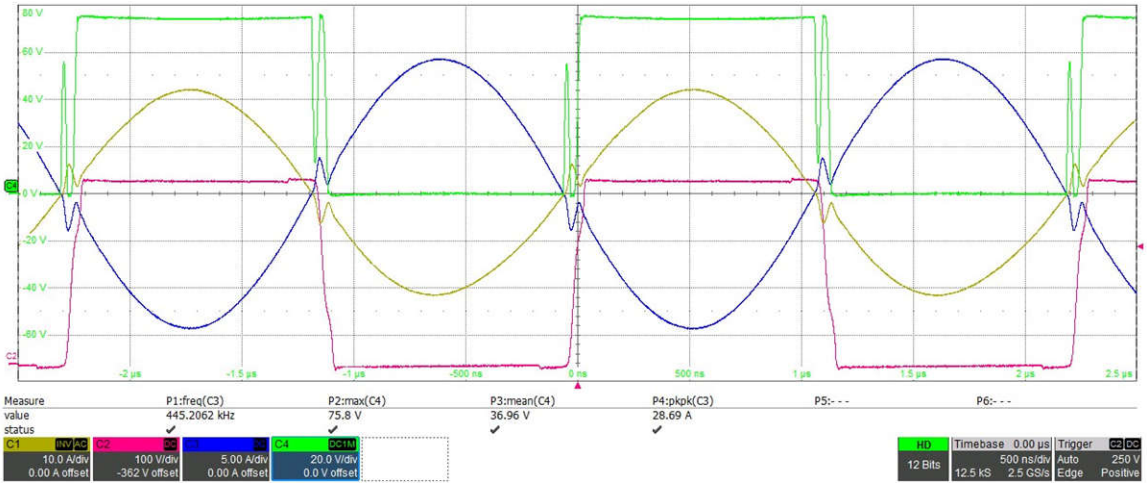
$$114\ \mu\text{J} \geq 16.6\ \mu\text{J} \quad (20)$$

Observe that the maximum magnetizing inductance is limited by a slew-rate requirement and not by an energy requirement.

This is a fixed frequency converter providing unit gain if operating at the resonance frequency. In this design, the leakage inductor of the transformer is 140 nH. A resonant capacitance of 660 nF was selected. The series resonant frequency can be calculated with Equation 9.

The resulting resonant frequency of the resonant tank is 523.6 kHz, which is very close to the desired value 500 kHz. To avoid parasitic effects, the converter is supposed to operate with a frequency slightly lower than the resonant one.

Figure 3-6 shows waveforms of the designed CLLLC converter transferring power from the LV to HV side. Ringing on the LV switching node is caused by parasitic current between the primary and secondary side. To reduce this ringing, increase the value of the resonant inductor.



C1 -LV side current, C2 - HV side SW node voltage, C3 - HV side current, C4 - LV side SW node voltage

Figure 3-6. CLLLC Converter Waveforms

3.2.2.1 Low-Voltage Side

The LV side of the CLLLC converter is designed in full-bridge configuration. The full-bridge requires twice as many switches as the half-bridge.

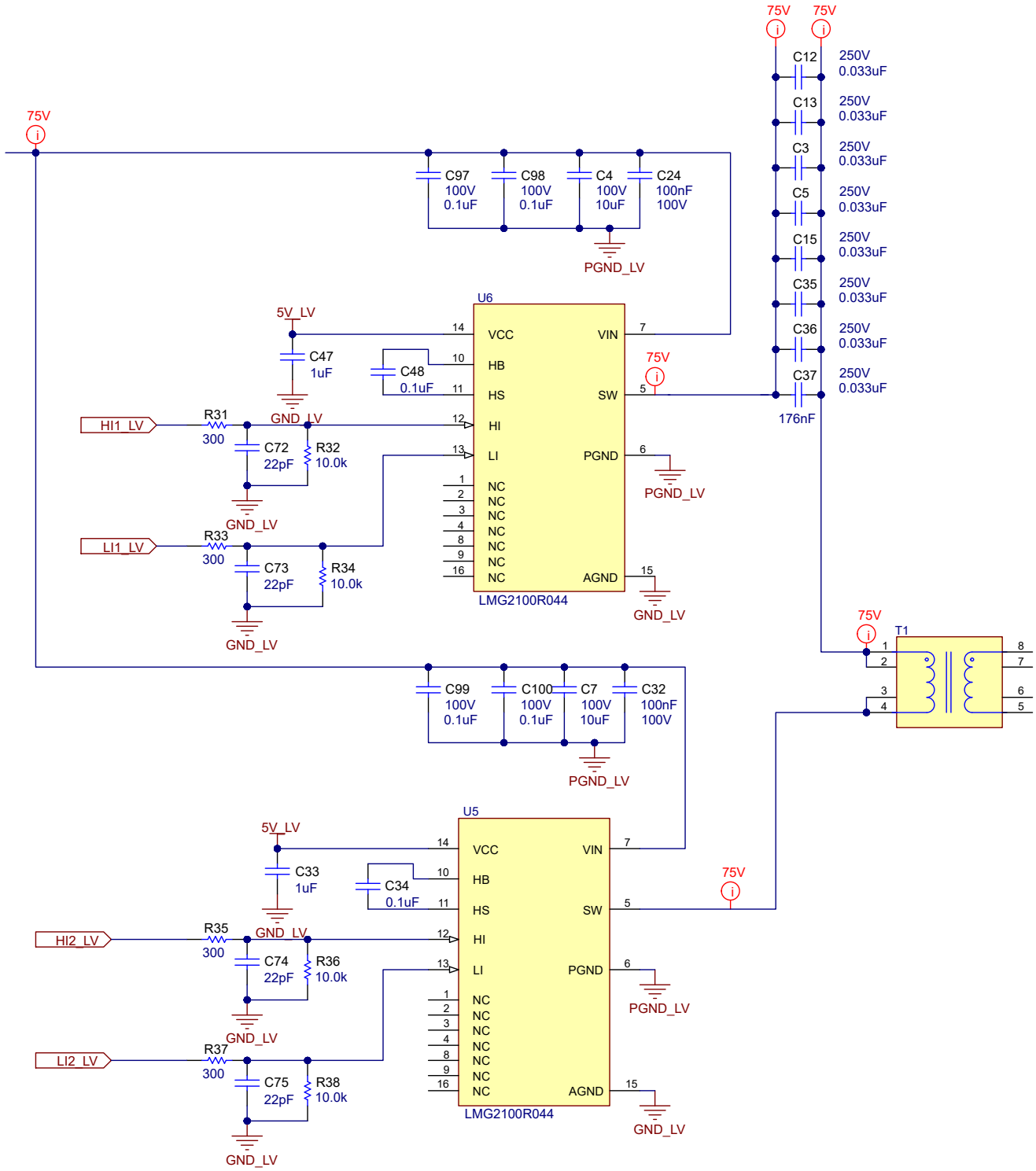


Figure 3-7. LV Side of CLLLC Converter

LMG2100R044 is used for this stage due to low0output capacitance and good switching performance. The device is supposed to work in soft switching and has no significant turn-on losses.

Resonant capacitors experience high RMS current and need to have small Equivalent Series Resistance (ESR). Also these capacitors are part of the resonant tank and need to have stable characteristics. For the resonant tank, high performance NP0 dielectric type capacitors were used.

3.2.2.2 High-Voltage Side

The HV side uses two LMG3522R050 devices in half-bridge configuration combined with a voltage doubler circuit. These switches are placed on the HV side and require isolation from the MCU. The signal isolation is based on digital isolators ISO6741. The power supply isolation is based on the SN6505 push-pull transformer driver.

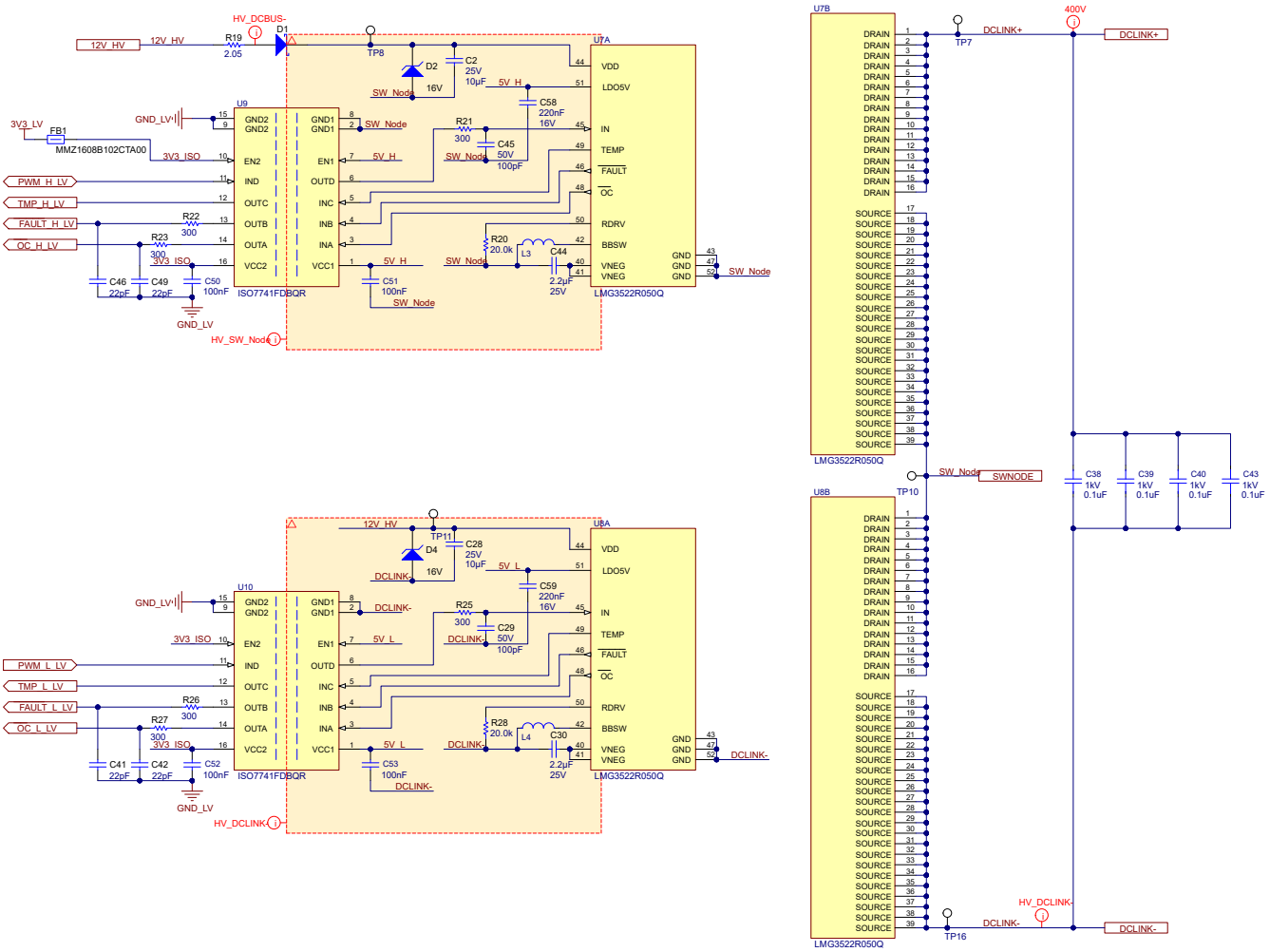


Figure 3-8. HV Side of CLLLC Converter

3.2.3 DC/AC Converter

3.2.3.1 Active Components Selection

Two GaN FET designs were identified for the DC/AC stage:

- 50-mΩ $R_{DS(on)}$ (LMG3522R050)
- 30-mΩ $R_{DS(on)}$ (LMG3522R030)

Both the devices are top-side cooled, thus allowing higher power dissipation performance with respect to bottom-side cooled devices. By means of PLECs simulations, a 50-mΩ device was identified as a fit for a 230-VAC grid. Efficiency is higher because LMG3522R050 has lower output parasitic capacitance compared to LMG3522R030. For a 120-VAC grid variant, LMG3522R030 is the better choice.

3.2.3.1.1 High-Frequency FETs: GaN FETs

LMG3522R050 with top-side cooling design was used. This GaN FET has integrated protections and drivers. The gate drive speed can be configured by an external resistor. In the current setup, the switching speed is 80 kV / µs. The control signal is isolated from the MCU with digital isolator ISO6741. LMG3522R050 has junction temperature reporting. This temperature signal is isolated by using the same digital isolator. The temperature information can be used in the control MCU to thermally protect the converter when ambient temperature is high.

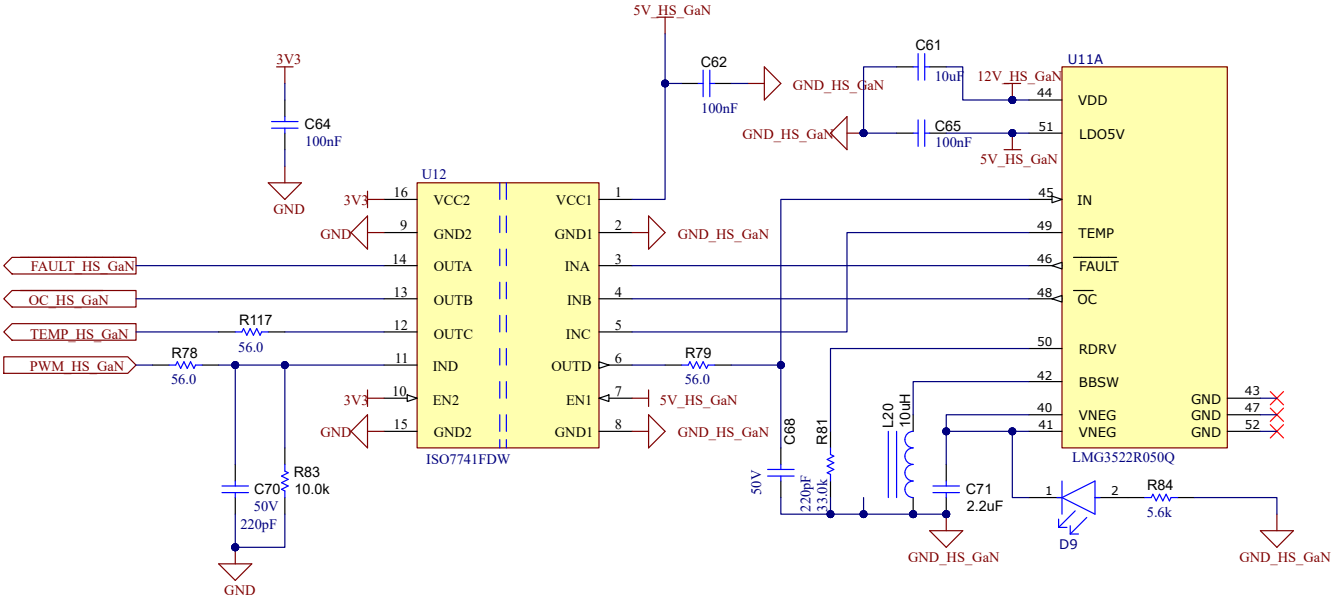


Figure 3-9. GaN FETs

3.2.3.1.2 Isolated Power Supply

Isolated power supplies for the GaNs, LF FETs, and isolated amplifiers were generated with SN6505x. A voltage double-circuit configuration was selected to generate 12 V from the 5 V. Figure 3-10 shows the isolated power supply schematic.

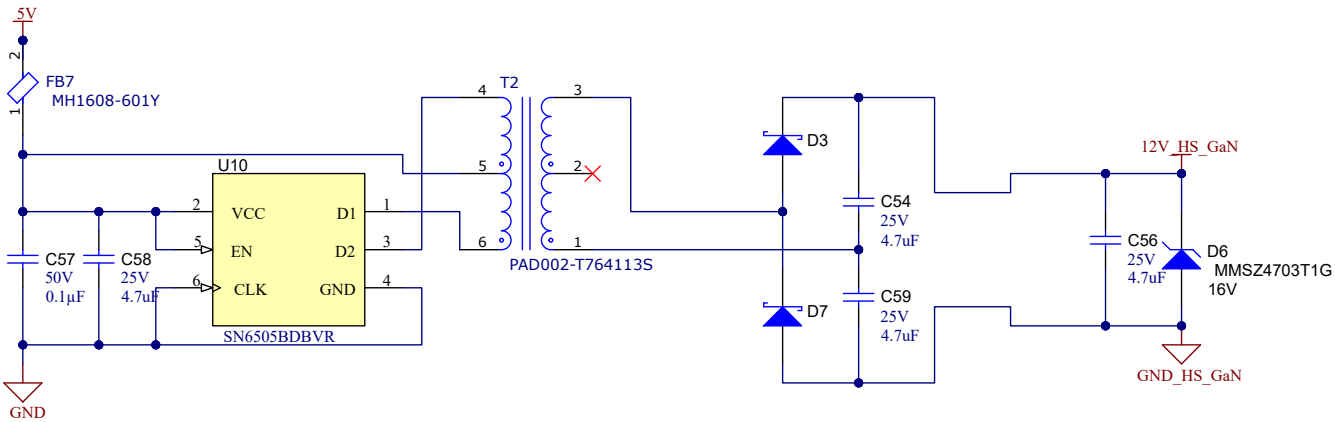


Figure 3-10. Isolated Power Supply

3.2.3.1.3 Low-Frequency FETs

For low-frequency commutation switches, super-junction Si MOSFETs with 22-mΩ $R_{DS(on)}$ were selected. An isolated dual-channel gate driver (UCC21540DW) was selected to drive these MOSFETs. The UCC21540DW device provides reinforced isolation between the MCU and the power MOSFETs. In this design, a dead time of 100 ns was programmed with 10 kΩ (R87).

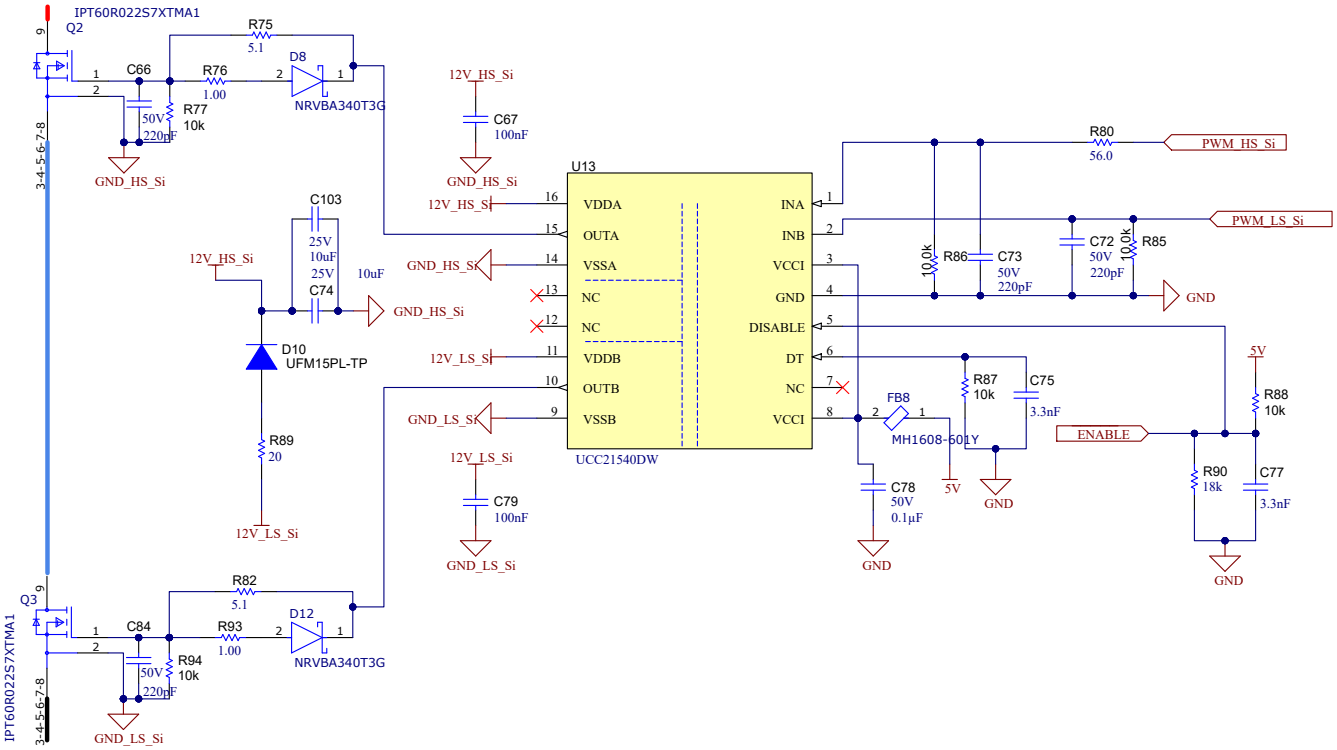


Figure 3-11. Low-Frequency FETs

3.2.3.2 Passive Components Selection

As Figure 3-12 shows, multiple passive components are present in the DC/AC stage. As follows, the design theory of each of the passive components is given in Section 2.4. The EMI filter is composed of a boost inductor, two common-mode chokes, and Cx and Cy capacitors.

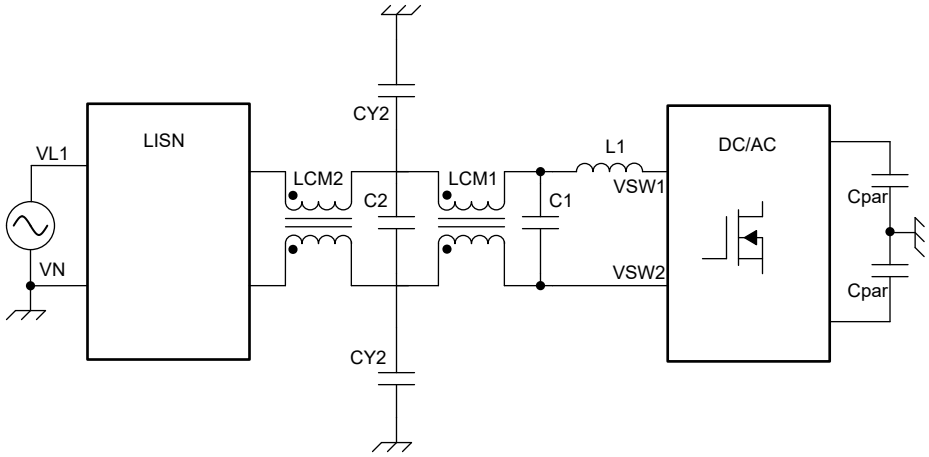


Figure 3-12. Block Diagram DC/AC Filter

3.2.3.2.1 Boost Inductor Selection

The mission mask for many standards starts at 150 kHz; therefore, selecting a switching frequency below 150 kHz is good design practice. In this design, a switching frequency of 125 kHz was selected for the totem pole DC/AC. By selecting an operating frequency of 125 kHz, the first harmonic does not require significant attenuation but only the successive one as the 2nd, 3rd, and so forth. A current ripple factor of 20 % was selected for the boost inductor, when having 120-VAC output. The inductance value was calculated by using Equation 13 and Equation 14 for a worst-case duty cycle equal to 50%:

$$I_{pk-pk} = \frac{0.2 \times 1600\ W}{(110 \times \sqrt{2})\ V} = 2.06\ A \quad (21)$$

$$L = \frac{0.5 \times (1 - 0.5)}{2.06\ A \times 125\ kHz} \times (110 \times \sqrt{2})V = 106\ \mu H \quad (22)$$

An inductance value equal to 106 µH was calculated. Bourns 145450 (D6746) was selected and this is an inductor rated 111 µH. In general, the boost inductor contributes to the differential and common mode noise attention.

3.2.3.2.2 Cx Capacitance Selection

Cx are the capacitors connected between line-to-line or line-to-neutral. The aim of these capacitors is to attenuate the differential mode noise injected from the DC/AC into the grid. The value of these capacitors is a trade-off between reactive power provided to the grid and the differential mode attenuation. By default, the reactive power injected into the grid is equal to Equation 23:

$$Q = V_{rms}^2 \times C \times \omega \quad (23)$$

At 5 % load, a power factor equal to 0.7 (45°) has been set up as requirement. Thus, leading to limit the quantity of reactive power to:

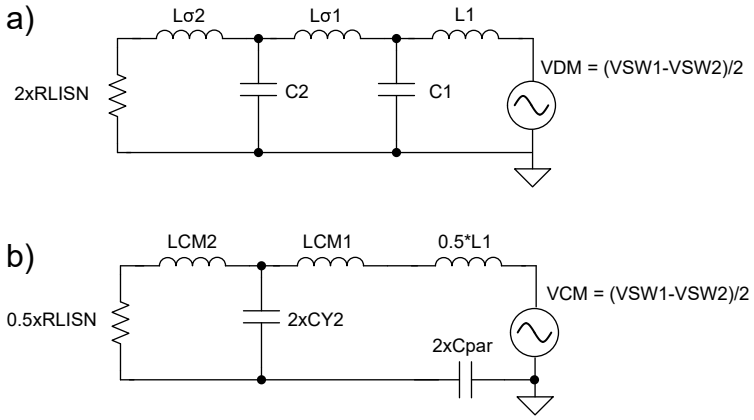
$$Q_{max} = 0.05 \times P_{nom} \times \tan(\varphi) = 56\ VAR \quad (24)$$

The maximum value of capacitance can be calculated from Equation 23 and Equation 24 and is equal to 3.5 µF. Two Cx capacitors, respectively, with values of 1 µF and 2.2 µF were selected.

3.2.3.2.3 EMI Filter Design

The following EMI filter was designed to attenuate both the differential-mode and common-mode noise injected into the grid.

The EMI filter can be analyzed in the common-mode and differential-mode domains. From the EMI filter shown in Figure 3-13, it is possible to derive the equivalent common- and differential-mode circuits as shown respectively in parts a) and b), where Lσ represents the leakage inductance of the common-mode choke.



a) Equivalent differential-mode model
b) Equivalent common-mode model

Figure 3-13. EMI Filter

The first critical frequency to be attenuated is the 250 kHz. The 125 kHz was not considered because that value is not in the EMI mask.

Differential-Mode Attenuation at 250 kHz	84 dB
Common-Mode Attenuation at 250 kHz	84 dB

An EMI filter with the values listed in Table 3-1 was designed:

Table 3-1. EMI Filter Values

PARAMETER	VALUE
L1	110 µH
C1	2.2 µF
Lcm1	L_{cm} 6 mH, Lσ 6 µH
C2	1 µF
Lcm2	L_{cm} 6 mH, Lσ 6 µH
Cy1 and Cy2	2.2 nF

Two Bourns 47690 (D6744) CMCs were used in this EMI filter.

3.2.3.2.4 DC-Link Output Capacitance

In single-phase applications, power ripple is present and can cause voltage ripple on the DC link. The DC-link capacitor value was calculated using Equation 15:

$$C_{OUT} \geq \frac{1600\ W}{2 \times 400\ V \times \pi \times 50\ Hz \times 36\ V} \quad (25)$$

A total capacitance of 360 µF was calculated for the 1.6-kW, 400-V, and 50-Hz operating condition. The ALC80A121BD450 device was selected.

3.2.3.3 Voltage and Current Measurements

The measurement of the AC grid voltage was done using the AMC3330. This device is a precision voltage-sensing reinforced isolated amplifier with integrated DC/DC. This IC has ±1-V input voltage range optimized for voltage measurement with high input impedance. The AC voltage is passed through a voltage divider, thus leading to a linear range of the measurement ±401 V, see Figure 3-14.

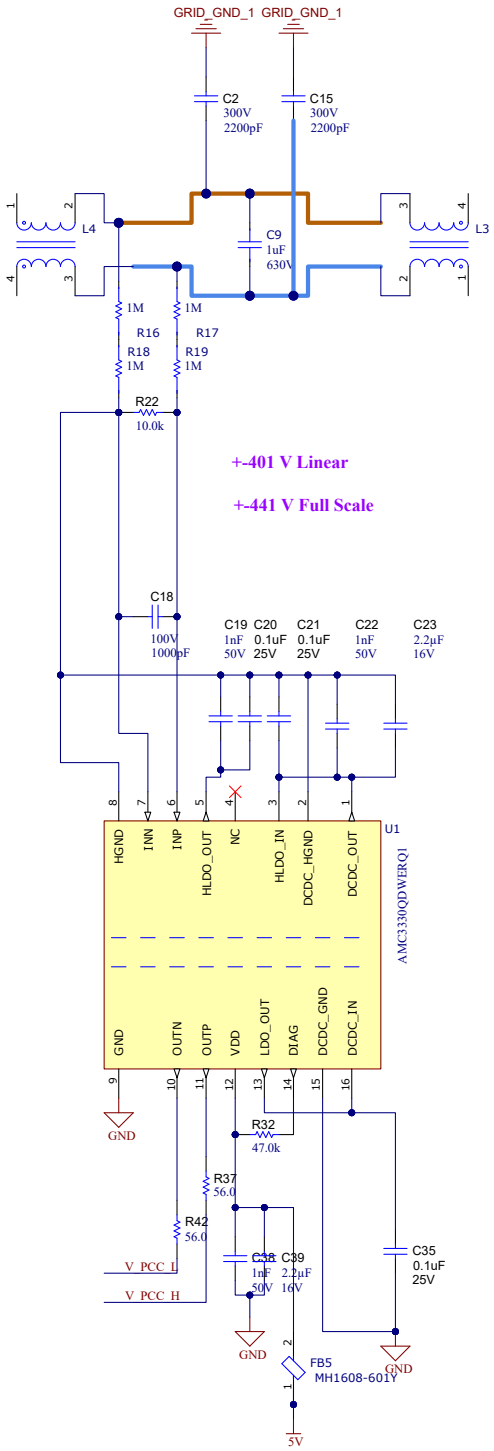


Figure 3-14. AC Voltage Measurement

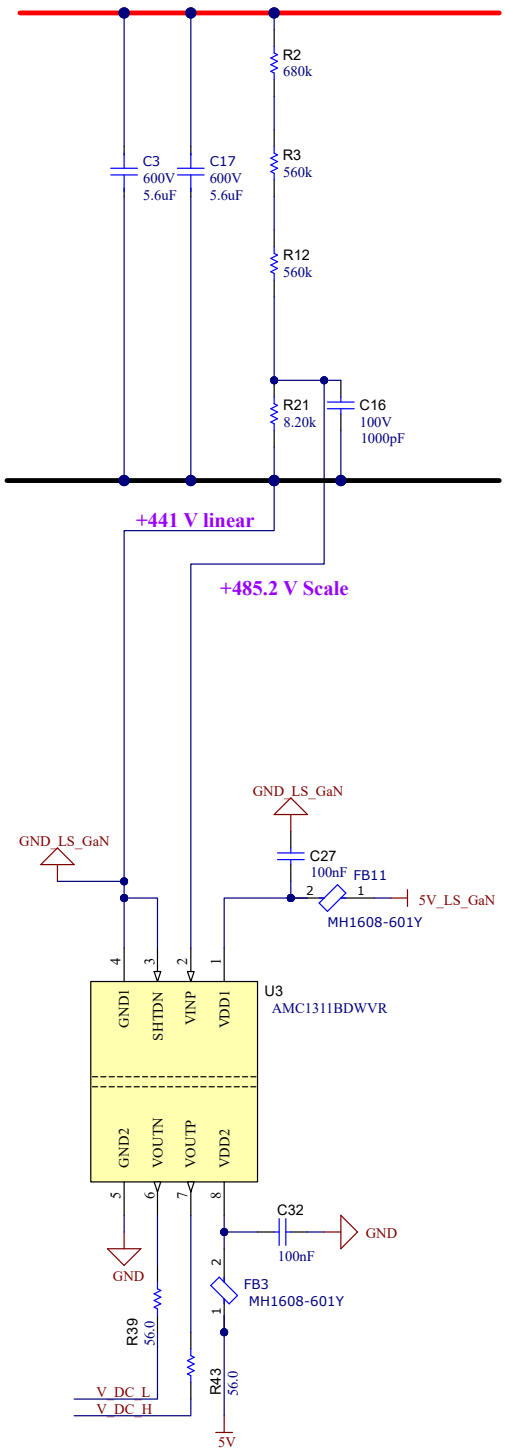


Figure 3-15. DC-Link Voltage Measurement

The measurement of the DC-link voltage was done with AMC1311, see Figure 3-15. This device is a precision voltage sensing reinforced isolated amplifier without integrated DC/DC. This IC has +2-V input voltage range optimized for voltage measurement with high input impedance. The DC voltage is passed through a voltage divider, thus leading to a linear range of the measurement between 0 V and 441 V. Since the IC does not include a power supply on the high-voltage side, the GaN power supply was used for this purpose.

The measurement of the DC-link current was done with AMC1302. This device is a precision current sensing reinforced isolated amplifier without integrated DC/DC. This IC has +50-mV input voltage range optimized for current measurement with low input impedance. The DC current is passed through a 2-mΩ shunt, thus leading to a linear range of the measurement ±25 A.

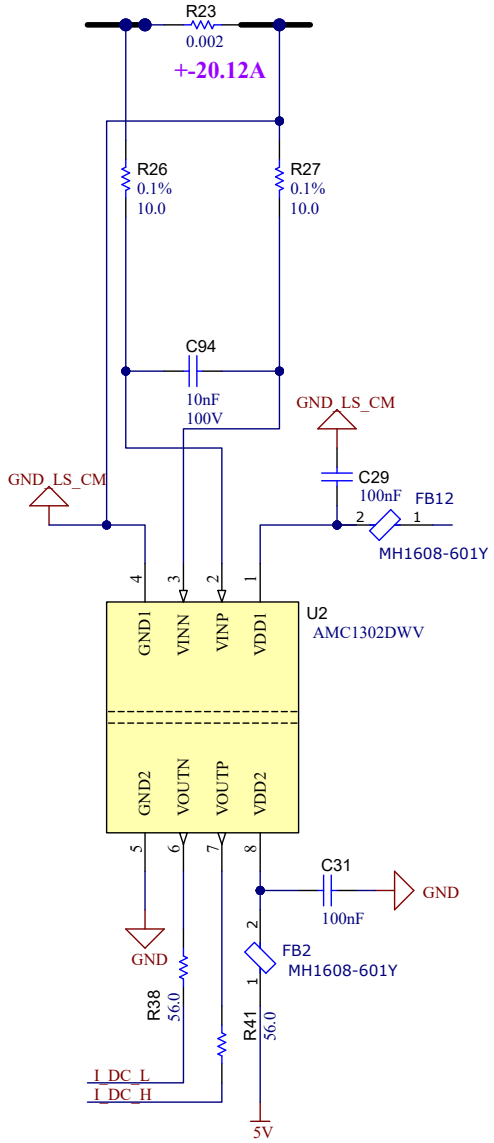


Figure 3-16. DC-Link Current Measurement

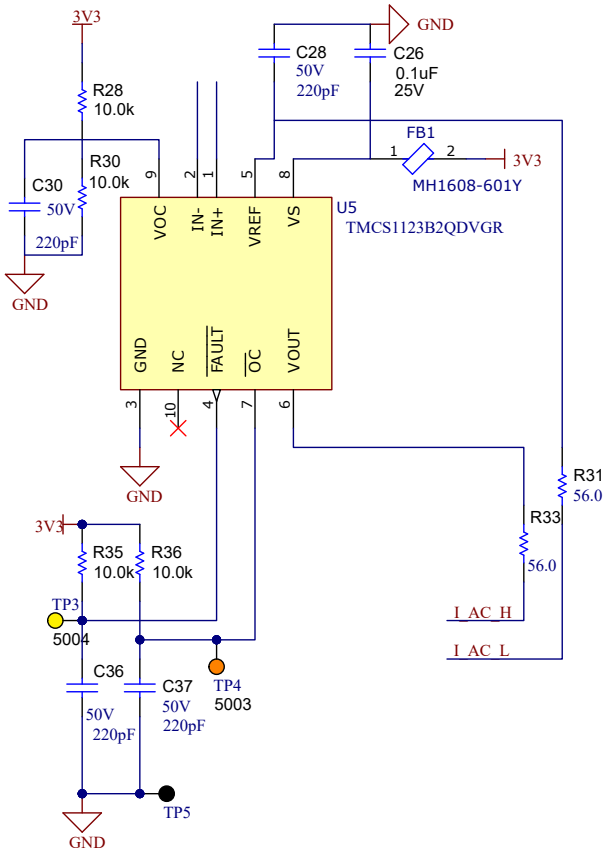


Figure 3-17. AC Current Measurement

The current in the grid is measured by means of a Hall-based current sensor TMCS1123 which allows measurement of the current into the Point of Common Coupling (PCC) with high accuracy. This design allows a reinforced isolation between the grid and the MCU.

3.3 Highlighted Products

3.3.1 TMDSCNCD280039C - TMS320F280039C Evaluation Module C2000™ MCU controlCARD™

The F280039C controlCARD (TMDSCNCD280039C) from Texas Instruments (TI) provides a great way to learn and experiment with F28003x devices. The F28003x devices are members of TI's family of microcontrollers (MCUs), the C2000™ MCU. This 120-pin controlCARD is intended to provide a well-filtered robust design that is capable of working in most environments.

The controlCARD™ has the following features:

- F280039C Microcontroller – High-performance C2000 microcontroller is located on the controlCARD
- 120-pin HSEC8 Edge Card Interface – Allows for compatibility with all of the 180-pin controlCARD-based application kits and controlCARDs of C2000.
- Built-in Isolated JTAG Emulation – An XDS110 emulator provides a convenient interface to Code Composer Studio™ IDE without additional hardware. Flipping a switch allows an external JTAG emulator to be used.
- Built-in Isolated Power Supply – Passes the 5-V supply from the USB Type-C® connector through an isolation barrier. Allows for the controlCARD to be completely powered and operated from the USB Type-C connector. The F280039C is fully isolated from the USB port.
- Automatic Power Supply Switch – The controlCARD automatically switches to external 5-V power when present. No additional configuration is required.

3.3.2 LMG3522R050 - 650-V 50-mΩ GaN FET With Integrated Driver

The LMG3522R050 GaN FET with integrated driver and protections is targeting switch-mode power converters and enables designers to achieve new levels of power density and efficiency. The LMG3522R050 integrates a silicon driver that enables switching speed up to 150 V/ns. TI's integrated precision gate bias results in higher switching SOA compared to discrete silicon gate drivers. This integration, combined with TI's low inductance package, delivers clean switching and minimal ringing in hard-switching power supply topologies. Adjustable gate drive strength allows control of the slew rate from 15 V/ns to 150 V/ns, which can be used to actively control EMI and optimize switching performance. Advanced power management features include digital temperature reporting and fault detection. The temperature of the GaN FET is reported through a variable duty cycle PWM output, which simplifies managing device loading. Faults reported include overtemperature, overcurrent, and UVLO monitoring.

3.3.3 LMG2100R044 - 100-V, 35-A GaN Half-Bridge Power Stage

The LMG2100R044 device is an 80-V continuous, 100-V pulsed, 35-A half-bridge power stage, with integrated gate-driver and enhancement-mode Gallium Nitride (GaN) FETs. The device consists of two 100-V GaN FETs driven by one high-frequency 80-V GaN FET driver in a half-bridge configuration. GaN FETs provide significant advantages for power conversion since GaN FETs have near-zero reverse recovery and very small input capacitance C_{ISS} and output capacitance C_{OSS}. All the devices are mounted on a completely bond-wire free package platform with minimized package parasitic elements. The LMG2100R044 device is available in a 5.5-mm × 4.5-mm × 0.89-mm lead-free package and can be easily mounted on PCBs. The TTL logic-compatible inputs can withstand input voltages up to 12 V regardless of the V_{CC} voltage. The proprietary bootstrap voltage clamping technique provides the gate voltages of the enhancement mode GaN FETs are within a safe operating range. The device extends advantages of discrete GaN FETs by offering a more user-friendly interface. This device is an excellent choice for applications requiring high-frequency, high-efficiency operation in a small form factor.

3.3.4 TMCS1123 - Precision Hall-Effect Current Sensor

The TMCS1123 is a galvanically isolated Hall-effect current sensor with industry leading isolation and accuracy. An output voltage proportional to the input current is provided with excellent linearity and low drift at all sensitivity options. Precision signal conditioning circuitry with built-in drift compensation is capable of less than 1.75% maximum total error over temperature and lifetime with no system level calibration, or less than 1% maximum total error with a one-time room temperature calibration (including both lifetime and temperature drift). AC or DC input current flows through an internal conductor generating a magnetic field measured by integrated on-chip Hall-effect sensors. Coreless construction eliminates the need for magnetic concentrators. Differential Hall sensors reject interference from stray external magnetic fields. Low conductor resistance increases measurable

current ranges up to ± 96 A while minimizing power loss and easing thermal dissipation requirements. Insulation capable of withstanding 5000 V_{RMS}, coupled with minimum 8.1-mm creepage and clearance provide up to 1100-VDC reliable lifetime reinforced working voltage. Integrated shielding enables excellent common-mode rejection and transient immunity. Fixed sensitivity allows the TMCS1123 to operate from a single 3-V to 5.5-V power supply, eliminates ratiometry errors, and improves supply noise rejection.

3.3.5 AMC1302 - Precision, ±50-mV Input, Reinforced Isolated Amplifier

The AMC1302 is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 5 kV_{RMS} according to VDE V 0884-11 and UL1577, and supports a working voltage of up to 1.5 kV_{RMS}. The isolation barrier separates parts of the system that operate on different common-mode voltage levels and protects the low-voltage side from hazardous voltages and damage. The input of the AMC1302 is optimized for direct connection to a low-impedance shunt resistor or other low-impedance voltage source with low signal levels. The excellent DC accuracy and low temperature drift supports accurate current control in PFC stages, DC/DC converters, AC-motor and servo drives over the extended industrial temperature range from –40°C to +125°C. The integrated missing-shunt and missing high-side supply detection features simplify system-level design and diagnostics.

3.3.6 AMC3330 - Precision, ±1-V Input, Reinforced Isolated Amplifier With Integrated DC/DC Converter

The AMC3330 is a precision, isolated amplifier with a fully-integrated, isolated DC/DC converter that allows single-supply operation from the low-side of the device. The reinforced capacitive isolation barrier is certified according to VDE V 0884-11 and UL1577 and separates sections of the system that operate on different common-mode voltage levels and protects low-voltage domains from damage. The input of the AMC3330 is optimized for direct connection to high-impedance, voltage-signal sources such as a resistor-divider network to sense high-voltage signals. The integrated isolated DC/DC converter allows measurement of non-ground-referenced signals and makes the device a unique design for noisy, space-constrained applications. The excellent performance of the device supports accurate voltage monitoring and control. The integrated DC/DC converter fault-detection and diagnostic output pin of the AMC3330 simplify system-level design and diagnostics. The AMC3330 is specified over the temperature range of –40°C to +125°C.

3.3.7 AMC1311 - High-Impedance, 2-V Input, Reinforced Isolated Amplifier

The AMC1311 is a precision, isolated amplifier with an output separated from the input circuitry by a capacitive isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 5 kV_{RMS} according to DIN EN IEC 60747-17 (VDE 0884-17) and UL1577 and supports a working voltage of up to 1500 V_{RMS}. The isolation barrier separates parts of the system that operate on different common-mode voltage levels and protects the low-voltage side from voltages that can cause electrical damage or be harmful to an operator. The high-impedance input of the AMC1311 is optimized for connection to high-impedance resistive dividers or any other high-impedance voltage signal source. The excellent DC accuracy and low temperature drift support accurate, isolated voltage sensing and control in closed-loop systems. The integrated missing high-side supply voltage detection feature simplifies system-level design and diagnostics. The AMC1311 is offered with two performance grade options: the AMC1311B is specified over the extended industrial temperature range of –55°C to +125°C, and the AMC1311 is specified for operation at –40°C to +125°C.

3.3.8 ISO6741 - General-Purpose Reinforced Quad-Channel Digital Isolators with Robust EMC

The ISO674x devices are high-performance, quad-channel digital isolators designed for cost-sensitive applications requiring up to 5000-V_{RMS} isolation ratings per UL 1577. These devices are also certified by VDE, TUV, CSA, and CQC. The ISO674x devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by TI's double capacitive silicon dioxide (SiO2) insulation barrier. These devices come with enable pins which can be used to put the respective outputs in high impedance for multi-master driving applications. The ISO6740 device has all four channels in the same direction, the ISO6741 device has three forward and one reverse-direction channels, and the ISO6742 device has two forward and two reverse direction channels. In the event of input power or signal loss, the default output is high for devices without suffix F and low for devices with suffix F.

3.3.9 UCC21540 - Reinforced Isolation Dual-Channel Gate Driver

The UCC21540 is an isolated dual-channel gate-driver family designed with up to 4-A, 6-A peak source, sink current to drive power MOSFET, IGBT, and GaN transistors. The UCC2154x in a DWK package also offers 3.3-mm minimum channel-to-channel spacing which facilitates higher bus voltage. The UCC2154x family can be configured as two low-side drivers, two high-side drivers, or a half-bridge driver. The input side is isolated from the two output drivers by a 5.7-kV_{RMS} isolation barrier, with a minimum of 100-V/ns common-mode transient immunity (CMTI). Protection features include: resistor programmable dead time, disable feature to shut down both outputs simultaneously, integrated de-glitch filter that rejects input transients shorter than 5 ns, and negative voltage handling for up to –2-V spikes for 200 ns on input and output pins. All supplies have UVLO protection.

3.3.10 LM5164 - 100-V Input, 1-A Synchronous Buck DC/DC Converter with Ultra-low IQ

The LM5164 synchronous buck converter is designed to regulate over a wide input voltage range, minimizing the need for external surge suppression components. A minimum controllable on-time of 50 ns facilitates large step-down conversion ratios, enabling the direct step-down from a 48-V nominal input to low-voltage rails for reduced system complexity and design cost. The LM5164 operates during input voltage dips as low as 6 V, at nearly 100% duty cycle if needed, making this device an excellent choice for wide input supply range industrial and high cell count battery pack applications. With integrated high-side and low-side power MOSFETs, the LM5164 delivers up to 1 A of output current. A constant on-time (COT) control architecture provides nearly constant switching frequency with excellent load and line transient response. Additional features of the LM5164 include ultra-low I_Q and diode emulation mode operation for high light-load efficiency, remarkable peak and valley overcurrent protection, integrated V_{CC} bias supply and bootstrap diode, precision enable and input UVLO, and thermal shutdown protection with automatic recovery. An open-drain PGOOD indicator provides sequencing, fault reporting, and output voltage monitoring. The LM5164 is available in a thermally-enhanced, 8-pin SO PowerPAD™ integrated circuit package. The 1.27-mm pin pitch provides adequate spacing for high-voltage applications.

4 Hardware, Software, Testing Requirements, and Test Results

4.1 Hardware Requirements

The hardware for this reference design is composed of the following:

- DC/DC Board (TIDA-010933-DCDC)
- DC/AC Board (TIDA-010933-ACDC)
- TMDSCNCD280039C control card
- USB Type-C cable
- USB isolator
- Laptop

The following equipment was used to power and evaluate the DUT:

- DC Power source Keysight N8950A
- DC Power source Elektro-Automatik EA-PS 3080-20C
- AC Power source Chroma 61611
- DC Load Chroma 63208A
- AC load
- Power Analyzer Tektronix PA-4000

4.2 Test Setup

The recommended sequence of tests follow:

1. DC/DC board with four independent DC power sources on inputs and DC load on the output
2. DC/AC board with DC power source on input and resistive load on the output
3. DC/AC board with DC power source on input and AC load on the output
4. Both boards together with four independent DC power sources on inputs and resistive load on the output
5. Both boards together with four independent DC power sources on inputs and AC load on the output

4.2.1 DC/DC Board

Figure 4-1 shows the DC/DC board connections. For safety reasons make sure that proper voltage and current limits are selected on DC power sources. DC load needs to be configured in constant voltage mode with 400 V and 4-A limits.

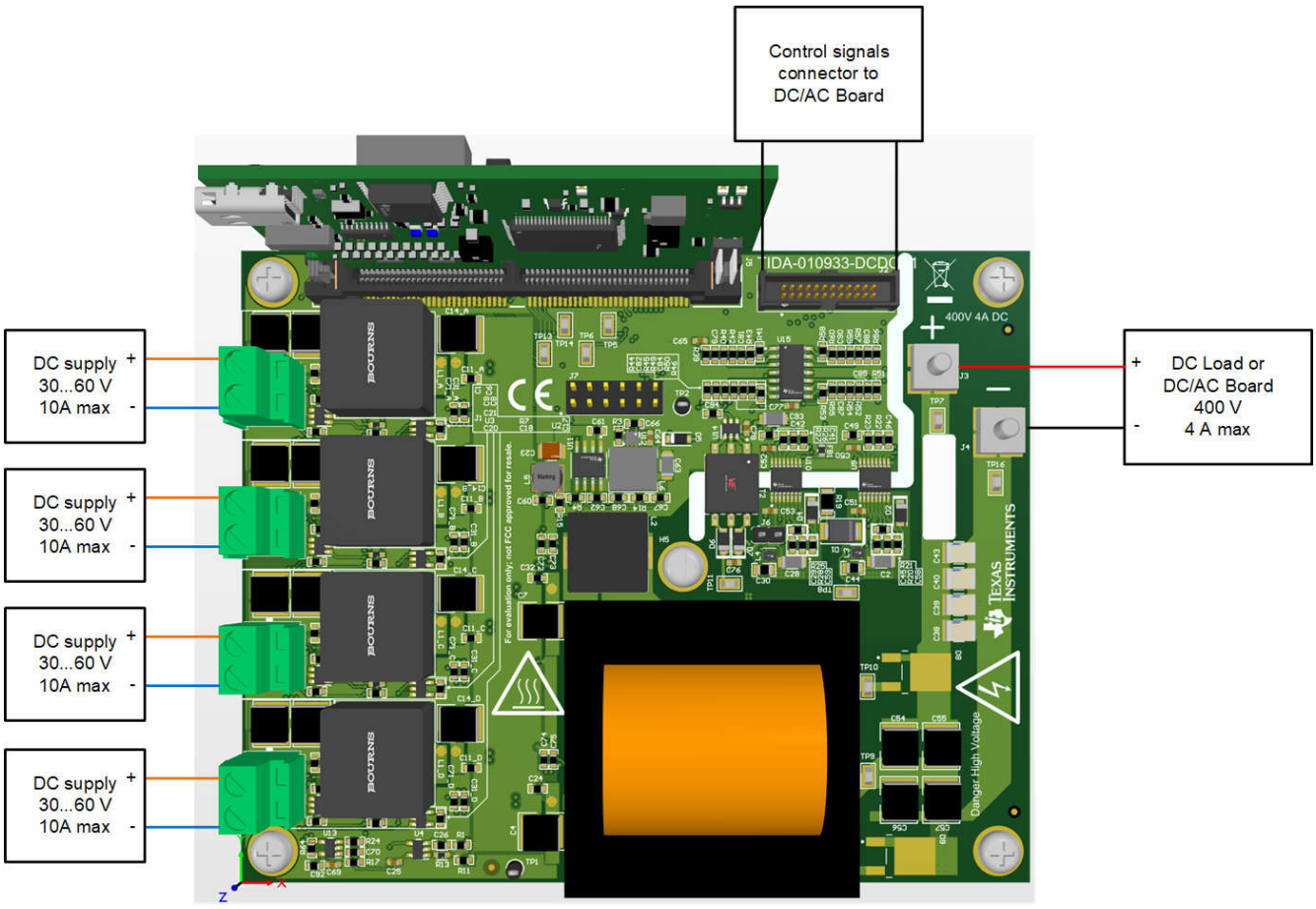


Figure 4-1. DC/DC Board Connections for Test

4.2.2 DC/AC Board

Figure 4-2 shows connections for the DC/AC board. For safety reasons, make sure that the proper voltage and current limits are selected on DC power sources. DC source needs to be configured in constant voltage mode with 400 V and 4.5-A maximum current.

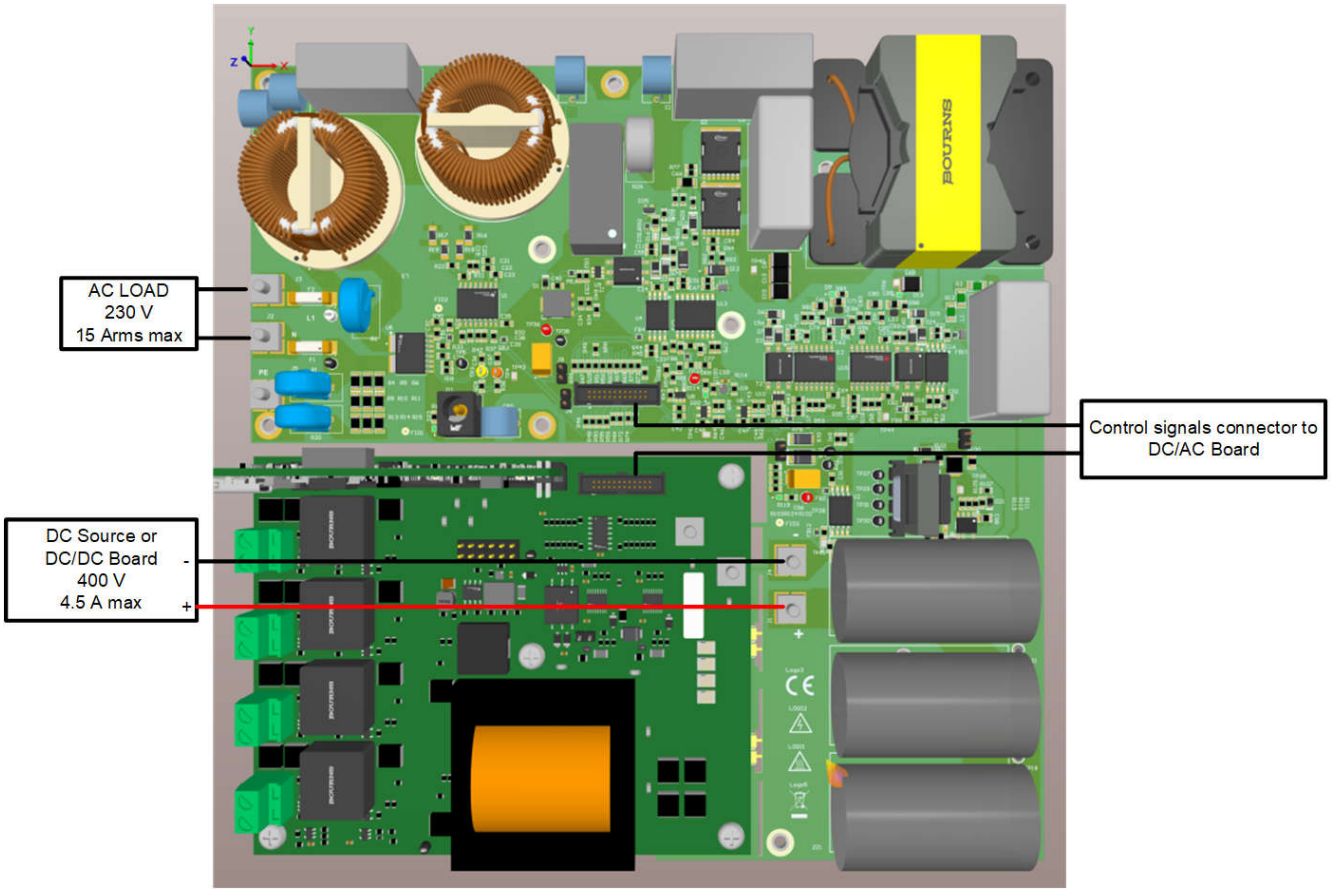


Figure 4-2. DC/AC Board Connections for Test

4.3 Test Results

Table 4-1 and Figure 4-3 show overall efficiency converting from DC inputs to 230-VAC output. The table shows that the reference design achieves a peak efficiency of 96.3% at approximately 800 W and 60-V input and has a full load efficiency of 94.2% at 1.6 kW.

Table 4-1. TIDA-010933 Efficiency

OUTPUT POWER	80 W	160 W	320 W	480 W	640 W	800 W	960 W	1280 W	1600 W
V_{IN} = 60 V	88,1%	94,1%	95,2%	95,6%	96,1%	96,3%	96,2%	95,5%	94,2%
V_{IN} = 50 V	87,6%	93,7%	94,8%	95,3%	95,9%	96,1%	96,0%	95,3%	94,0%
V_{IN} = 40 V	87,3%	93,5%	94,6%	95,1%	95,7%	95,9%	95,8%	95,1%	93,8%

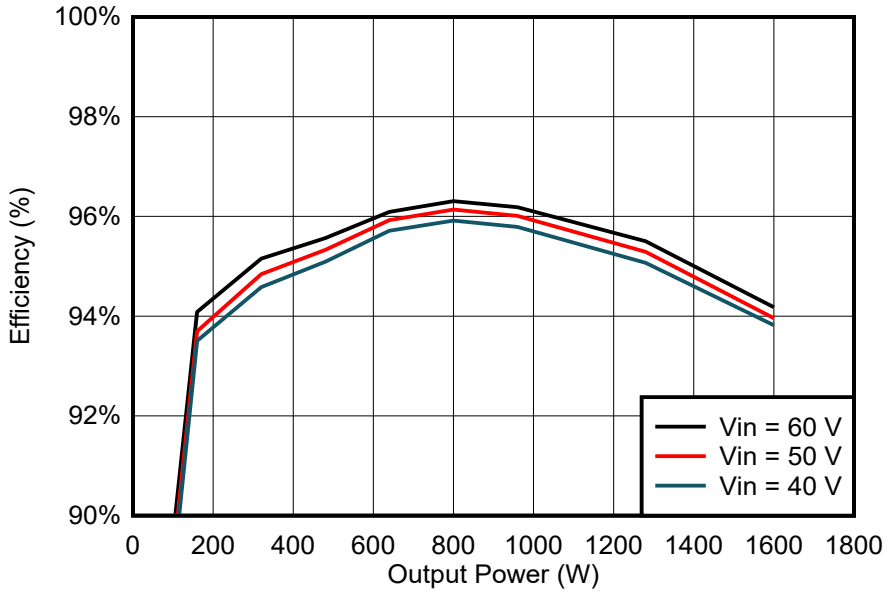


Figure 4-3. TIDA-010933 Efficiency vs Output Power

4.3.1 Input DC/DC Boost Results

The voltage of the switching node was measured as shown in Figure 4-4. From the picture, observe the sharp switching edges without overshoot and ringing.

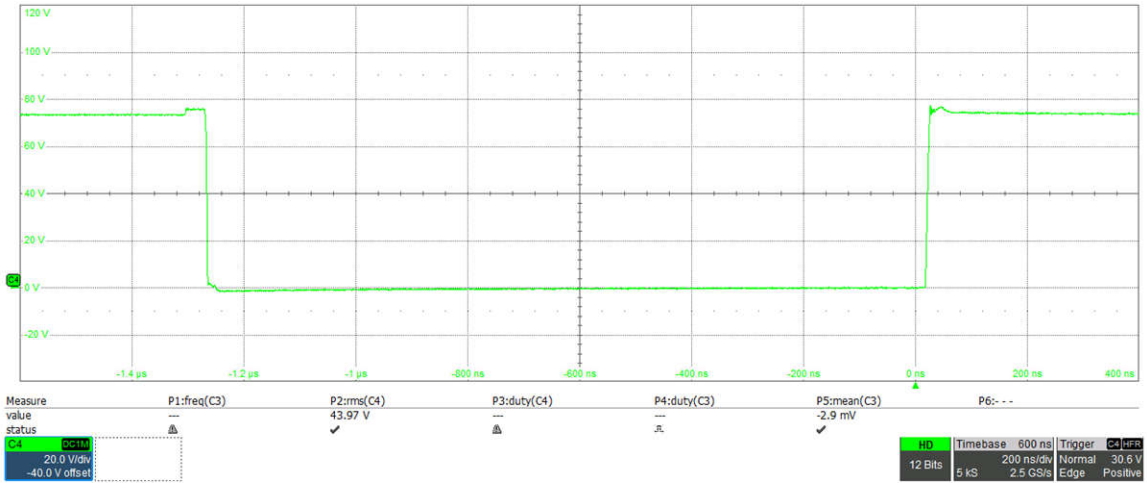


Figure 4-4. Switching Node Voltage of DC/DC Converter at 50 V and 7-A Input

Table 4-2 and Figure 4-5 show the efficiency of an input DC/DC converter to 75-V rail. The table shows that the converter achieves a peak efficiency of 99.3% at full load of 400 W.

Table 4-2. DC/DC Converter Efficiency

OUTPUT POWER	20 W	40 W	80 W	120 W	160 W	200 W	240 W	320 W	400 W
V_{IN} = 60 V	97,0%	97,7%	98,4%	98,7%	99,0%	99,1%	99,2%	99,3%	99,3%
V_{IN}= 50 V	96,5%	97,3%	98,1%	98,4%	98,8%	98,9%	99,0%	99,1%	99,1%
V_{IN} = 40 V	96,1%	97,1%	97,8%	98,2%	98,6%	98,7%	98,8%	98,8%	98,9%

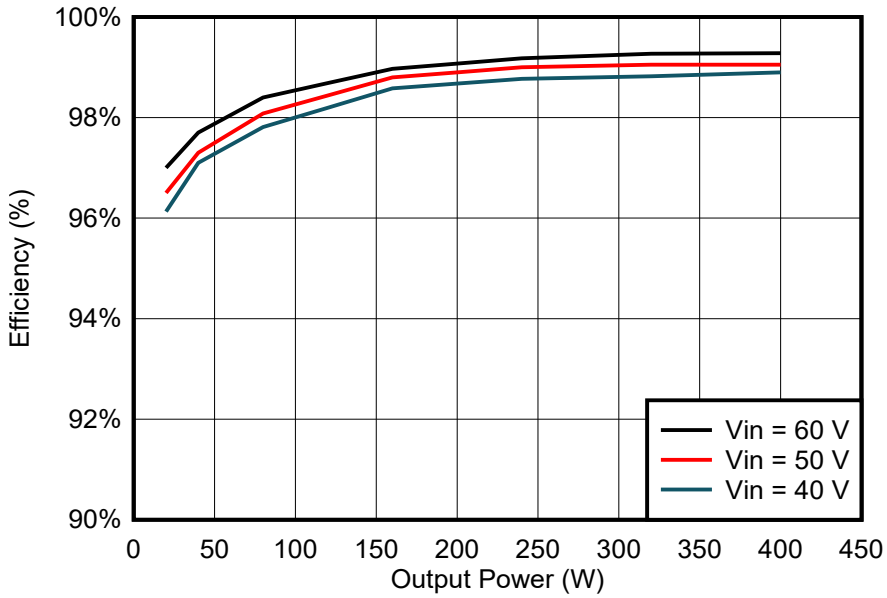


Figure 4-5. Input DC/DC Boost Efficiency vs Output Power

4.3.2 CLLLC Results

Table 4-3 and Figure 4-6 show efficiency of the CLLLC converter from 75-V rail to 400-V DC-Link. The table shows that the converter achieves a peak efficiency of 98.3% at 800 W.

Table 4-3. CLLLC Converter Efficiency

OUTPUT POWER	87 W	268 W	353 W	499 W	622 W	746 W	1070 W	1307 W	1618 W
Efficiency	92,0%	97,5%	97,9%	98,1%	98,2%	98,4%	98,3%	98,0%	97,5%

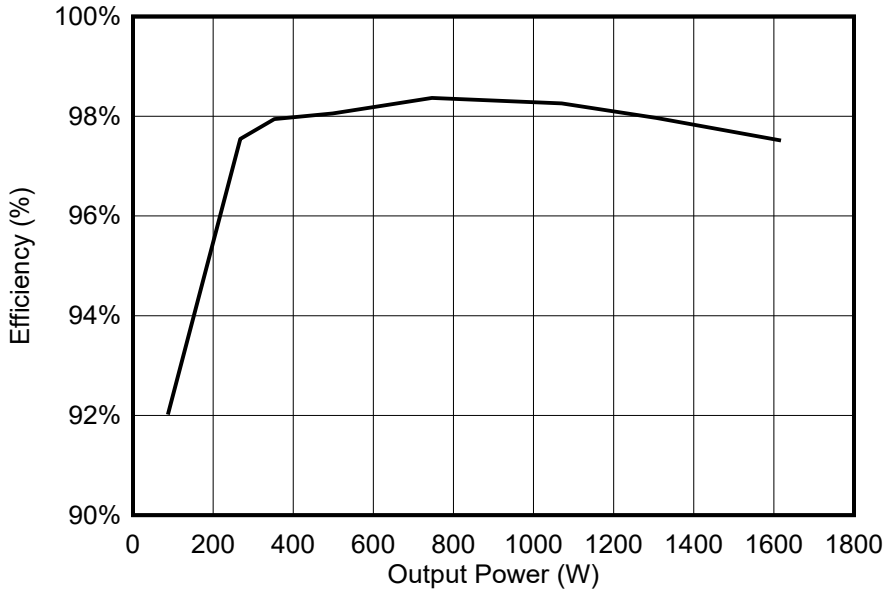
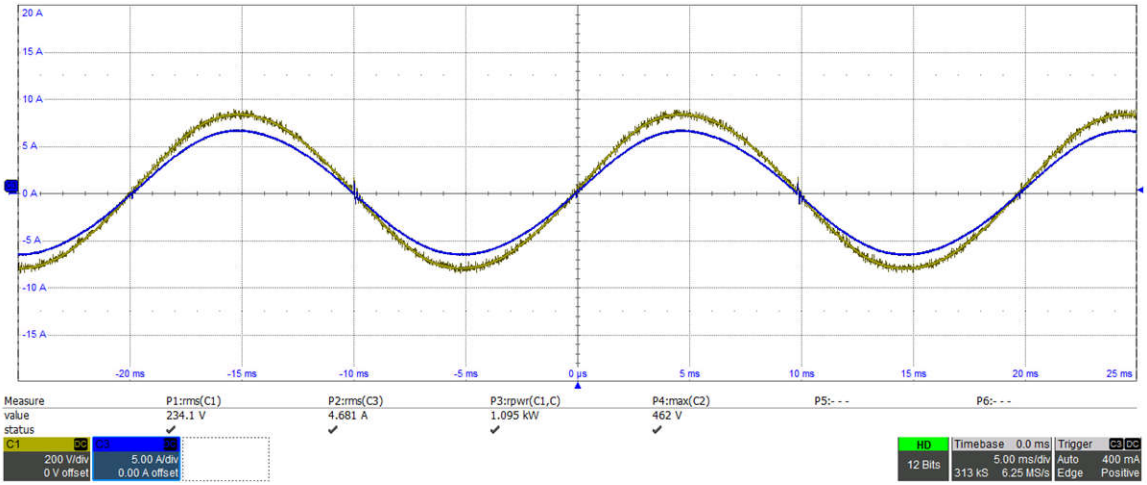


Figure 4-6. CLLLC Efficiency vs Output Power

4.3.3 DC/AC Results

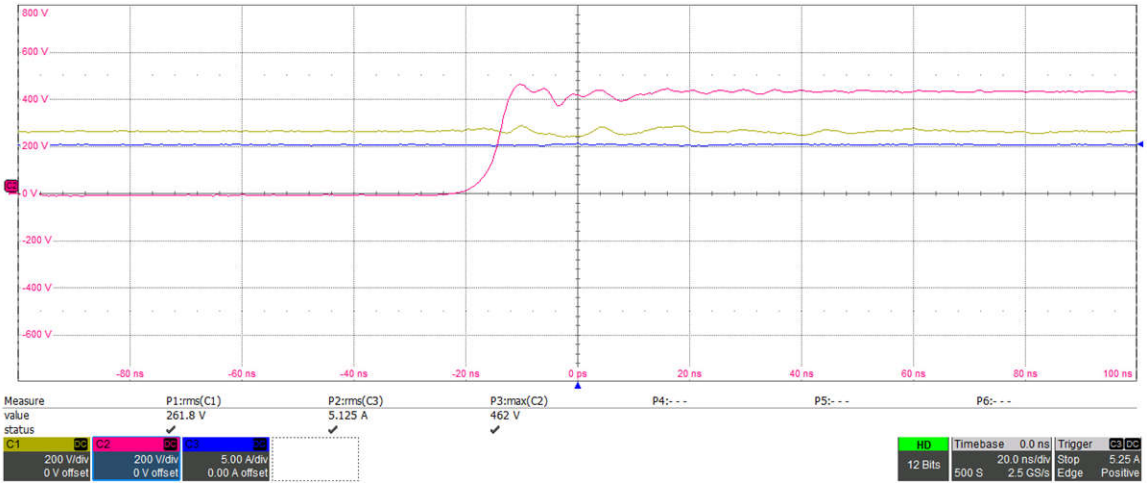
In Figure 4-7, 1.1-kW output power was sourced from 400-V DC link to 230 VAC. Notice that no important current ripple is injected into the resistor.



C1 - Output voltage, C3 - Output current. Output power - 1.1 kW

Figure 4-7. DC/AC Line Voltage and Current

The voltage of the switching node was measured as shown in Figure 4-8. Observe from the image that no important overvoltage was detected even when the switching was at 80 kV / µs.



C1 - Line voltage, C2 - Switching node voltage, C3 - Line current

Figure 4-8. DC/AC Converter Switching Node

Table 4-4 and Figure 4-9 show efficiency of the CLLLC converter from 400-V DC link to 230-VAC output. The table shows that the converter achieves a peak efficiency of 98.9% at 640 W.

Table 4-4. DC/AC Converter Efficiency

OUTPUT POWER	80 W	160 W	320 W	480 W	640 W	800 W	960 W	1280 W	1600 W
Efficiency	97,3%	98,2%	98,7%	98,8%	98,9%	98,8%	98,7%	98,7%	98,7%

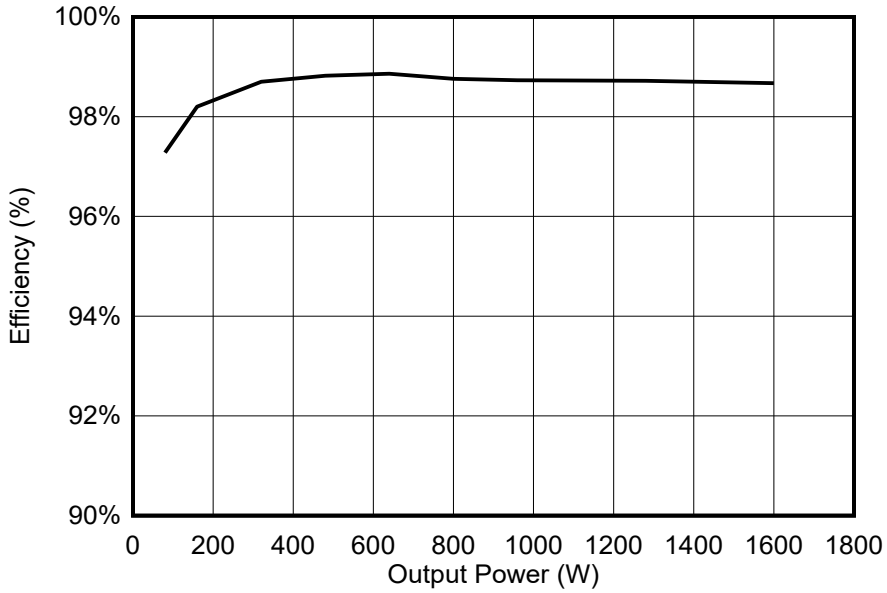


Figure 4-9. DC/AC Converter vs Output Power

5 Design and Documentation Support

5.1 Design Files

To download the design files, see the design files at TIDA-010933.

5.1.1 Schematics

To download the schematics, see the design files at TIDA-010933.

5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010933.

5.2 Tools and Software

Tools

TMDSCNCD280039C	TMS320F280039C evaluation module C2000™ MCU controlCARD™

Software

Code Composer Studio™	Integrated development environment (IDE)
C2000WARE-DIGITALPOWER-SDK	DigitalPower software development kit (SDK) for C2000™ MCUs

5.3 Documentation Support

1. Texas Instruments, *Designing an LLC Resonant Half-Bridge Power Converter* Application note
2. Texas Instruments, *400-W GaN-Based MPPT Charge Controller and Power Optimizer Reference Design* Design Guide

5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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