REV	DESCRIPTION	DATE	Author
A	INITIAL CAPTURE	06/19/2019	BMc
B	Increase "letter Rev" designator for any net or component changes that impact netlist.	06/06/2017	JAC
B1	BETA-1 (Minor text or note updates designated w/ -#)	06/13/2017	JAC
C	APPROVED for PCB layout design	09/08/2017	JAC
1.0	Released SCH & PCB	02/20/2018	BMc
1.1	Minor SCH/BOM changes tthat don't impact PCB routing (i.e. no blue-wire mods).	02/28/2018	BMc
2.0	Major PCB/SCH/BOM changes tthat impact netlist & PCB routing (i.e. blue-wire mods).	03/28/2018	BMc

Needs updating:
Table of Contents
Title Block (all SCH pgs need updating)
Rev History

*** DISCLAIMER ***

The SoC Reference Design Study provides SCH & PCB source files that can be used as a good starting point for new designs. Please be aware that the SCH & PCB are NOT 100% complete for implementing an End Product. An End Product's feature set will define additional required signaling and SoC interfaces. As a result, a majority of signals in this SCH are "single-pin" / "unconnected" nets.

The SoC's schematic symbol has been organized based upon each ball's "primary signaling interface". For End Products, unused primary interface signals can then be re-defined by SoC's internal muxmode controll (see Data Manual for details) to use "alternate functions" (i.e. GPIOs) to support other key system needs (i.e. interupts, debug, etc.).

Primary objectives of this Ref Design are to demonstrate:
1. 100% signal & power breakout routing of SoC using recommended PCB design rules & strategies.
2. Key high-speed signals with controlled impedance PCB routing (i.e. DDR & SERDES).
3. Power Distribution Network (PDN) with the following:
   a) Recommended SoC power solution components (2nd stage) showing preferred SoC voltage domain to power resource mapping.
   b) Optimized decoupling capacitor scheme per key power rail using only automotive qualified caps to meet SoC recommended power integrity (PI) parameters based on this specific PCB design (stack-up, placement, routing, via types, etc).
   c.) A typical 1st stage power conversion interfaced directly to input battery has been captured as an example. An end product's 1st stage power conversion components may need to be different.

Sheet # - Name
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TEXAS INSTRUMENTS INCORPORATED

Title: DRA76xP/DRA77xP/TDA2Px-ACD REFERENCE DESIGN STUDY		
Page Contents: TITLE PAGE		
Size: C	DOC NO: TIDEP-01020	REV: 1.0
Date: Tuesday, June 16, 2020	Sheet 1 of 36	

Preliminary

REVISION HISTORY

REV #	DATE	DESCRIPTION OF CHANGES	AUTHOR	
1.0	16 June 2020	Initial release of DRA829x/TDA4VMx reference design. Drafted from EVM SoM SCH rev E5 - E7 with additional new pages added as needed.	TI EVM Design Team	

REVISION SCHEME

1.0	Released SCH & PCB	02/20/2018	BMc
1.1	Minor SCH/BOM changes tthat don't impact PCB routing (i.e. no blue-wire mods).	02/28/2018	BMc
2.0	Major PCB/SCH/BOM changes tthat impact netlist & PCB routing (i.e. blue-wire mods).	03/28/2018	BMc

Project :

J7 EVM

TEXAS INSTRUMENTS

Title: REVISION HISTORY

Size: C | TIDEP-01020 | Rev: E5

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Project : J7 EVM	TEXAS INSTRUMENTS	Title: BLOCK DIAGRAM	
		Size: C	TIDEP-01020 — Rev: E5
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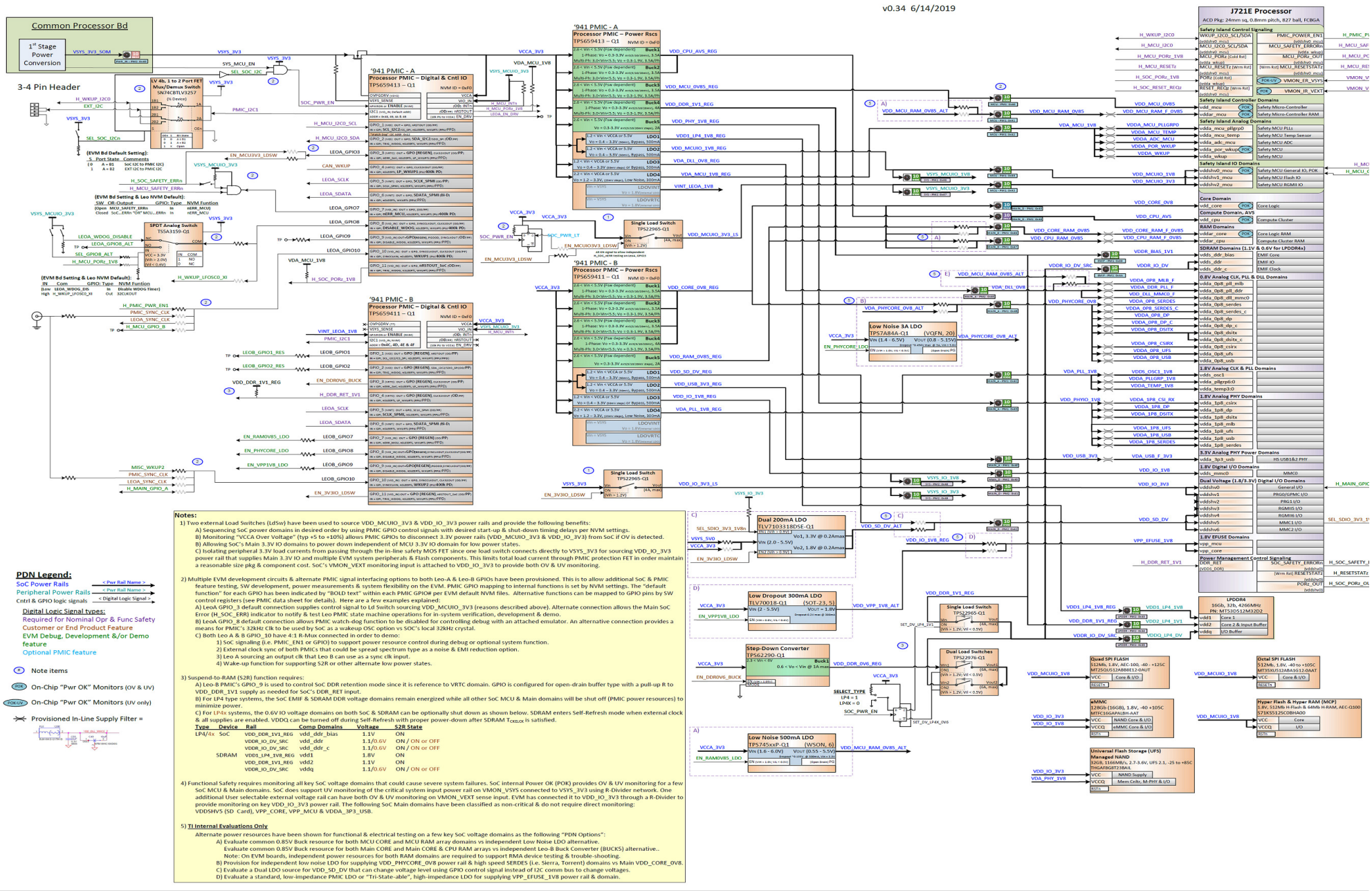
Preliminary

DUAL TPS65941x-Q1 PMICs POWER FLOW DIAGRAM

Recommended for Superset Use Case max power

v0.34 6/14/2019



Notes:

1) Two external Load Switches (LdSw) have been used to source VDD_MCUIO_3V3 & VDD_IO_3V3 power rails and provide the following benefits:
   A) Sequencing SoC power domains in desired order by using PMIC GPIO control signals with desired start-up & shut-down timing delays per NVM settings.
   B) Monitoring "VCCA Over Voltage" (typ +5 to +10%) allows PMIC GPIOs to disconnect 3.3V power rails (VDD_MCUIO_3V3 & VDD_IO_3V3) from SoC if OV is detected.
   B) Allowing SoC's Main 3.3V IO domains to power down independent of MCU 3.3V IO domain for low power states.
   C) Isolating peripheral 3.3V load currents from passing through the in-line safety MOS FET since one load switch connects directly to VSYS_3V3 for sourcing VDD_IO_3V3 power rail that supplies Main 3.3V IO and multiple EVM system peripherals & Flash components. This limits total load current through PMIC protection FET in order maintain a reasonable size pkg & component cost. SoC's VMON_VEXT monitoring input is attached to VDD_IO_3V3 to provide both OV & UV monitoring.

2) Multiple EVM development circuits & alternate PMIC signal interfacing options to both Leo-A & Leo-B GPIOs have been provisioned. This is to allow additional SoC & PMIC feature testing, SW development, power measurements & system flexibility on the EVM. PMIC GPIO mapping to internal functions is set by NVM settings. The "default function" for each GPIO has been indicated by "BOLD text" within each PMIC GPIO# per EVM default NVM files. Alternative functions can be mapped to GPIO pins by SW control registers (see PMIC data sheet for details). Here are a few examples explained:
   A) LeoA GPIO_3 default connection supplies control signal to Ld Switch sourcing VDD_MCUIO_3V3 (reasons described above). Alternate connection allows the Main SoC Error (H_SOC_ERR) indicator to notify & test Leo PMIC state machine operations for in-system verification, development & demo.
   B) LeoA GPIO_8 default connection allows PMIC watch-dog function to be disabled for controlling debug with an attached emulator. An alternative connection provides a means for PMIC's 32kHz Clk to be used by SoC as a wakeup OSC option vs SOC's local 32kHz crystal.
   C) Both Leo A & B GPIO_10 have 4:1 R-Mux connected in order to demo:
      1) SoC signaling (i.e. PMIC_EN1 or GPIO) to support power resource control during debug or optional system function.
      2) External clock sync of both PMICs that could be spread spectrum type as a noise & EMI reduction option.
      3) Leo A sourcing an output clk that Leo B can use as a sync clk input.
      4) Wake-up function for supporting S2R or other alternate low power states.

3) Suspend-to-RAM (S2R) function requires:
   A) Leo-B PMIC's GPIO_9 is used to control SoC DDR retention mode since it is reference to VRTC domain. GPIO is configured for open-drain buffer type with a pull-up R to VDD_DDR_1V1 supply as needed for SoC's DDR_RET input.
   B) For LP4 type systems, the SoC EMIF & SDRAM DDR voltage domains remain energized while all other SoC MCU & Main domains will be shut off (PMIC power resources) to minimize power.
   C) For LP4x systems, the 0.6V IO voltage domains on both SoC & SDRAM can be optionally shut down as shown below. SDRAM enters Self-Refresh mode when external clock & all supplies are enabled. VDDQ can be turned off during Self-Refresh with proper power-down after SDRAM T_{CKELCK} is satisfied.

Type	Device	Rail	Comp Domains	Voltage	S2R State
LP4/4x	SoC	VDD_DDR_1V1_REG	vdd_ddr_bias	1.1V	ON
		VDDR_IO_DV_SRC	vdd_ddr	1.1/0.6V	ON / ON or OFF
		VDDR_IO_DV_SRC	vdd_ddr_c	1.1/0.6V	ON / ON or OFF
	SDRAM	VDD1_LP4_1V8_REG	vdd1	1.8V	ON
		VDD_DDR_1V1_REG	vdd2	1.1V	ON
		VDDR_IO_DV_SRC	vddq	1.1/0.6V	ON / ON or OFF

4) Functional Safety requires monitoring all key SoC voltage domains that could cause severe system failures. SoC internal Power OK (POK) provides OV & UV monitoring for a few SoC MCU & Main domains. SoC does support UV monitoring of the critical system input power rail on VMON_VSYS connected to VSYS_3V3 using R-Divider network. One additional User selectable external voltage rail can have both OV & UV monitoring on VMON_VEXT sense input. EVM has connected it to VDD_IO_3V3 through a R-Divider to provide monitoring on key VDD_IO_3V3 power rail. The following SoC Main domains have been classified as non-critical & do not require direct monitoring: VDDSHV5 (SD_Card), VPP_CORE, VPP_MCU & VDDA_3P3_USB.

5) **TI Internal Evaluations Only**

   Alternate power resources have been shown for functional & electrical testing on a few key SoC voltage domains as the following "PDN Options":
   A) Evaluate common 0.85V Buck resource for both MCU CORE and MCU RAM array domains vs independent Low Noise LDO alternative.
      Evaluate common 0.85V Buck resource for both Main CORE and Main CORE & CPU RAM arrays vs independent Leo-B Buck Converter (BUCK5) alternative..
      Note: On EVM boards, independent power resources for both RAM domains are required to support RMA device testing & trouble-shooting.
   B) Provision for independent low noise LDO for supplying VDD_PHYCORE_0V8 power rail & high speed SERDES (i.e. Sierra, Torrent) domains vs Main VDD_CORE_0V8.
   C) Evaluate a Dual LDO source for VDD_SD_DV that can change voltage level using GPIO control signal instead of I2C comm bus to change voltages.
   D) Evaluate a standard, low-impedance PMIC LDO or "Tri-State-able", high-impedance LDO for supplying VPP_EFUSE_1V8 power rail & domain.

Project : J7 EVM	TEXAS INSTRUMENTS	Title: DUAL TPS65941 POWER FLOW DIAGRAM	
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SoM I2C TREE DIAGRAM

Project : J7 EVM	TEXAS INSTRUMENTS	Title: SoM I2C TREE DIAGRAM	
		Size: C	TIDEP-01020 — Rev: E5
		Date: Tuesday, June 16, 2020	Sheet 5 of 36

Preliminary

SoM I2C ADDRESS TABLE

Project : J7 EVM	TEXAS INSTRUMENTS	Title: SoM I2C TREE DIAGRAM	
		Size: C	TIDEP-01020 — Rev: E5
		Date: Tuesday, June 16, 2020	Sheet 6 of 36

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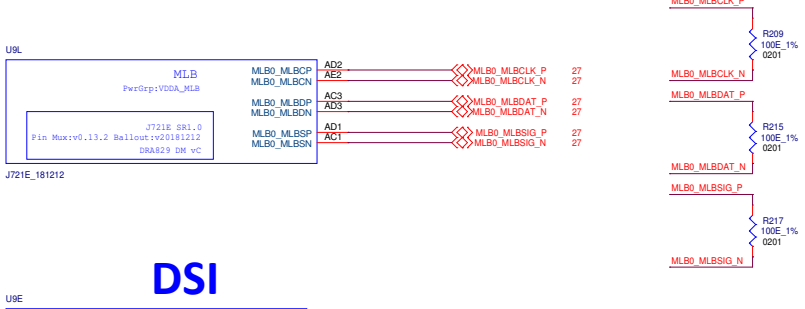
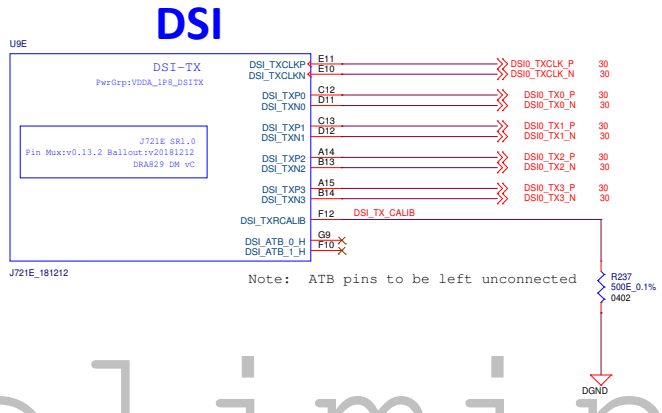
GPIO MAPPING TABLE

Project : J7 EVM	TEXAS INSTRUMENTS	Title: GPIO MAPPING TABLE	
		Size: C	TIDEP-01020 — Rev: E5
		Date: Friday, June 12, 2020	Sheet 7 of 36

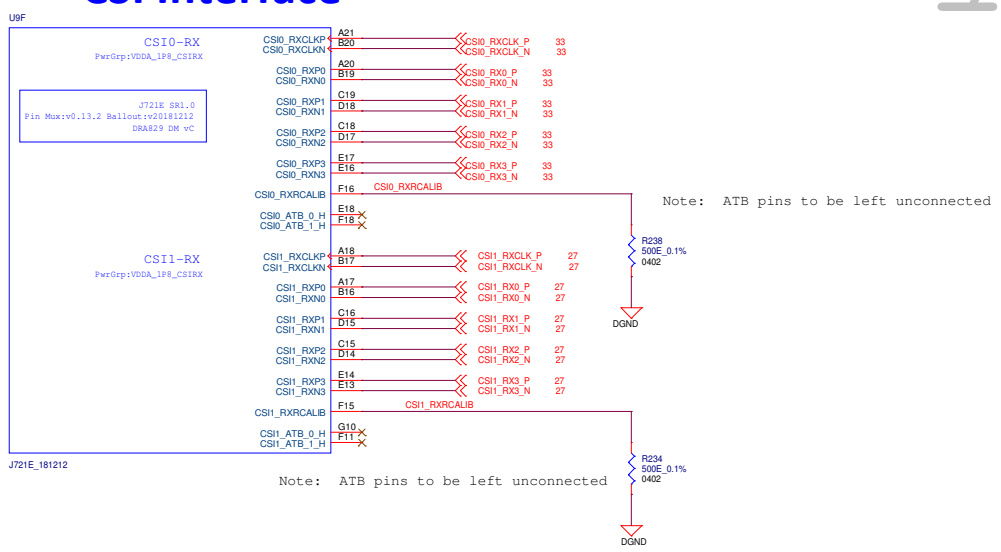
MLB



DSI



CSI Interface

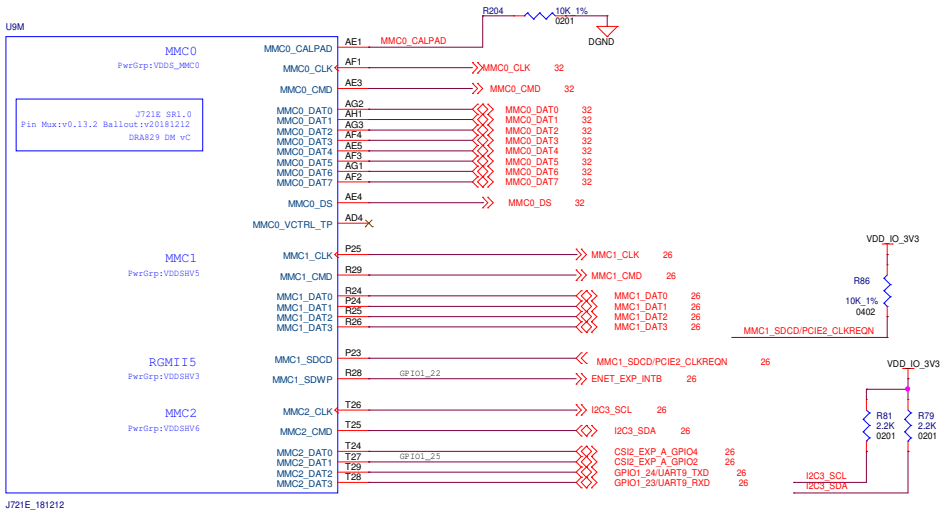


Project : J7 EVM	TEXAS INSTRUMENTS	Title: MLB,CSI&DSI_INTERFACE
		Size: C — TIDEP-01020 — Rev: E5
		Date: Friday, June 12, 2020 — Sheet 8 of 36

SERDES

Project : J7 EVM	TEXAS INSTRUMENTS	Title: SERDES_INTERFACE
		Size: C — TIDEP-01020 — Rev: E5
		Date: Friday, June 12, 2020 — Sheet 9 of 36

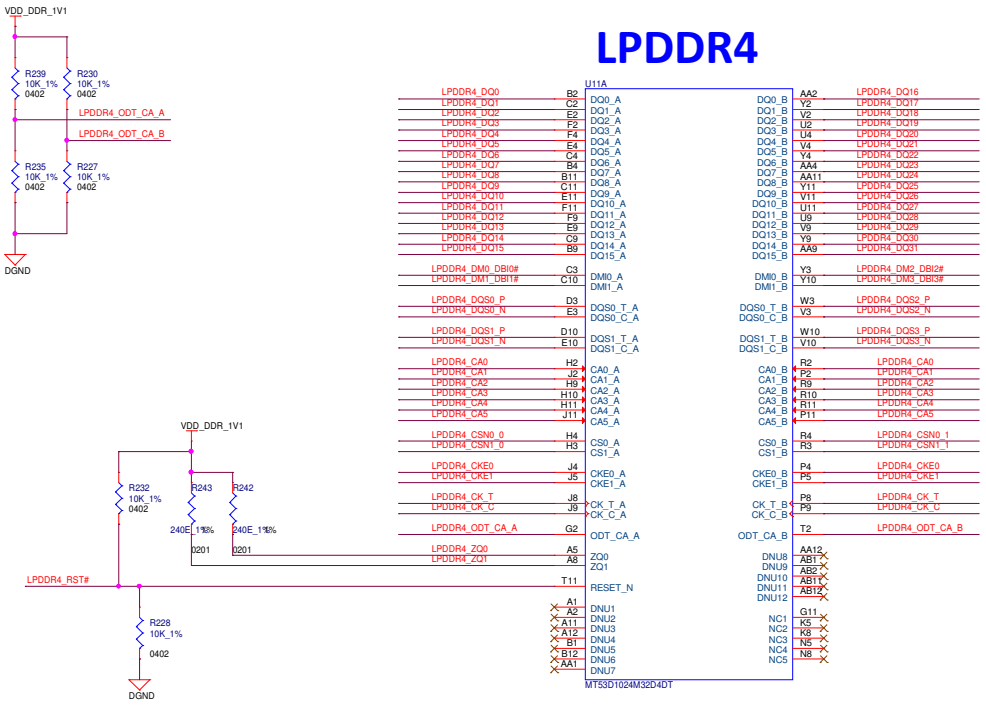
MMC Interface



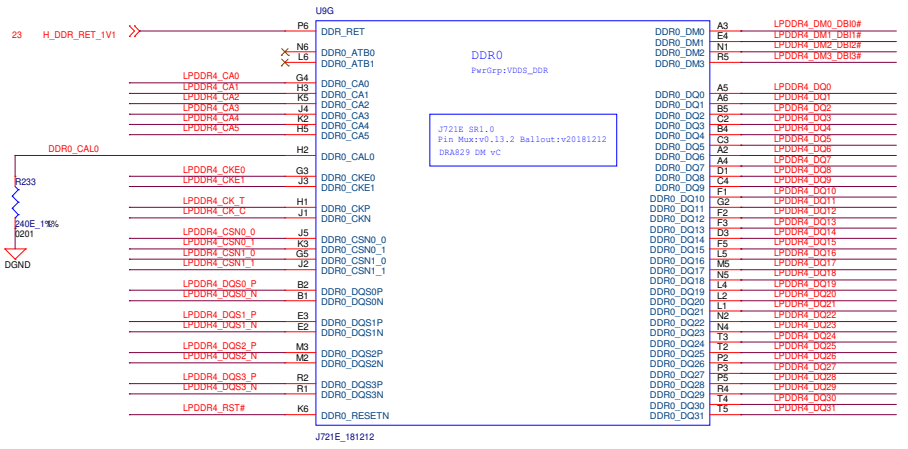
UFS Interface

Project : J7 EVM	Texas Instruments	Title: MMC,UFS_INTERFACE
		Size: C — TIDEP-01020 — Rev: E5
		Date: Friday, June 12, 2020 — Sheet 10 of 36

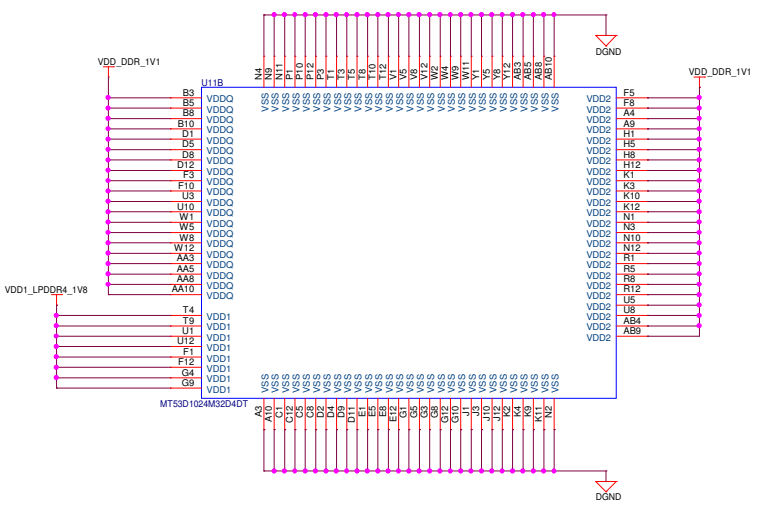
LPDDR4



EMIF



Dcap scheme needs improvement to reduce Zpk vs F (WiP)



Project : J7 EVM

TEXAS INSTRUMENTS

Title: LPDDR4

Size: C | TIDEP-01020 | Rev: E5

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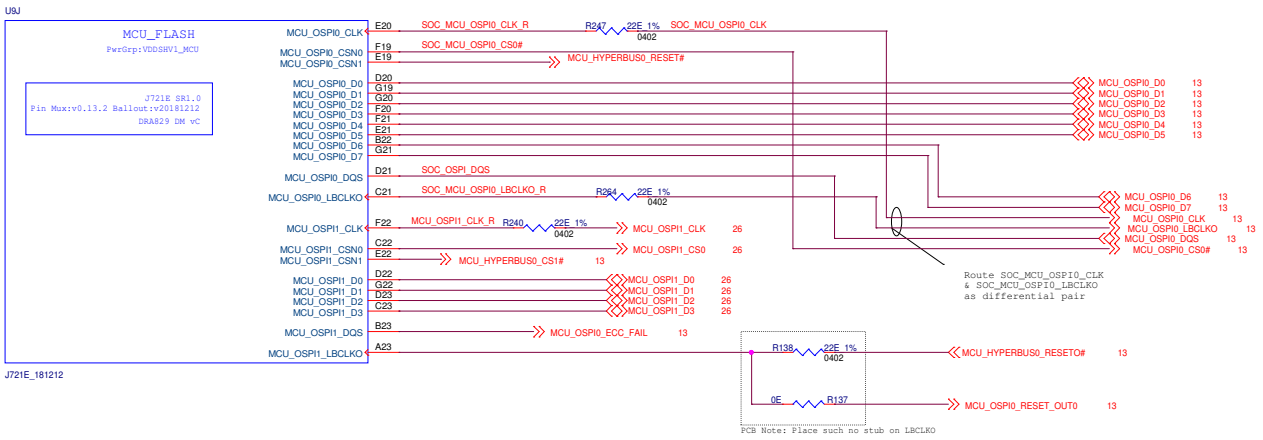
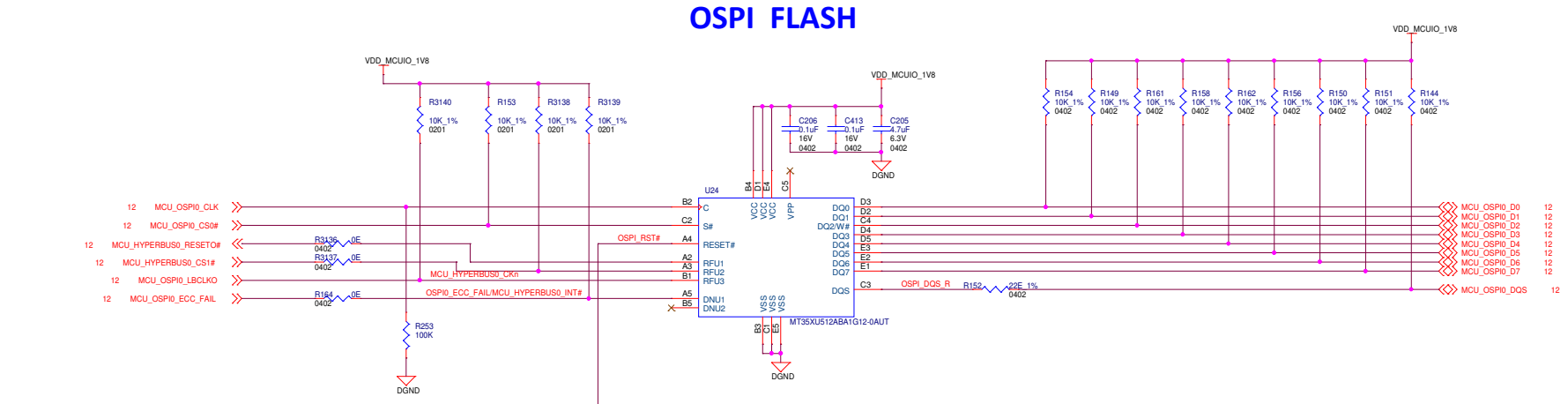
MCU FLASH

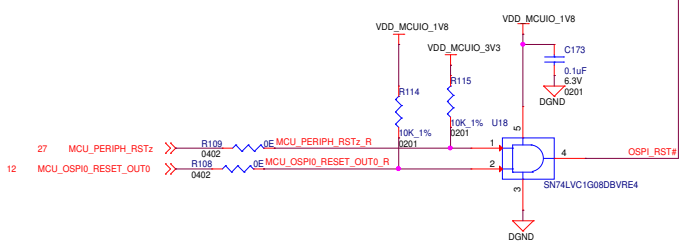


Project : J7 EVM	TEXAS INSTRUMENTS	Title: SOC_OSPI
		Size: C — TIDEP-01020 — Rev: E5
		Date: Friday, June 12, 2020 — Sheet 12 of 36

OSPI FLASH

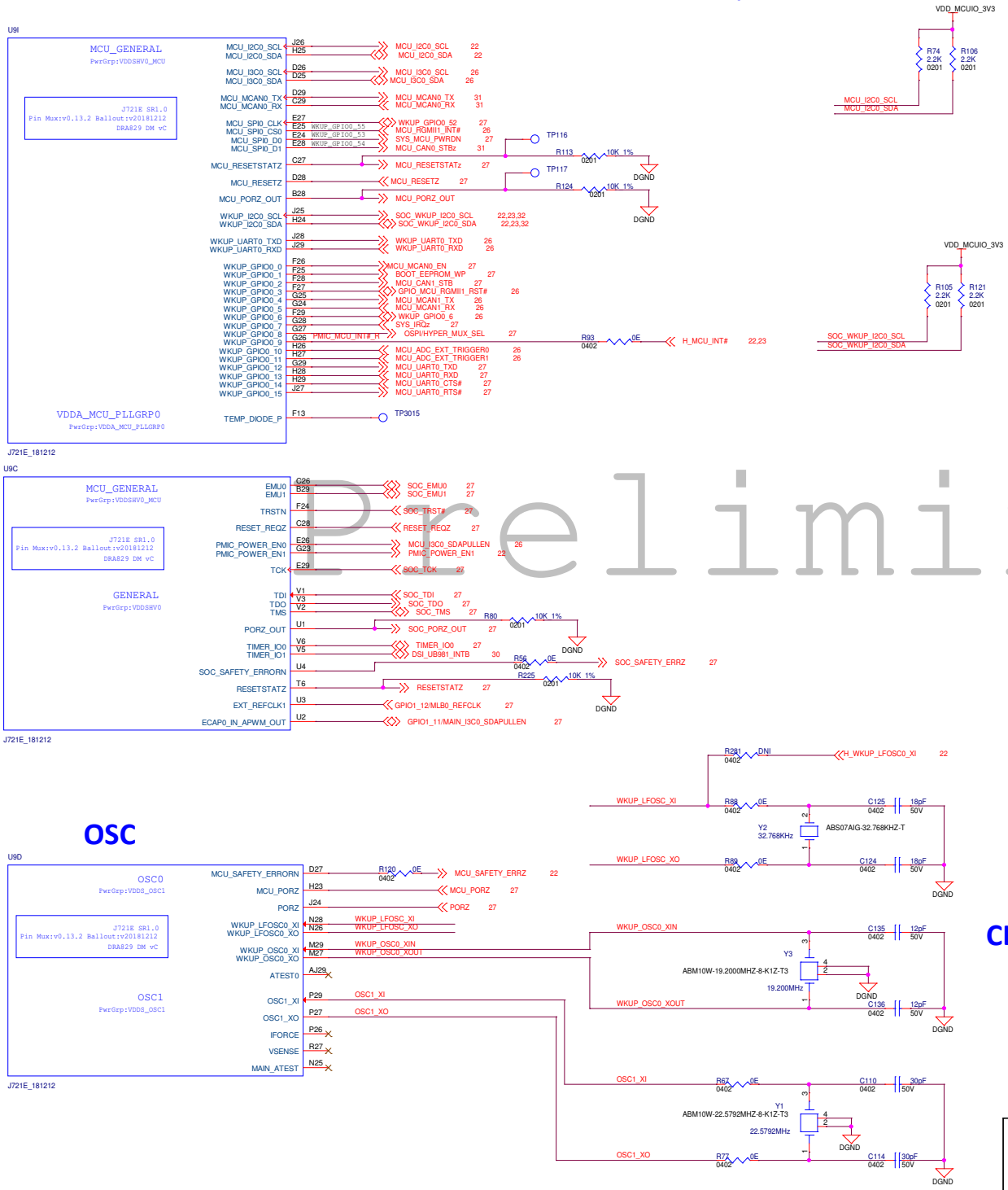


OSPI FLASH RESET



Project : J7 EVM	TEXAS INSTRUMENTS	Title: OSPIFLASH/HYPERFLAS/HYPERRAM	
		Size: C	TIDEP-01020 — Rev: E5
		Date: Friday, June 12, 2020	Sheet 13 of 36

MCU & MAIN GENERAL IO, OSC CLKS



Project : J7 EVM	TEXAS INSTRUMENTS	Title: SOC_GENERAL&MCU_GENERAL
		Size: C — TIDEP-01020 — Rev: E5
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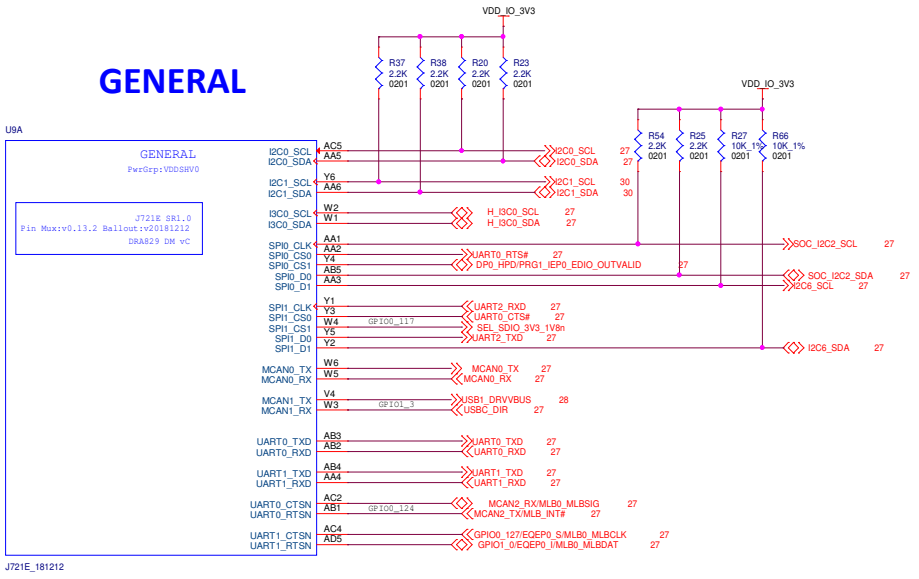
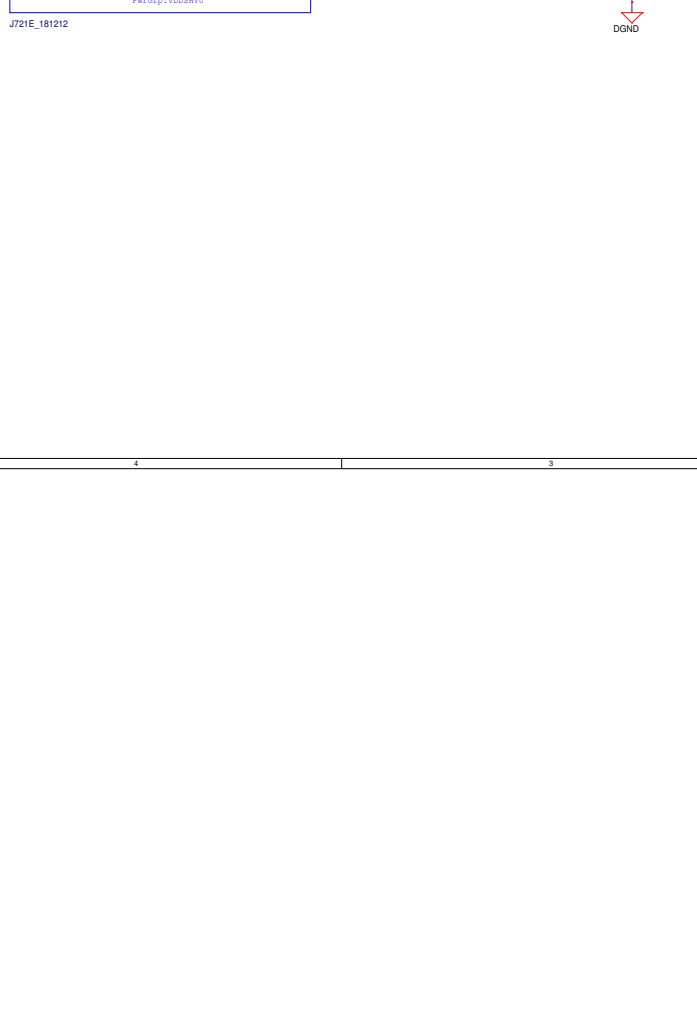
GENERAL

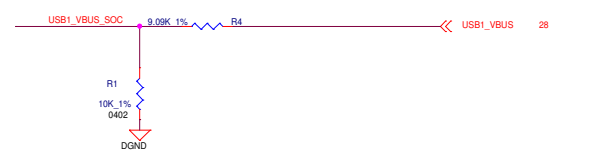


USB

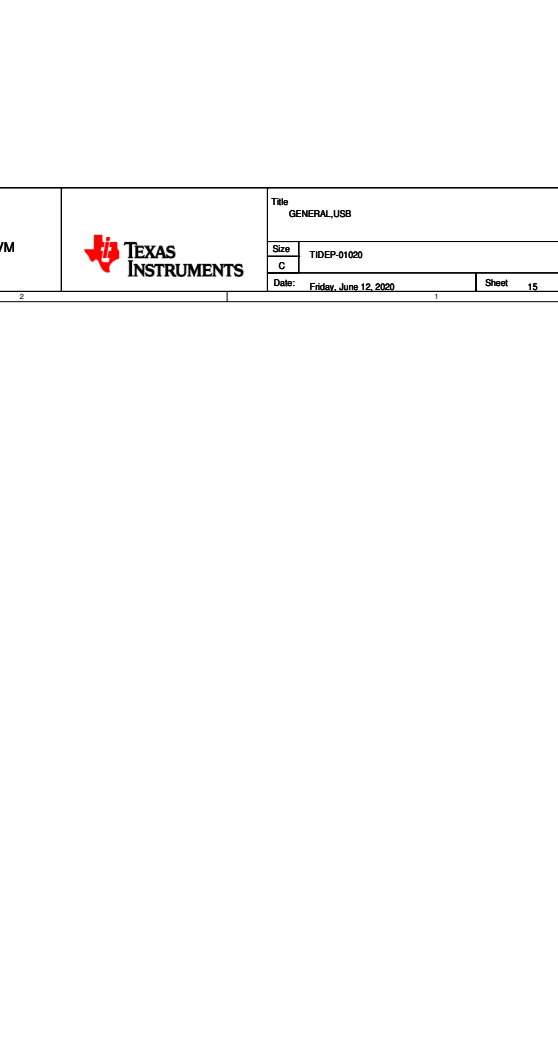


USB VBUS Resistor divider circuit

Note: Recommended VBUS circuit for USB connector. Supports 5V-30V VBUS



Note: Recommended VBUS circuit for embedded Hub



Project : J7 EVM	TEXAS INSTRUMENTS	Title: GENERAL,USB	
		Size: C	TIDEP-01020 — Rev: E5
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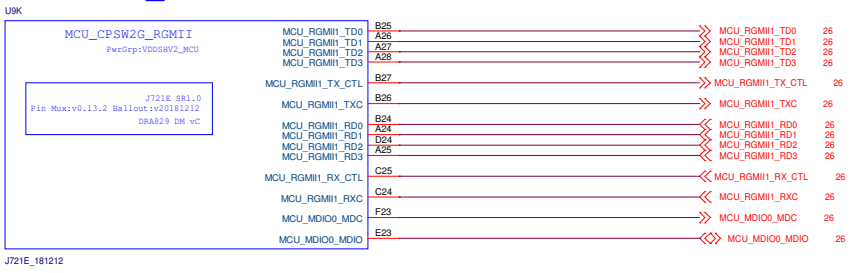
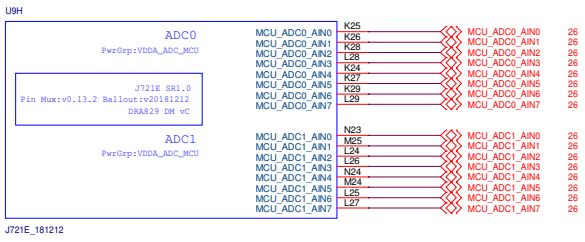
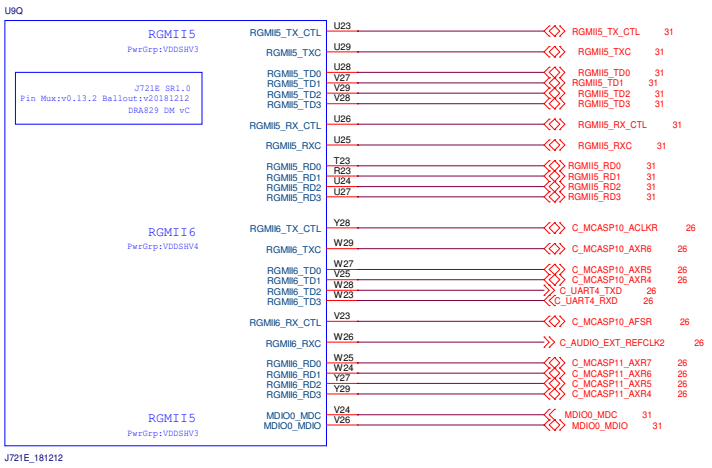
MCU_RGMII



MCU ADCs

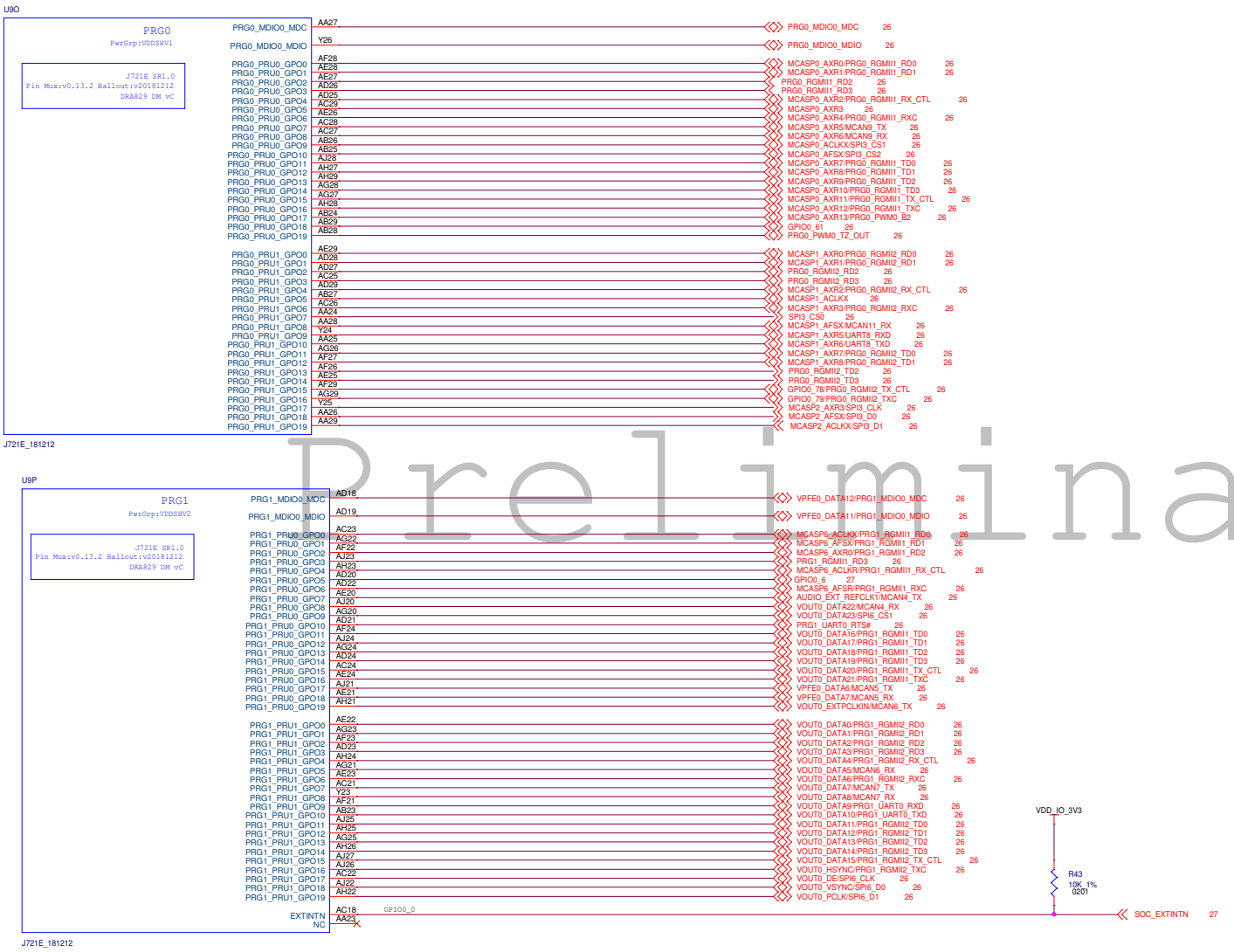


MAIN RGMII



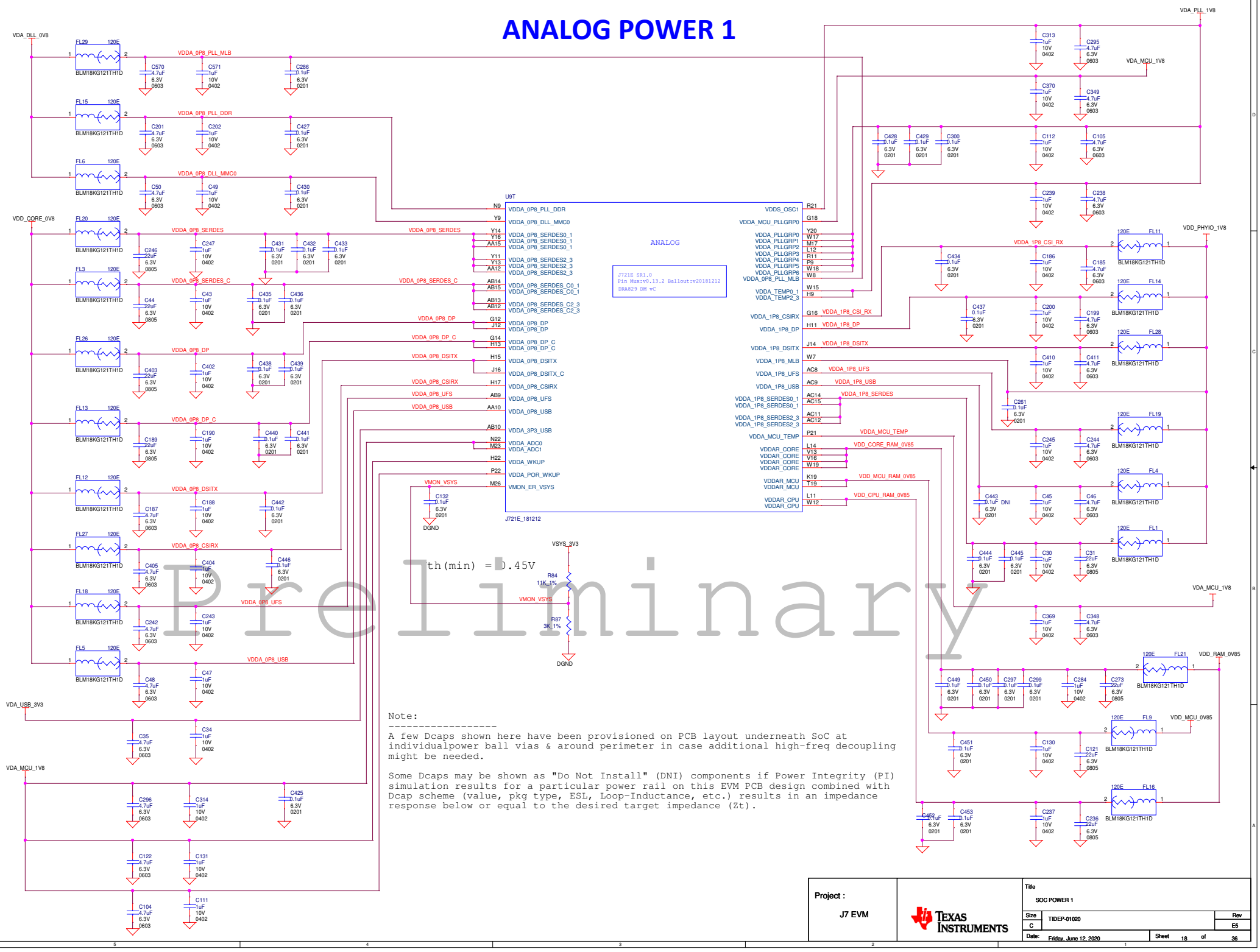
Project : J7 EVM	TEXAS INSTRUMENTS	Title: MCU_RGMII&MCU_ADC
	Size: C	TIDEP-01020 — Rev: E5
	Date: Friday, June 12, 2020	Sheet 16 of 36

PRG0 & PRG1



Project : J7 EVM	TEXAS INSTRUMENTS	Title: PRG
	Size: C — TIDEP-01020	Rev: E5
	Date: Friday, June 12, 2020	Sheet 17 of 36

ANALOG POWER 1



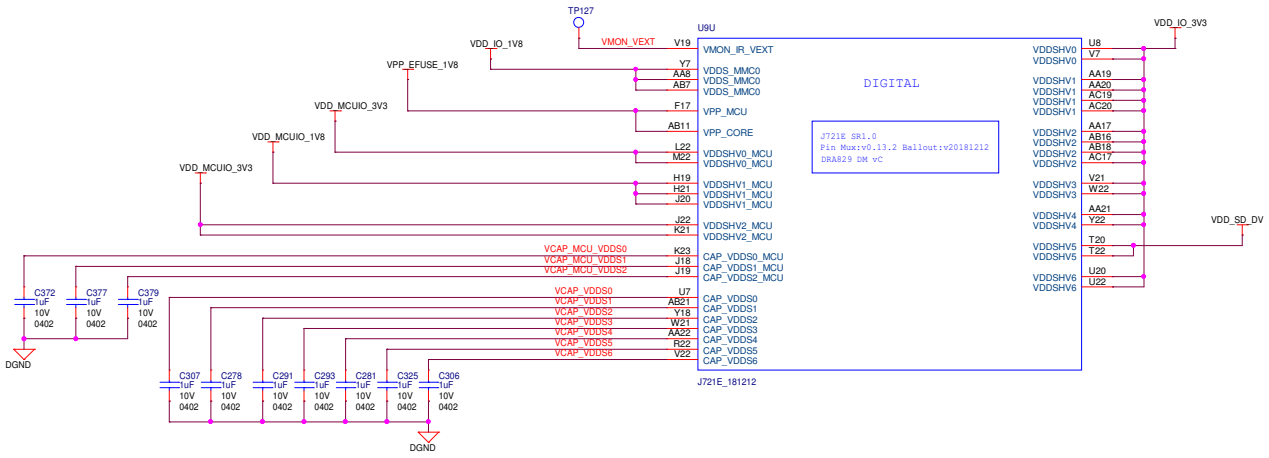
Note:

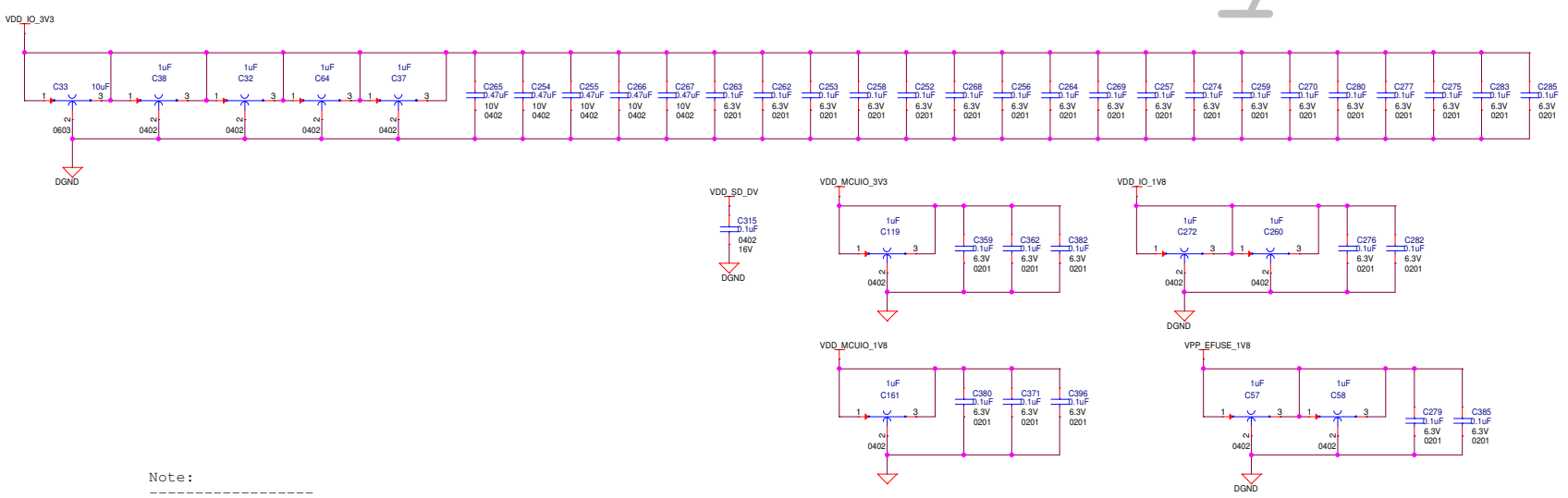
A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individualpower ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

Project : J7 EVM	TEXAS INSTRUMENTS	Title: SOC POWER 1 Size: C — TIDEP-01020 — Rev: E5 Date: Friday, June 12, 2020 — Sheet 18 of 36

DIGITAL POWER 2





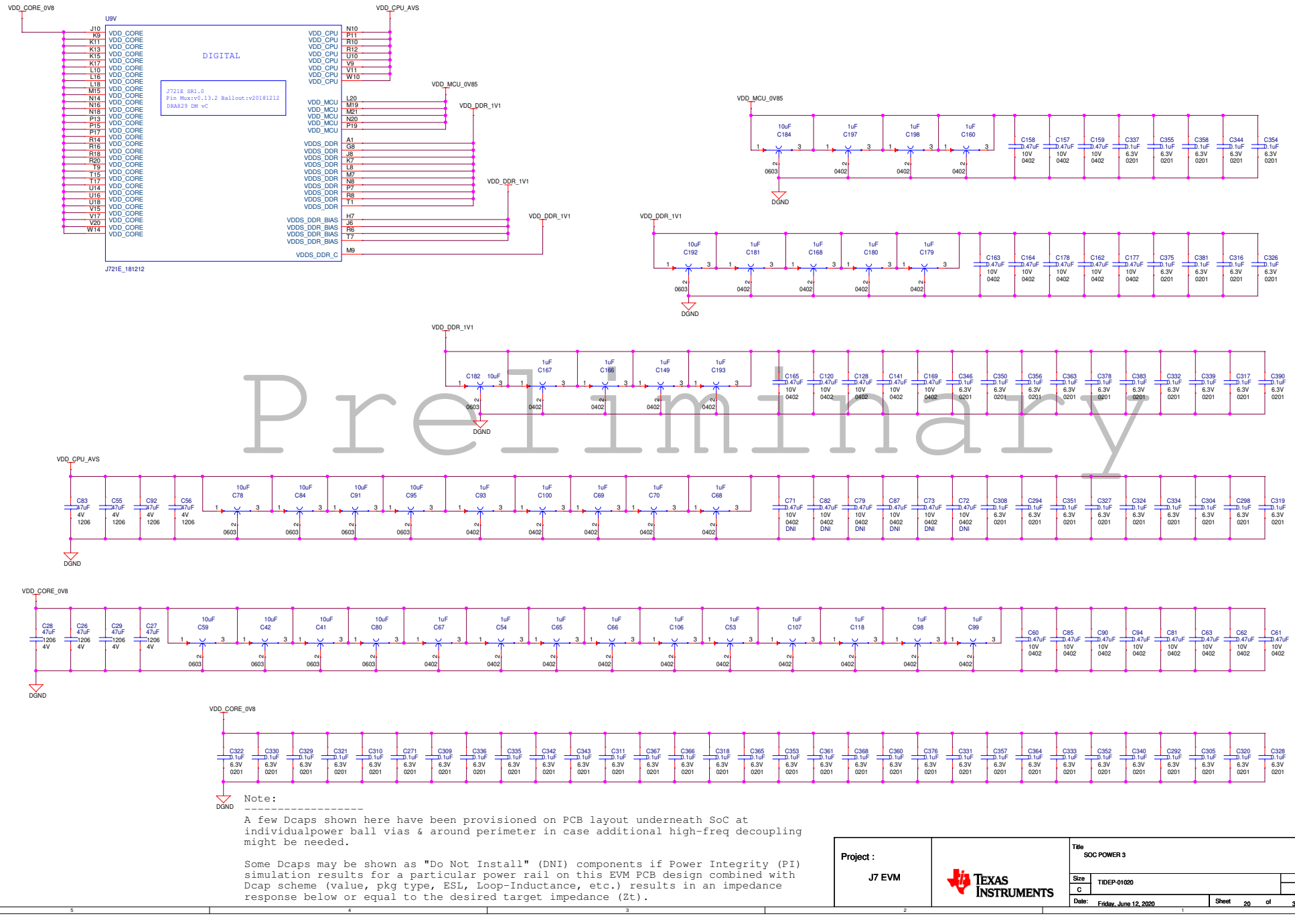
Note:

A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individualpower ball vias & around perimeter in case additional high-freq decoupling might be needed.

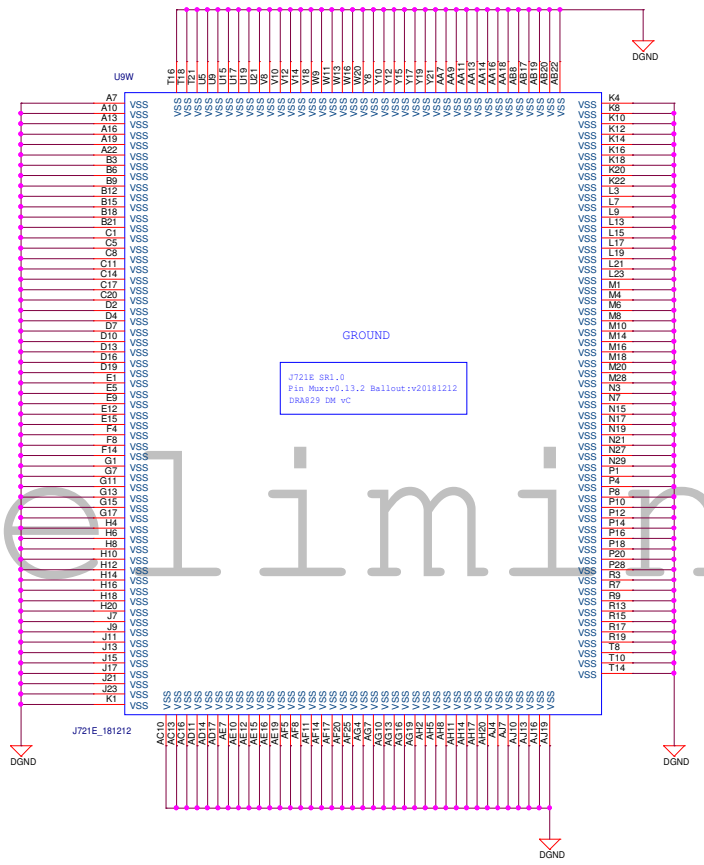
Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

Project : J7 EVM	TEXAS INSTRUMENTS	Title: SOC POWER 2 Size: C — TIDEP-01020 — Rev: E5 Date: Friday, June 12, 2020 — Sheet 19 of 36

DIGITAL POWER 3



SOC GROUND

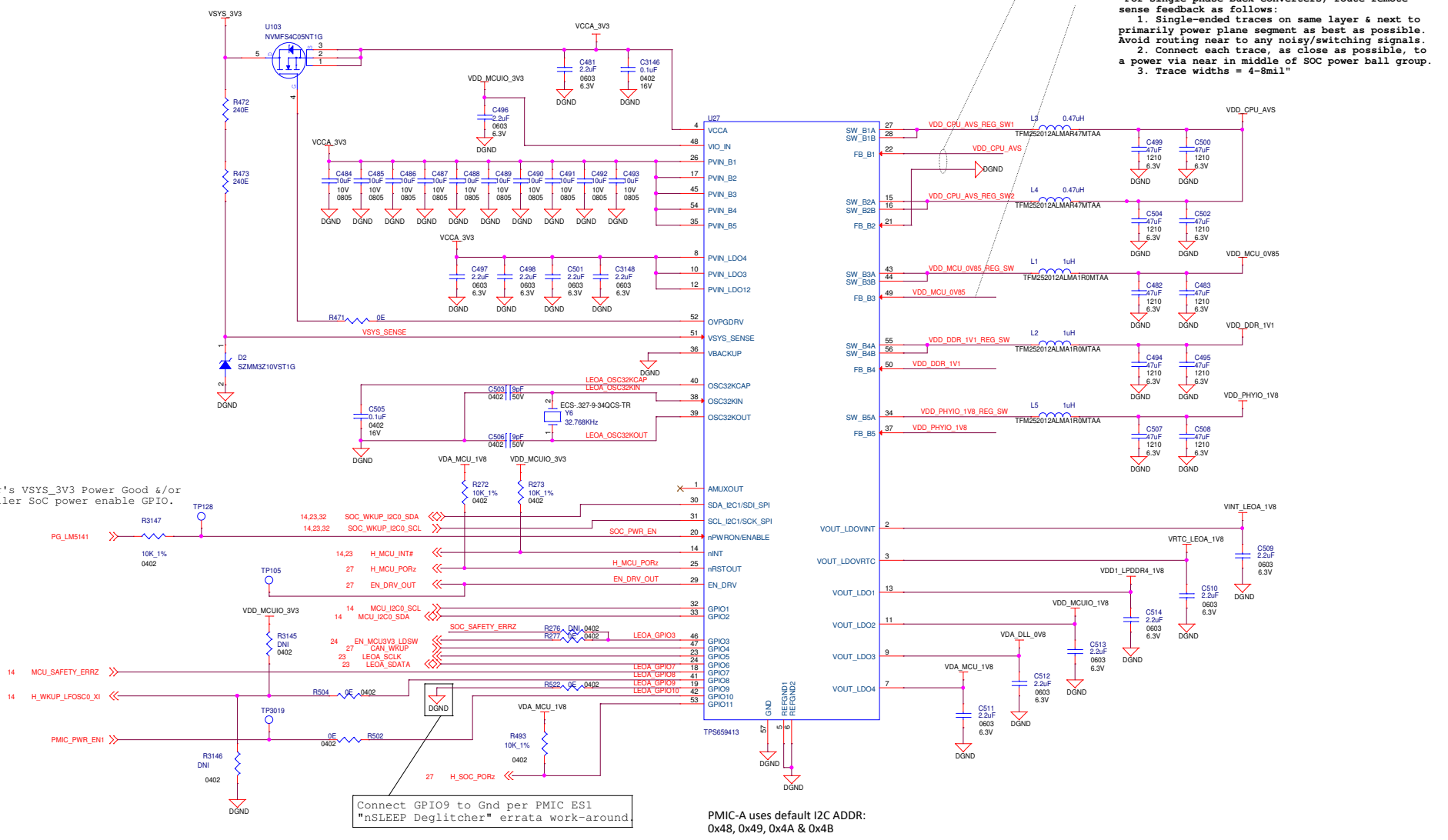


Project : J7 EVM	TEXAS INSTRUMENTS	Title: SOC GROUND
		Size: C — TIDEP-01020 — Rev: E5
		Date: Friday, June 12, 2020 — Sheet 21 of 36

PMIC- A

"PCB Notes:
For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd vias or across Dcap in middle of SOC power ball group.
3. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible while

For single-phase Buck converters, route remote sense feedback as follows:
1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"



1st Stage Cnvtr's VSYS_3V3 Power Good &/or from a uController SoC power enable GPIO.

Connect GPIO9 to Gnd per PMIC ES1 "nSLEEP Deglitcher" errata work-around.

PMIC-A uses default I2C ADDR: 0x48, 0x49, 0x4A & 0x4B

PMIC-A, GPIO8 can be used either for "Watch Dog Disable" (high) or Low Freq (32kHz) PMIC generated clk for SoC instead of local 32kHz crystal osc. If using same PMIC-A NVM as J7ES EVM, then GPIO8's default functiion is Watch Dog Disable. For system supporting Functional Safety, normal operation would install a pull-down resistor to keep PMIC Watch Dog Timer functionality enabled. Alternatively, a pull-up resistor could be installed if product is in development &/or debug and Functional Safety features are not needed.

PMIC-A, GPIO10 has net PMIC_PWR_EN1 connecting to SoC MCU through series R to allow PMIC power resource control during debug if needed via emualtor.

Project : J7 EVM

Texas Instruments

Title: POWER SUPPLY 1

Size: C | TIDEP-01020 | Rev: E5

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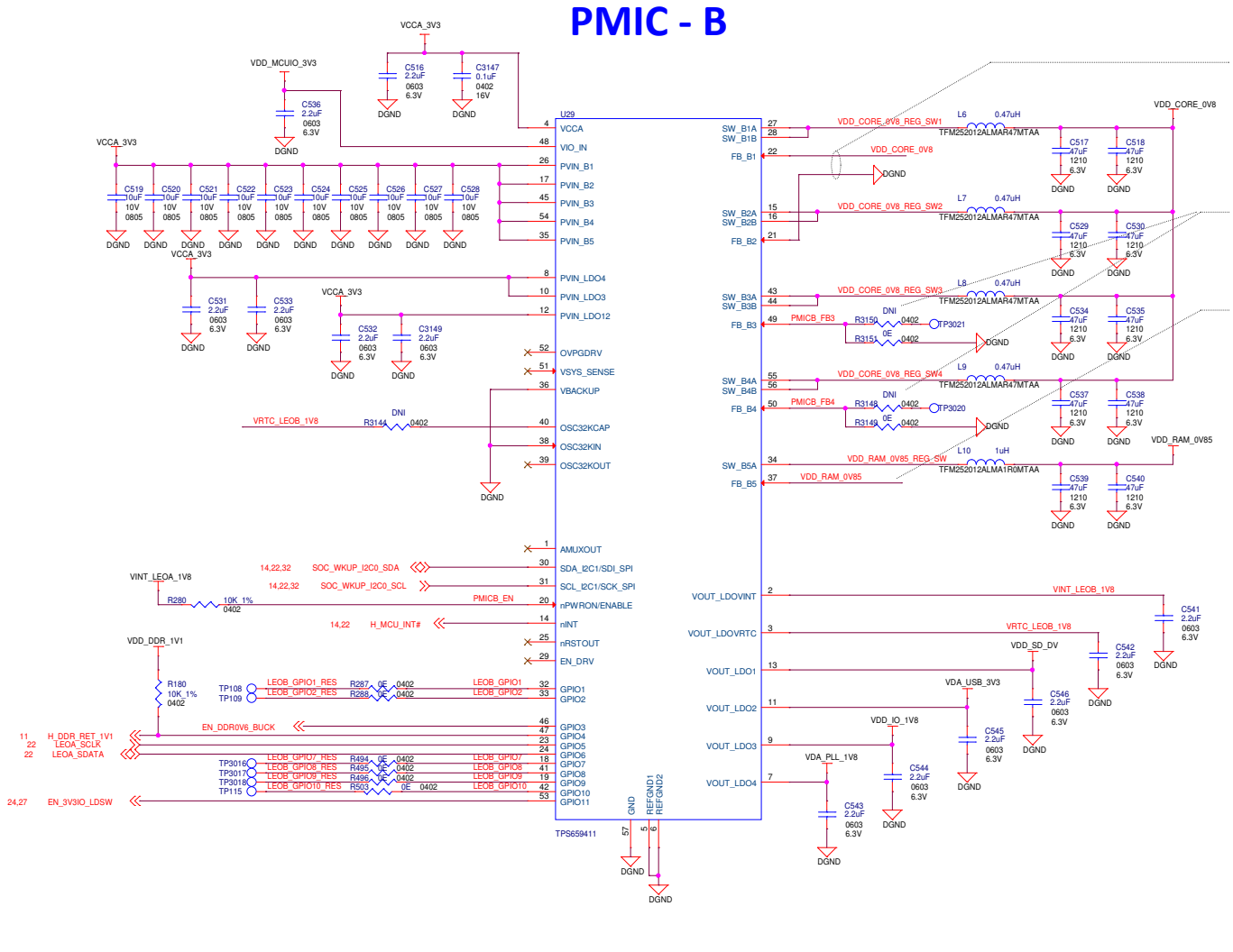
PMIC - B



PCB Note:
For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd vias or across Dcap in middle of SOC power ball group.
3. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible while

SCH Note:
1. For 3 & 4 phase Buck converter configs, the unused feedback sense inputs on Buck 3 & 4 can be optionally re-assigned to provide additional "external voltage monitoring" for functional safety coverage, see PMIC data sheet for details.

PCB Note:
For single-phase Buck converters, route remote sense feedback as follows:
1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"

PMIC-B uses NVM to set I2C ADDR:
0x4C, 0x4D, 0x4E & 0x4F

Project : J7 EVM	TEXAS INSTRUMENTS	Title: POWER SUPPLY 2
		Size: C — TIDEP-01020 — Rev: E5
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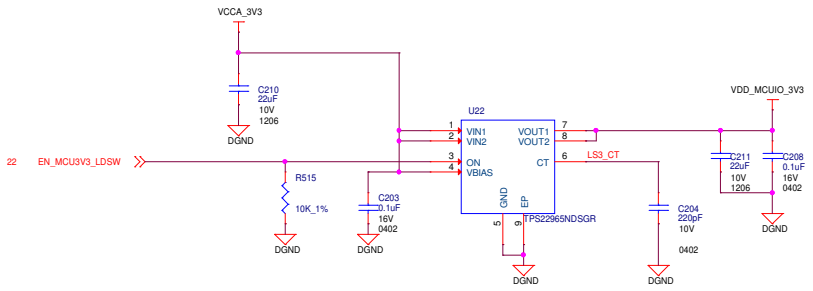
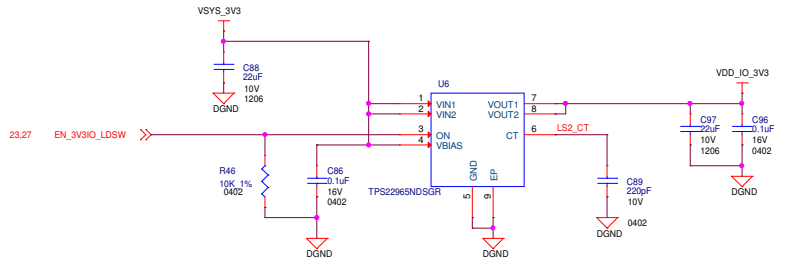
LOAD SWITCHES

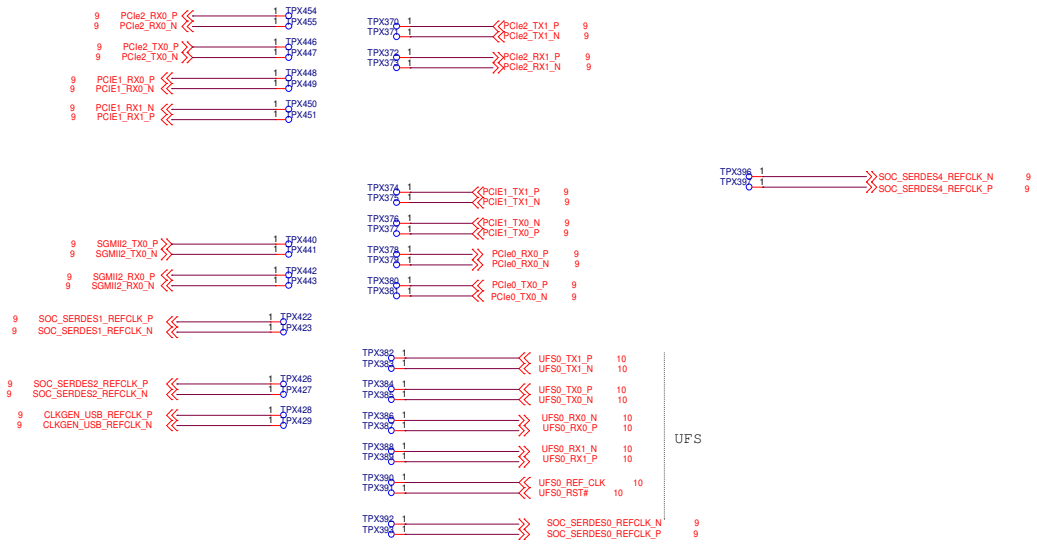




DGND

Project : J7 EVM	TEXAS INSTRUMENTS	Title: POWER SUPPLY 3
		Size: C — TIDEP-01020 — Rev: E5
		Date: Tuesday, June 16, 2020 — Sheet 24 of 36

SOM to COMM PROC SERDES CONNECTORS



Project : J7 EVM	TEXAS INSTRUMENTS	Title: SOM B-B MOLEX CONNECTORS	
		Size: C — TIDEP-01020	Rev: E5
		Date: Friday, June 12, 2020	Sheet 25 of 36

SOM to COMM PROC PRIMARY CONN #1

Project : J7 EVM	TEXAS INSTRUMENTS	Title: SOM B-B SAMTEC CONN#1	
		Size: C	TIDEP-01020 — Rev: E5
		Date: Friday, June 12, 2020	Sheet 26 of 36

SOM to COMM PROC PRIMARY CONN #2

TPX203 SOC_I2C2_SDA 15
TPX204 GPIO0_127/EQEP0_S/MLB0_MLBCLK 15
TPX205 DP0_HPD/PRG1_IEP0_EDIO_OUTVALID 15
TPX206 SOC_EXTINTN 17

TPX214 MCU_UART0_CTS# 14
TPX215 MCU_UART0_RTS# 14

TPX222 MCAN2_RX/MLB0_MLBSIG 15

TPX226 UART0_TXD 15

TPX228 GPIO1_12/MLB0_REFCLK 14
TPX230 SOC_SAFETY_ERRZ 14
TPX240 I2C6_SDA 15

TPX232 SYS_IRQz 14
TPX233 OSPI/HYPER_MUX_SEL 14

TPX243 GPIO1_0/EQEP0_I/MLB0_MLBDAT 15

TPX248 UART2_TXD 15
TPX249 UART1_RXD 15

TPX253 WKUP_GPIO0_52 14

TPX255 H_I3C0_SCL 15
TPX256 GPIO1_11/MAIN_I3C0_SDAPULLEN 14

TPX258 MCU_UART0_RXD 14
TPX259 MCU_MCAN0_EN 14

TPX265 I2C0_SCL 15

TPX270 MCAN0_RX 15

TPX274 UART0_RTS# 15
TPX275 WKUP_GPIO0_1 BOOT_EEPROM_WP 14

TPX278 SOC_PORZ_OUT 14
TPX279 EN_DRV_OUT 22

TPX291 I2C0_SDA 15
TPX292 I2C6_SCL 15

TPX293 MCAN0_TX 15
TPX294 USBC_DIR 15

TPX295 H_MCU_PORz 22
TPX296 SOC_I2C2_SCL 15

TPX298 CAN_WKUPn UART2_RXD 15

TPX301 H_I3C0_SDA 15

TPX312 UART1_TXD 15
TPX313 UART0_CTS# 15

TPX315 TIMER_IO0 14

TPX318 MCU_UART0_TXD 14

TPX323 GPIO0_6 17
TPX324 WKUP_GPIO0_2 MCU_CAN1_STB 14

TPX333 MLB0_MLBDAT_N 8
TPX334 MLB0_MLBDAT_P 8

TPX337 UART0_RXD 15

TPX347 CSI1_RXCLK_N 8
TPX348 CSI1_RXCLK_P 8

TPX283 CSI1_RX3_N 8
TPX284 CSI1_RX3_P 8

TPX368 CSI1_RX2_N 8
TPX369 CSI1_RX2_P 8

TPX239 CSI1_RX1_N 8
TPX240 CSI1_RX1_P 8

TPX327 CSI1_RX0_N 8
TPX328 CSI1_RX0_P 8

TPX351 MLB0_MLBCLK_N 8
TPX352 MLB0_MLBCLK_P 8

TPX353 MLB0_MLBSIG_P 8
TPX354 MLB0_MLBSIG_N 8

TPX357 [GPIO0_124] MCAN2_TX/MLB_INT# 15

TPX208 RESETSTATz 14
TPX217 SYS_MCU_PWRDN 14
TPX234 H_SOC_PORz 22
TPX299 CAN_WKUP 22
TPX282 [SoC PORz In] PORz 14
TPX67 MCU_PERIPH_RSTz 13
TPX92 MCU_RESETSTATz 14
TPX192 SOC_WARMRESET# RESET_REQz 14
TPX193 [MCU Warm Reset In] MCU_RESETz 14
TPX165 MCU_PORZ 14

TCK,TRSTn,EMU0,EMU1 ON VDDSHV0_MCU POWER DOMAIN.
TMS,TDI,TDO ON VDDSHV0 POWER DOMAIN.
ISOLATE TMS,TDI,TDO TO PREVENT EMULATOR
DRIVING INTO SOC WHEN VDDSHV0 IS OFF.
TCK,TRSTn,EMU0/1 DRIVE CONTROLLED BY
VDDSHV0_MCU (I.E. VREF_DBG).

VDD_MCUIO_3V3
R3143 100
R1207 4.7K
R1206 4.7K
R1208 4.7K
R3135 0
R1205 0

XDS560v2(default jtag support)

J1011
MIPI-QSH-030

1	VREF_DBG	TMS	2
3	TCK	TDO	4
5	TDI	nRESET	6
7	RTCK	TRSTPD	8
9	nTRST	EXTE	10
11	EXTF	VREF_TR	12
13	TR_CLK0	TR_CLK1	14
15	TGT_DETECT	Gnd16	16
17	TRD0.0	TRD1.0	18
19	TRD0.1	TRD1.1	20
21	TRD0.2	TRD1.2	22
23	TRD0.3	TRD1.3	24
25	TRD0.4	TRD1.4	26
27	TRD0.5	TRD1.5	28
29	TRD0.6	TRD1.6	30
31	TRD0.7	TRD1.7	32
33	TRD0.8	TRD1.8	34
35	TRD0.9	TRD1.9	36
37	TRD3.0	TRD2.0	38
39	TRD3.1	TRD2.1	40
41	TRD3.2	TRD2.2	42
43	TRD3.3	TRD2.3	44
45	TRD3.4	TRD2.4	46
47	TRD3.5	TRD2.5	48
49	TRD3.6	TRD2.6	50
51	TRD3.7	TRD2.7	52
53	TRD3.8	TRD2.8	54
55	TRD3.9	TRD2.9	56
57	Gnd57	Gnd58	58
59	TR_CLK3	TR_CLK2	60
61	GndCt1	GndCt2	62
63	GndCt3	GndCt4	64

14 SOC_TCK
27 EXT_TDI
14 SOC_EMU0
14 SOC_EMU1
EMU0
EMU1
EXT_TMS 27
EXT_TDO 27
EMU_RSTn

XDS560V2 OPEN-DRAIN, PULLUP AT DESTINATION TO APPROPRIATE VOLTAGE LEVEL IF USED.

VDD_MCUIO_3V3
R1209 4.7K
nTRST
TRSTPD
RJ1025 0.A
SOC_TRST# 14
R1221 4.7K
TRSTn == MIPI TRSTPD PULL DOWN VERSION
TRSTn == MIPI nTRST MIPI PULLUP VERSION
FOR CJTAG SET THE RJ TO PINS 3-2.

VSYS_3V3
R625 10K
Q13 BSS138
23,24 EN_3V3IO_LDSW
DOUBLE CHECK VOLTAGE LEVEL ON EN_3V3IO_LDSW AND PULLDOWN.

VSYS_3V3
27 EXT_TDI
U131 74CBTLV1G125CRG4
SOC_TDI 14

VDD_IO_3V3
R1219 4.7K
VSYS_3V3
C3145 0.1uF
27 EXT_TMS
U129 74CBTLV1G125CRG4
SOC_TMS 14

VSYS_3V3
14 SOC_TDO
U130 74CBTLV1G125CRG4
EXT_TDO 27

Project : J7 EVM

TEXAS INSTRUMENTS

Title: SOM B-B SAMTEC CONN#2
Size: C
TIDEP-01020
Rev: E5
Date: Friday, June 12, 2020
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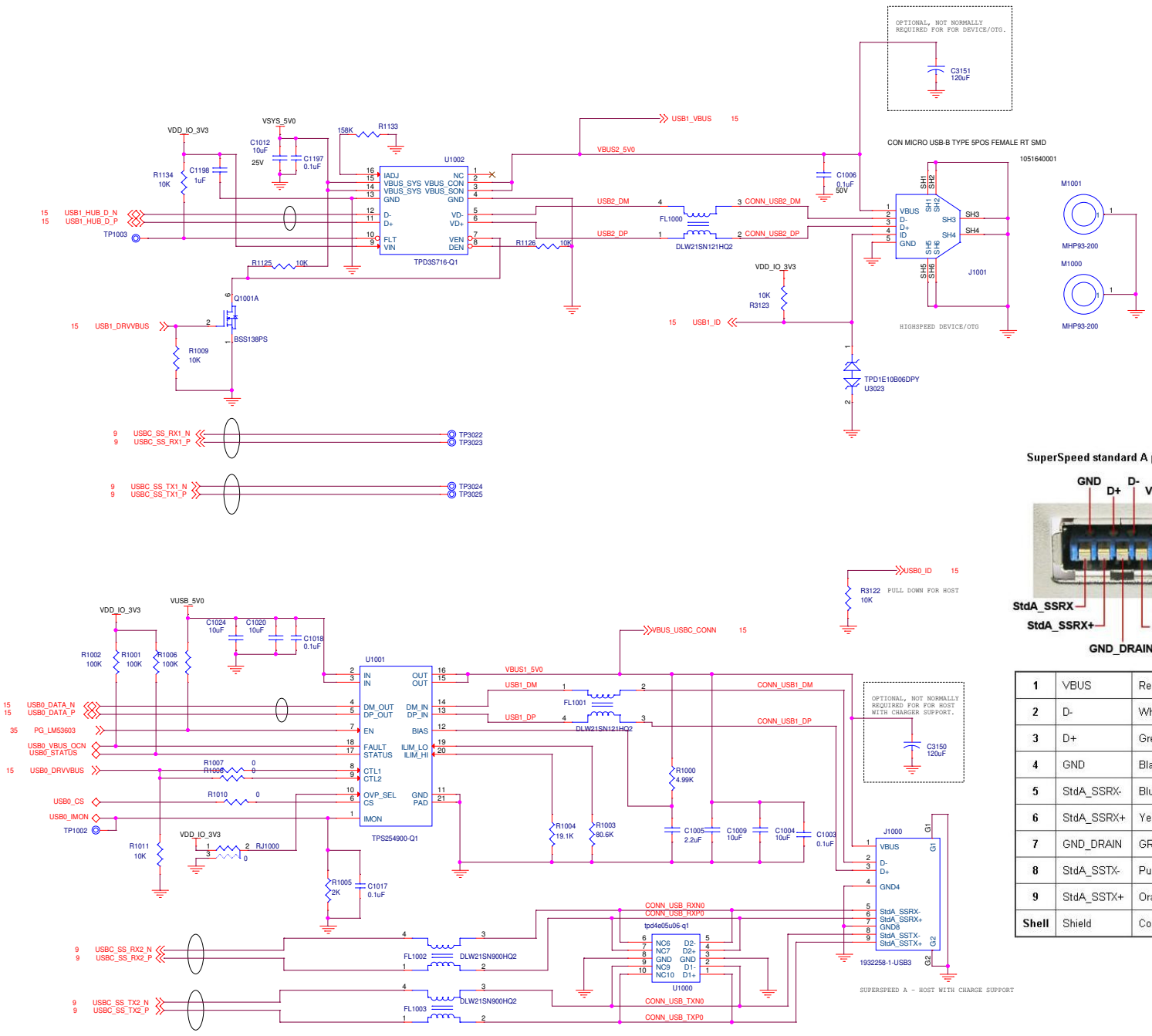
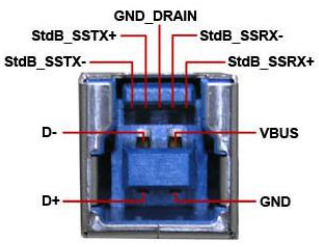


SuperSpeed standard A plug pinout

1	VBUS	Red
2	D-	White
3	D+	Green
4	GND	Black
5	StdA_SSRX-	Blue
6	StdA_SSRX+	Yellow
7	GND_DRAIN	GROUND
8	StdA_SSTX-	Purple
9	StdA_SSTX+	Orange
Shell	Shield	Connector Shell

SuperSpeed standard B plug pinout



1	VBUS	Red
2	D-	White
3	D+	Green
4	GND	Black
5	StdA_SSTX-	Blue
6	StdA_SSTX+	Yellow
7	GND_DRAIN	GROUND
8	StdA_SSRX-	Purple
9	StdA_SSRX+	Orange
Shell	Shield	Connector Shell

TEXAS INSTRUMENTS INCORPORATED

Title:	DRA71x LCARD CPU Board		
Page Contents:	USB MEDIA		
Size: C	DOC NO: TIDEP-01020	REV: B	
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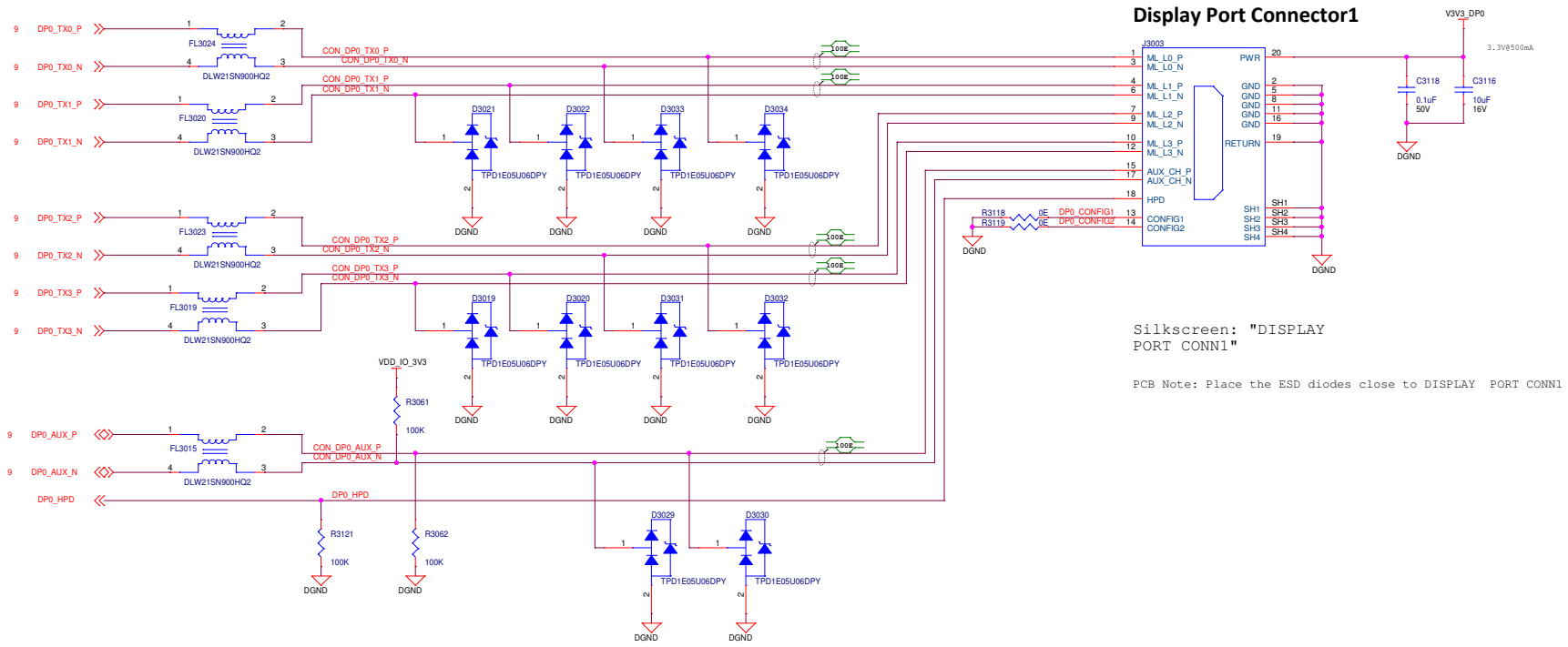
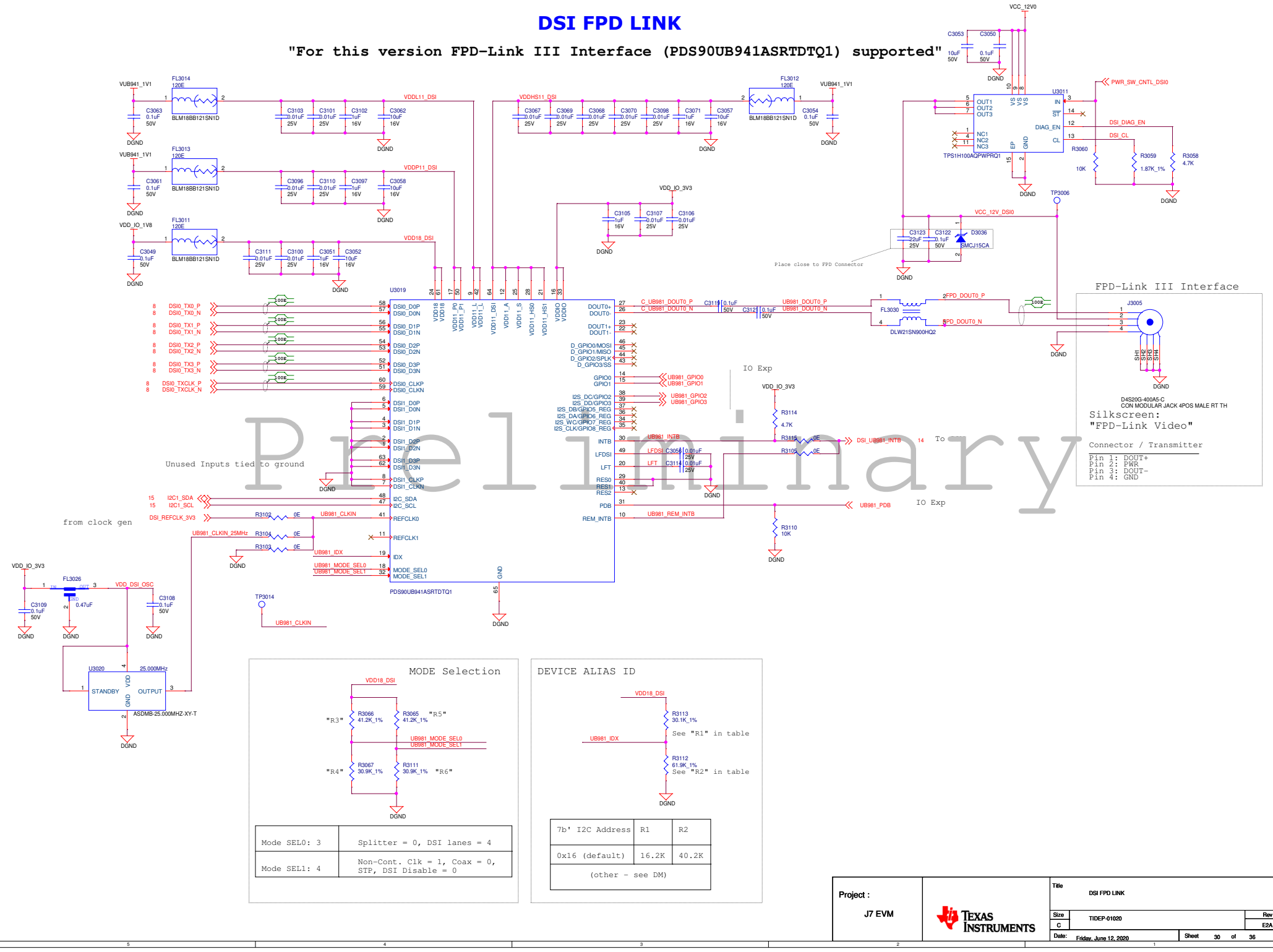
DISPLAY PORT INTERFACE



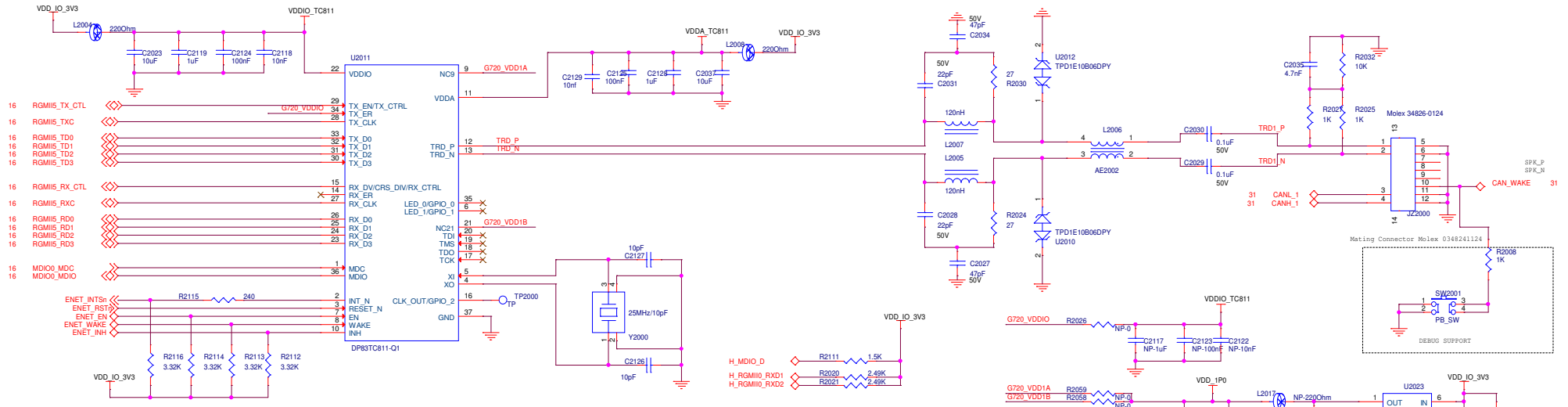
Project : J7 EVM	TEXAS INSTRUMENTS	Title: DISPLAY PORT INTERFACE
		Size: C — TIDEP-01020 — Rev: E2A
		Date: Friday, June 12, 2020 — Sheet 29 of 36

DSI FPD LINK

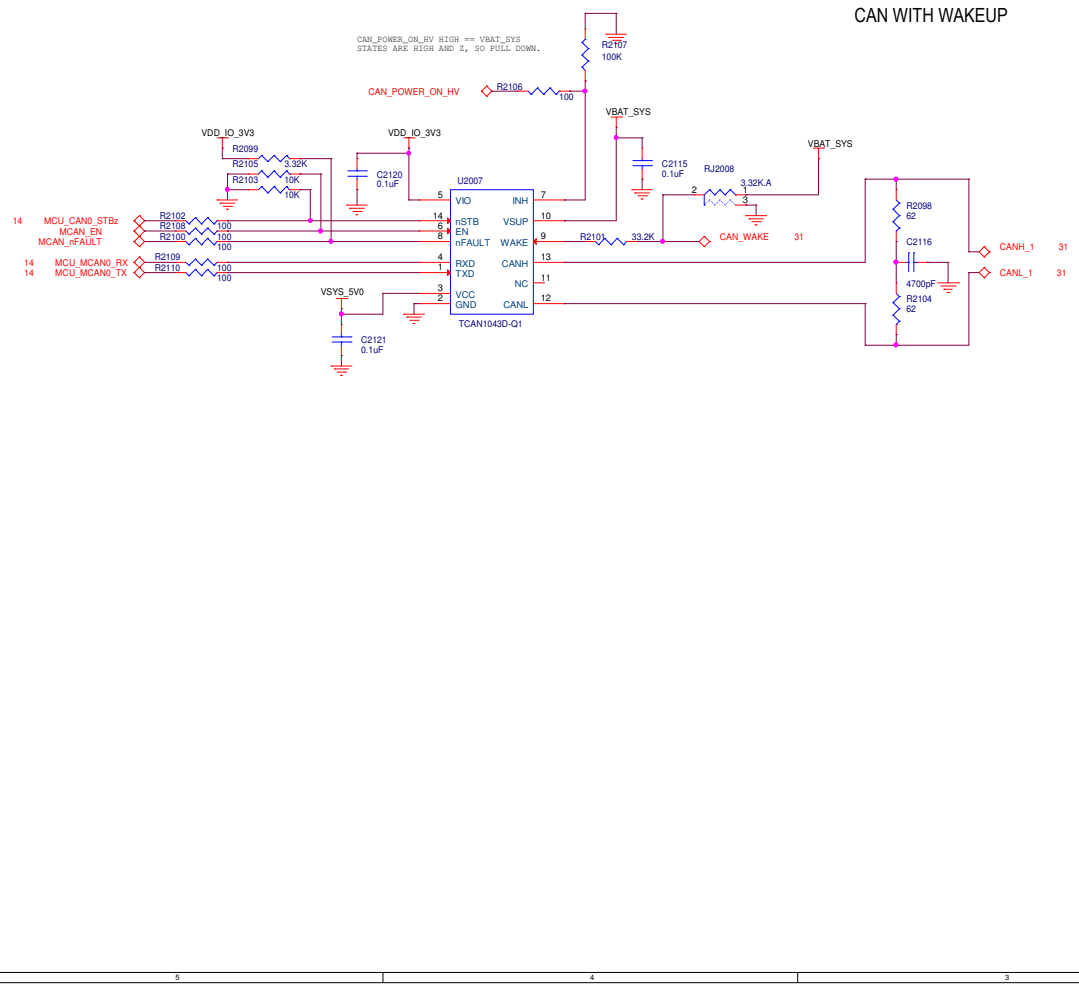
"For this version FPD-Link III Interface (PDS90UB941ASRTDTQ1) supported"



ENET - DP83TC811/DP83TG720 (OPTION)



CAN WITH WAKEUP



TEXAS INSTRUMENTS INCORPORATED
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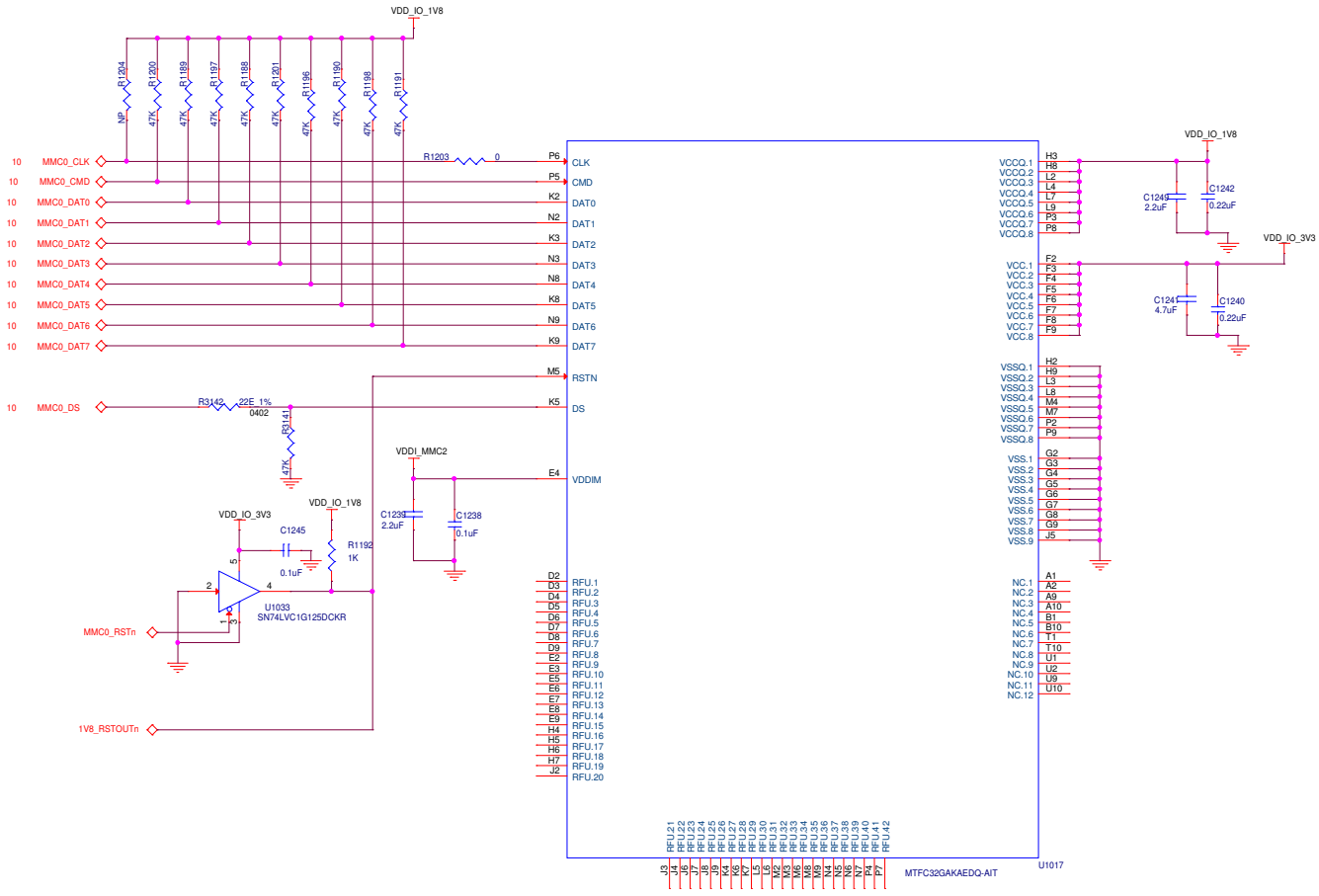
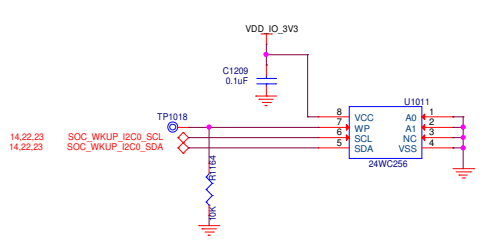
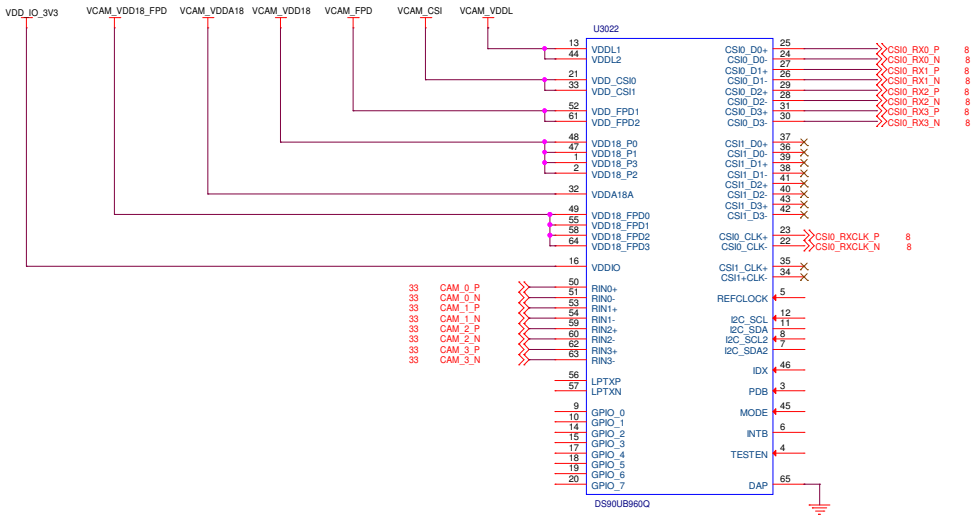
Title: DRA78x Amplifier		
Page Contents: ENET/CAN/BOOT		
Size: C	DOC NO: TIDEP-01020	REV: A
Date: Friday, June 12, 2020	Sheet 31 of 36	



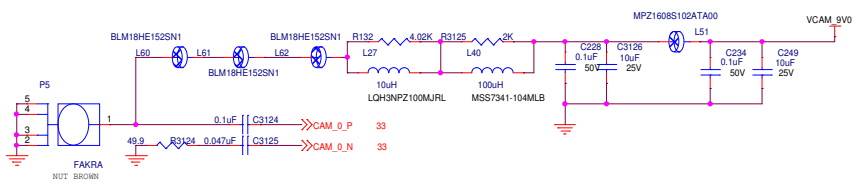


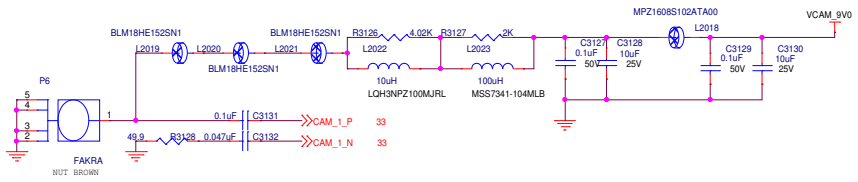
TEXAS INSTRUMENTS INCORPORATED

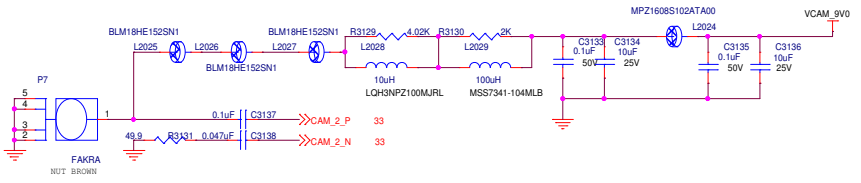
Title: DRA71x LCARD CPU Board		
Page Contents: MEM eMMC/SD CARD		
Size: C	DOC NO: TIDEP-01020	REV: B
Date: Friday, June 12, 2020	Sheet 32 of 36	

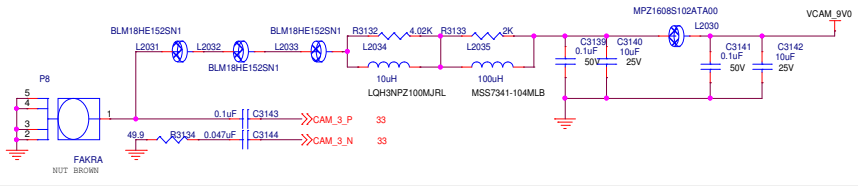


FUSION REV C, DUAL FREQ SUPPORT,
LCARD POWER 350mA@9v

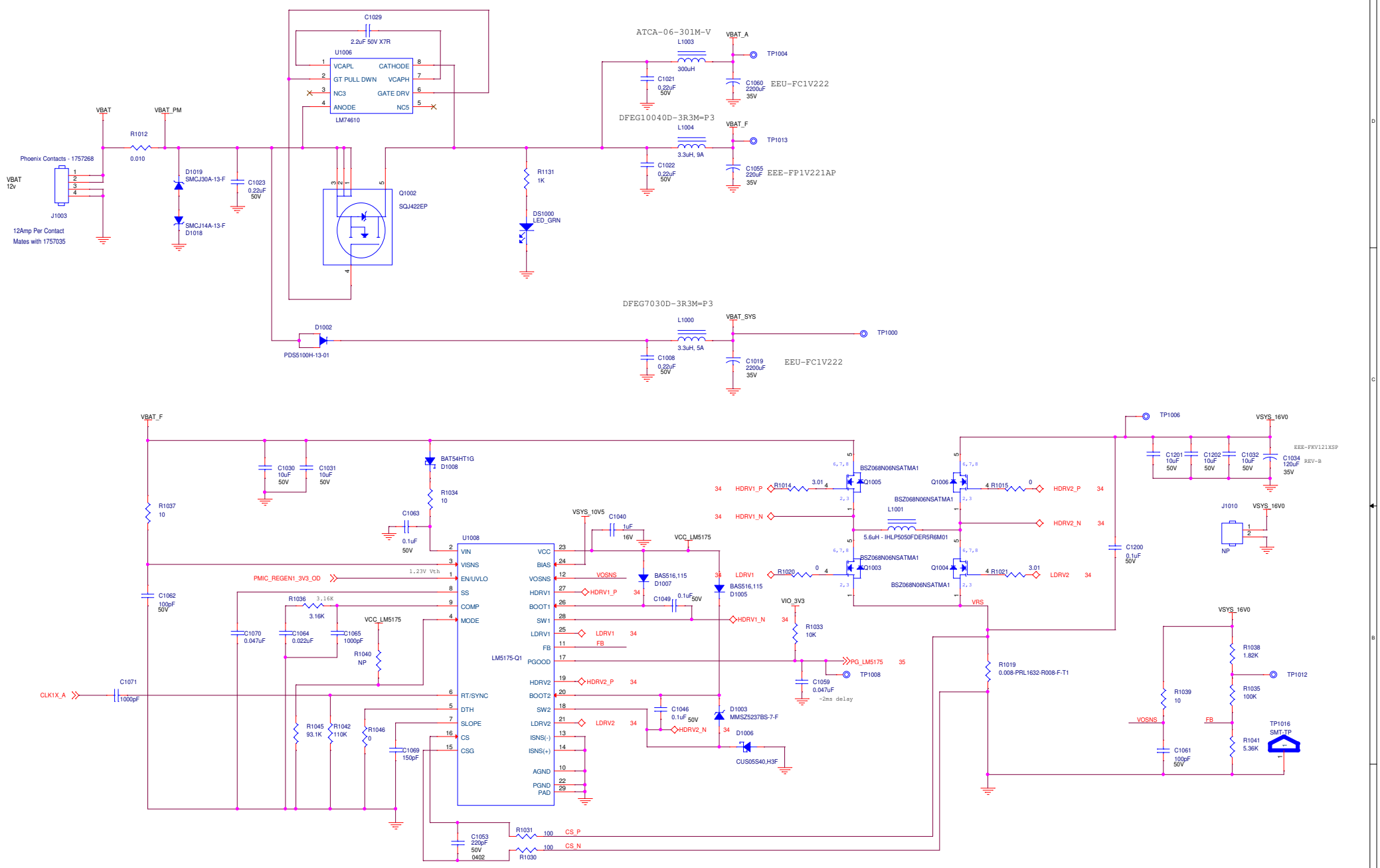




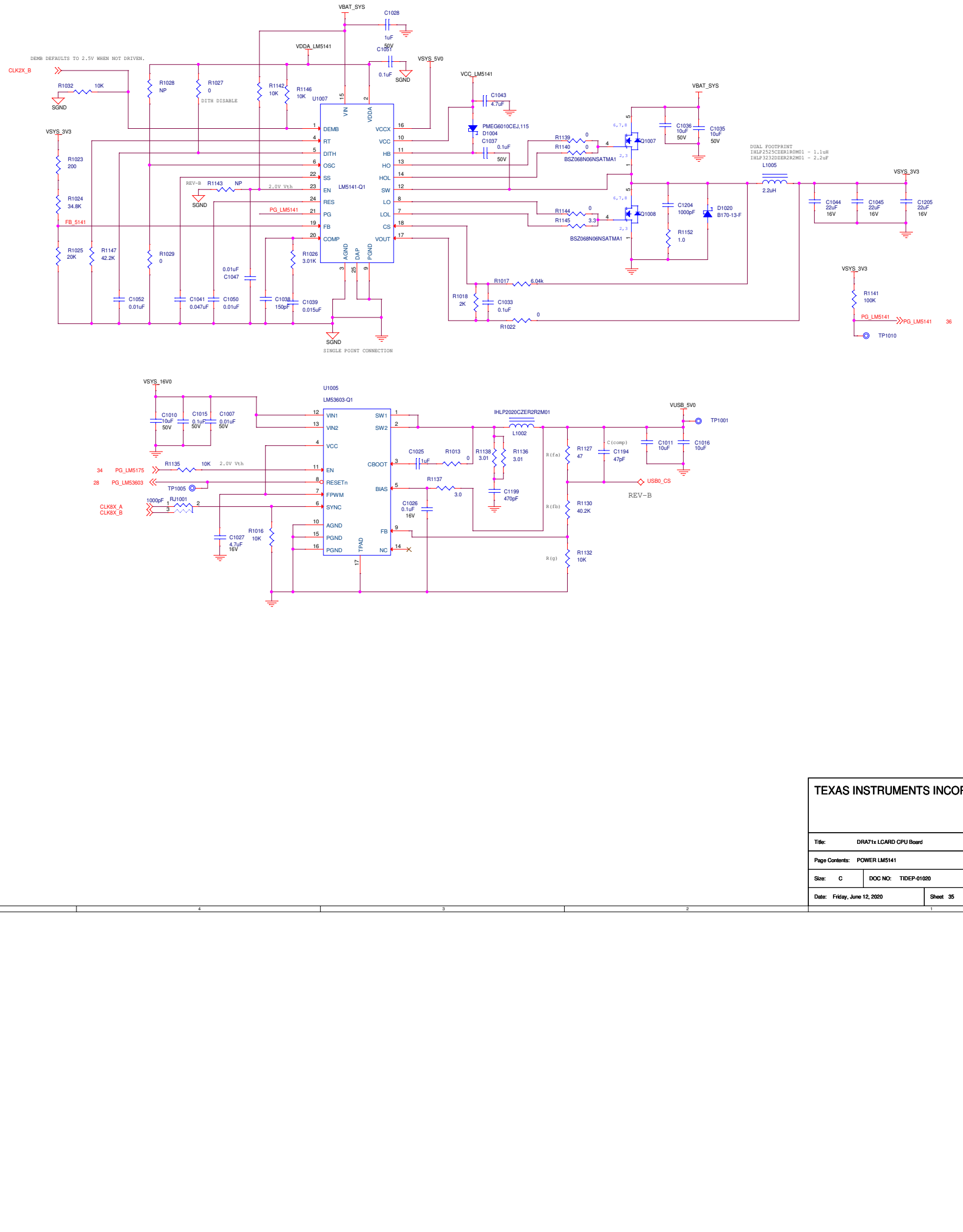




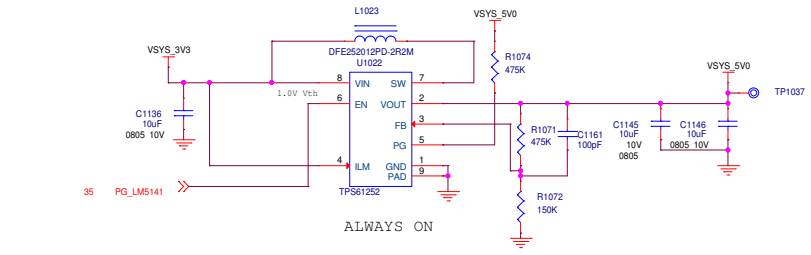
TEXAS INSTRUMENTS INCORPORATED			
Title: DRA71x LCARD CPU Board			
Page Contents: MEM eMMC/SD CARD			
Size: C	DOC NO: TIDEP-01020	REV: B	
Date: Friday, June 12, 2020	Sheet 33 of 36		

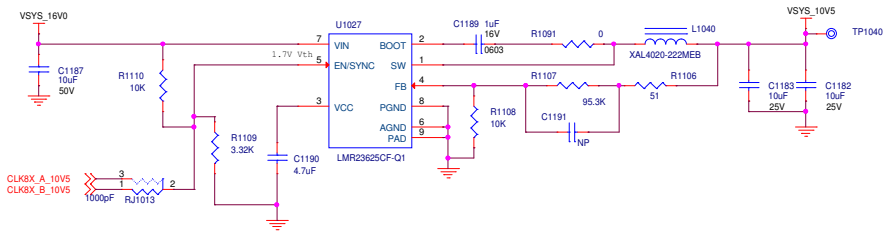


TEXAS INSTRUMENTS INCORPORATED		
Title: DRA71x LCARD CPU Board		
Page Contents: POWER LM5175		
Size: C	DOC NO: TIDEP-01020	REV: B1
Date: Friday, June 12, 2020	Sheet 34 of 36	



TEXAS INSTRUMENTS INCORPORATED	
Title:	DRA71x LCARD CPU Board
Page Contents:	POWER LM5141
Size: C	DOC NO: TIDEP-01020 REV: B1
Date: Friday, June 12, 2020	Sheet 35 of 36





TEXAS INSTRUMENTS INCORPORATED

Title:	DRA71x LCARD CPU Board		
Page Contents:	SECONDARY LDO'S/SWITCHES		
Size: C	DOC NO: TIDEP-01020	REV: B2	
Date: Tuesday, June 16, 2020	Sheet 36 of 36		

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