REV	DESCRIPTION	DATE	Author
A	INITIAL CAPTURE	10/29/2019	JAC
A1	REV A BOARD BRING UP CHANGES	12/18/2019	JAC
B	REV B BOARD BRING UP CHANGES	12/20/2019	JAC

*** DISCLAIMER ***

The SoC Reference Design Study provides SCH & PCB source files that can be used as a good starting point for new designs. Please be aware that the SCH & PCB are NOT 100% complete for implementing an End Product. An End Product's feature set will define additional required signaling and SoC interfaces. As a result, a majority of signals in this SCH are "single-pin" / "unconnected" nets.

The SoC's schematic symbol has been organized based upon each ball's "primary signaling interface". For End Products, unused primary interface signals can then be re-defined by SoC's internal muxmode controll (see Data Manual for details) to use "alternate functions" (i.e. GPIOs) to support other key system needs (i.e. interupts, debug, etc.).

Primary objectives of this Ref Design are to demonstrate:

1. 100% signal & power breakout routing of SoC using recommended PCB design rules & strategies.
2. Key high-speed signals with controlled impedance PCB routing (i.e. DDR & SERDES).
3. Power Distribution Network (PDN) with the following:
   a) Recommended SoC power solution components (2nd stage) showing preferred SoC voltage domain to power resource mapping.
   b) Optimized decoupling capacitor scheme per key power rail using only automotive qualified caps to meet SoC recommended power integrity (PI) parameters based on this specific PCB design (stack-up, placement, routing, via types, etc).
   c.) A typical 1st stage power conversion interfaced directly to input battery has been captured as an example.

Sheet # - Name

REVISION STATUS OF SHEETS

REV	A	B	B	A	A	A	A	A	A	A
SH	31	32	33	34	35	36	37	38	39	40
REV	A	A	A	A	A	A	A	A	A	B
SH	21	22	23	24	25	26	27	28	29	30
REV	A	B	A	A	A	A	A	A	A	A
SH	11	12	13	14	15	16	17	18	19	20
REV	B	B	A	A	A	B	B	A	A	A
SH	1	2	3	4	5	6	7	8	9	10

NEXT ASSY | USED ON

APPLICATION

DWN	J.A.C.	DATE 10/29/2019
CHK	T.W.K.	DATE 10/29/2019
ENGR	J.A.C.	DATE 10/29/2019
ENGR-MGR	J.A.C.	DATE 10/29/2019
QA	C.M.D.	DATE 10/29/2019
MFG	J.A.C.	DATE 10/29/2019
RLSE	J.A.C.	DATE 10/29/2019

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Preliminary Information - Subject to change

Title: J7ES CCARD		
Page Contents: Title		
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REVISION HISTORY

DATE	CHANGE	AUTHOR
01/03/2020	REV B CHANGES SHEET 6/7 UPDATE TABLES SHEET 12 NO-POP R186, MCU_OSPI1_LBCLKO AS GPIO SHEET 30 CON_DP0_AUX_N PULLUP TO 3V3 SHEET 30 ISOLATE AND ESD PROTECT DPO_HPD SHEET 32 MIRROR MCU_MCAN1_RX/TX AT U44 SHEET 33 MIRROR UB960 I2C6 SDA/SCL	TNYC
02/24/2020	SHEET 19 DELETE C656, C661, C721, C729 TO MAKE ROOM FOR 3-T UNDER SOC.	

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Title: J7ES CCARD		
Page Contents: EVM REVISION HISTORY		
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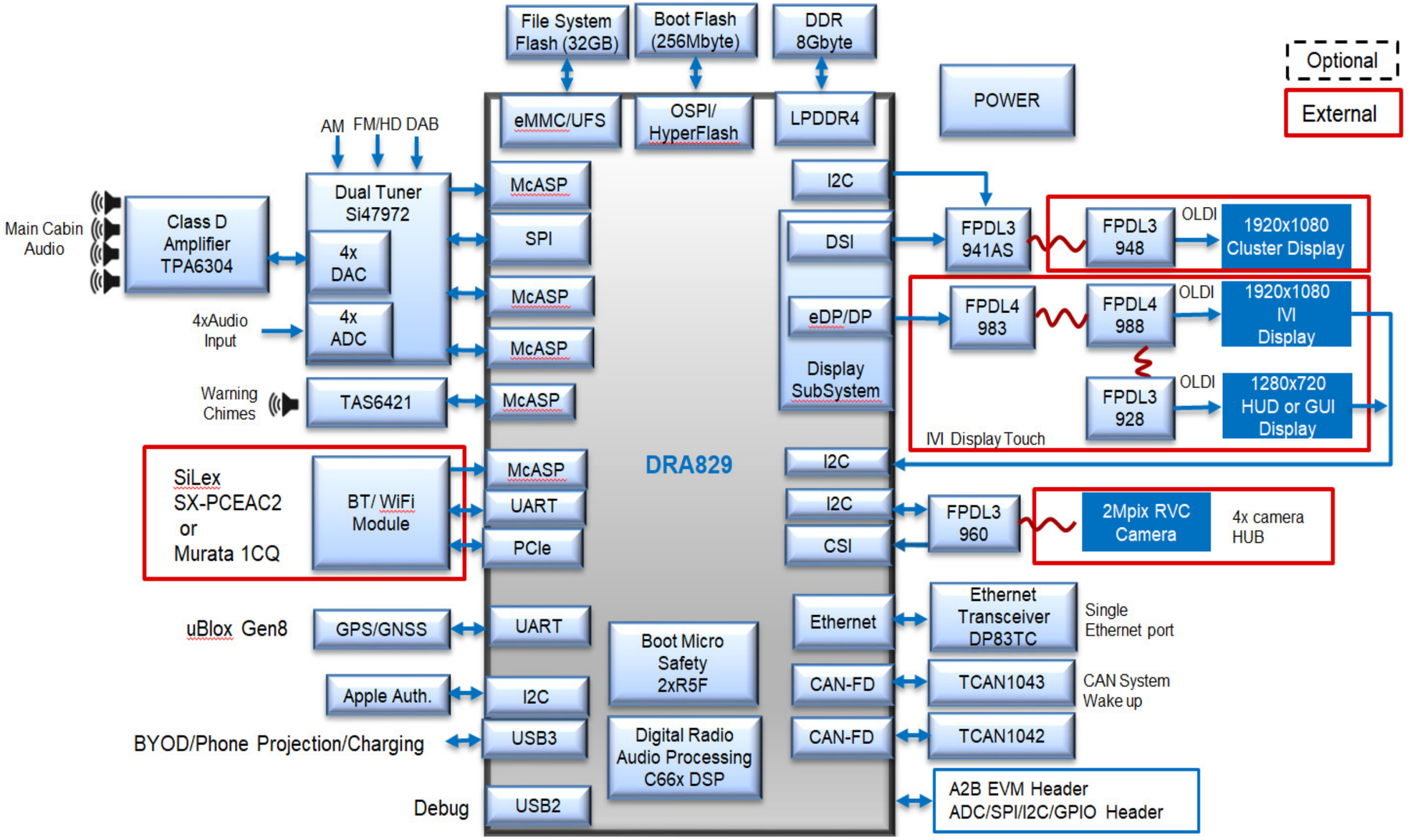

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Title: J7ES CCARD		
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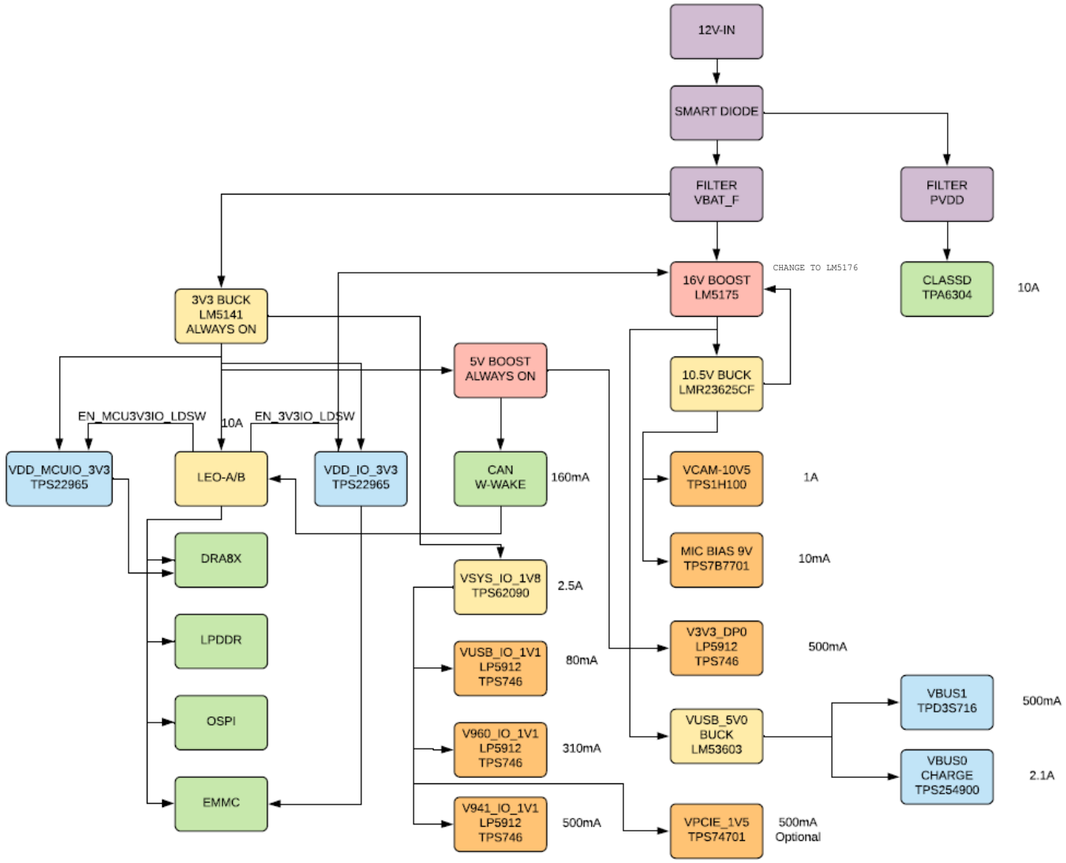

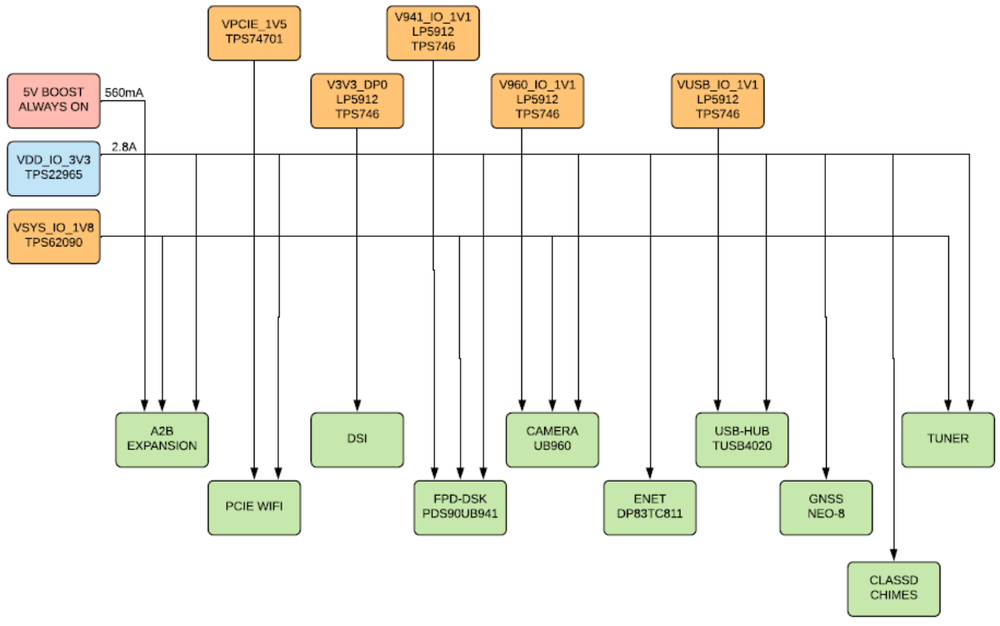

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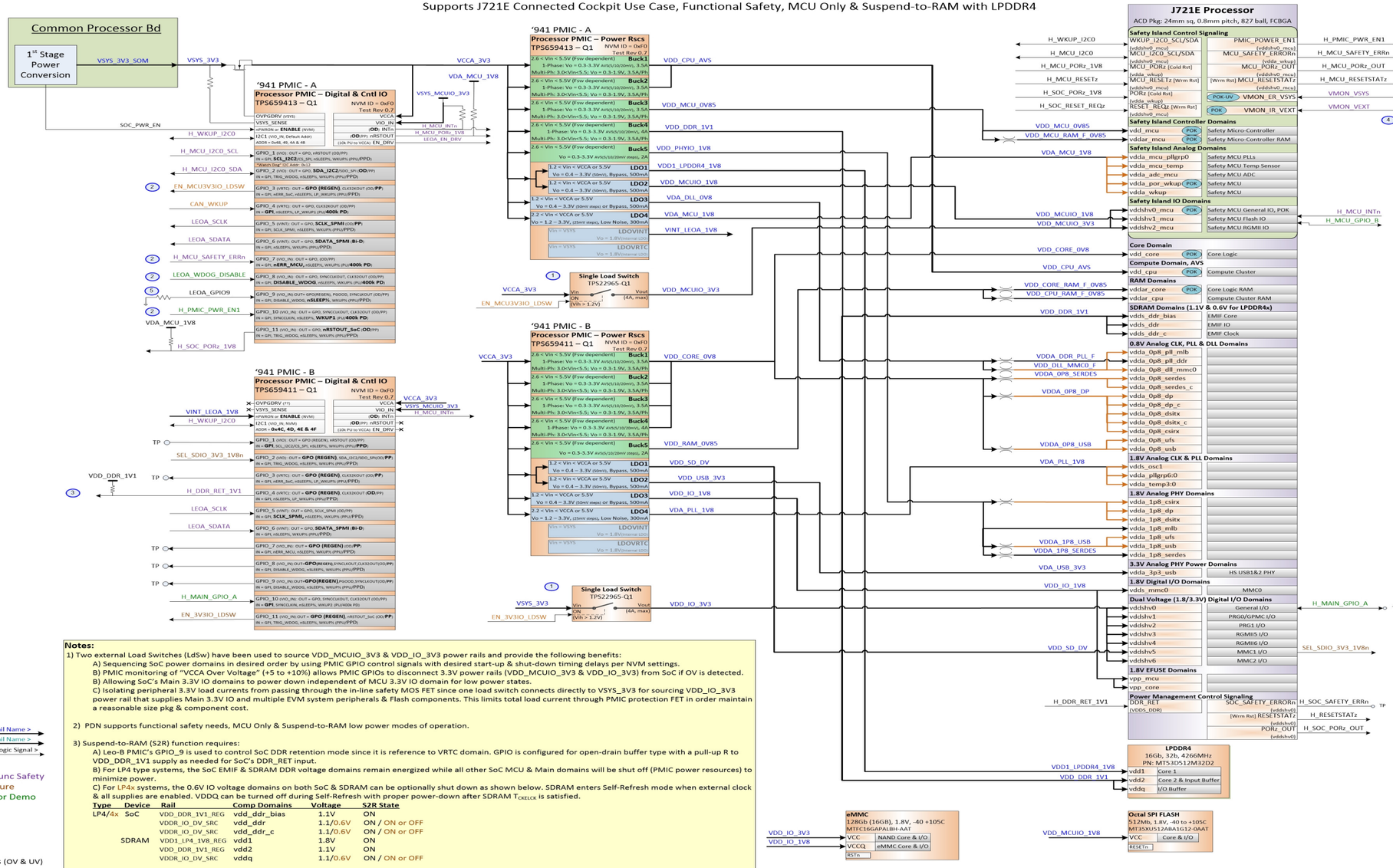
J721E CCARD Dual TPS65941 SoC PDN Overview

v0.2 10/29/2019

(Power Rail & GPIO Mapping Overview)

Supports J721E Connected Cockpit Use Case, Functional Safety, MCU Only & Suspend-to-RAM with LPDDR4



Notes:

1) Two external Load Switches (LdSw) have been used to source VDD_MCUIO_3V3 & VDD_IO_3V3 power rails and provide the following benefits:
   A) Sequencing SoC power domains in desired order by using PMIC GPIO control signals with desired start-up & shut-down timing delays per NVM settings.
   B) PMIC monitoring of "VCCA Over Voltage" (+5 to +10%) allows PMIC GPIOs to disconnect 3.3V power rails (VDD_MCUIO_3V3 & VDD_IO_3V3) from SoC if OV is detected.
   B) Allowing SoC's Main 3.3V IO domains to power down independent of MCU 3.3V IO domain for low power states.
   C) Isolating peripheral 3.3V load currents from passing through the in-line safety MOS FET since one load switch connects directly to VSYS_3V3 for sourcing VDD_IO_3V3 power rail that supplies Main 3.3V IO and multiple EVM system peripherals & Flash components. This limits total load current through PMIC protection FET in order maintain a reasonable size pkg & component cost.

2) PDN supports functional safety needs, MCU Only & Suspend-to-RAM low power modes of operation.

3) Suspend-to-RAM (S2R) function requires:
   A) Leo-B PMIC's GPIO_9 is used to control SoC DDR retention mode since it is reference to VRTC domain. GPIO is configured for open-drain buffer type with a pull-up R to VDD_DDR_1V1 supply as needed for SoC's DDR_RET input.
   B) For LP4 type systems, the SoC EMIF & SDRAM DDR voltage domains remain energized while all other SoC MCU & Main domains will be shut off (PMIC power resources) to minimize power.
   C) For LP4x systems, the 0.6V IO voltage domains on both SoC & SDRAM can be optionally shut down as shown below. SDRAM enters Self-Refresh mode when external clock & all supplies are enabled. VDDQ can be turned off during Self-Refresh with proper power-down after SDRAM T_{CKELCK} is satisfied.

Type	Device	Rail	Comp Domains	Voltage	S2R State
LP4/4x	SoC	VDD_DDR_1V1_REG	vdd_ddr_bias	1.1V	ON
		VDDR_IO_DV_SRC	vdd_ddr	1.1/0.6V	ON / ON or OFF
		VDDR_IO_DV_SRC	vdd_ddr_c	1.1/0.6V	ON / ON or OFF
	SDRAM	VDD1_LP4_1V8_REG	vdd1	1.8V	ON
		VDD_DDR_1V1_REG	vdd2	1.1V	ON
		VDDR_IO_DV_SRC	vddq	1.1/0.6V	ON / ON or OFF

4) Functional Safety requires monitoring all key SoC voltage domains that could cause severe system failures. SoC internal Power OK (POK) provides OV & UV monitoring for a few SoC MCU & Main domains. SoC does support UV monitoring of the critical system input power rail on VMON_VSYS connected to VSYS_3V3 using R-Divider network. One additional User selectable external voltage rail can have both OV & UV monitoring on VMON_VEXT sense input. EVM has connected it to VDD_IO_3V3 through a R-Divider to provide monitoring on key VDD_IO_3V3 power rail. The following SoC Main domains have been classified as non-critical & do not require direct monitoring: VDDSHV5 (SD Card), VPP_CORE, VPP_MCU & VDDA_3P3_USB.

5) PMIC-A's NVM setting must set GPIO9 = nSLEEP function & connected to Gnd on the board as a "Work-Around" for PMIC ES1.0 "nSLEEP Deglitcher" errata item. This allows SoC power management SW to control entry & exit of low power modes (i.e. MCU Only & S2R) as desired without any SW changes to address PMIC errata. PMIC ES 2.0 will fix this issue & GPIO9 can be recovered for other uses with ES2.0 or later PMICs.

PDN Legend:

SoC Power Rails — < Pwr Rail Name >
Peripheral Power Rails — < Pwr Rail Name >
Cntrl & GPIO logic signals — < Digital Logic Signal >

Digital Logic Signal types:
Required for Nominal Opr & Func Safety
Customer or End Product Feature
EVM Debug, Development &/or Demo feature
Optional PMIC feature

(#) Note items
POK On-Chip "Pwr OK" Monitors (OV & UV)
POK-UV On-Chip "Pwr OK" Monitors (UV only)
Provisioned In-Line Supply Filter =

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SoM I2C ADDRESS TABLE

Device	WKUP_I2C0	MCU_I2C0	CPU_I2C0	CPU_I2C1	CPU_I2C2	CPU_I2C3	CPU_I2C4	CPU_I2C5	CPU_I2C6
MCU ID EEPROM	0x50								
PMIC-A	0x48-0X4B	0x48-0X4B							
PMIC-B	0x4C-0x4F								
APPLE AUTH			0x10,0x11						
CPU UB941				0x16					
CPU TPA6304						0x2D			
CPU TAS2505						0x18			
MINI-PCIE							TBD		
A2B EXPANSION								TBD	
CPU UB960			0x3D						0x3D

CPU UB960	Move from I2C6 to I2C0 due to UB960 SCL/SDA line swap. Swap to I2C0 can be wired.
CPU TPA6304	Delta from ACARD. On ACARD set pin measures ~1.2V for addr 0x2C, on CCARD measures 3.2V for addr 0x2D. Looks like on-chip pulldown not enabled? No datasheet and parts shipped in two different batches.

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GPIO MAPPING TABLE

INDEX	BALL	SIGNAL	GPIO	IPU/IPD	SCHEMATIC NET	XPU/XPD
1	AJ23	PRG1_PRU0_GPO3	GPIO0_4	OFF	TPA6304_nSTANDBY	PD-3.32K
2	AH23	PRG1_PRU0_GPO4	GPIO0_5	OFF	CHIMES_nSTANDBY	PD-3.32K
3	AH21	PRG1_PRU0_GPO19	GPIO0_20	OFF	A2B_GPIO_OUT_57	PD-10K
4	AJ25	PRG1_PRU1_GPO10	GPIO0_32	OFF	A2B_GPIO_INTR_77	
5	AH25	PRG1_PRU1_GPO11	GPIO0_33	OFF	A2B_GPIO_OUT_74	
6	AG25	PRG1_PRU1_GPO12	GPIO0_34	OFF	A2B_GPIO_INTR_43	
7	AH26	PRG1_PRU1_GPO14	GPIO0_35	OFF	PCIe0_WAKE#	PU-100K
8	AJ27	PRG1_PRU1_GPO15	GPIO0_36	OFF	PCIe0_W_DISABLE#	PD-10K
9	AJ26	PRG1_PRU1_GPO16	GPIO0_37	OFF	PCIe0_RC_RSTz	PD-10K
10	W28	RGMII6_TD1	GPIO0_100	OFF	TUNER_INTB_CHIP0	PU-10K
11	Y27	RGMII6_RD2	GPIO0_106	OFF	TUNER_RSTB_CHIP0	PD-10K
12	AA2	SPI0_CS0	GPIO0_111	OFF	UB960_FRAME_SYNC	
13	AA1	SPI0_CLK	GPIO0_113	OFF	UB960_PDB	PD-10K
14	AB5	SPI0_D0	GPIO0_114	OFF	UB960_CAM_nPOWERON	PU-10K
15	Y3	SPI1_CS0	GPIO0_116	OFF	UB981_GPIO0	
16	W4	SPI1_CS1	GPIO0_117	OFF	UB981_GPIO1	
17	Y1	SPI1_CLK	GPIO0_118	OFF	UB981_PDB	PD-10K
18	Y5	SPI1_D0	GPIO0_119	OFF	UB981_GPIO2	
19	Y2	SPI1_D1	GPIO0_120	OFF	UB981_GPIO3	
20	AC2	UART0_CTSn	GPIO0_123	OFF	NEO_RESETN	
21	AB1	UART0_RTSn	GPIO0_124	OFF	PWR_SW_CNTL_DSI0	PD-10K
22	AC4	UART1_CTSn	GPIO0_127	OFF	DSI_UB981_INTB	PU-4.7K
23	AD5	UART1_RTSn	GPIO1_0	OFF	USB0_STATUS	PU-100K
24	W5	MCAN0_RX	GPIO1_1	OFF	UB960_INTB	PU-4.7K
25	W6	MCAN0_TX	GPIO1_2	OFF	USB0_VBUS_OCN	PU-100K
26	W3	MCAN1_RX	GPIO1_3	OFF	APL_RSTn	PU-2.2K
27	Y23	PRG1_PRU1_GPO8	GPIO0_29	OFF	ENET_WAKE	PD-3.32K
28	W23	RGMII6_TD3	GPIO0_99	OFF	ENET_INH	PD-3.32K
29	V23	RGMII6_RX_CTL	GPIO0_98	OFF	ENET_INTSn	PU-3.32K
30	T27	MMC2_DAT1	GPIO1_25	OFF	ENET_EN	PU-3.32K
31	F27	WKUP_GPIO0_3	WKUP_GPIO0_3	OFF	MCAN_nFAULT	PU-3.32K
32	F29	WKUP_GPIO0_6	WKUP_GPIO0_6	OFF	MCAN_EN	PD-10K
33	H26	WKUP_GPIO0_10	WKUP_GPIO0_10	OFF	MCU_CAN0_STBz	PD-10K
34	H27	WKUP_GPIO0_11	WKUP_GPIO0_11	OFF	MCU_CAN1_STBz	PD-10K
35	AH29	PRG0_PRU0_GPO13	GPIO0_56	OFF	SEL_SDIO_3V3_1V8n	PU-10K
36	AG29	PRG0_PRU1_GPO16	GPIO0_79	OFF	MMC_PWR_ON	PU-10K
37	G26	WKUP_GPIO0_9	WKUP_GPIO0_9	OFF	H_MCU_INT#	PU-10K
38	A23	WKUP_GPIO0_30	MCU_OSPI1_LBCLK0	OFF	WKUP_GPIO0_30	PU-10K

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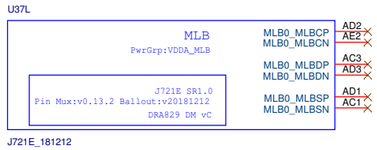
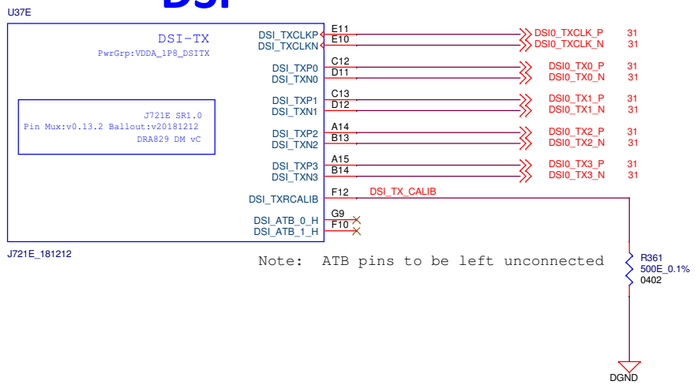
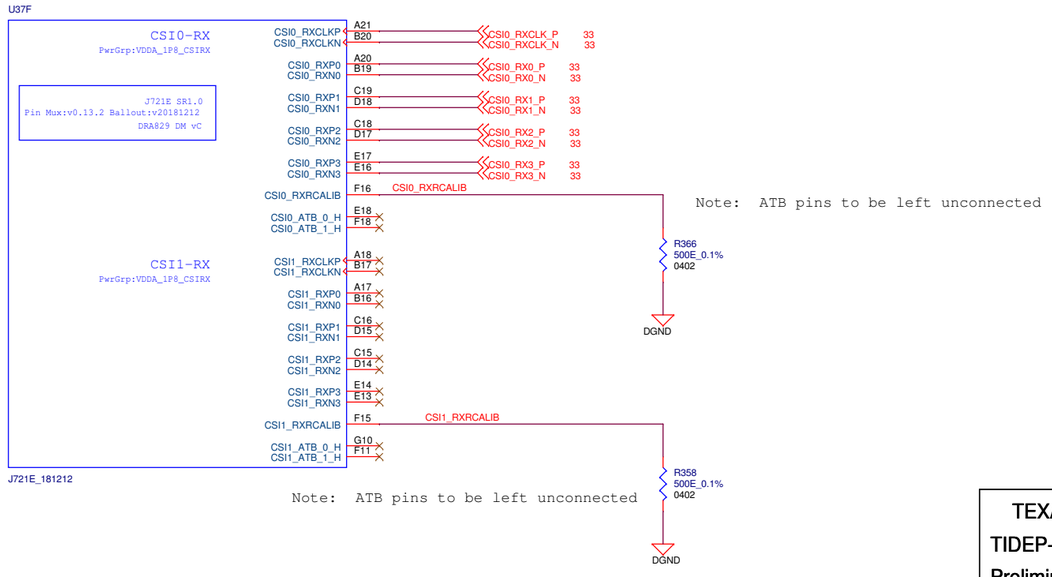
MLB



DSI



CSI Interface



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Title: J7ES CCARD		
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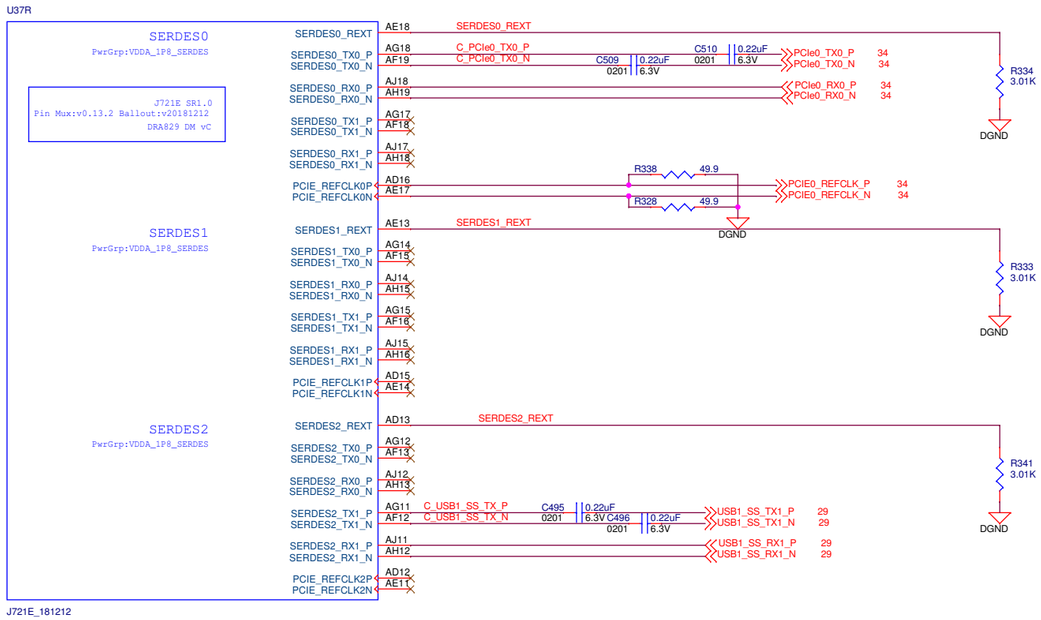
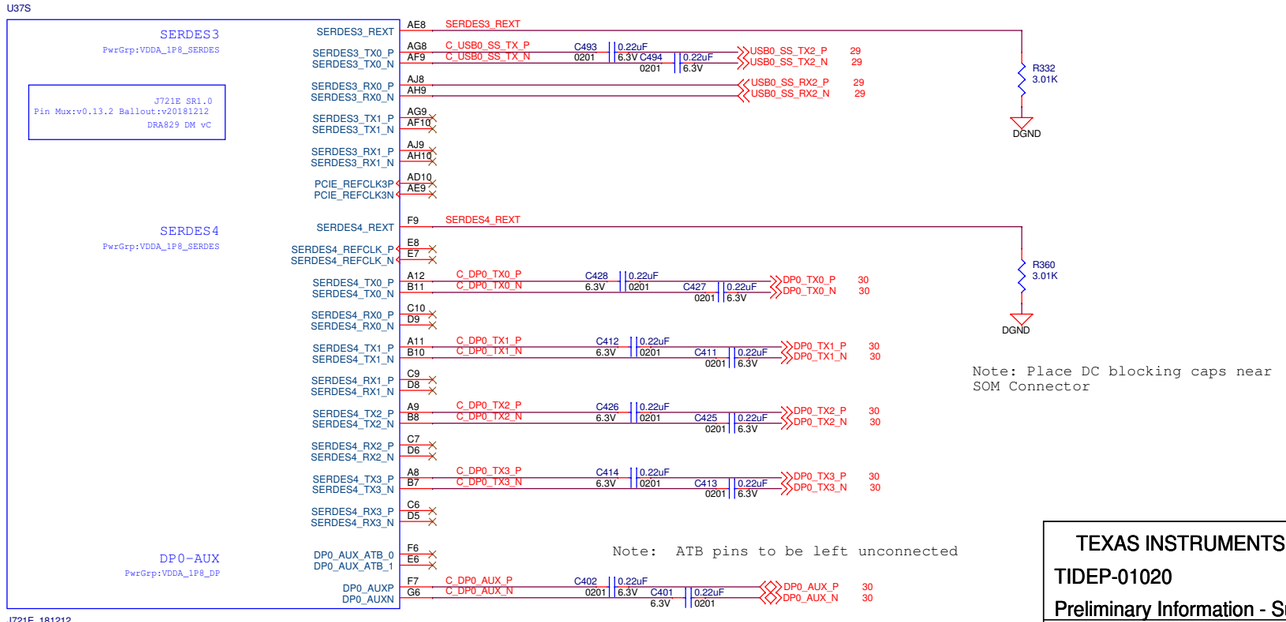
SERDES





Note: Place DC blocking caps near SOM Connector

Note: ATB pins to be left unconnected

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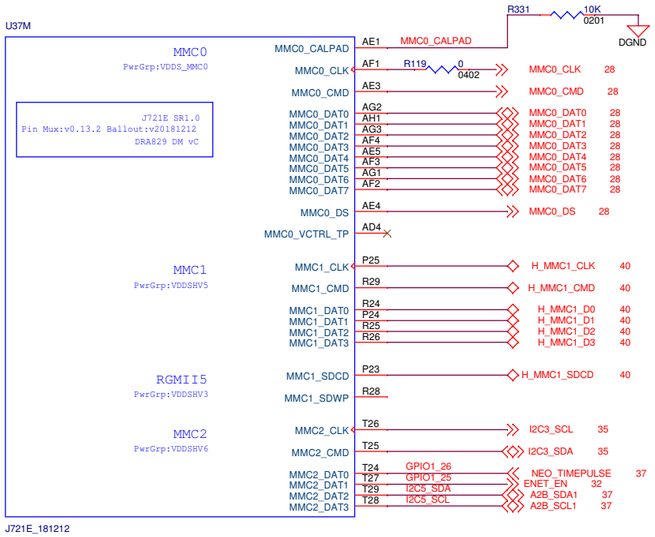
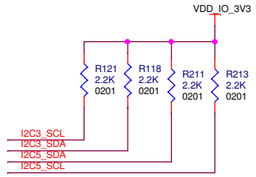
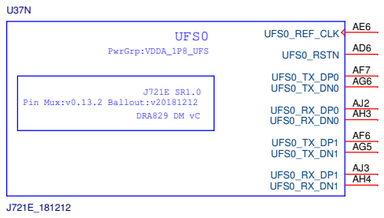
MMC Interface





UFS Interface



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Page Contents: SOC MMC & UFS IF		
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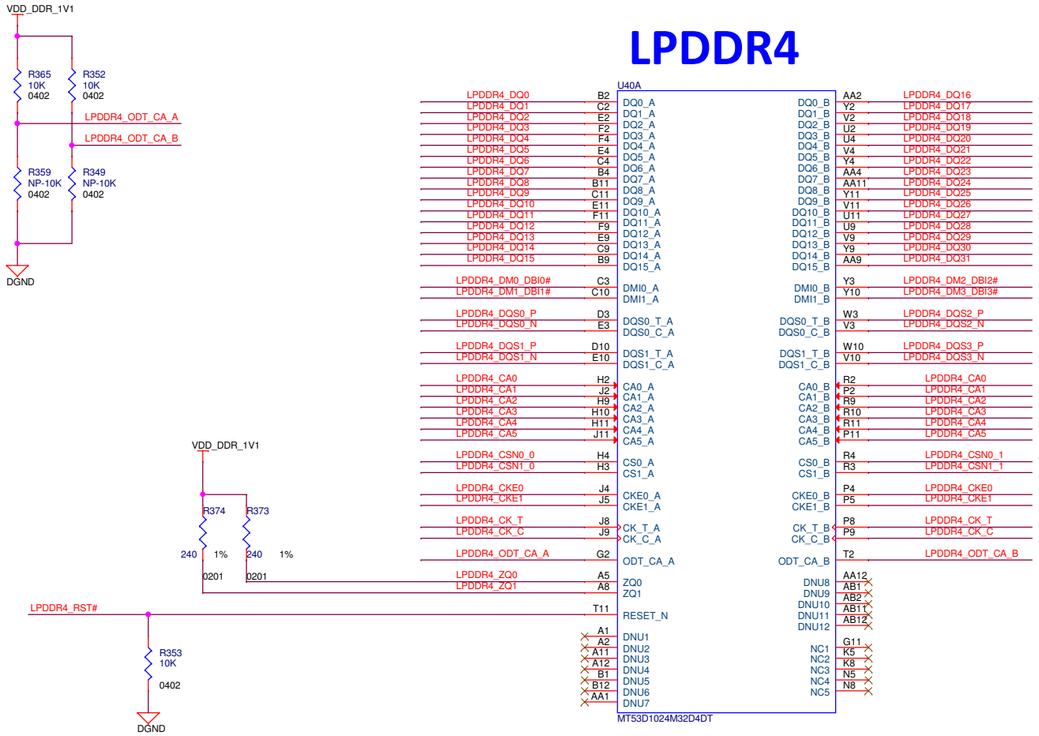
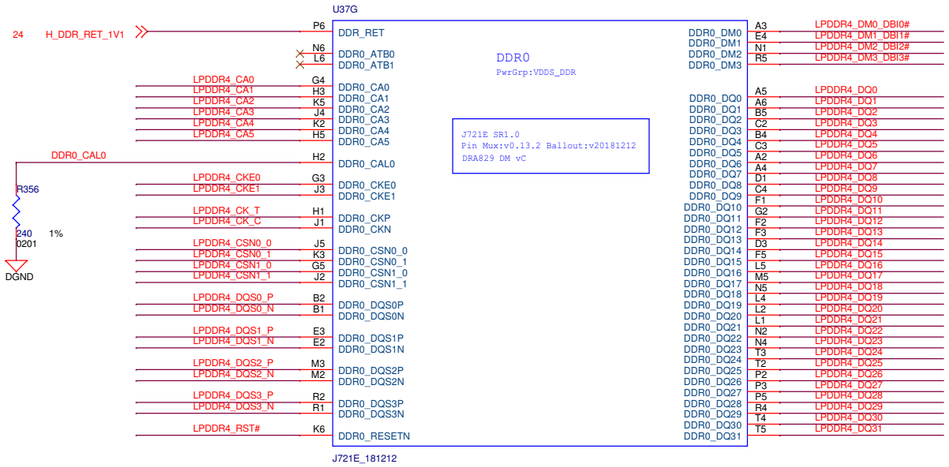
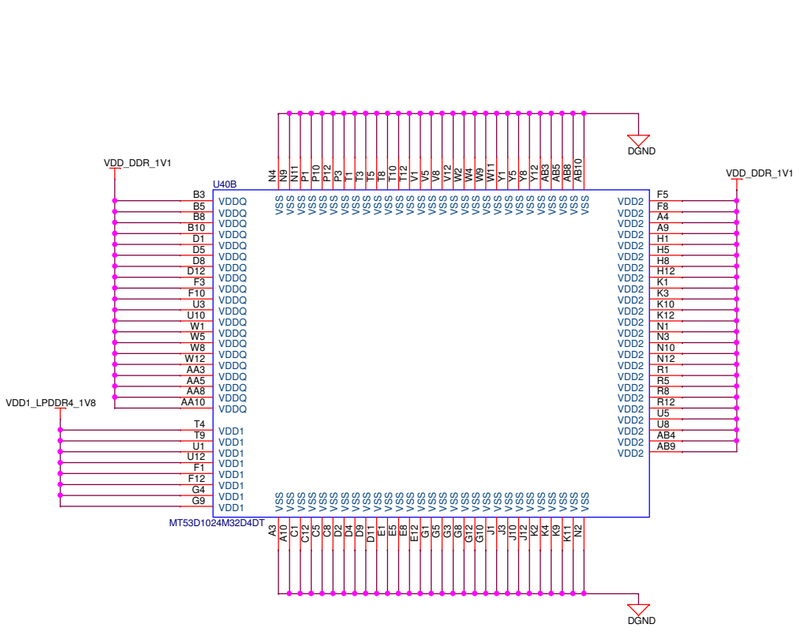
LPDDR4

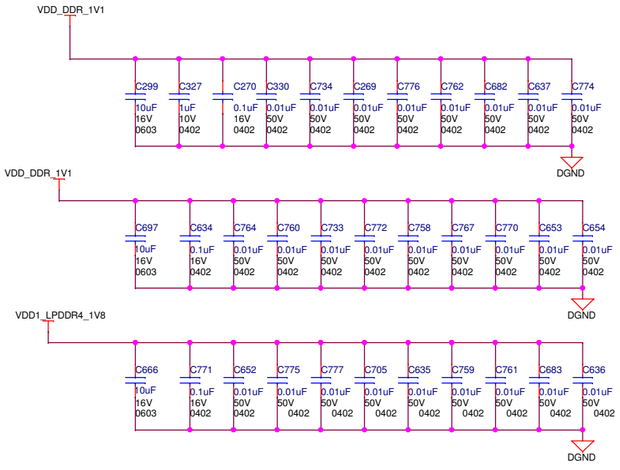


EMIF



Dcap scheme needs improvement to reduce Zpk vs F (WiP)





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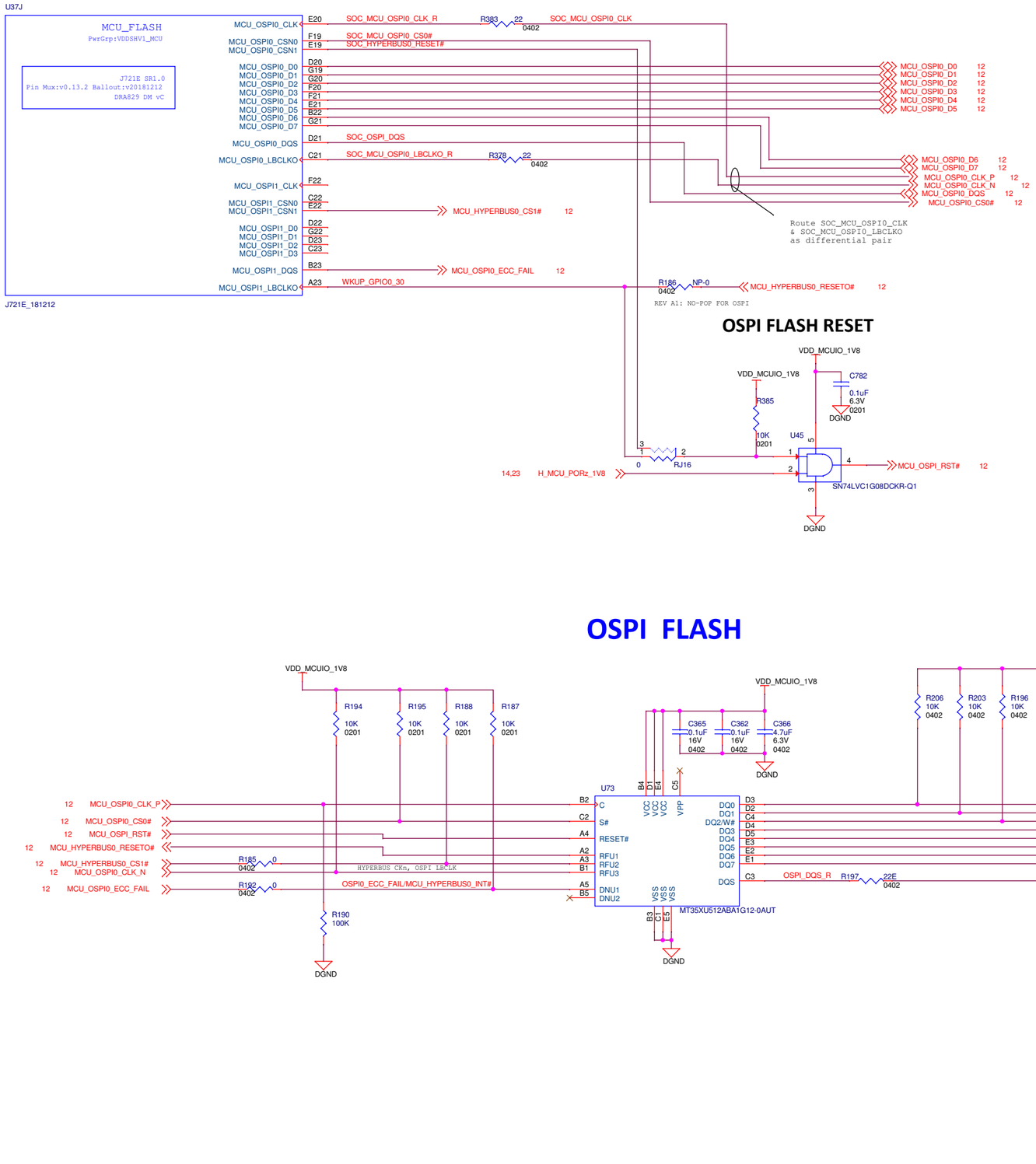
MCU FLASH



OSPI FLASH

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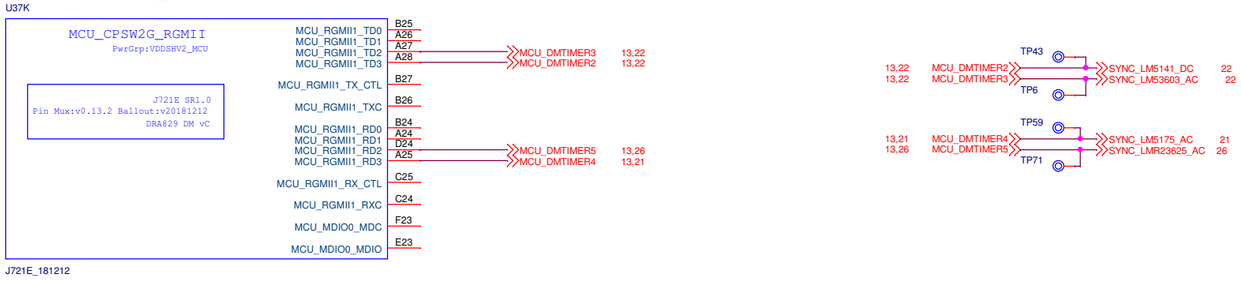
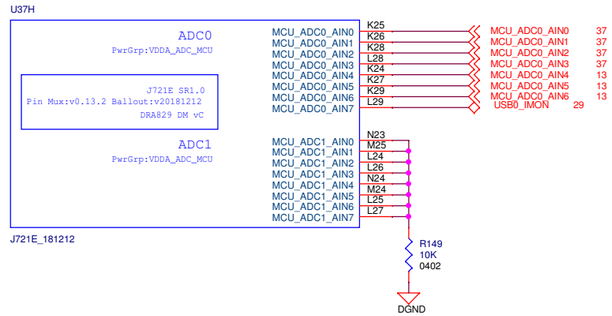
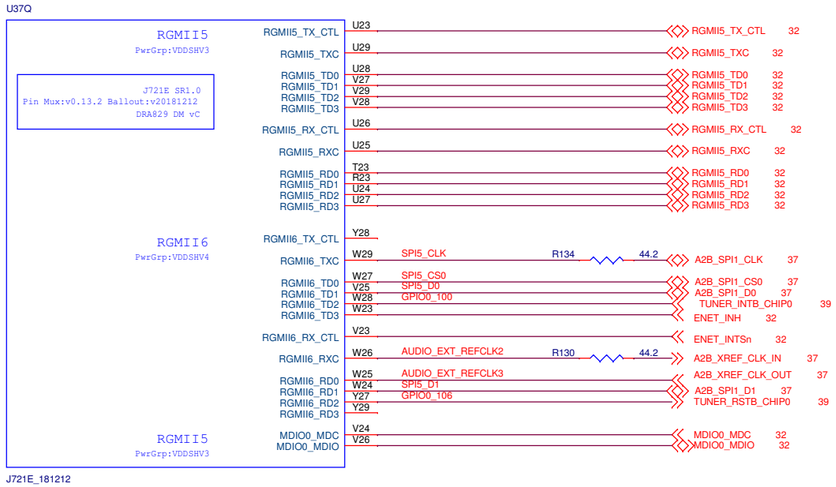
MCU_RGMII



MCU ADCs



MAIN RGMII



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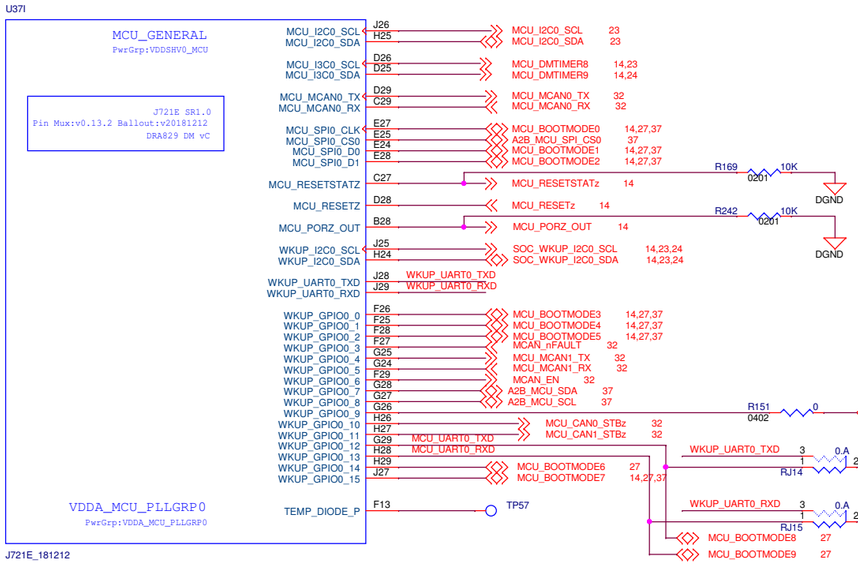
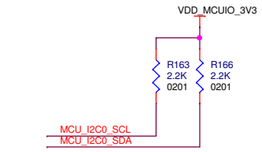
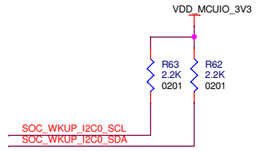
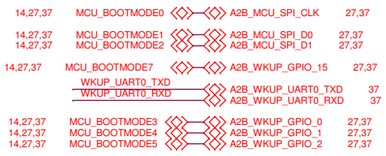
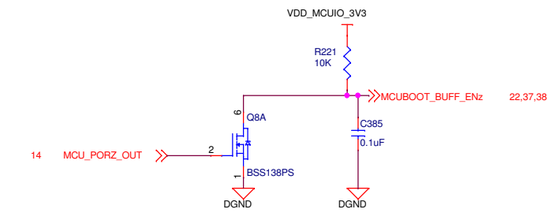
MCU & MAIN GENERAL IO, OSC CLKS

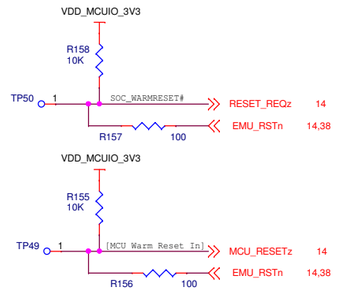


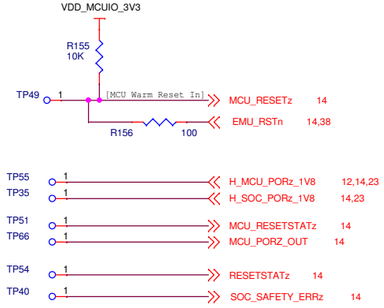


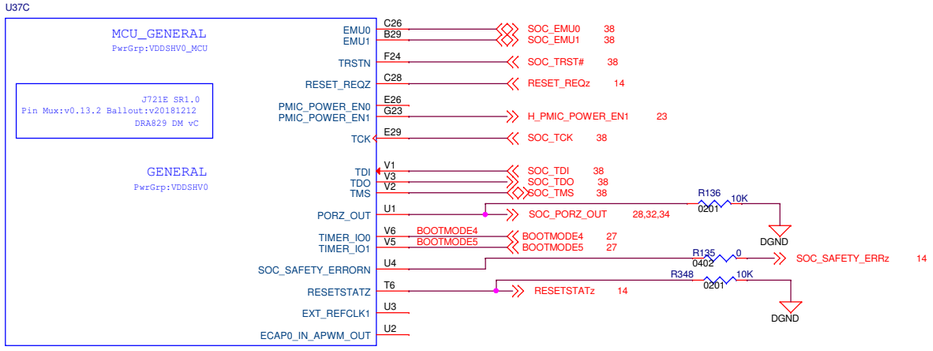


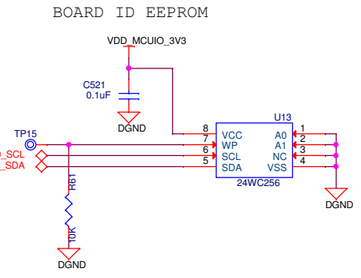




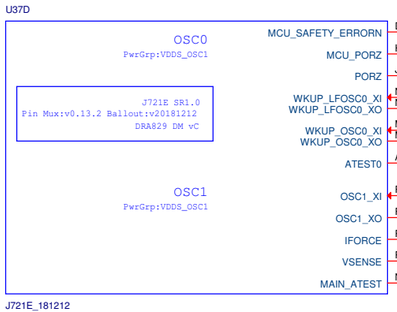




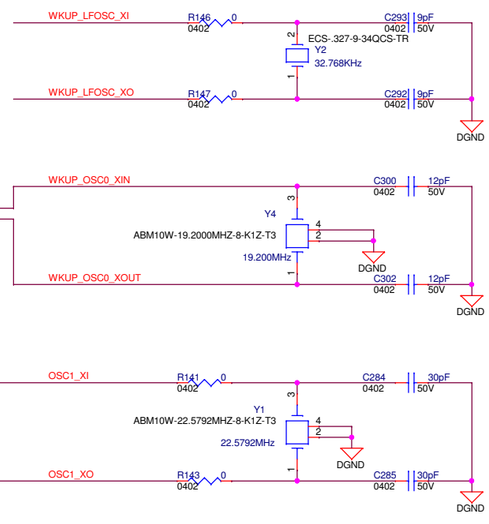




OSC



CLKS



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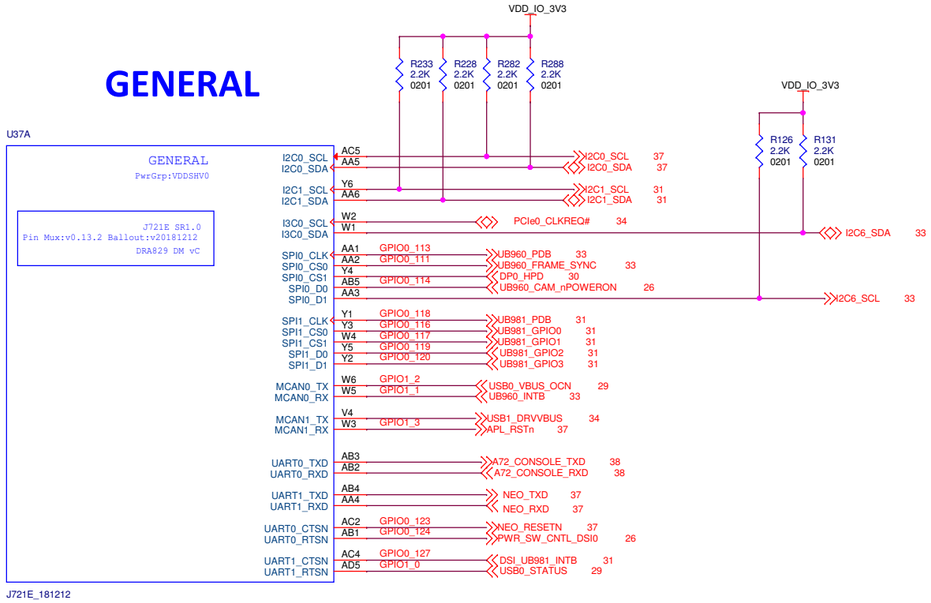
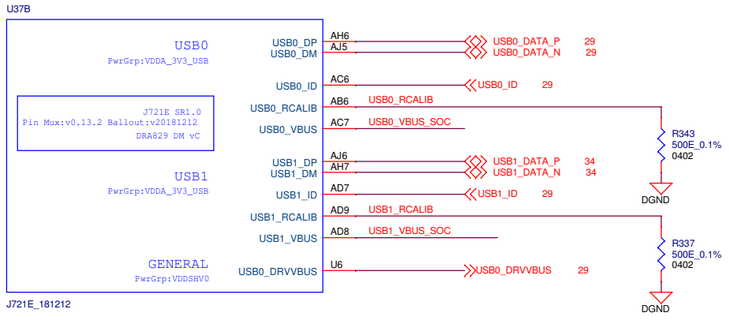
GENERAL

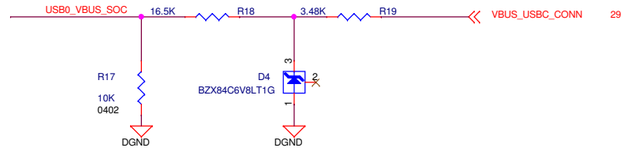


USB

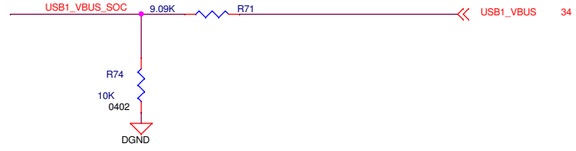


USB VBUS Resistor divider circuit

Note: Recommended VBUS circuit for USB connector. Supports 5V-30V VBUS



Note: Recommended VBUS circuit for embedded Hub



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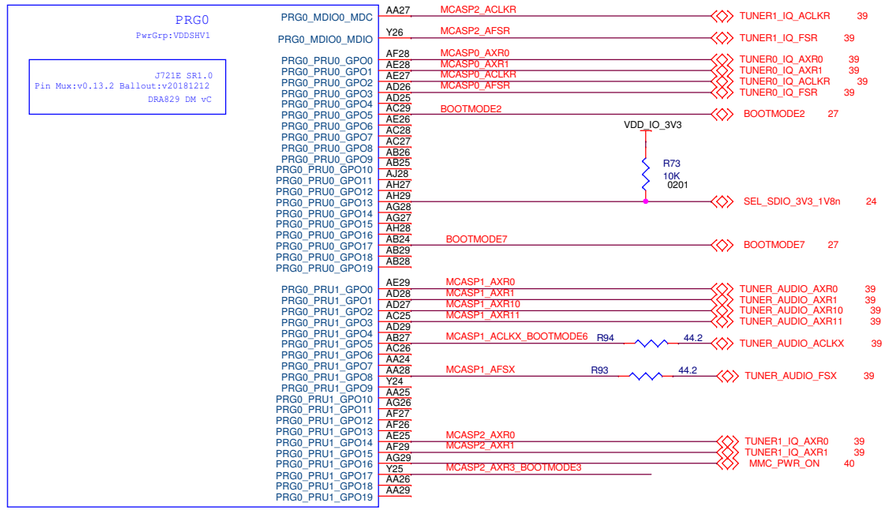
PRG0 & PRG1

U37O



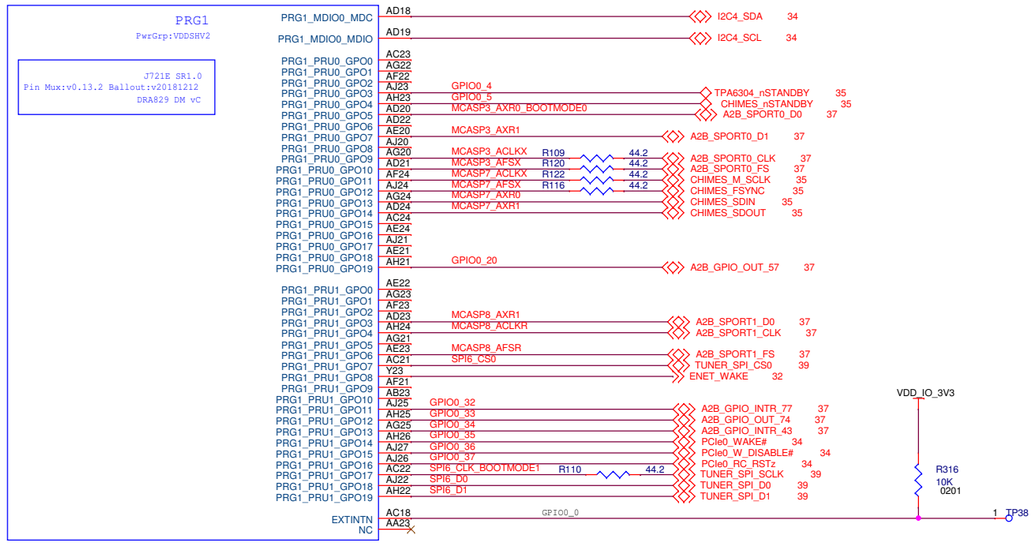
MCASP1_ACLKX_BOOTMODE6 R100 1K BOOTMODE6 27

MCASP2_AXR3_BOOTMODE3 R128 1K BOOTMODE3 27

SPI6_CLK_BOOTMODE1 R115 1K BOOTMODE1 27

MCASP3_AXR0_BOOTMODE0 R209 1K BOOTMODE0 27

U37P



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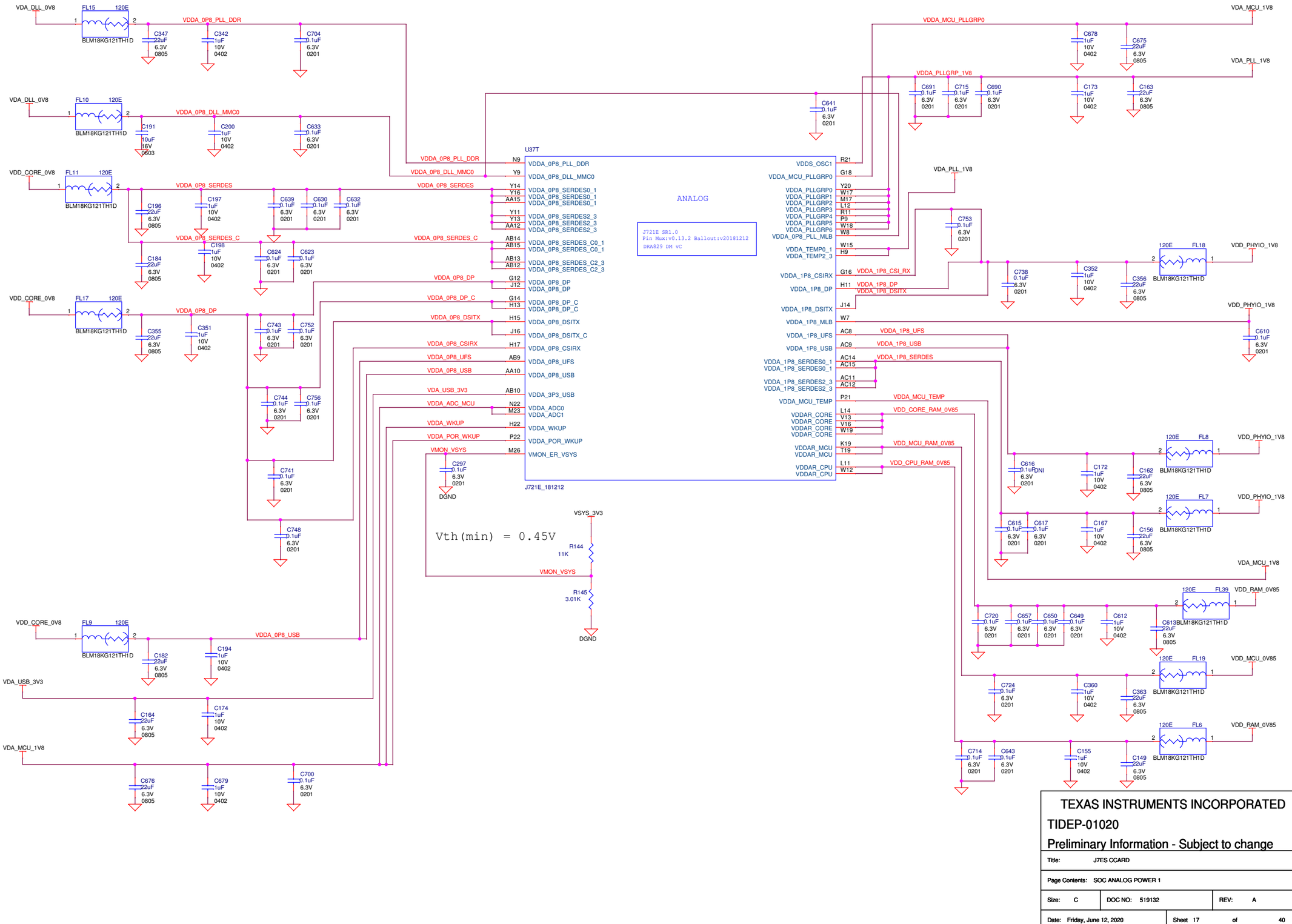
ANALOG POWER 1



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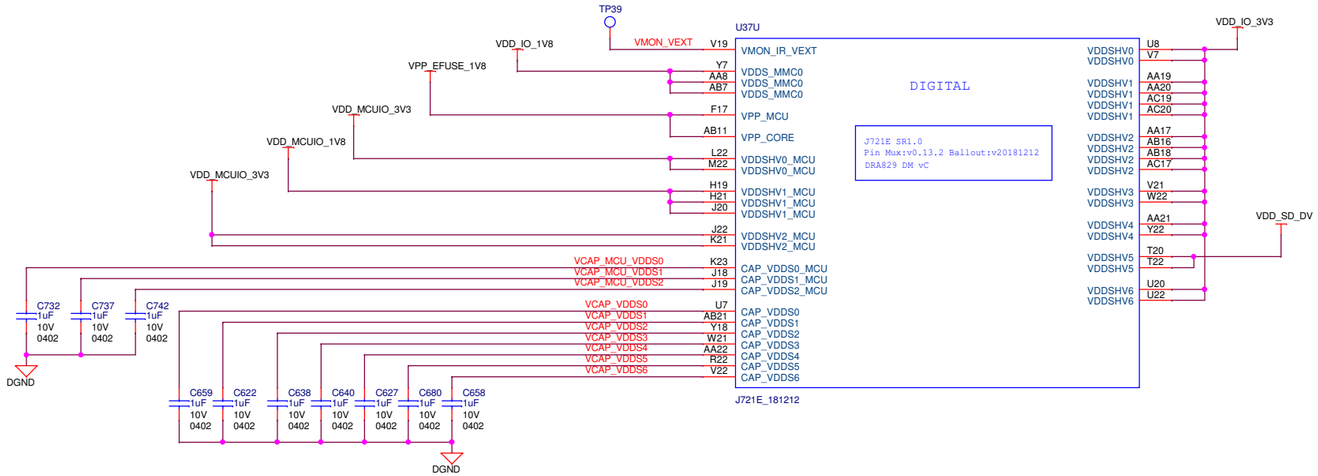
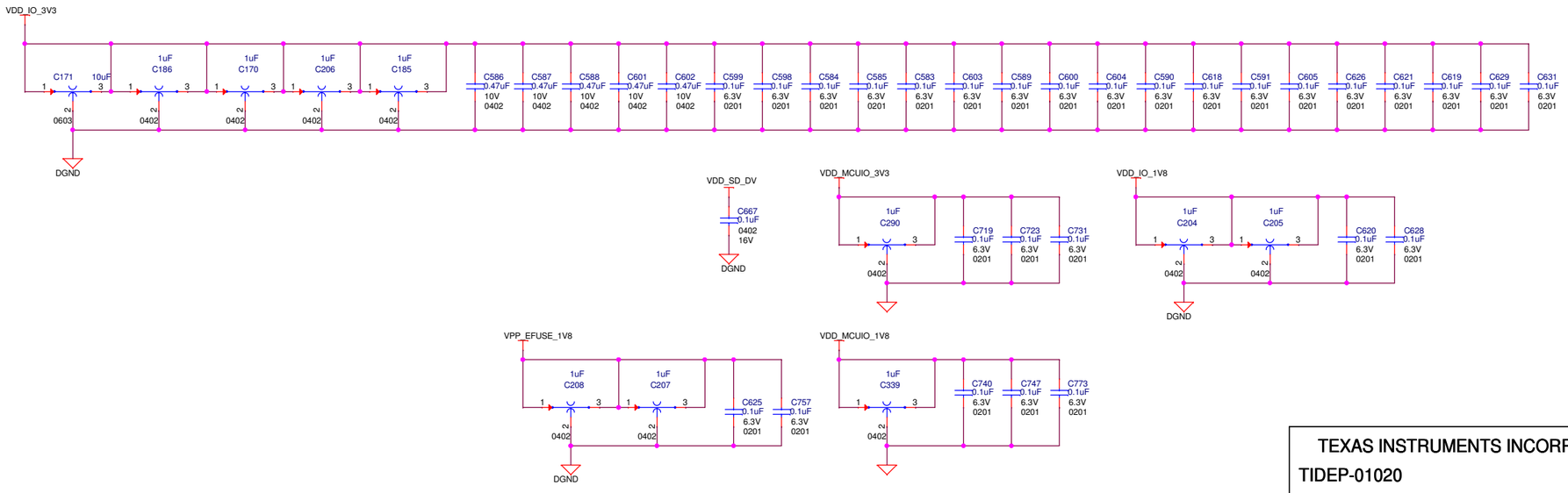
DIGITAL POWER 2





TEXAS INSTRUMENTS INCORPORATED

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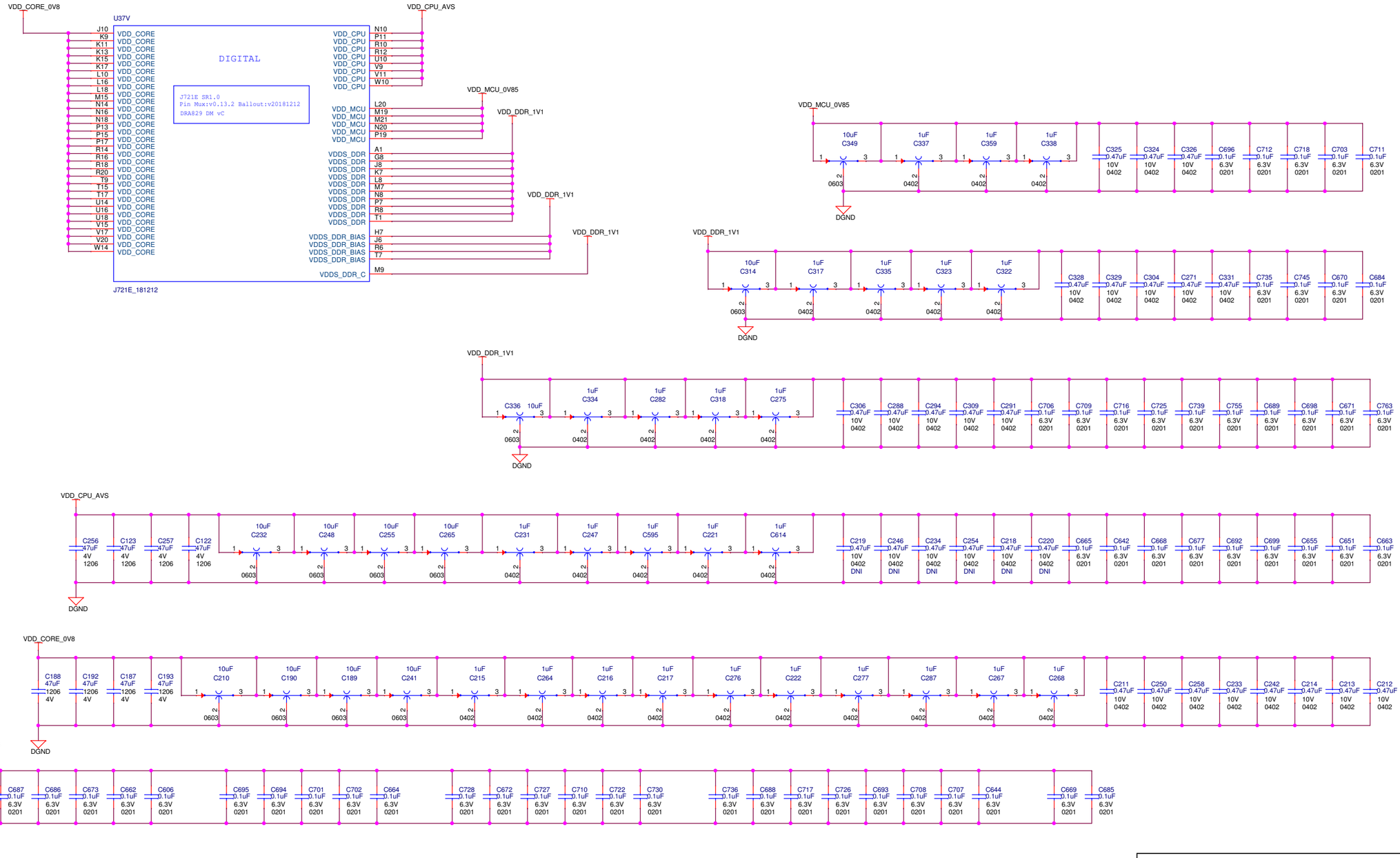
DIGITAL POWER 3



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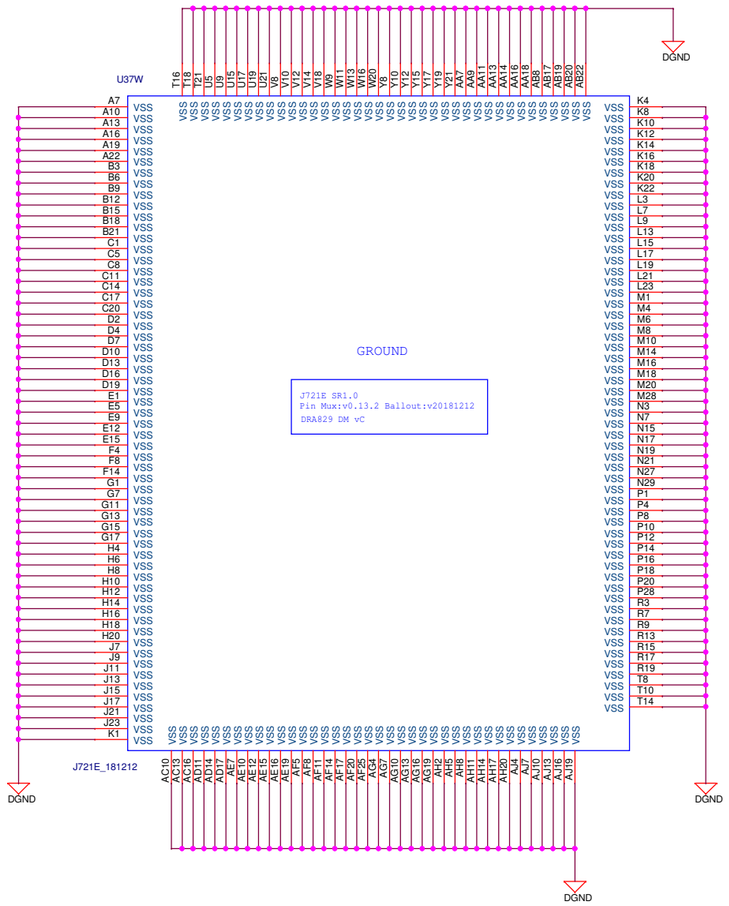
SOC GROUND



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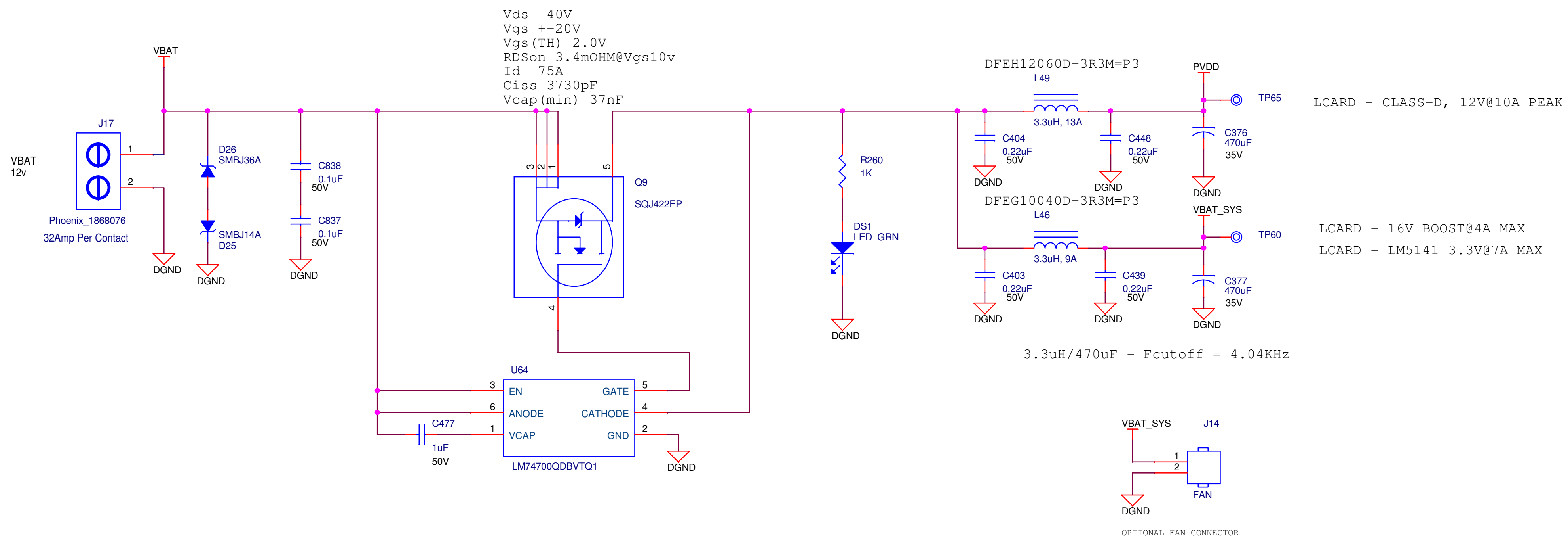
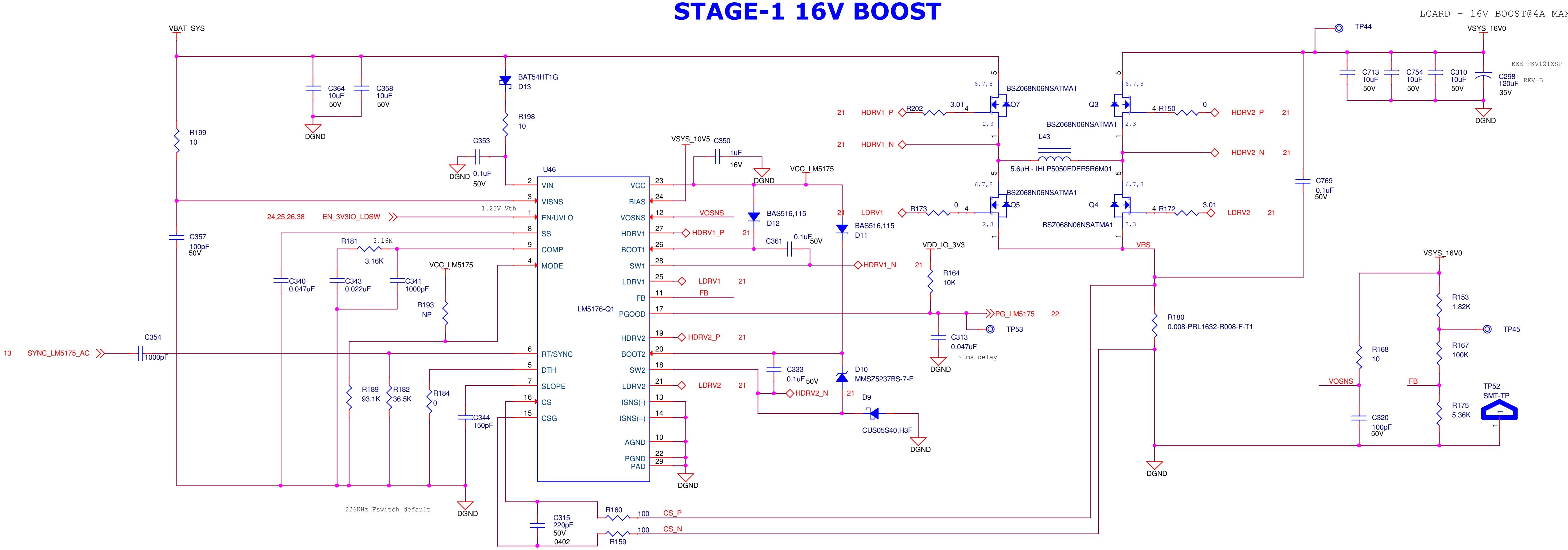
INPUT PROTECTION AND FILTER

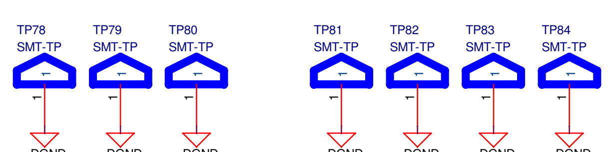


Vds 40V
Vgs +-20V
Vgs(TH) 2.0V
RDSon 3.4mOHM@Vgs10v
Id 75A
Ciss 3730pF
Vcap(min) 37nF
VBAT
VBAT 12v
J17
Phoenix_1868076
32Amp Per Contact
D26 SMBJ36A
SMBJ14A D25
C838 0.1uF 50V
C837 0.1uF 50V
Q9 SQJ422EP
U64
EN
ANODE
VCAP
GATE
CATHODE
GND
C477 1uF 50V
LM74700QDBVTQ1
R260 1K
DS1 LED_GRN
DFEH12060D-3R3M=P3
L49 3.3uH, 13A
C404 0.22uF 50V
C448 0.22uF 50V
PVDD
TP65
C376 470uF 35V
LCARD - CLASS-D, 12V@10A PEAK
DFEG10040D-3R3M=P3
L46 3.3uH, 9A
C403 0.22uF 50V
C439 0.22uF 50V
VBAT_SYS
TP60
C377 470uF 35V
LCARD - 16V BOOST@4A MAX
LCARD - LM5141 3.3V@7A MAX
3.3uH/470uF - Fcutoff = 4.04KHz
VBAT_SYS
J14
FAN
OPTIONAL FAN CONNECTOR
DGND

STAGE-1 16V BOOST



LCARD - 16V BOOST@4A MAX
VBAT_SYS
C364 10uF 50V
C358 10uF 50V
BAT54HT1G D13
R198 10
R199 10
C353 0.1uF 50V
VSYS_10V5
C350 1uF 16V
VCC_LM5175
U46
VIN
VISNS
EN/UVLO
SS
COMP
MODE
RT/SYNC
DTH
SLOPE
CS
CSG
VCC
BIAS
VOSNS
HDRV1
BOOT1
SW1
LDRV1
FB
PGOOD
HDRV2
BOOT2
SW2
LDRV2
ISNS(-)
ISNS(+)
AGND
PGND
PAD
LM5176-Q1
1.23V Vth
24,25,26,38 EN_3V3IO_LDSW
C357 100pF 50V
R181 3.16K
C340 0.047uF
C343 0.022uF
C341 1000pF
VCC_LM5175
R193 NP
13 SYNC_LM5175_AC
C354 1000pF
R189 93.1K
R182 36.5K
R184 0
C344 150pF
226KHz Fswitch default
BAS516,115 D12
BAS516,115 D11
C361 0.1uF 50V
C333 0.1uF 50V
D10 MMSZ5237BS-7-F
D9 CUS05S40,H3F
VDD_IO_3V3
R164 10K
PG_LM5175 22
TP53
C313 0.047uF
~2ms delay
C315 220pF 50V 0402
R160 100 CS_P
R159 100 CS_N
HDRV1_P
HDRV1_N
LDRV1
HDRV2_P
HDRV2_N
LDRV2
R202 3.01
R173 0
BSZ068N06NSATMA1 Q7
BSZ068N06NSATMA1 Q5
Q3 BSZ068N06NSATMA1
Q4 BSZ068N06NSATMA1
R150 0
R172 3.01
L43 5.6uH - IHLP5050FDER5R6M01
VRS
R180 0.008-PRL1632-R008-F-T1
C769 0.1uF 50V
TP44
VSYS_16V0
C713 10uF 50V
C754 10uF 50V
C310 10uF 50V
C298 120uF 35V
EEE-FKV121XSP
REV-B
VSYS_16V0
R153 1.82K
TP45
R167 100K
R168 10
VOSNS
FB
R175 5.36K
C320 100pF 50V
TP52 SMT-TP
DGND



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STAGE-1 3.3V AND 5 V POWER

FOR 3.3v@15A
L = SRP1265A-2R2 - DCR=3.8-4.2mOHM, Irms=22A, Isat=40A
MQH/QL = BSZ034N04LS (lower Rdson, or no change)
Cout 22uFx2 + 120uF EEE-FKV121XSP
Cin 22uF x2 (10uFX4)
Comp - 8.45K, 3.3nF, 68pf, Cross 55KHz, Phase Margin 51
Current sense 5.49K (5.79K-5.24K)

LCARD - LM5141 3.3V@7A MAX

LCARD - USB2.0 - 500mA
LCARD - USB3.0 - CDP: Charge + Data (2.1A)

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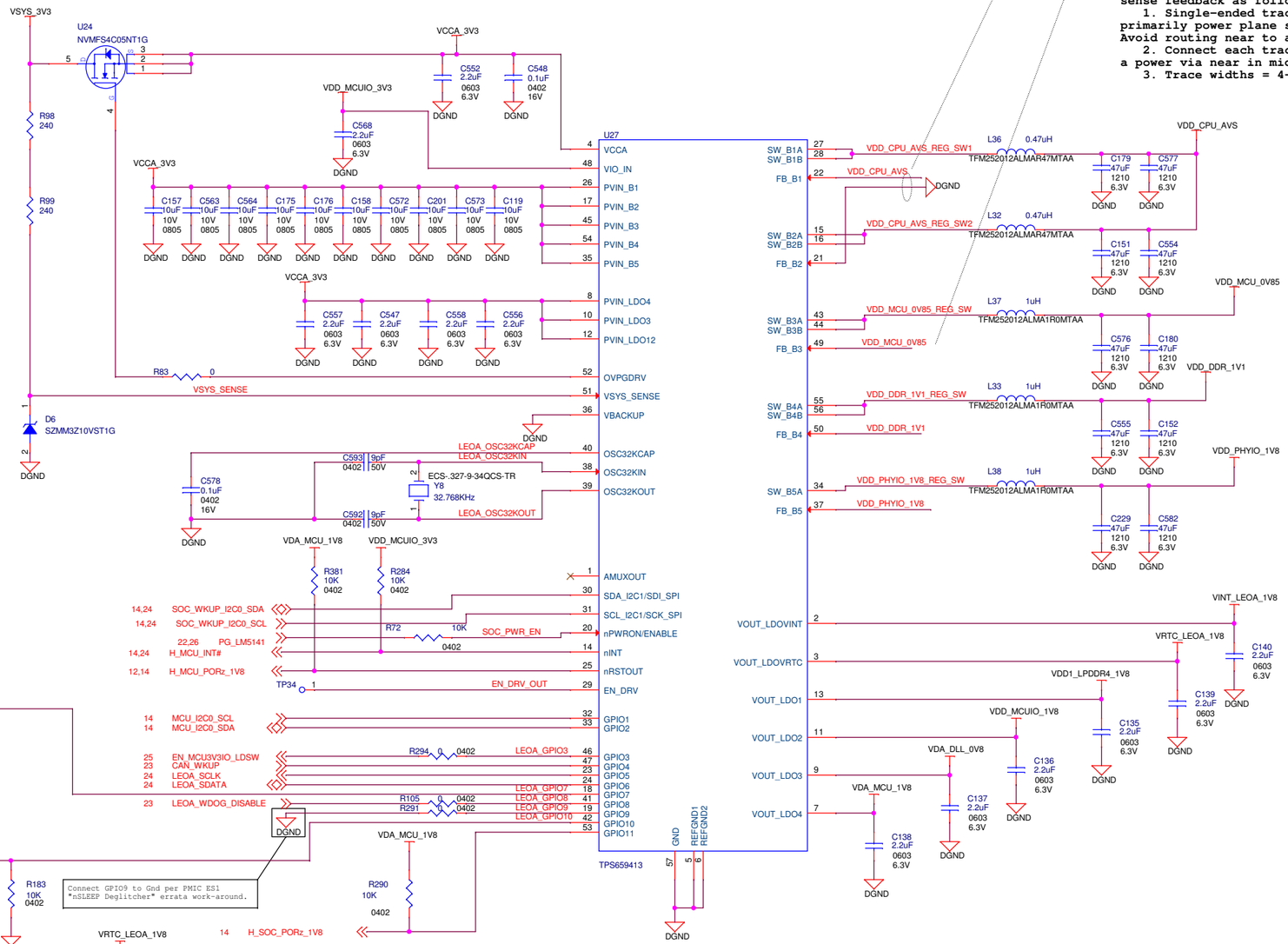
PMIC- A

"PCB Notes:
For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd vias or across Dcap in middle of SOC power ball group.
3. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible while

For single-phase Buck converters, route remote sense feedback as follows:
1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"



PMIC-A uses default I2C ADDR:
0x48, 0x49, 0x4A & 0x4B

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Title: J7ES CCARD		
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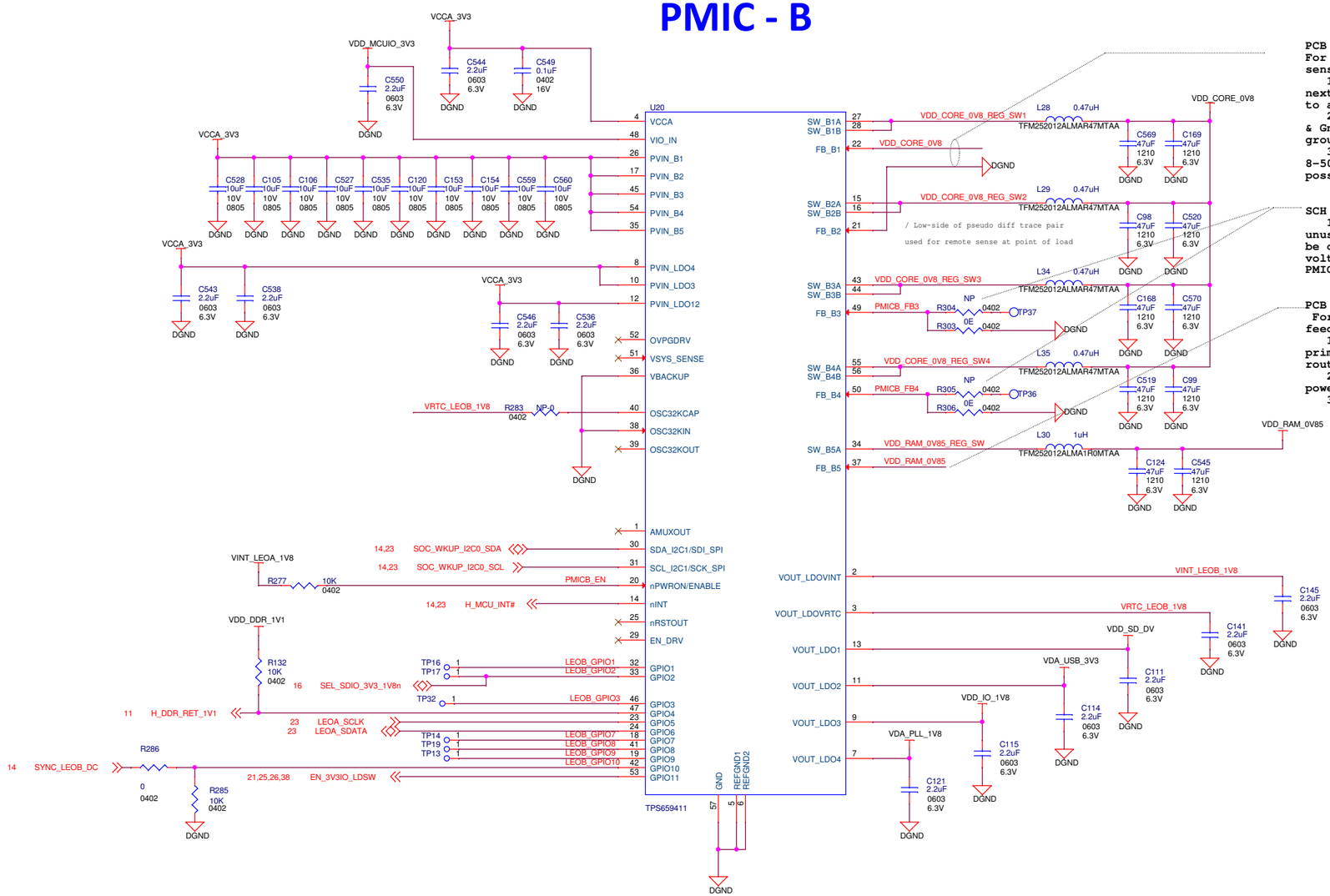
PMIC - B



PCB Note:
For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd vias or across Dcap in middle of SOC power ball group.
3. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible while

SCH Note:
1. For 3 & 4 phase Buck converter configs, the unused feedback sense inputs on Buck 3 & 4 can be optionally re-assigned to provide additional "external voltage monitoring" for functional safety coverage, see PMIC data sheet for details.

PCB Note:
For single-phase Buck converters, route remote sense feedback as follows:
1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"

PMIC-B uses NVM to set I2C ADDR:
0x4C, 0x4D, 0x4E & 0x4F

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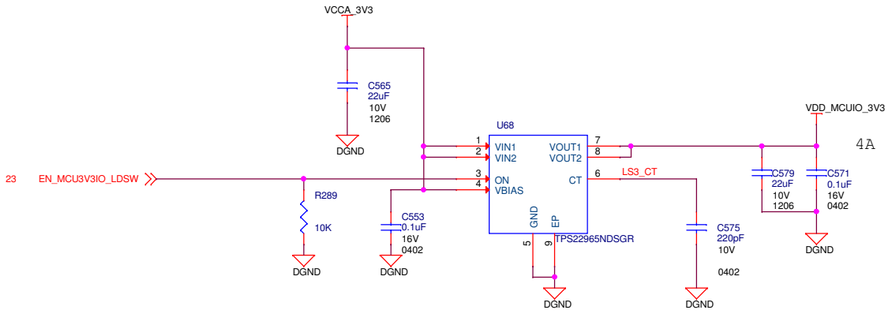
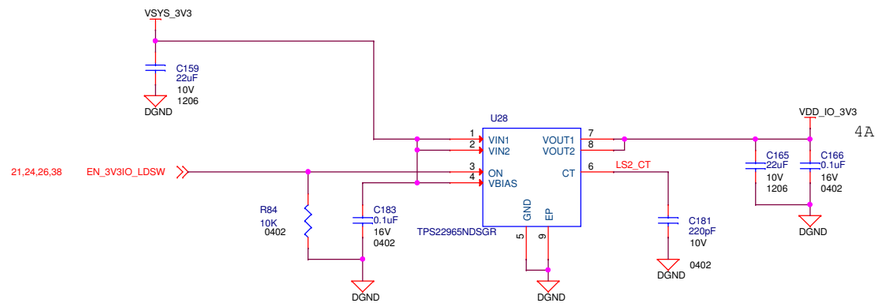
LOAD SWITCHES





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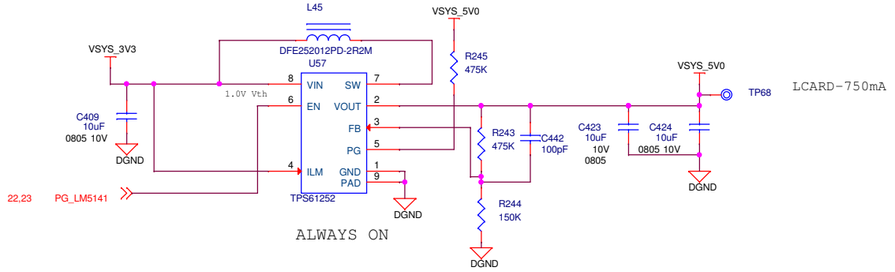
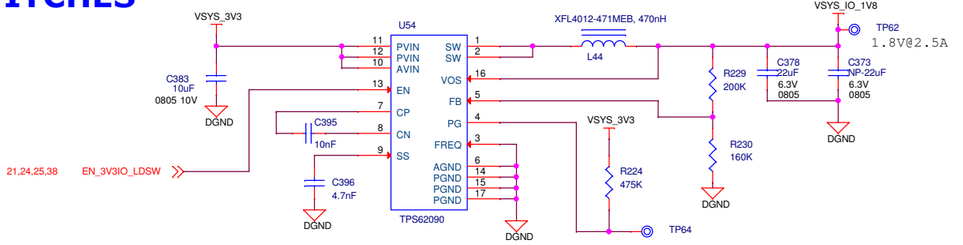
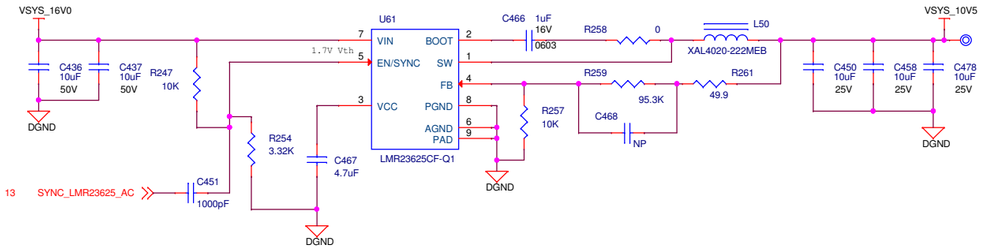
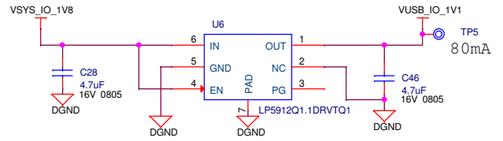
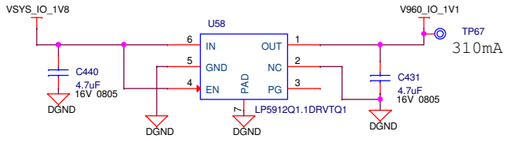
SECONDARY LDO'S/SWITCHES

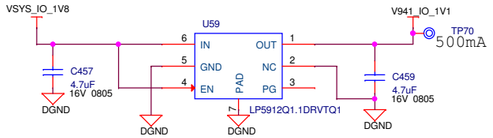


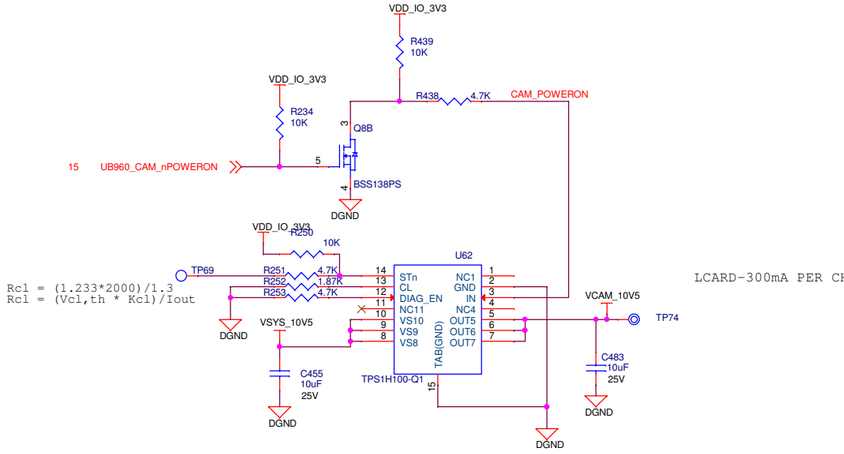


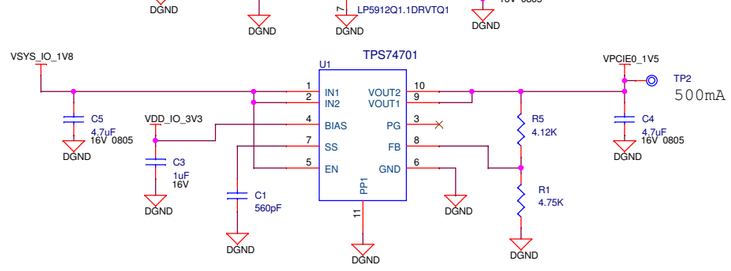




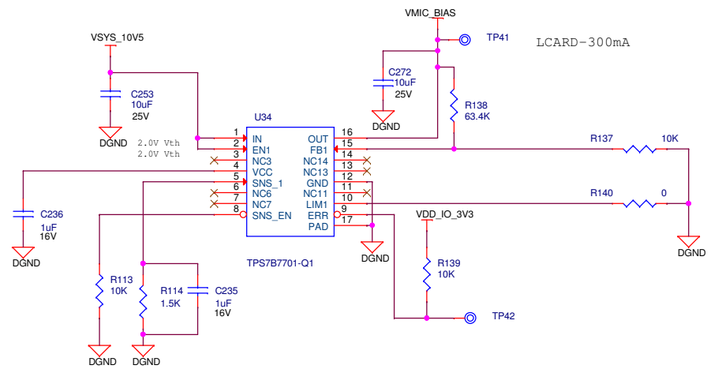


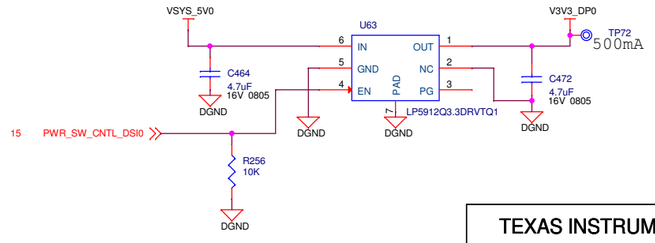






LP5912-500mA $0.38
TPS746Q1-1000mA, ADVANCE PART, SAME PACKAGE $0.5
TPS74701-500mA, $0.80





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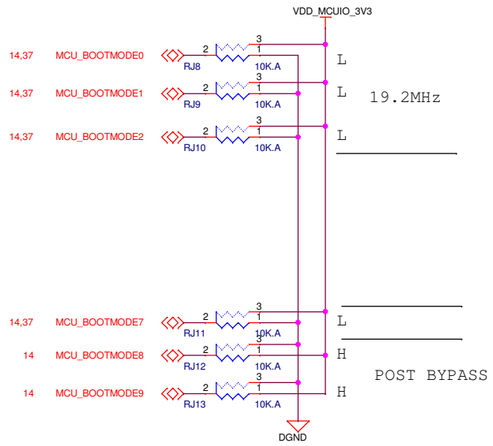
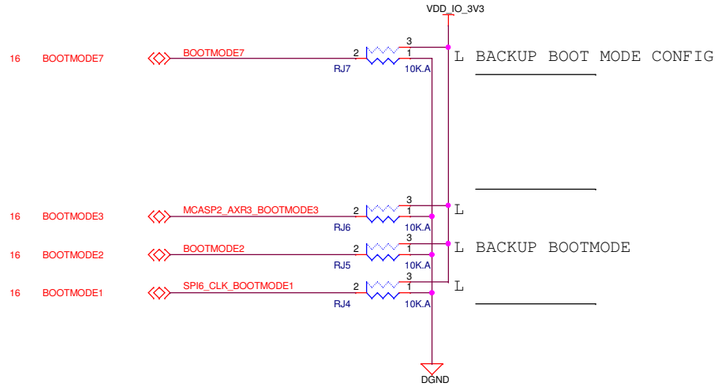
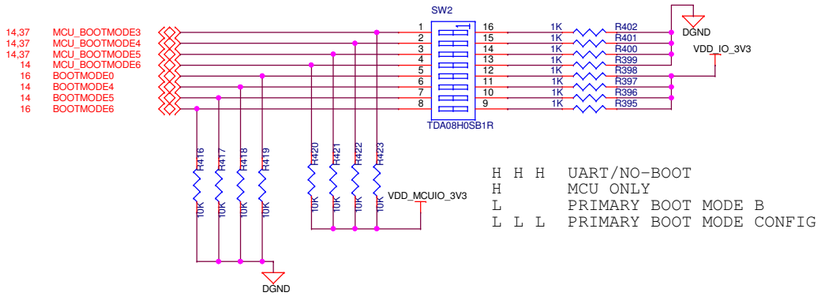
BOOT MODE SELECTION







BOOTMODE [7:0]									MCU_BOOTMODE[9:0]										
7	6	5	4	3	2	1	0		9	8	7	6	5	4	3	2	1	0	
BACKUP BOOT MODE CONFIG	PRIMARY BOOT MODE CONFIG			BACKUP BOOT MODE			Prim Boot Mode B		POST CONFIG		RSV	MMC ONLY	PRIMARY BOOT MODE A			PLL CONFIG			
NA	NA	NA	NA	NA	NA	NA	NA		1	1	0	1	0	0	1	0	0	0	OSPI
NA	NA	NA	NA	NA	NA	NA	NA		1	1	0	1	1	1	1	0	0	0	UART/NO-BOOT(default)
0	0	0	0	0	0	0	0		1	1	0	0	0	0	1	0	0	0	OSPI
0	0	0	0	0	0	0	0		1	1	0	0	1	1	1	0	0	0	UART/NO-BOOT
0	0	0	0	0	0	0	1		1	1	0	0	0	0	1	0	0	0	EMMC
0	0	0	0	0	0	0	1		1	1	0	0	0	1	0	0	0	0	USB

PRIMARY BOOT MODE CONFIG		
OSPI		
6	SPEED	33HMz
5	ICLK	EXTERNAL
4	CSEL	CS 0
USB		
6	PORT	0
5	MODE	DFU
4	LANE SWAP	NO
UART		
6	RSV	
5	RSV	
4	PORT	MCU-0
EMMC		
6	PORT	0
5	BUS WIDTH	MAX
4	VOLTAGE	1.8V

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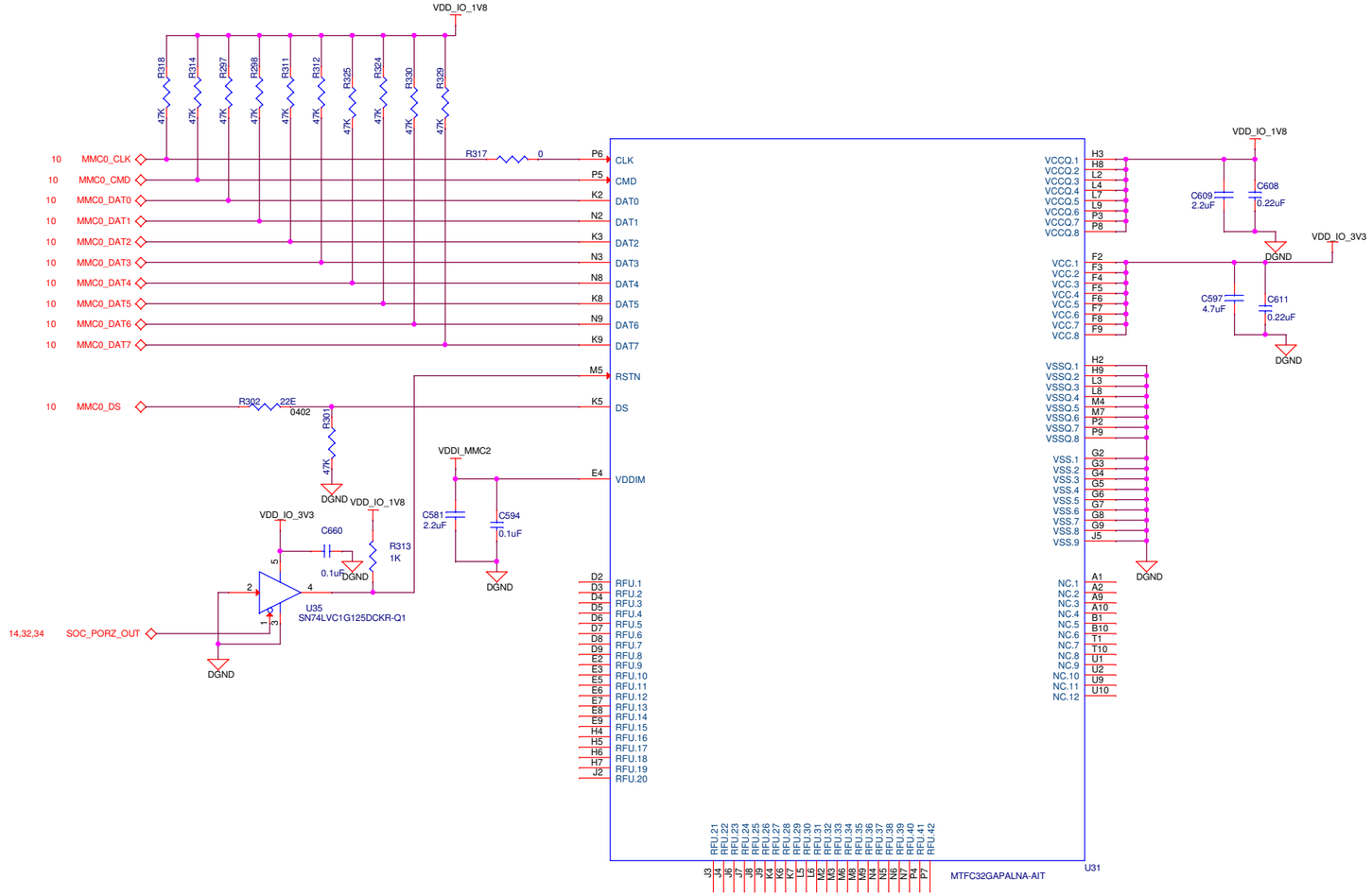
MEM eMMC



100BALL BGA 14mmX18mm, 1mm BALL PITCH
MTFC32GAKAEDQ-AIT - V5.0
MTFC32GAPALNA-AIT - V5.1
MTFC32GAPALNA-AAT - V5.1

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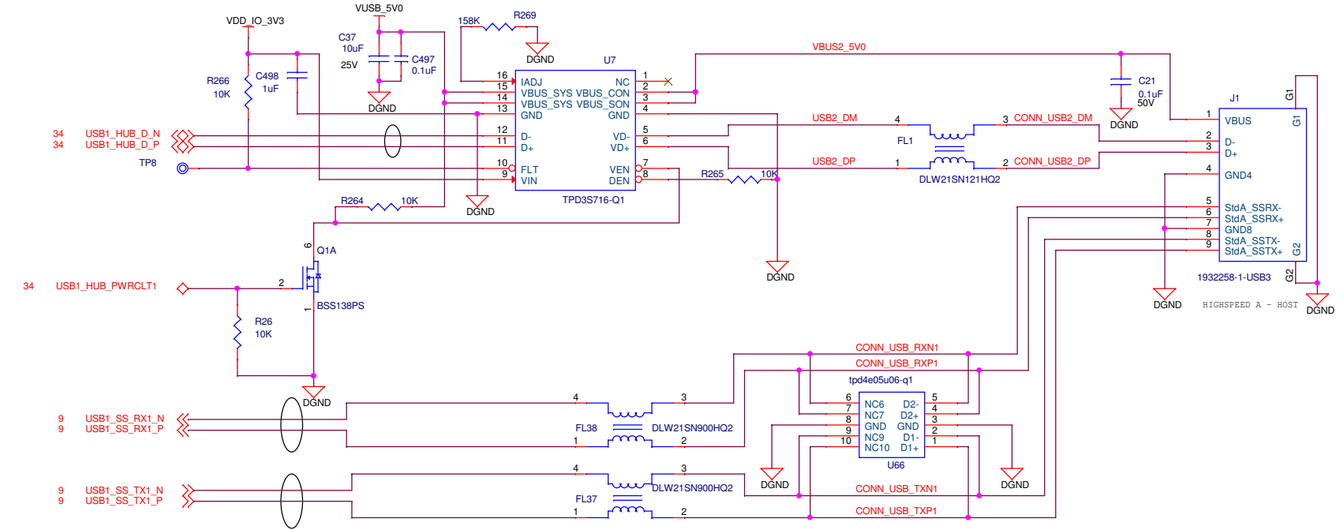
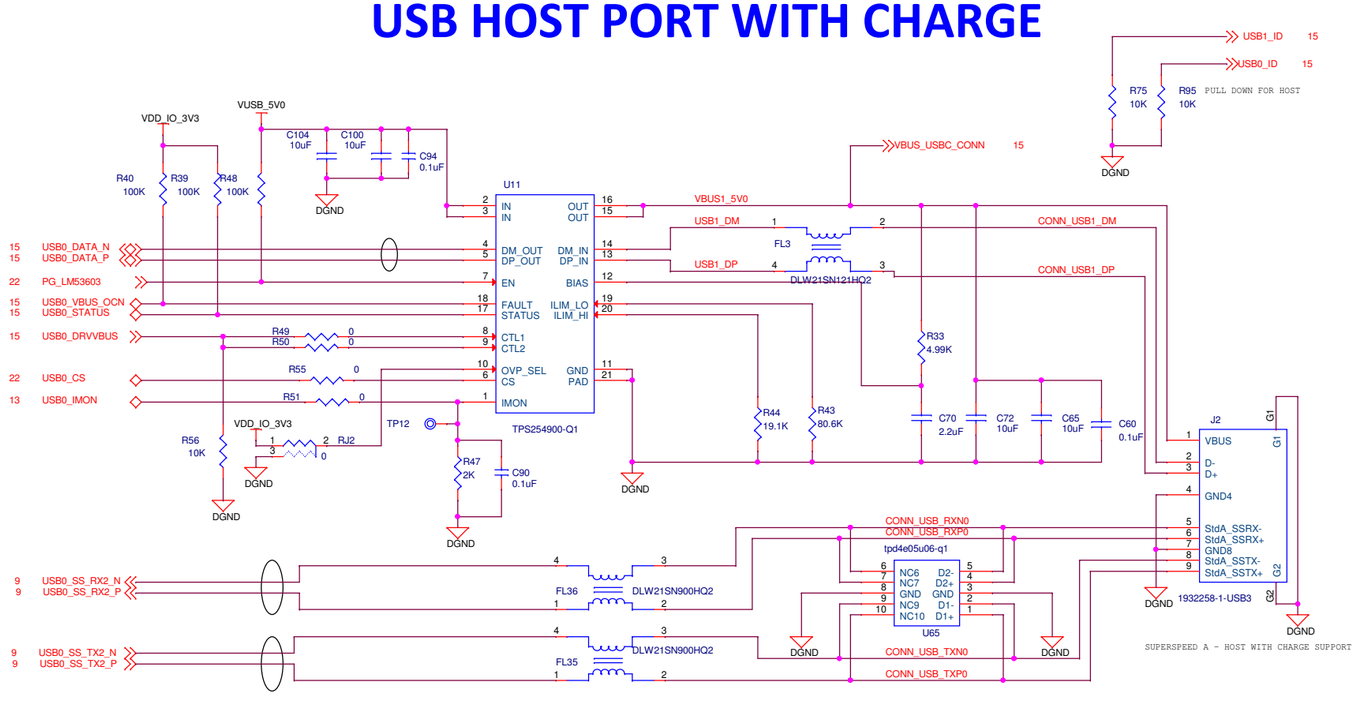
USB PORT FOR DEBUG

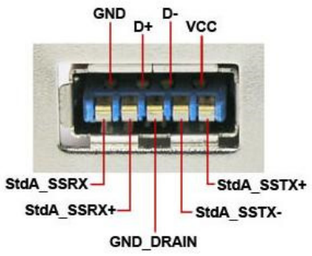


Q1B
BSS138PS

USB HOST PORT WITH CHARGE

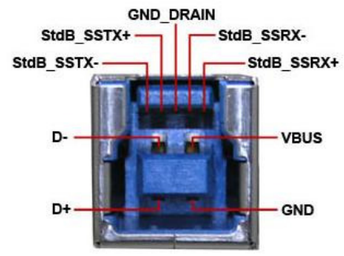


SuperSpeed standard A plug pinout



1	VBUS	Red
2	D-	White
3	D+	Green
4	GND	Black
5	StdA_SSRX-	Blue
6	StdA_SSRX+	Yellow
7	GND_DRAIN	GROUND
8	StdA_SSTX-	Purple
9	StdA_SSTX+	Orange
Shell	Shield	Connector Shell

SuperSpeed standard B plug pinout



1	VBUS	Red
2	D-	White
3	D+	Green
4	GND	Black
5	StdA_SSTX-	Blue
6	StdA_SSTX+	Yellow
7	GND_DRAIN	GROUND
8	StdA_SSRX-	Purple
9	StdA_SSRX+	Orange
Shell	Shield	Connector Shell

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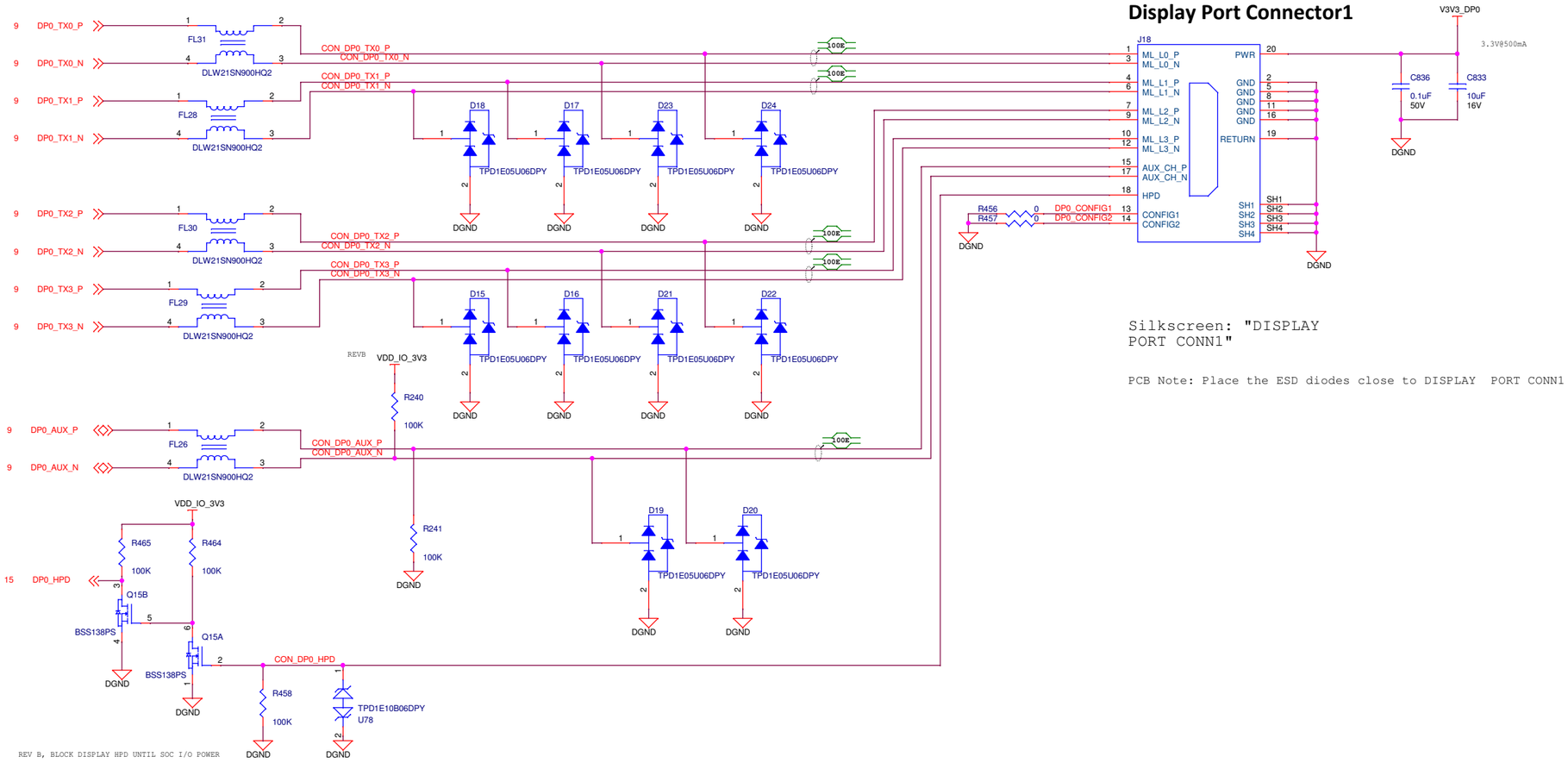
DISPLAY PORT INTERFACE



Silkscreen: "DISPLAY PORT CONN1"

PCB Note: Place the ESD diodes close to DISPLAY PORT CONN1

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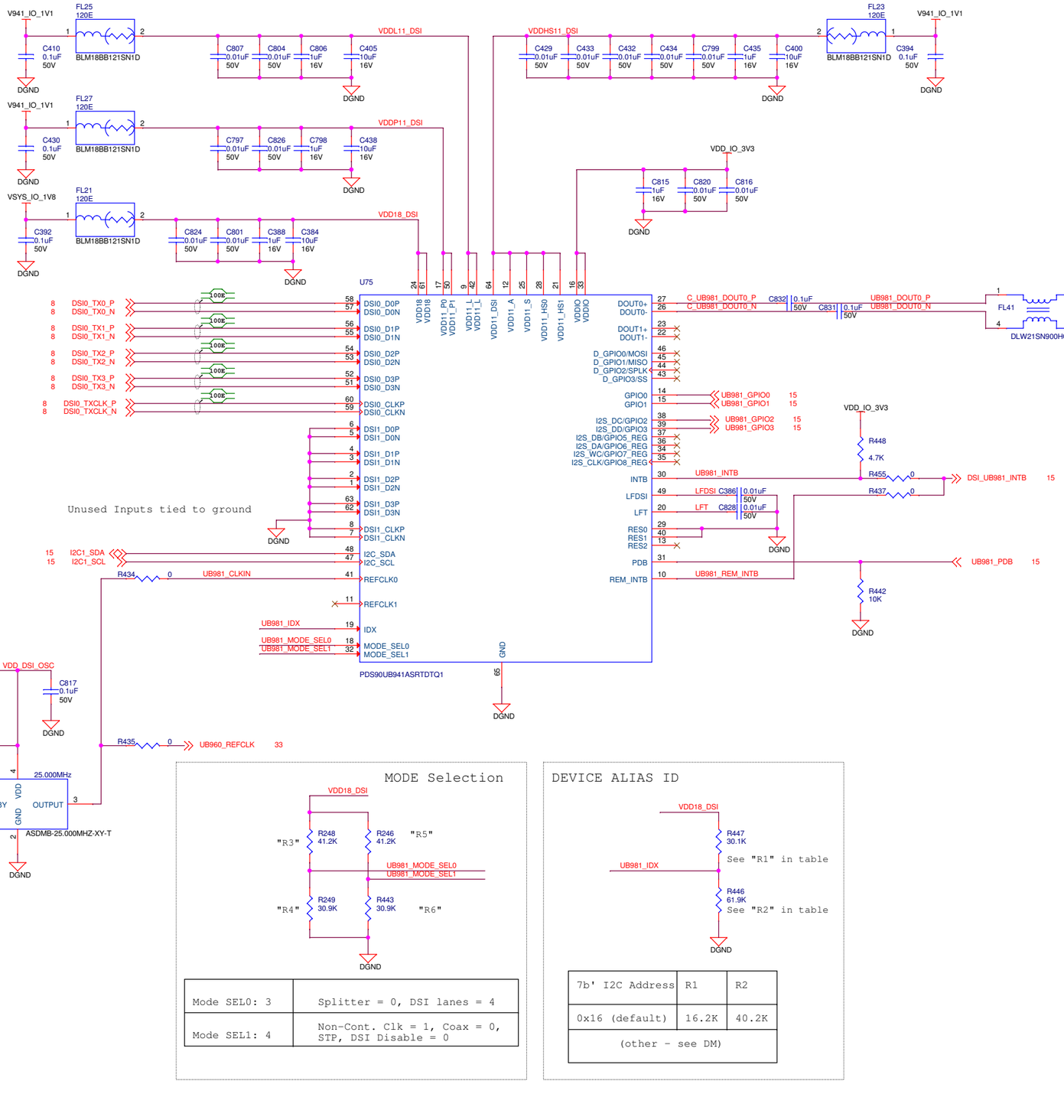
DSI FPD LINK

"For this version FPD-Link III Interface (PDS90UB941ASRTDTQ1) supported"



MODE Selection

Mode SEL0: 3	Splitter = 0, DSI lanes = 4
Mode SEL1: 4	Non-Cont. Clk = 1, Coax = 0, STP, DSI Disable = 0

DEVICE ALIAS ID

7b' I2C Address	R1	R2
0x16 (default)	16.2K	40.2K
(other - see DM)		

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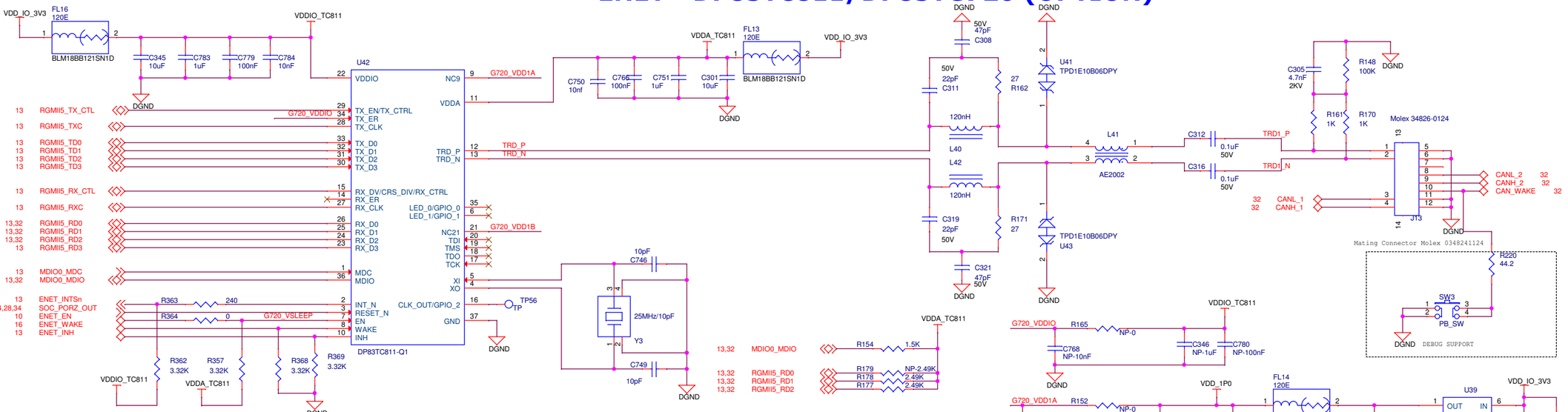
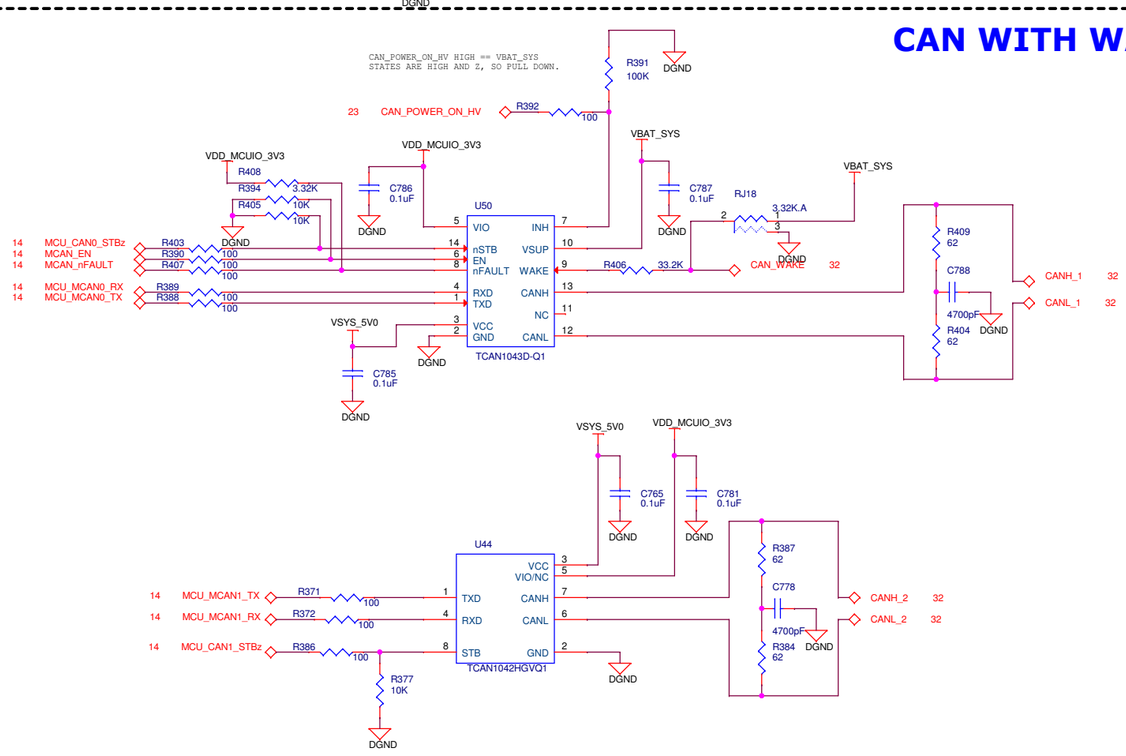
ENET - DP83TC811/DP83TG720 (OPTION)



CAN WITH WAKEUP



TEXAS INSTRUMENTS INCORPORATED

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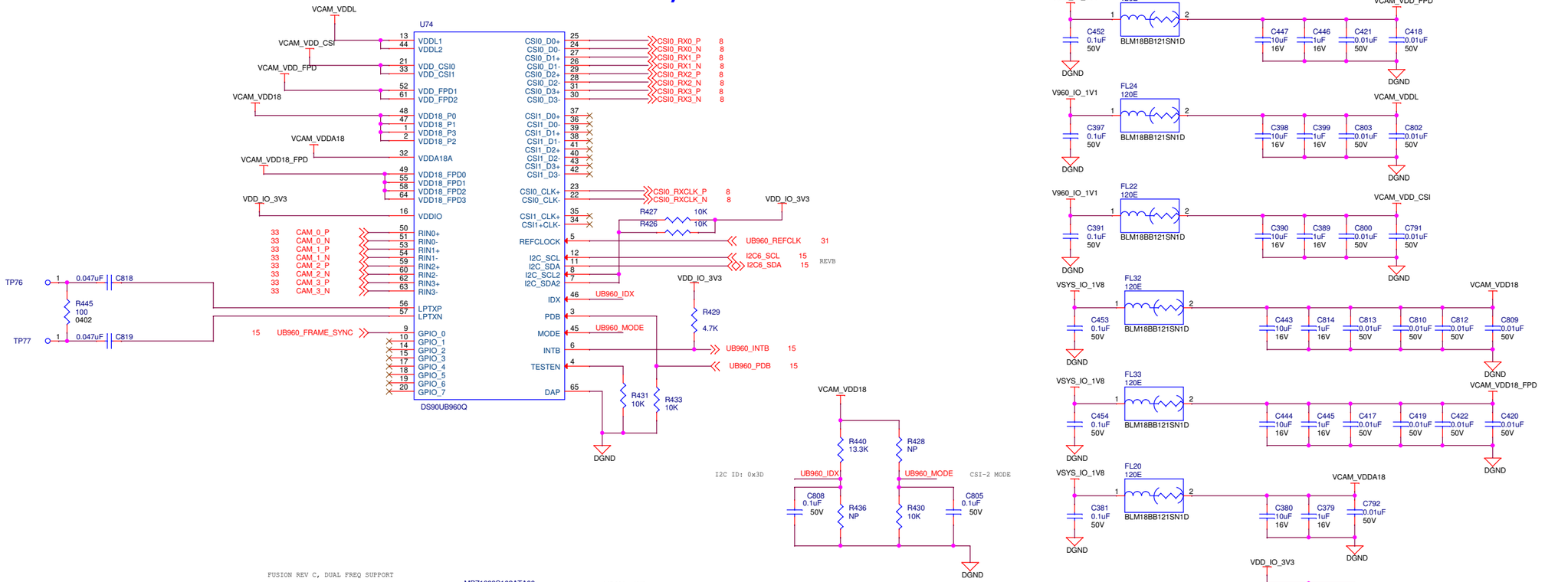
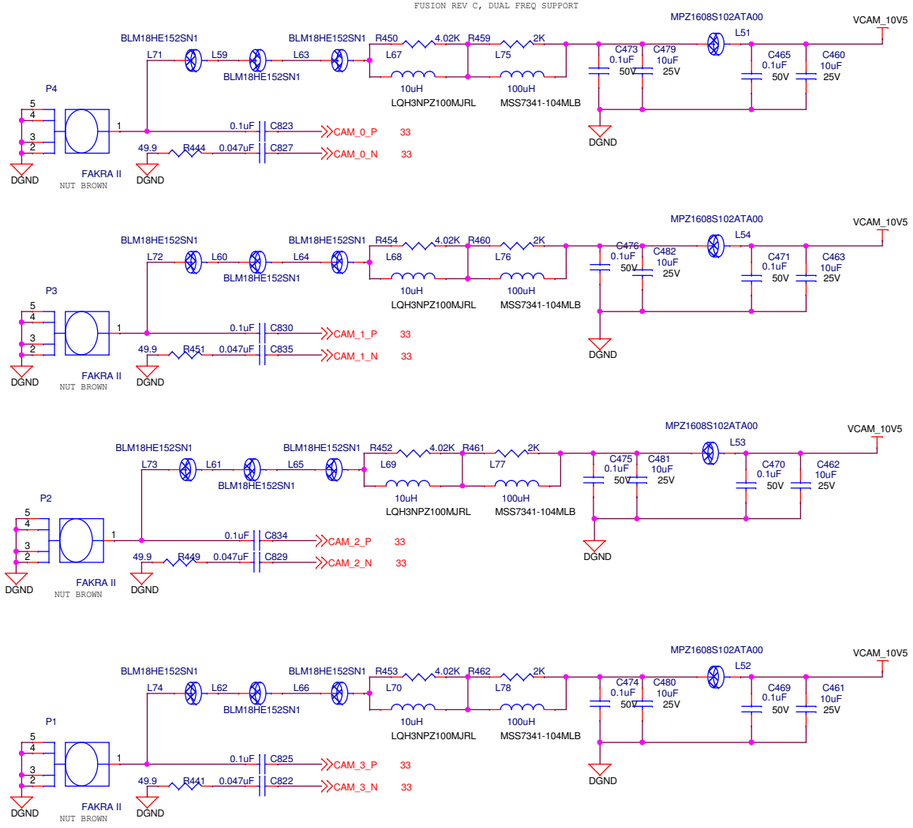
CSI2 CAMERA INTERFACE, FUSION I COMPATIBLE





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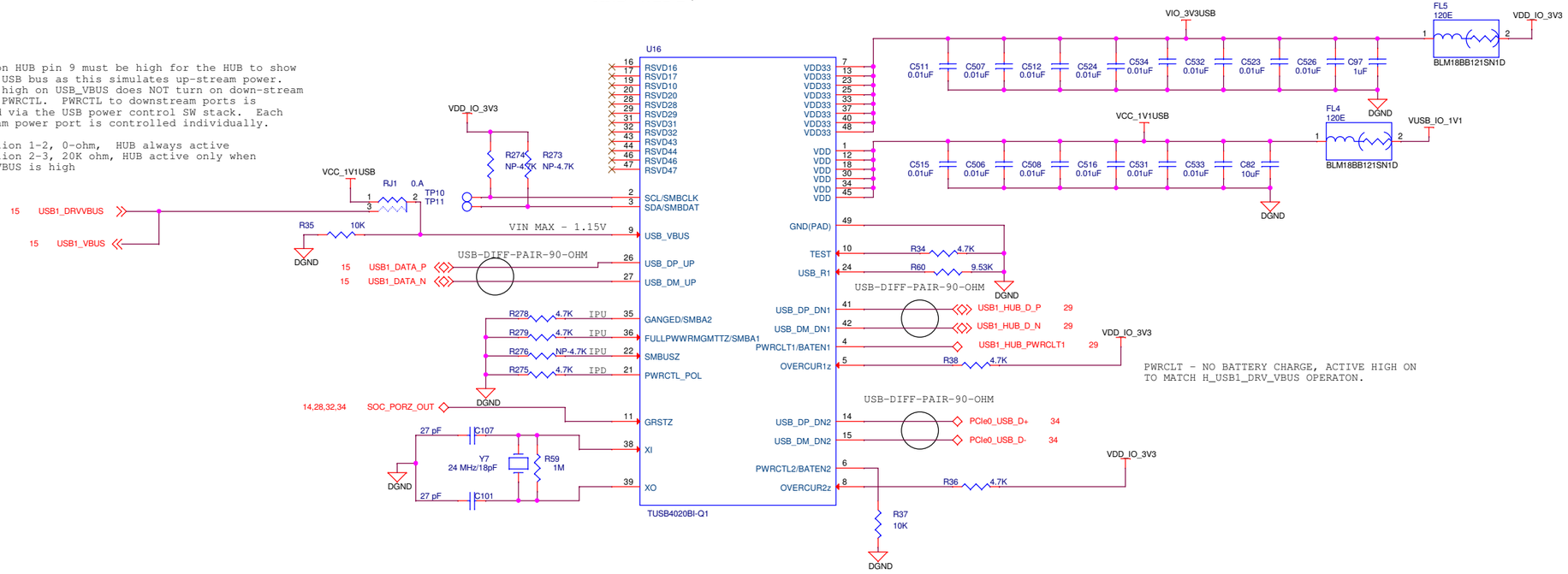
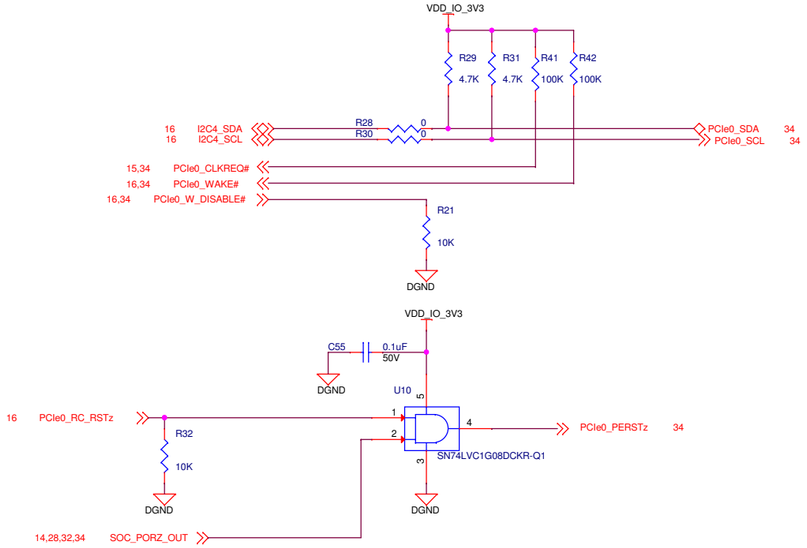
USB HUB FOR WIFI/DEBUG

USB HUB INCLUDED TO
SUPPORT USB DEBUG PORT
AND WIFI.

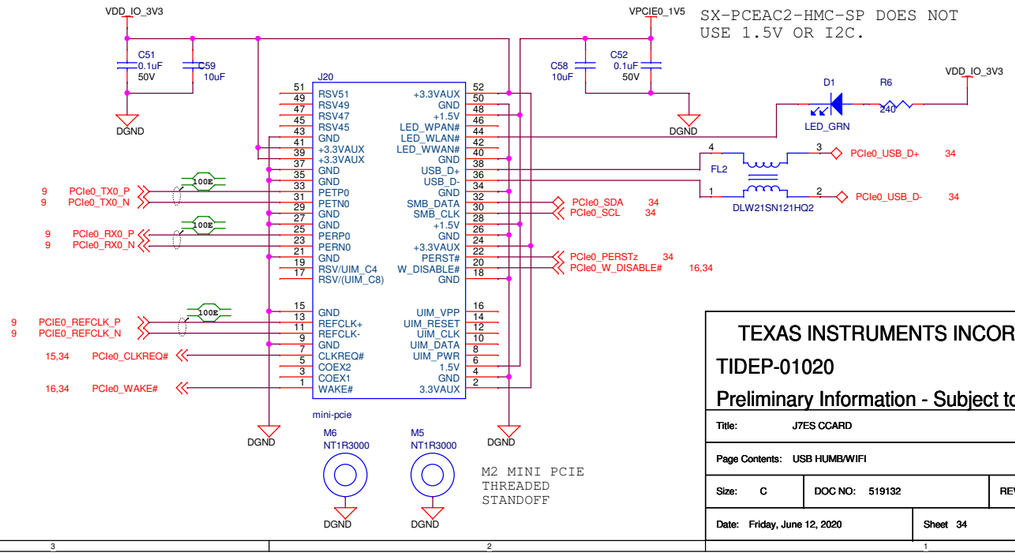
USB_VBUS on HUB pin 9 must be high for the HUB to show up on the USB bus as this simulates up-stream power. However a high on USB_VBUS does NOT turn on down-stream power via PWRCTL. PWRCTL to downstream ports is controlled via the USB power control SW stack. Each down-stream power port is controlled individually.

RJ16 - Option 1-2, 0-ohm, HUB always active
RJ16 - Option 2-3, 20K ohm, HUB active only when USB1_DRV_VBUS is high





Mini PCIe Half Card Interface (WiFi Only)



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Page Contents: USB HUMB/WIFI			
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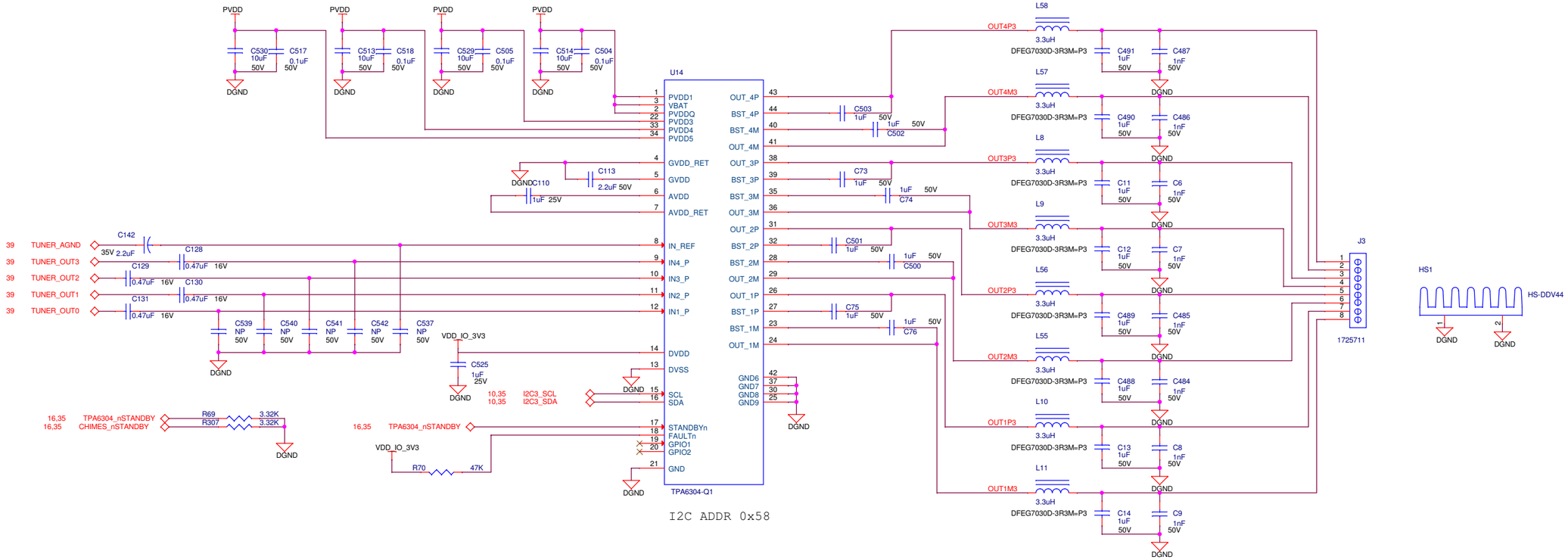
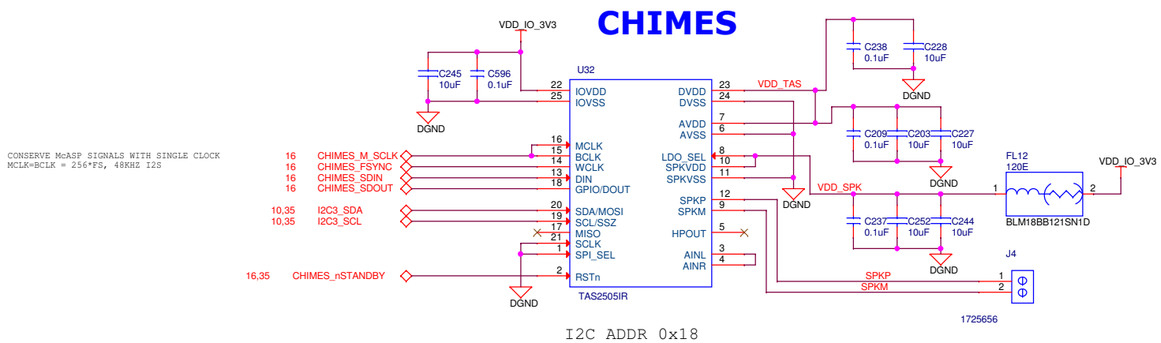
CLASS-D AUDIO OUT



CHIMES



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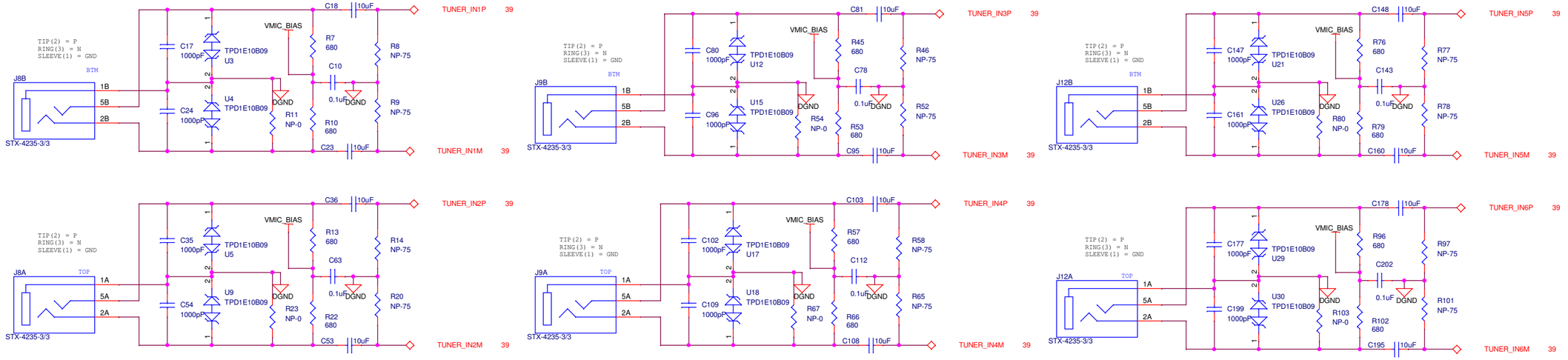
AUDIO IN



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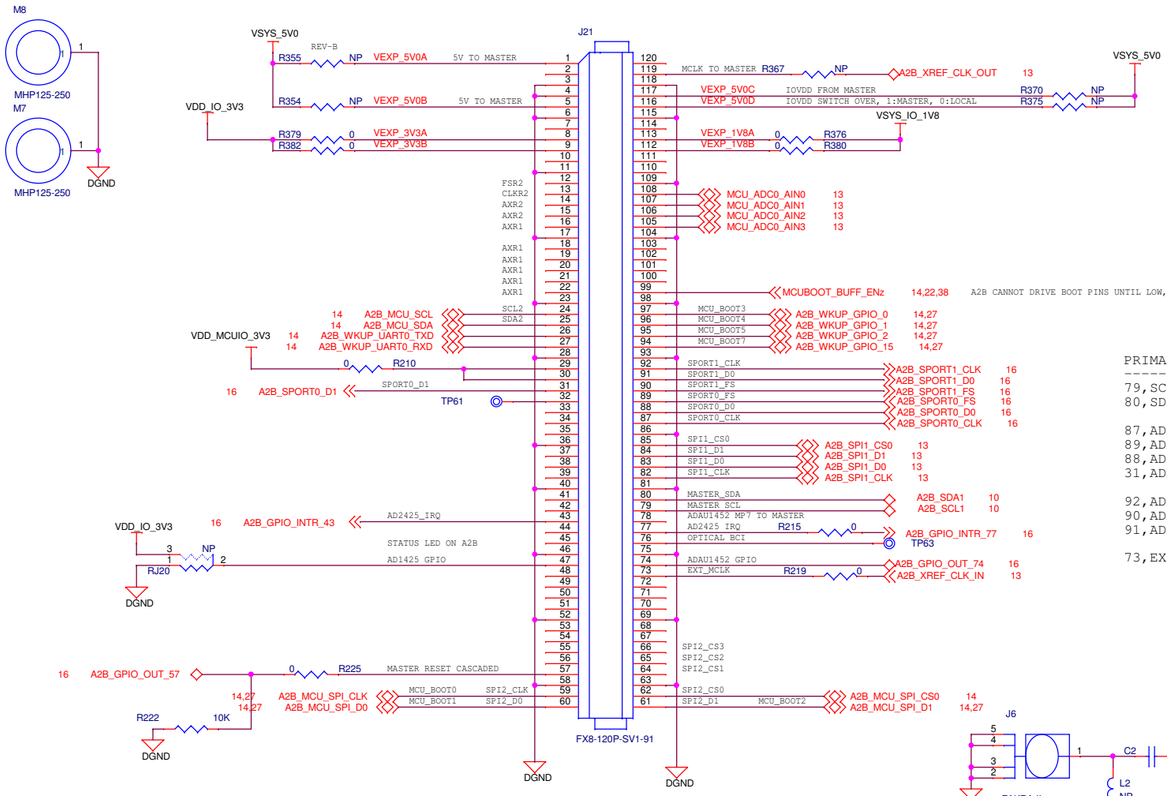
A2B EXPANSION



PRIMARY A2B SERIAL SIGNALS

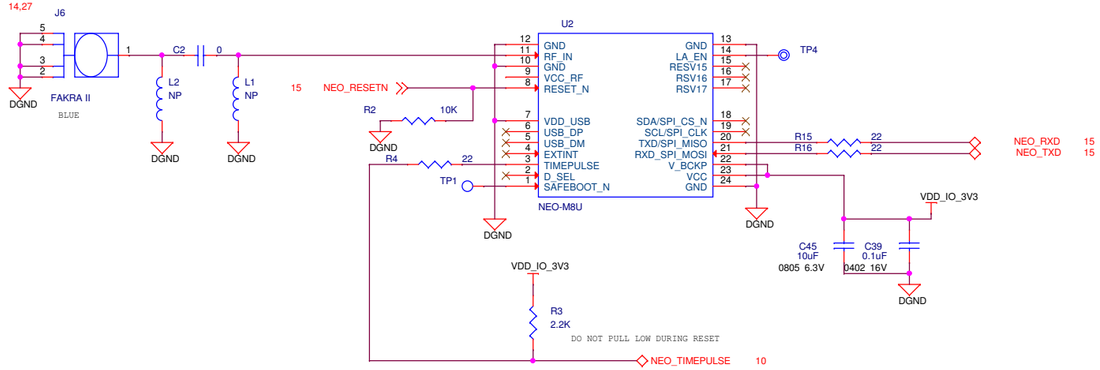
79,SCL from Master, local 3k32 pullup to IOVDD
80,SDA from Master, local 3k32 pullup to IOVDD

87,ADAU1452 BCLK_IN2 from Master (SPORT0_CLK,ALKX)
89,ADAU1452 LRCLK_IN2 from Master (SPORT0_FS,AFSX)
88,ADAU1452 SDATA_IN2 from Master (SPORT0_D0,AXRn)
31,ADAU1452 SDATA_OUT3 to Master (SPORT0_D1,AXRn)

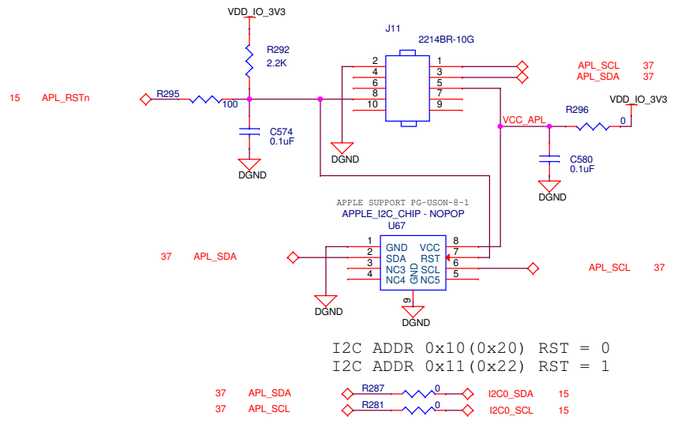
92,ADAU1452 BCLK_OUT2 to Master (SPORT1_CLK,ACLKR)
90,ADAU1452 LRCLK_OUT2 to Master (SPORT1_FS,AFSR)
91,ADAU1452 SDATA_OUT2 to Master (SPORT1_D0,AXRn)

73,EXT_MCLK from Master through resistor, normally OPEN (AHCLKX,XREF_CLK)

GNSS



APPLE SUPPORT MFISP00918596



I2C ADDR 0x10(0x20) RST = 0
I2C ADDR 0x11(0x22) RST = 1

37 APL_SDA R287 0 I2C0_SDA 15
37 APL_SCL R281 0 I2C0_SCL 15

M1 M2 M3 M4 MHP125-250 DGND

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DEBUG CONSOLE

Terminal Connector

J19 USBMINI_AB — USBVDD, SHIELD1–4, D-, D+, ID, USBVSS
Silkscreen: TERMINAL
R255 0

R237 240 — USART_LED — D14 LED_GRN — USART_PWREN
Silkscreen: FTDI_VBUS

U53 TPS73433 (VIN, NC, EN, VOUT, NR, GND)
VUSART_VBUS: C393 0.1uF, C456 4.7uF
VUSART_3V3: C374 0.01uF, C375 0.1uF
USART_NR

U60 TPD2E001DRL-Q1 (VCC, IO2, NC, IO1, GND)

VUSART_VBUS
USART_DM
USART_DP

U56 93AA46B (DO, GND, DIN, VCC, CS, CLK)
VUSART_3V3: C811 0.1uF
USART_EECS
USART_EESK
USART_EEDIN
USART_EEDOUT

VUSART_3V3: R239 1K, R432 1K, R238 1K
R232 2.2K

VPHY_USART: C408 0.1uF, C415 4.7uF — L47 BLM18AG601SN1D — VUSART_3V3: C371 4.7uF, C382 0.1uF, C370 0.1uF, C367 0.1uF, C372 0.1uF
VPLL_USART: C406 0.1uF, C416 4.7uF — L48 BLM18AG601SN1D — VUSART_1V8: C369 4.7uF, C407 0.1uF, C387 0.1uF, C368 0.1uF

Note: Buffers used for voltage translation and signal isolation.

VUSART_1V8
VUSART_3V3

U52 FT2232H
VPHY, VPLL, VCORE, VCCIO
VREGIN, VREGOUT
RESET#, REF
USBDM, USBDP
EECS, EESK, EEDATA
OSCI, OSCO
SUSPEND#, PWREN#
TEST, AGND, GND
ADBUS0/TXD/TCK … ADBUS7/RI#/GPIOL3
ACBUS0/TXDEN/GPIOH0 … ACBUS7/-/GPIOH7
BDBUS0/TXD/TCK … BDBUS7/RI#/GPIOL3
BCBUS0/TXDEN/GPIOH0 … BCBUS7/-/GPIOH7

USART_A_TXD
USART_A_RXD
USART_B_TXD
USART_B_RXD
USART_RESETn
USART_RSET
R236 1K
R235 12K

USART_OSCI: C441 27pF
USART_OSCO: C449 27pF
Y5 12MHz CRYSTAL (NC1, NC2)

USART_PWREN

VDD_MCUIO_3V3: C795 0.1uF, C794 0.1uF
VDD_IO_3V3: C790 0.1uF, C789 0.1uF

U55 SN74AVC4T245RGYR-Q1 (VCCA, VCCB, 1DIR, 2DIR, 1OE, 2OE, 1A1, 1A2, 2A1, 2A2, 1B1, 1B2, 2B1, 2B2, GND1, GND2, GND3)
U51 SN74AVC4T245RGYR-Q1 (same)

14,22,37 MCUBOOT_BUFF_ENz
USART_PD
R226 22
R231 10K
R227 10K
R217 22
R218 10K
R214 10K
R216 10K

TXDA — R223 — MCU_CONSOLE_RXD 14
RXDA — USART_PD — MCU_CONSOLE_TXD 14
TXDB — R212 — A72_CONSOLE_RXD 15
RXDB — USART_PD — A72_CONSOLE_TXD 15

DO RX/TX SWAP

MCU_BOOTMODE[9:8], HIGH-Z UNTIL BOOT DONE.

DEBUG JTAG

VDD_MCUIO_3V3
R424 100
R415 4.7K, R414 4.7K, R410 4.7K
R411 0
R413 0
R412 4.7K
R425 4.7K
R191 10K

J15 MIPI-QSH-030
VREF_DBG, TCK, TDI, RTCK, nTRST, EXTF, TR_CLK0, TGT_DETECT, TRD0.0 … TRD3.9, Gnd57, TR_CLK3, GndCt1, GndCt3
TMS, TDO, nRESET, TRSTPD, EXTE, VREF_TR, TR_CLK1, Gnd16, TRD1.0 … TRD2.9, Gnd58, TR_CLK2, GndCt2, GndCt4

XDS560v2(default jtag support)

14 SOC_TCK, 38 EXT_TDI
14 SOC_EMU0, 14 SOC_EMU1
EMU0, EMU1
nTRST
TRSTPD — RJ19 0.0A — SOC_TRST# 14

EXT_TMS 38
EXT_TDO 38
EMU_RSTn 14

XDS560V2 OPEN-DRAIN, PULLUP AT DESTINATION TO APPROPRIATE VOLTAGE LEVEL IF USED.

TRSTn == MIPI TRSTPD PULL DOWN VERSION
TRSTn == MIPI nTRST MIPI PULLUP VERSION
FOR CJTAG SET THE RJ TO PINS 3-2.

TCK,TRSTn,EMU0,EMU1 ON VDDSHV0_MCU POWER DOMAIN.
TMS,TDI,TDO ON VDDSHV0 POWER DOMAIN.
ISOLATE TMS,TDI,TDO TO PREVENT EMULATOR DRIVING INTO SOC WHEN VDDSHV0 IS OFF.
TCK,TRSTn,EMU0/1 DRIVE CONTROLLED BY VDDSHV0_MCU (I.E. VREF_DBG).

VSYS_3V3
38 EXT_TDI — U48 74CBTLV1G125CRG4 — SOC_TDI 14
38 EXT_TMS — U49 74CBTLV1G125CRG4 — SOC_TMS 14
14 SOC_TDO — U47 74CBTLV1G125CRG4 — EXT_TDO 38
C348 0.1uF
R393 4.7K

21,24,25,26 EN_3V3IO_LDSW — Q6 BSS138

DOUBLE CHECK VOLTAGE LEVEL ON EN_3V3IO_LDSW AND PULLDOWN.

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RADIO TUNER

BAND3/FM

J7 FAKRA II BLACK

C25 20pF, C32 11pF, C62 13pF

L12 62nH, L17 39nH, L23 68nH

C34 36pF, C61 680pF

D3

L5 72nH, C29 1nF, L22 160nH, C71 22pF

L14 100nH, L18 18nH

C38 470pF, C50 43pF

L26 72nH, C79 43pF

FMA

B3A

ANTENNA FROM LCARD

BAND3/FM/AM

J5 FAKRA II WHITE

C31 20pF, C48 11pF, C68 13pF

L16 62nH, L21 39nH, L25 68nH

C49 36pF, C69 680pF

D3B

D2

L3 72nH, C27 1nF, L20 160nH, C67 22pF

L15 100nH, L7 18nH

C44 470pF, C30 43pF

L24 72nH, C77 43pF

C22 82pF

FMB

AMI

L13 1.0uH, C26 3.6pF, C40 7.0pF

L6 330nH

D5

R24 120, R27 NP

C57 1pF

L19 1.5uH

C66 2200pF

POWER FROM LCARD

VSYS_IO_1V8 — 0805,1K OHMS,1.5A — L31 MPZ2012S102A — VTUN_1V8 — TP18

C133 0.1uF 16V, C132 10uF 10V, C134 10uF 10V

VDD_IO_3V3 — 0805,1K OHMS,1.5A — L27 MPZ2012S102A — VTUN_3V3 — TP9

C88 0.1uF 16V, C87 10uF 10V, C89 10uF 10V

Y6 36.864MHz — XTAL1, XTAL2

R64 10K TCN

PL1, PL0201

TUNER_AGND IS DGND SIGNAL TRACE ROUTED WITH TUNER_OUTx TO TPA6304 IN_REF.

TUNER_OUT0, TUNER_OUT1, TUNER_OUT2, TUNER_OUT3, TUNER_AGND

U19 Si47972

VTUN_3V3: C84 1uF, C86 2.2nF, C93 18pF

C92 1uF, C522 0.1uF

VA

VTUN_3V3: C83 1uF, C85 2.2nF, C91 18pF

AOUT5, ABYP1, VA1, CLKO, XTALO, XTALI, DACREF, FMA, B3A, B3B, FMB, AMO, AMI, AMVAG, LTB, LTA, ABYP2, VA2, AIN0P, AIN0N, AIN1P, AIN1N

TUNER_IN1P, TUNER_IN1M, TUNER_IN2P, TUNER_IN2M, TUNER_IN3P, TUNER_IN3M, TUNER_IN4P, TUNER_IN4M, TUNER_IN5P, TUNER_IN5M, TUNER_IN6P, TUNER_IN6M

DICLK3, DIFS3, DIN4, DICLK4, DIFS4, DOUT0, DCLK0, DFS0, DFSO, DOUT1, DCLK1, DFS1, DEBUGP, DEBUGN, ISFSP, ISFSN, ZIFI0, ZIFCLK, ZIFQ0, ZIFFS, ZIFI1, ZIFQ1, VIO2

DOUT0, DCLK0, DFS0, DOUT1, DEBUGP, DEBUGN, ZIFFS1, ZIFCLK1, ZIFI0, ZIFCLK0, ZIFQ0, ZIFFS0, ZIFI1, ZIFQ1

DIN3, DIN4

TUNER_AUDIO_AXR0 16, TUNER_AUDIO_AXR1 16, TUNER_AUDIO_ACLKX 16, TUNER_AUDIO_FSX 16

TP22, TP2

C561 1000pF, C562 0.1uF

U23 SN74LVC1G125DCKR-Q1 — R82 44.2 — TUNER_AUDIO_AXR10 16

U22 SN74LVC1G125DCKR-Q1 — R81 44.2 — TUNER_AUDIO_AXR11 16

C567 1000pF, C551 0.1uF, C566 1000pF

J10 NP-HDR3

U25 SN74AVC8T245RHL-Q1

R92 44.2 TUNER1_IQ_FSR 16,39

R91 44.2 TUNER1_IQ_ACLKR 16,39

R90 44.2 TUNER0_IQ_AXR0 16,39

R89 44.2 TUNER0_IQ_ACLKR 16,39

R88 44.2 TUNER0_IQ_AXR1 16,39

R87 44.2 TUNER0_IQ_FSR 16,39

R86 44.2 TUNER1_IQ_AXR0 16,39

R85 44.2 TUNER1_IQ_AXR1 16,39

TP27, TP31, TP26, TP30, TP25, TP29, TP24, TP28

TUNER1_IQ_FSR 16,39; TUNER1_IQ_ACLKR 16,39; TUNER0_IQ_AXR0 16,39; TUNER0_IQ_ACLKR 16,39; TUNER0_IQ_AXR1 16,39; TUNER0_IQ_FSR 16,39; TUNER1_IQ_AXR0 16,39; TUNER1_IQ_AXR1 16,39

VDD_IO_3V3: C146 2.2nF, C150 1uF, C144 18pF

VDD_IO_3V3: C118 18pF, C117 2.2nF, C116 1uF

VTUN_1V8: C127 18pF, C126 2.2nF, C125 1uF

TUNER_SPI_CS0 16, TUNER_SPI_SCLK 16, TUNER_SPI_D0 16, TUNER_SPI_D1 16

VDD_IO_3V3: R68 10K

TUNER_INTB_CHIP0 13, TUNER_RSTB_CHIP0 13

R280 0K

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TIDEP-01020			
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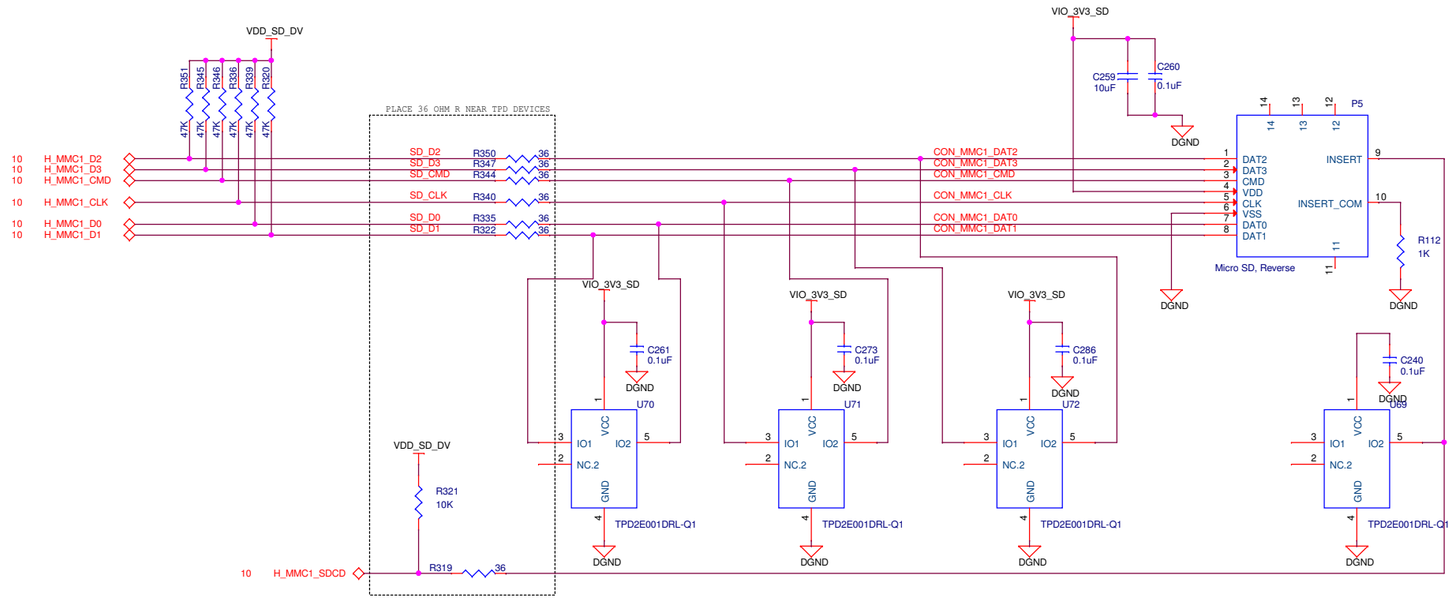
OPTIONAL SD CARD SUPPORT



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