| Revision History | | | | |
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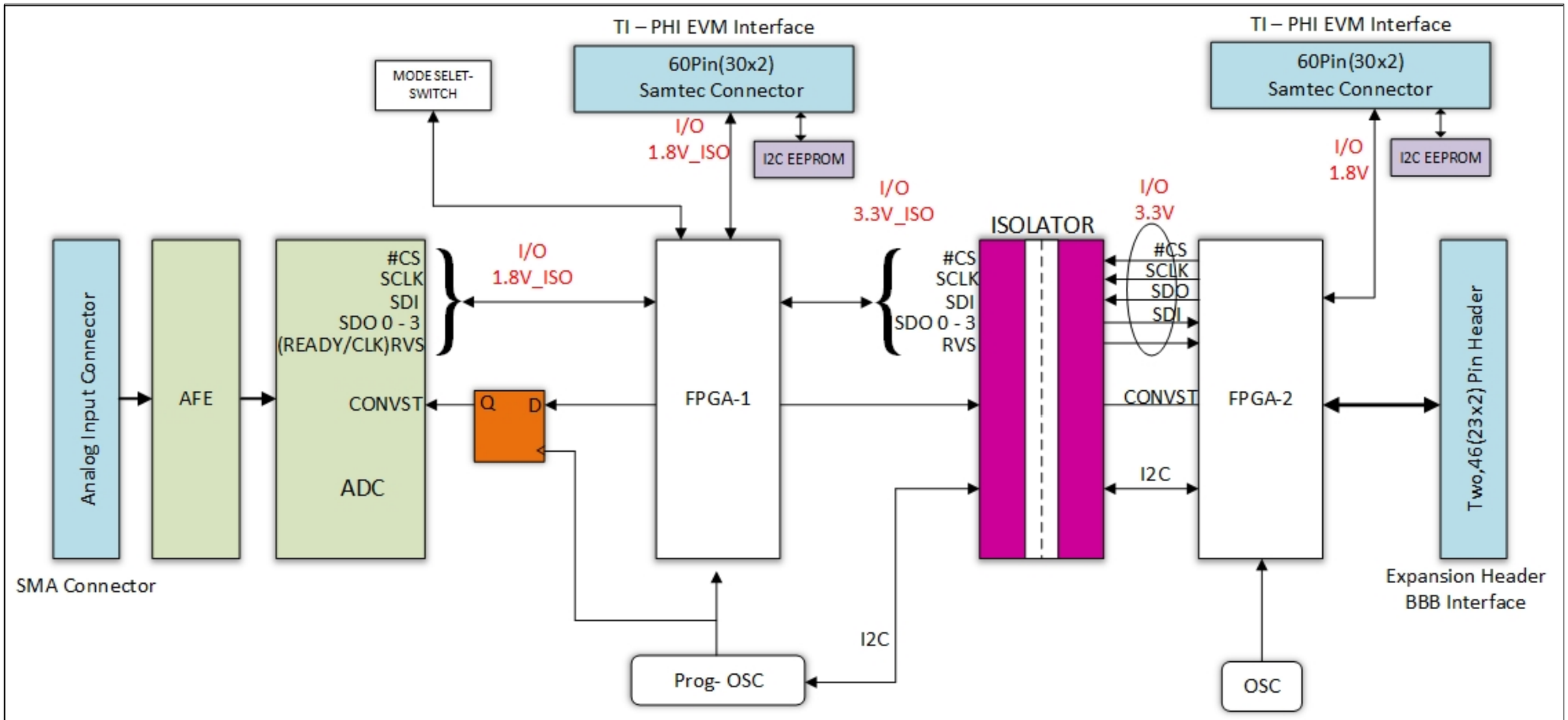
| Rev | ECN # | Approved Date | Approved by | Notes |
| N/A | N/A | N/A | N/A | N/A |




**TIDA-00732 -***Jitter minimizing techniques for digitally isolated high speed, high SNR (2.0 Msps, 18b) analog input DAQ Reference Design*



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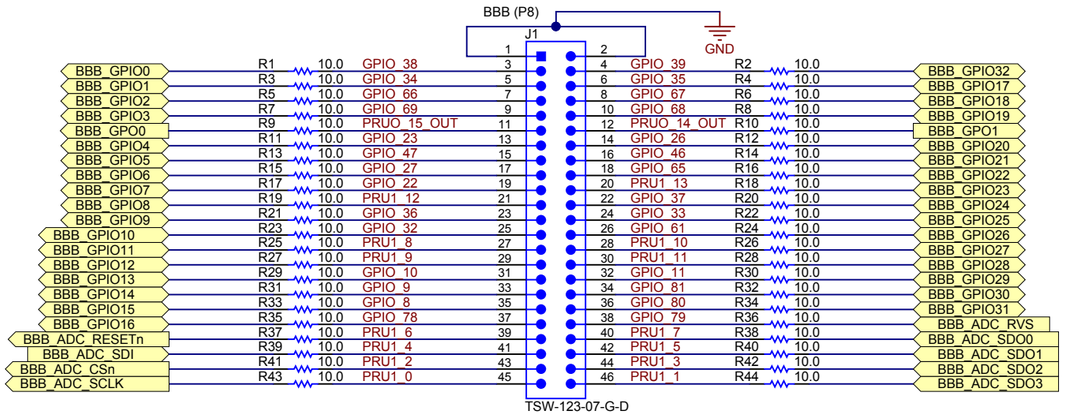
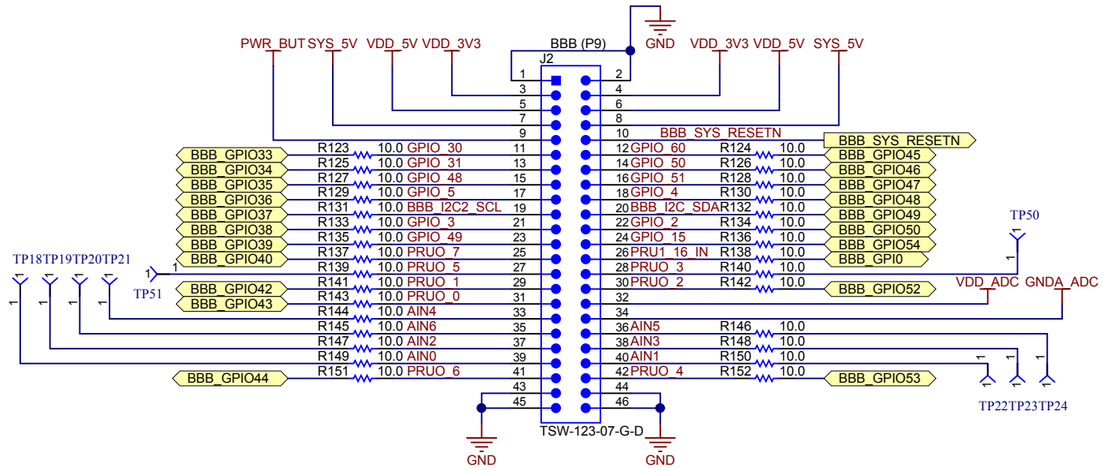
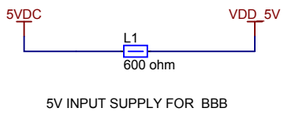
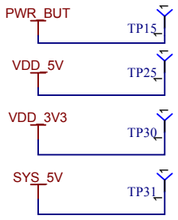
|---|---|---|
| Orderable: N/A | Designed for: Public Release | Mod. Date: 2/27/2016 |
| TID #: TID-00732 | Project Title: Jitter minimizing techniques for digitally isolated high | |
| Number: TIDA-00732 Rev: E1 | Sheet Title: Block Diagram | |
| SVN Rev: Version control disabled | Assembly Variant: ADS9110 w/REF5045 | Sheet: 1 of 10 |
| Drawn By: Anbu Mani | File: TIDA-00732_CoverSheet.SchDoc | Size: B |
| Engineer: Anbu Mani | Contact: http://www.ti.com/support | |

http://www.ti.com

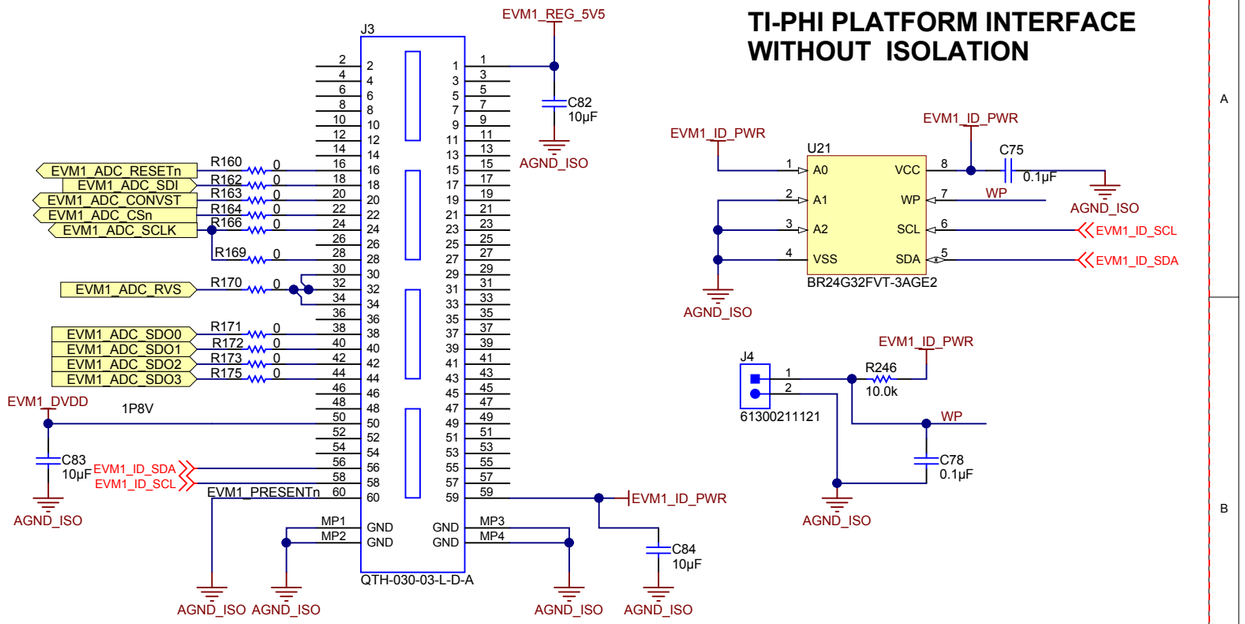


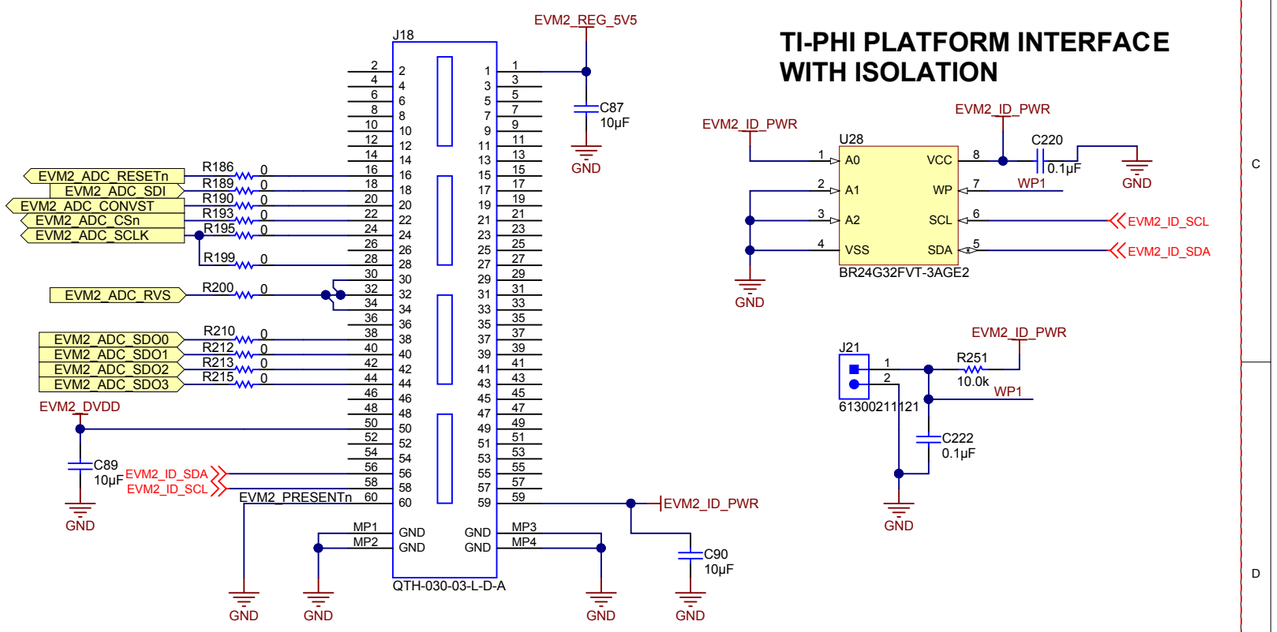




## BEAGLE BONE BLACK INTERFACE WITH ISOLATION



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| Orderable: N/A | | Designed for: Public Release | Mod. Date: 2/27/2016 |
| TID #: TID-00732 | | Project Title: Jitter minimizing techniques for digitally isolated high | |
| Number: TIDA-00732 | Rev: E1 | Sheet Title: Connector | |
| SVN Rev: Version control disabled | | Assembly Variant: ADS9110 w/REF5045 | Sheet: 2 of 10 |
| Drawn By: Anbu Mani | | File: TIDA-00732_Connector.SchDoc | Size: B |
| Engineer: Anbu Mani | | Contact: http://www.ti.com/support | |

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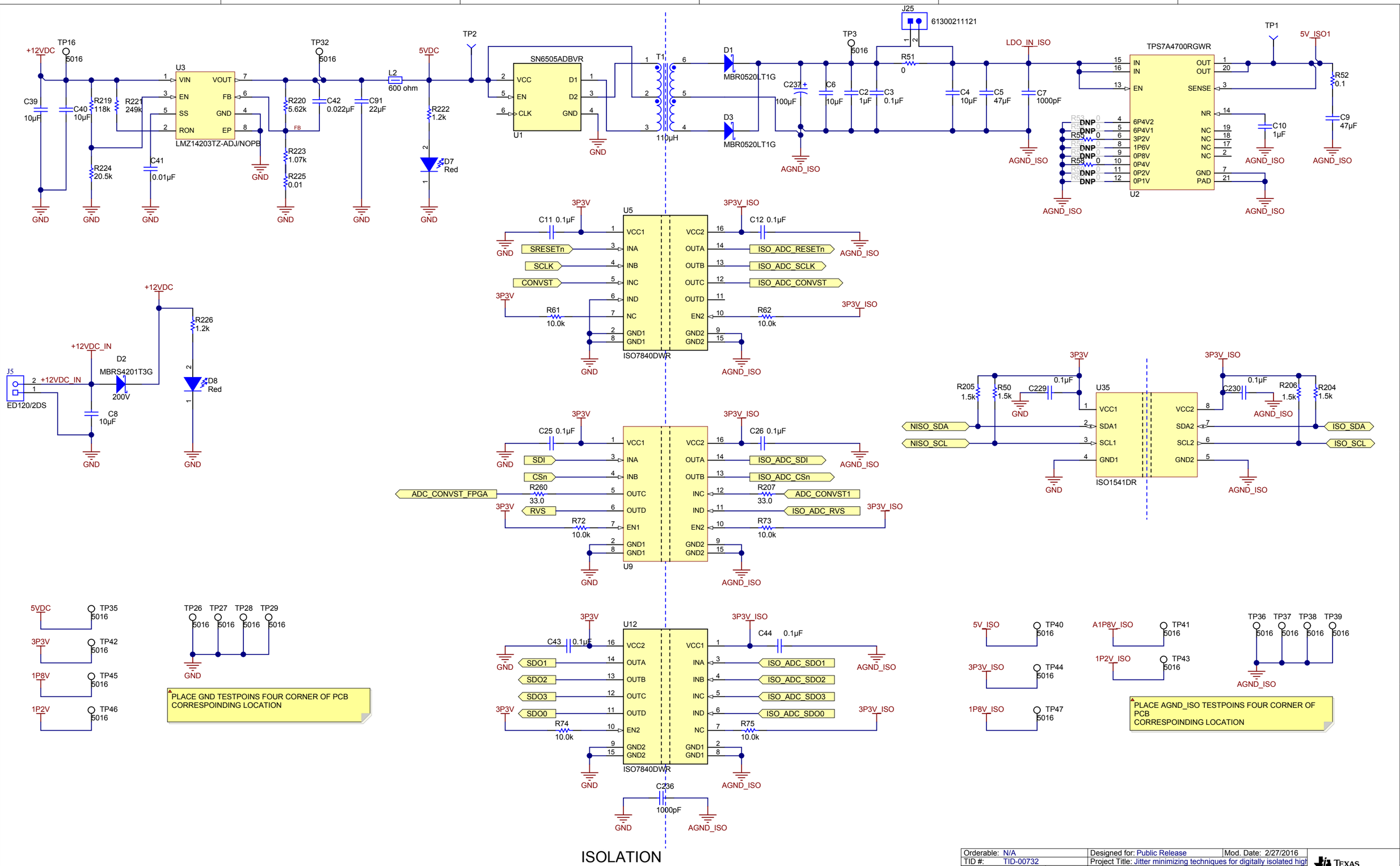




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| Number: TIDA-00732 | Rev: E1 | Sheet Title: Power & Isolators | |
| SVN Rev: Version control disabled | | Assembly Variant: ADS9110 w/REF5045 | Sheet: 3 of 10 |
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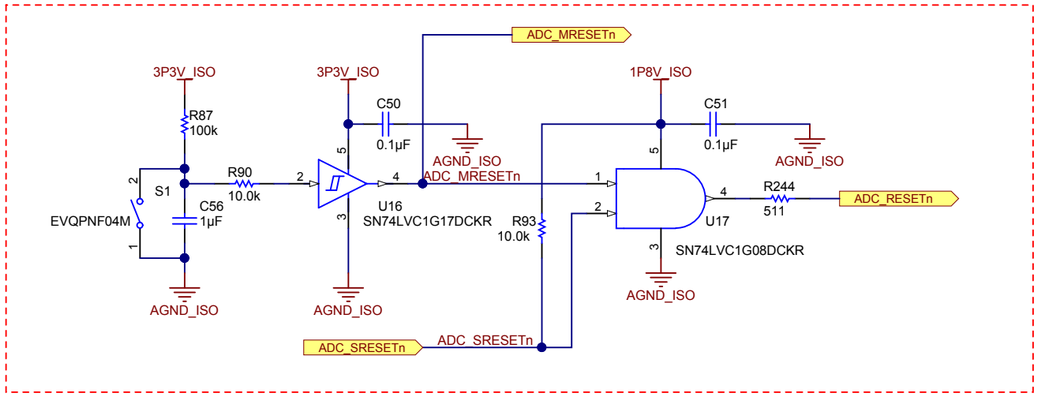
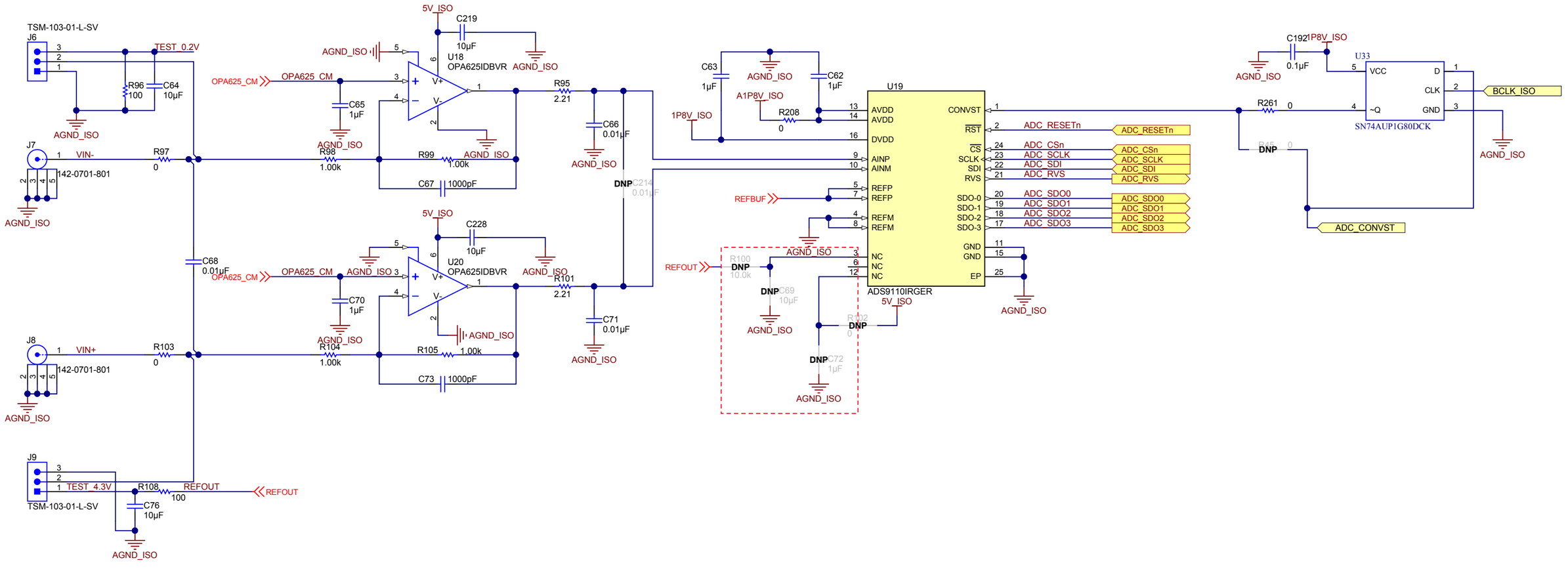
| Engineer: Anbu Mani | | Contact: http://www.ti.com/support | |

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| Number: TIDA-00732 | Rev: E1 | Sheet Title: Analog Front End & ADC | |
| SVN Rev: Version control disabled | | Assembly Variant: ADS9110 w/REF5045 | Sheet: 4 of 10 |
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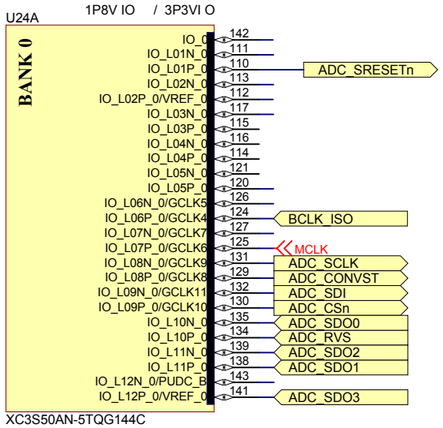


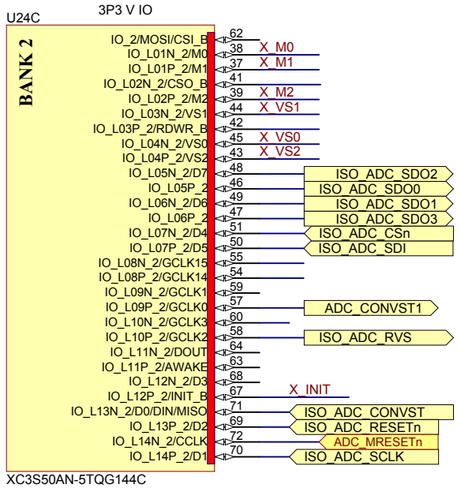


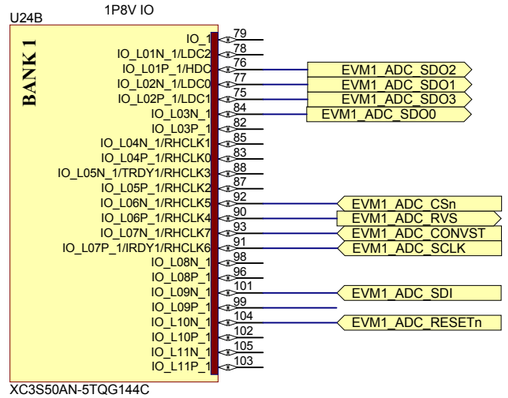


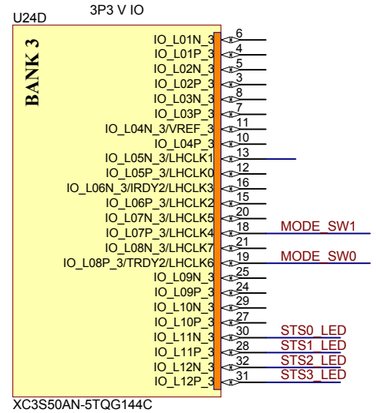


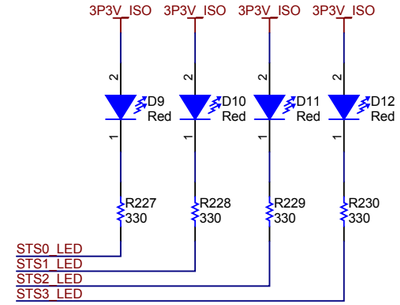


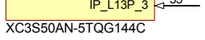


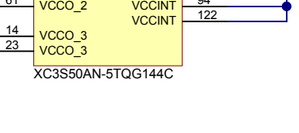


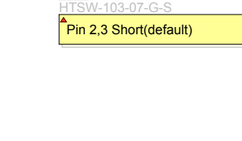


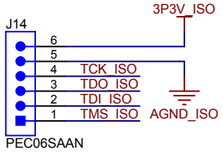


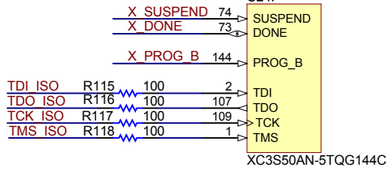


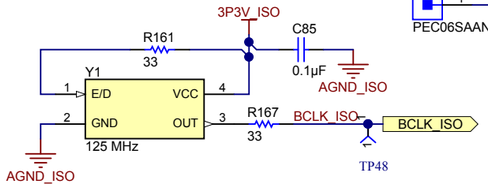


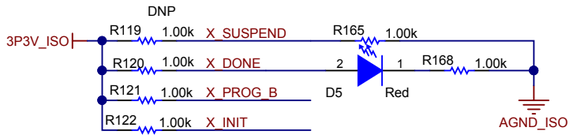


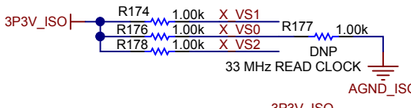


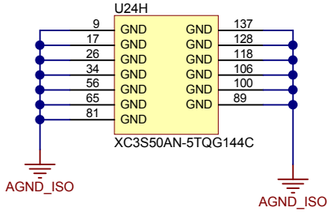





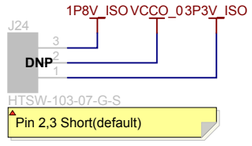


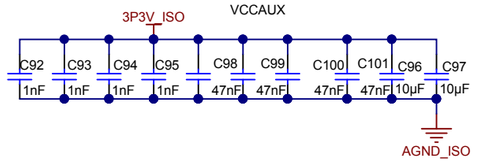


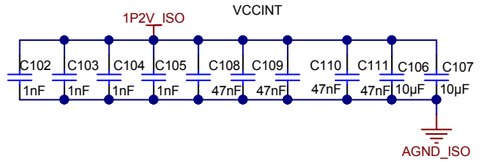


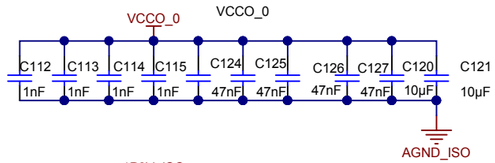


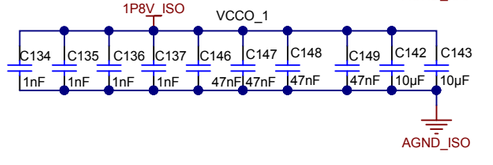


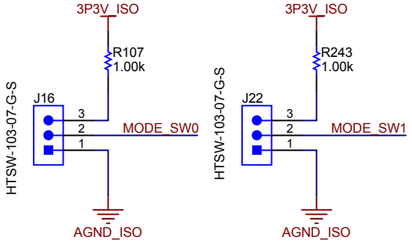


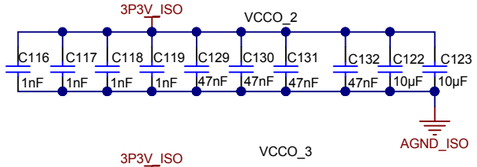


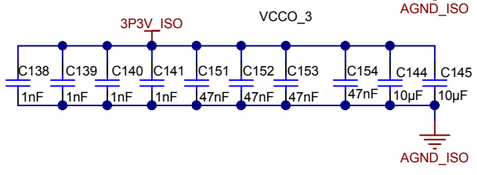


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| Orderable: N/A | | Designed for: Public Release | Mod. Date: 2/26/2016 |
| TID #: TID-00732 | | Project Title: Jitter minimizing techniques for digitally isolated high | |
| Number: TIDA-00732 | Rev: E1 | Sheet Title: FPGA 1 - Isolated End | |
| SVN Rev: Version control disabled | | Assembly Variant: ADS9110 w/REF5045 | Sheet: 5 of 10 |
| Drawn By: Anbu Mani | | File: TIDA-00732_FPGA_1.SchDoc | Size: B |
| Engineer: Anbu Mani | | Contact: http://www.ti.com/support | |

Text String

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XC3S50AN-5TQG144C

U25C 3P3VI O

BANK 2

XC3S50AN-5TQG144C

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U25D

BANK 3

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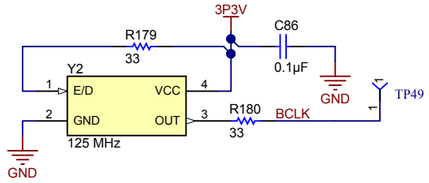
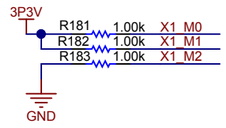
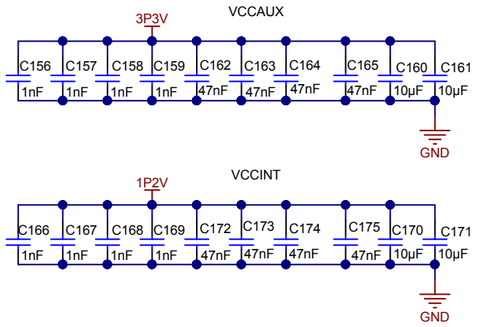
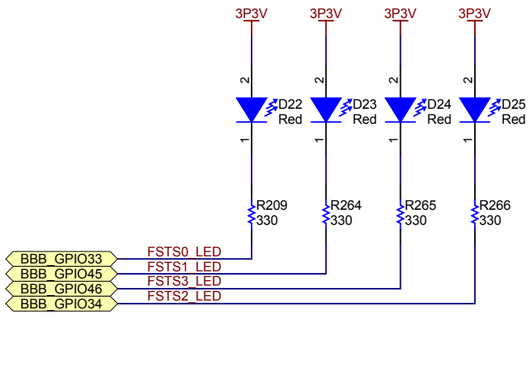


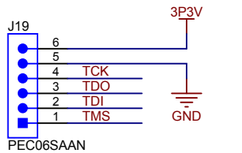



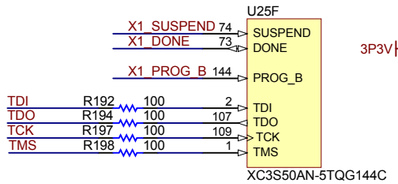



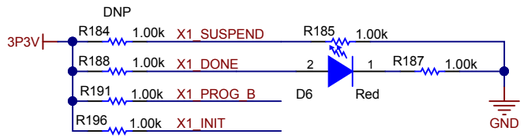


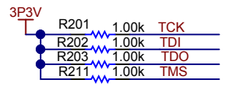


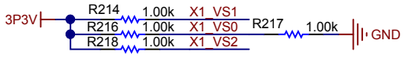


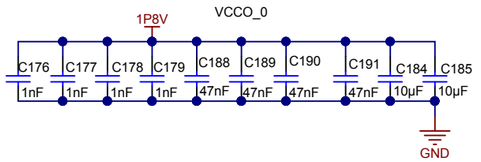



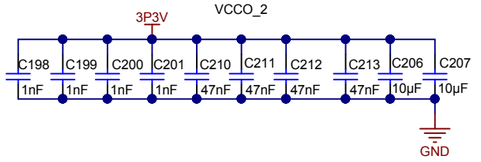



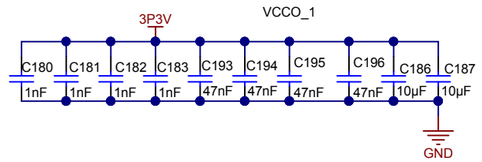



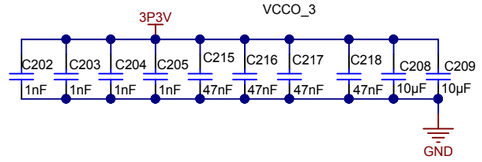



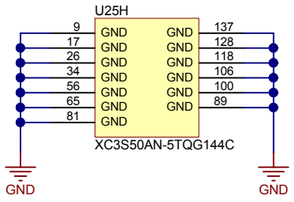



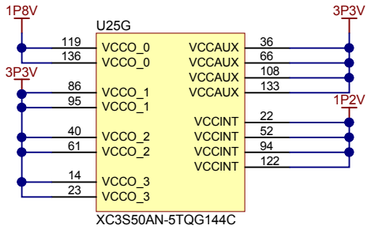



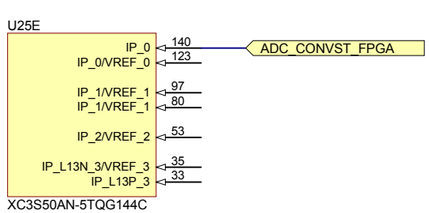




DNP
33 MHz READ CLOCK

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| Orderable: N/A | | Designed for: Public Release | Mod. Date: 2/26/2016 |
| TID #: TID-00732 | | Project Title: Jitter minimizing techniques for digitally isolated high | |
| Number: TIDA-00732 | Rev: E1 | Sheet Title: FPGA 2- Non-Isolated End | |
| SVN Rev: Version control disabled | | Assembly Variant: ADS9110 w/REF5045 | Sheet: 6 of 10 |
| Drawn By: Anbu Mani | | File: TIDA-00732_FPGA_2.SchDoc | Size: B |
| Engineer: Anbu Mani | | Contact: http://www.ti.com/support | |



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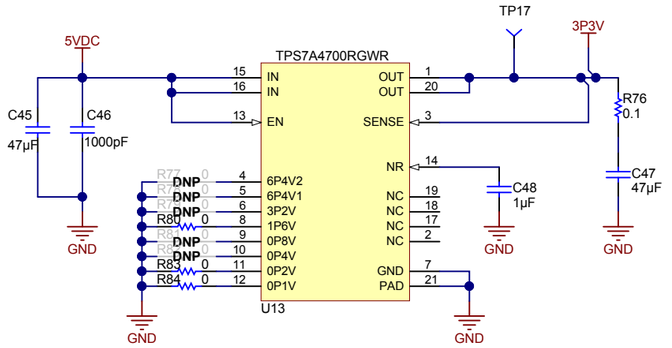
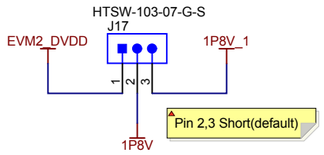
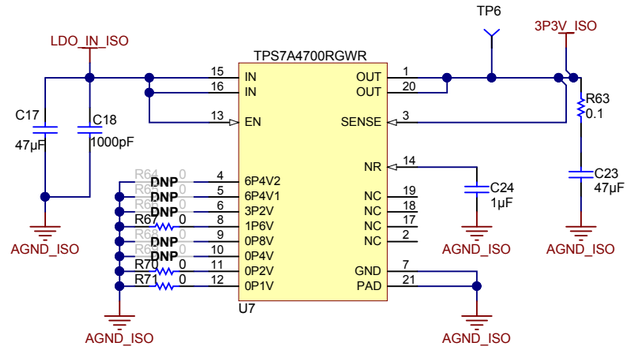
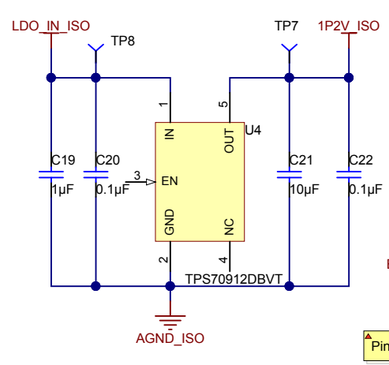
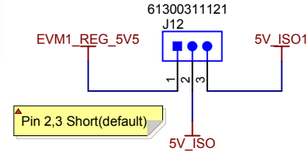
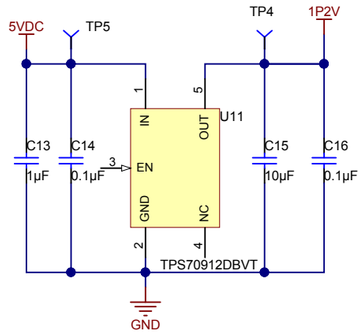


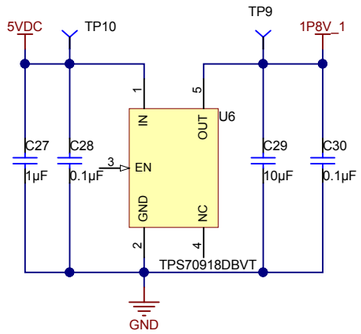



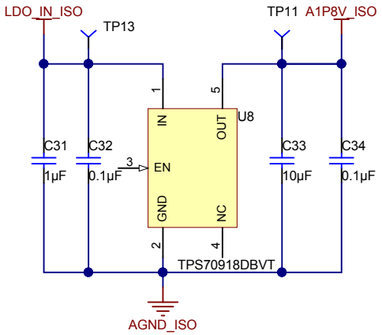



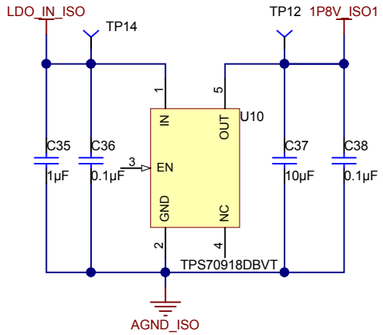



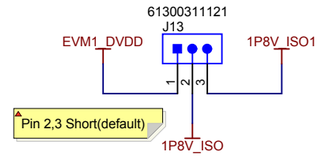



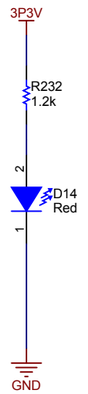



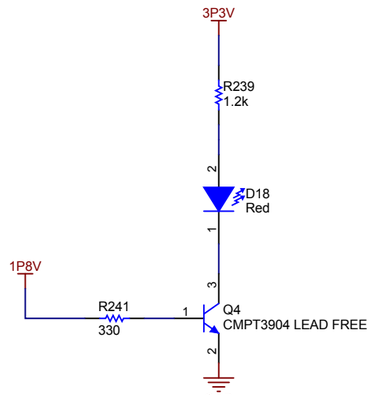



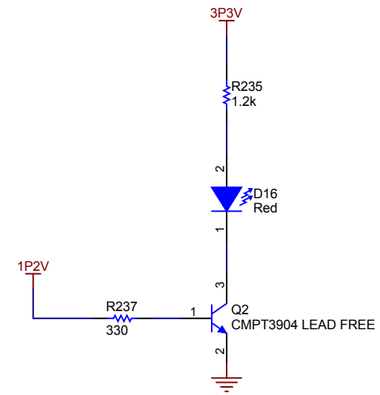



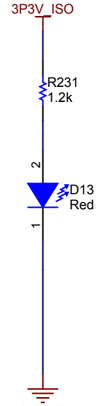



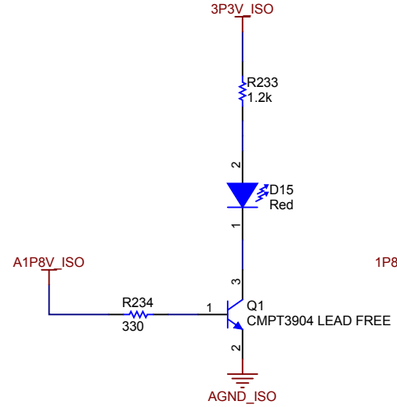



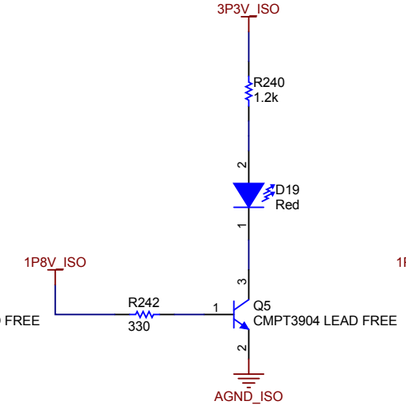



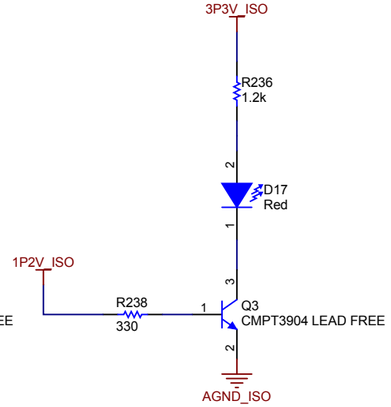



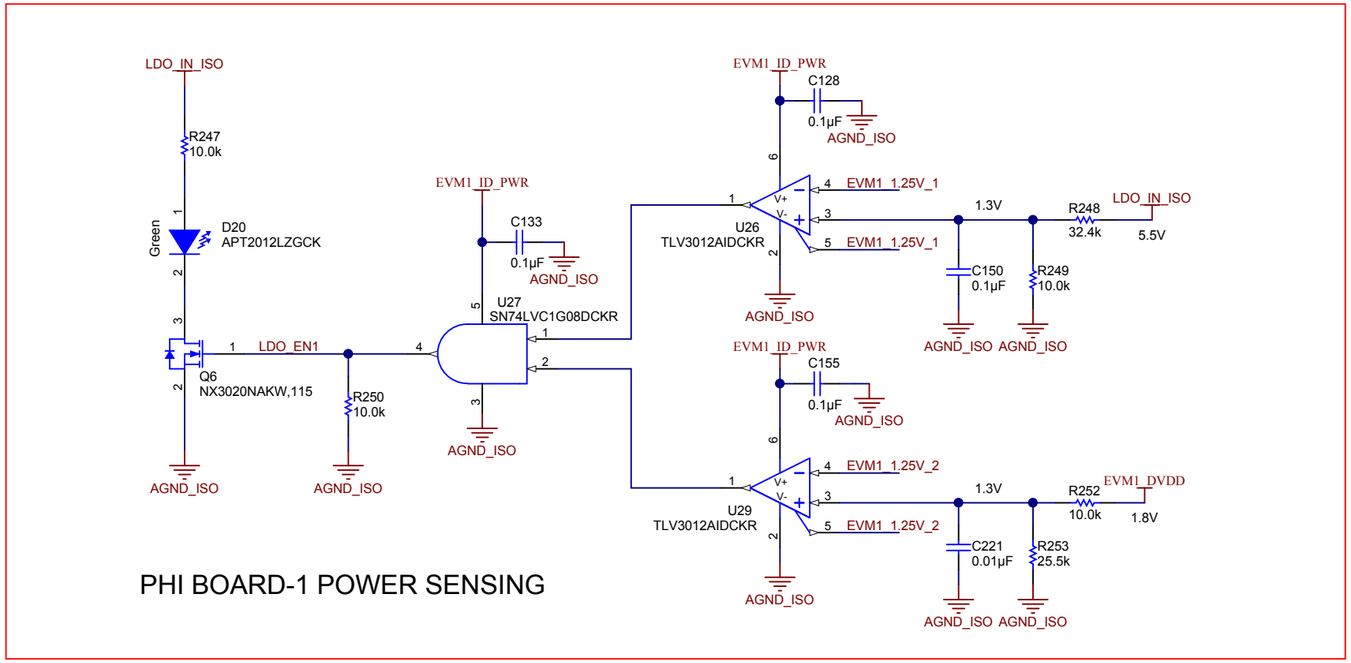

## NON-ISOLATED POWER RAIL

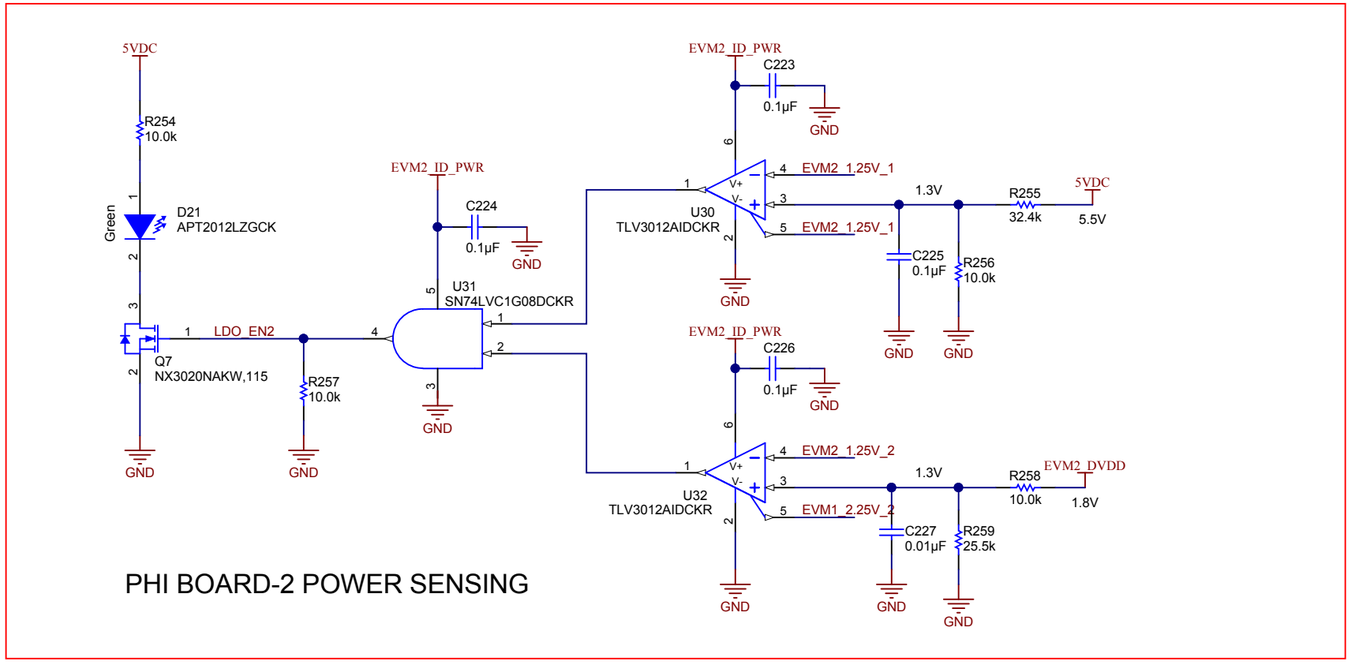
## ISOLATED POWER RAIL



| | | | |
|---|---|---|---|
| Orderable: N/A | | Designed for: Public Release | Mod. Date: 2/26/2016 |
| TID #: TID-00732 | | Project Title: Jitter minimizing techniques for digitally isolated high | |
| Number: TIDA-00732 | Rev: E1 | Sheet Title: LDO's Isolated & Non Isolated | |
| SVN Rev: Version control disabled | | Assembly Variant: ADS9110 w/REF5045 | Sheet: 7 of 10 |
| Drawn By: Anbu Mani | | File: TIDA-00732_Pwr.SchDoc | Size: B |
| Engineer: Anbu Mani | | Contact: http://www.ti.com/support | |

Texas Instruments
http://www.ti.com



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|---|---|---|
| Orderable: N/A | Designed for: Public Release | Mod. Date: 2/27/2016 |
| TID #: TID-00732 | Project Title: Jitter minimizing techniques for digitally isolated high | |
| Number: TIDA-00732 Rev: E1 | Sheet Title: Power Sense - PH1 & PH2 Interface | |
| SVN Rev: Version control disabled | Assembly Variant: ADS9110 w/REF5045 | Sheet: 8 of 10 |
| Drawn By: Anbu Mani | File: TIDA-00732_Pwr_Sense.SchDoc | Size: B |
| Engineer: Anbu Mani | Contact: http://www.ti.com/support | |

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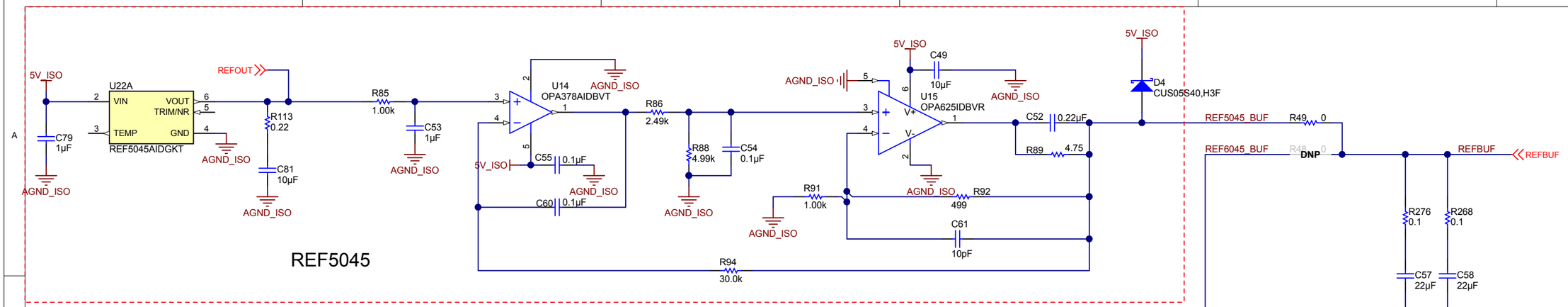


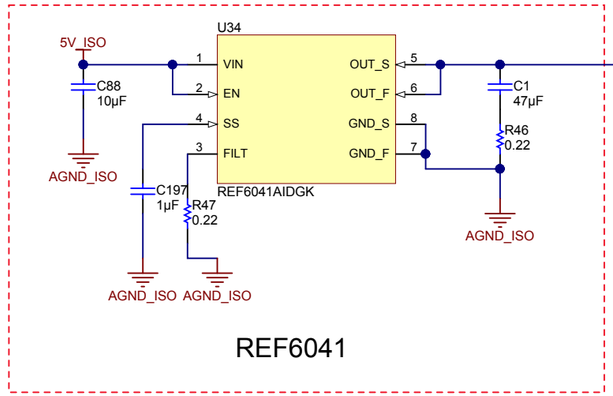


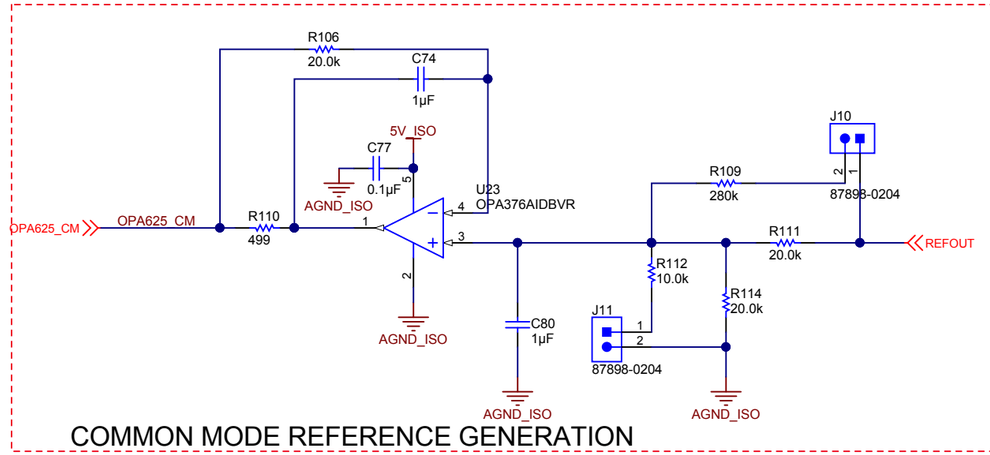


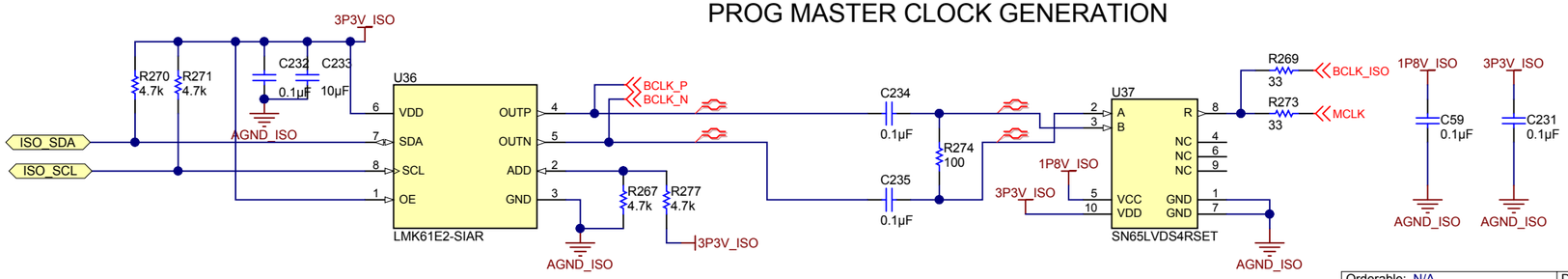




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|---|---|---|
| Orderable: N/A | Designed for: Public Release | Mod. Date: 2/27/2016 |
| TID #: TID-00732 | Project Title: Jitter minimizing techniques for digitally isolated high | |
| Number: TIDA-00732 Rev: E1 | Sheet Title: ADC Reference Selection | |
| SVN Rev: Version control disabled | Assembly Variant: ADS9110 w/REF5045 | Sheet: 9 of 10 |
| Drawn By: Anbu Mani | File: TIDA-00732_ADC_Ref_Select.SchDoc | Size: B |
| Engineer: Anbu Mani | Contact: http://www.ti.com/support | |

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| Label Table | |
|---|---|
| Variant | Label Text |
| | |
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| | |
| | |

DNP FID1 DNP FID2 DNP FID3 FID4 FID5 FID6 FID7 FID8

PCB Number: TIDA-00732
PCB Rev: E1

PCB
LOGO
Texas Instruments

## For Corner Mounting

H1 PMSSS 440 0025 PH
H2 PMSSS 440 0025 PH
H3 PMSSS 440 0025 PH
H4 PMSSS 440 0025 PH
H18 PMSSS 440 0025 PH
H17 PMSSS 440 0025 PH
H9 1902C
H10 1902C
H11 1902C
H12 1902C
H19 1902C
H20 1902C

## For PHI1 Mounting

H5 9774050360R
H6 9774050360R
H7 9774050360R
H8 9774050360R
H29 PMSSS 440 0025 PH
H22 PMSSS 440 0025 PH
H23 PMSSS 440 0025 PH
H24 PMSSS 440 0025 PH

LBL1
PCB Label
Size: 0.65" x 0.20 "

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

## For Beagle Bone Block Mounting

H21 PMSSS 440 0025 PH
H30 1902C

## For PHI2 Mounting

EVM2 mounting

H13 9774050360R
H14 9774050360R
H15 9774050360R
H16 9774050360R
H25 PMSSS 440 0025 PH
H26 PMSSS 440 0025 PH
H27 PMSSS 440 0025 PH
H28 PMSSS 440 0025 PH



| | | | |
|---|---|---|---|
| Orderable: N/A | | Designed for: Public Release | Mod. Date: 2/27/2016 |
| TID #: TID-00732 | | Project Title: Jitter minimizing techniques for digitally isolated high | |
| Number: TIDA-00732 | Rev: E1 | Sheet Title: Fastners | |
| SVN Rev: Version control disabled | | Assembly Variant: ADS9110 w/REF5045 | Sheet: 10 of 10 |
| Drawn By: Anbu Mani | | File: TIDA-00732_TID_Hardware.SchDoc | Size: B |
| Engineer: Anbu Mani | | Contact: http://www.ti.com/support | |

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