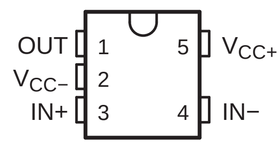
10-MHz LOW-NOISE LOW-VOLTAGE LOW-POWER OPERATIONAL AMPLIFIERS

Check for Samples: LMV721, LMV722

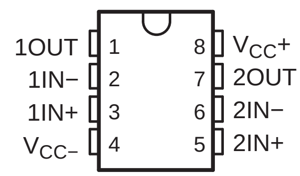
FEATURES

- **Power-Supply Voltage Range: 2.2 V to 5.5 V**
- **Low Supply Current: 930 μA/Amplifier at 2.2 V**
- **High Unity-Gain Bandwidth: 10 MHz**
- **Rail-to-Rail Output Swing**
  - **600-Ω Load: 120 mV From Either Rail at 2.2 V**
  - **2-kΩ Load: 50 mV From Either Rail at 2.2 V**
- **Input Common-Mode Voltage Range Includes Ground**
- **Input Voltage Noise: 9 nV/$\sqrt{Hz}$ at f = 1 kHz**

LMV721...DBV or DCK PACKAGE
(TOP VIEW)



LMV722...D, DGK, OR DRG PACKAGE
(TOP VIEW)



APPLICATIONS

- **Cellular and Cordless Phones**
- **Active Filter and Buffers**
- **Laptops and PDAs**
- **Battery Powered Electronics**

DESCRIPTION/ORDERING INFORMATION

The LMV721 (single) and LMV722 (dual) are low-noise low-voltage low-power operational amplifiers that can be designed into a wide range of applications. The LMV721 and LMV722 have a unity-gain bandwidth of 10 MHz, a slew rate of 5 V/μs, and a quiescent current of 930 μA/amplifier at 2.2 V.

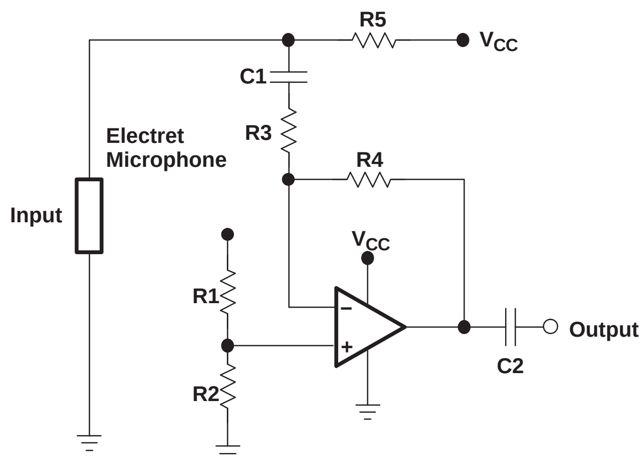
The LMV721 and LMV722 are designed to provide optimal performance in low-voltage and low-noise systems. They provide rail-to-rail output swing into heavy loads. The input common-mode voltage range includes ground, and the maximum input offset voltage are 3.5 mV (over recommended temperature range) for the devices. Their capacitive load capability is also good at low supply voltages. The operating range is from 2.2 V to 5.5 V.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)			ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
–40°C to 105°C	Single	SC-70 – DCK	Reel of 3000	LMV721IDCKR	RK_
			Reel of 250	LMV721IDCKT	
		SOT-23 – DBV	Reel of 3000	LMV721IDBVR	RBF_
	Dual	SOIC – D	Reel of 2500	LMV722IDR	MV722I
			Tube of 75	LMV722ID	
		VSSOP – DGK	Reel of 2500	LMV722IDGKR	R6_
		QFN – DRG	Reel of 2500	LMV722IDRGR	ZYY

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) DBV/DCK/DGK: The actual top-side marking has one additional character that designates the wafer fab/assembly site.

Typical Application



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC+} – V_{CC–}$	Supply voltage(2)			6	V
V_{ID}	Differential input voltage(3)			±Supply voltage	V
θ_{JA}	Package thermal impedance(4)	D package(5)		97	°C/W
		DBV package(5)		206	
		DCK package(5)		252	
		DGK package(5)		172	
		DRG package(6)		50.7	
T_J	Operating virtual-junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.
(3) Differential voltages are at IN+ with respect to IN−.
(4) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(5) The package thermal impedance is calculated in accordance with JESD 51-7.
(6) The package thermal impedance is calculated in accordance with JESD 51-5.

Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{CC+} – V_{CC–}$	Supply voltage	2.2	5.5	V
T_J	Operating virtual-junction temperature	–40	105	°C

ESD Protection

	TYP	UNIT
Human-Body Model	2000	V
Machine Model	100	V

Electrical Characteristics

V_{CC+} = 2.2 V, V_{CC-} = GND, V_{ICR} = V_{CC+}/2, V_O = V_{CC+}/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_J	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		25°C		0.02	3	mV
			–40°C to 105°C			3.5	
TCV_{IO}	Input offset voltage average drift		25°C		0.6		μV/°C
I_{IB}	Input bias current		25°C		260		nA
I_{IO}	Input offset current		25°C		25		nA
CMMR	Common-mode rejection ratio	V_{ICR} = 0 V to 1.3 V	25°C	70	88		dB
			–40°C to 105°C	64			
PSRR	Power-supply rejection ratio	V_{CC+} = 2.2 V to 5 V, V_O = 0, V_{ICR} = 0	25°C	80	90		dB
			–40°C to 105°C	70			
V_{ICR}	Input common-mode voltage	CMRR ≥ 50 dB	25°C		–0.3		V
					1.3		
A_{VD}	Large-signal voltage gain	R_L = 600 Ω, V_O = 0.75 V to 2 V	25°C	75	81		dB
			–40°C to 105°C	70			
		R_L = 2 kΩ, V_O = 0.5 V to 2.1 V	25°C	75	84		
			–40°C to 105°C	70			
V_O	Output swing	R_L = 600 Ω to V_{CC+}/2	25°C	2.090	2.125		V
			–40°C to 105°C	2.065			
			25°C		0.071	0.120	
			–40°C to 105°C			0.145	
		R_L = 2 kΩ to V_{CC+}/2	25°C	2.150	2.177		
			–40°C to 105°C	2.125			
			25°C		0.056	0.080	
			–40°C to 105°C			0.105	
I_O	Output current	Sourcing, V_O = 0 V, $V_{IN(diff)}$ = ±0.5 V	25°C	10	14.9		mA
			–40°C to 105°C	5			
		Sinking, V_O = 2.2 V, $V_{IN(diff)}$ = ±0.5 V	25°C	10	17.6		
			–40°C to 105°C	5			
I_{CC}	Supply current	LMV721	25°C		0.93	1.3	mA
			–40°C to 105°C			1.5	
		LMV722	25°C		1.81	2.4	
			–40°C to 105°C			2.6	
SR	Slew rate(1)		25°C		4.9		V/μs
GBW	Gain bandwidth product		25°C		10		MHz
Φ_m	Phase margin		25°C		67.4		°
G_m	Gain margin		25°C		–9.8		dB
V_n	Input-referred voltage noise	f = 1 kHz	25°C		9		nV/√Hz
I_n	Input-referred current noise	f = 1 kHz	25°C		0.3		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, AV = 1, R_L = 600 Ω, V_O = 500 mV_{pp}	25°C		0.004		%

(1) Connected as voltage follower with 1-V step input. Number specified is the slower of the positive and negative slew rate.

Electrical Characteristics

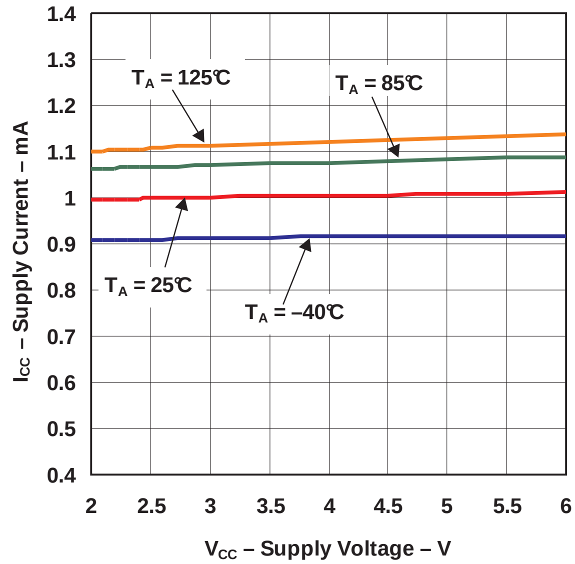
V_{CC+} = 5 V, V_{CC-} = GND, V_{ICR} = V_{CC+}/2, V_O = V_{CC+}/2, and R_L > 1 MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_J	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		25°C		–0.08	3	mV
			–40°C to 105°C			3.5	
TCV_{IO}	Input offset voltage average drift		25°C		0.6		μV/°C
I_{IB}	Input bias current		25°C		260		nA
I_{IO}	Input offset current		25°C		25		nA
CMMR	Common-mode rejection ratio	V_{ICR} = 0 V to 4.1 V	25°C	80	89		dB
			–40°C to 105°C	75			
PSRR	Power-supply rejection ratio	V_{CC+} = 2.2 V to 5 V, V_O = 0, V_{ICR} = 0	25°C	70	90		dB
			–40°C to 105°C	64			
V_{ICR}	Input common-mode voltage	CMRR ≥ 50 dB	25°C		–0.3		V
					4.1		
A_{VD}	Large-signal voltage gain	R_L = 600 Ω, V_O = 0.75 V to 4.8 V	25°C	80	87		dB
			–40°C to 105°C	70			
		R_L = 2 kΩ, V_O = 0.7 V to 4.9 V	25°C	80	94		
			–40°C to 105°C	70			
V_O	Output swing	R_L = 600 Ω to V_{CC+}/2	25°C	4.84	4.882		V
			–40°C to 105°C	4.815			
			25°C		0.134	0.19	
			–40°C to 105°C			0.215	
		R_L = 2 kΩ to V_{CC+}/2	25°C	4.93	4.952		
			–40°C to 105°C	4.905			
			25°C		0.076	0.11	
			–40°C to 105°C			0.135	
I_O	Output current	Sourcing, V_O = 0 V, $V_{IN(diff)}$ = ±0.5 V	25°C	20	52.6		mA
			–40°C to 105°C	12			
		Sinking, V_O = 2.2 V, $V_{IN(diff)}$ = ±0.5 V	25°C	15	23.7		
			–40°C to 105°C	8.5			
I_{CC}	Supply current	LMV721	25°C		1.03	1.4	mA
			–40°C to 105°C			1.7	
		LMV722	25°C		2.01	2.4	
			–40°C to 105°C			2.8	
SR	Slew rate(1)		25°C		5.25		V/μs
GBW	Gain bandwidth product		25°C		10		MHz
Φ_m	Phase margin		25°C		72		°
G_m	Gain margin		25°C		–11		dB
V_n	Input-referred voltage noise	f = 1 kHz	25°C		8.5		nV/√Hz
I_n	Input-referred current noise	f = 1 kHz	25°C		0.2		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, AV = 1, R_L = 600 Ω, V_O = 500 mV_{pp}	25°C		0.001		%

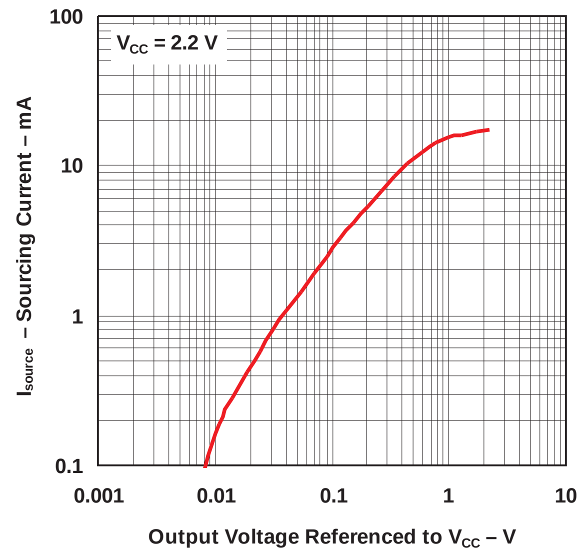
(1) Connected as voltage follower with 1-V step input. Number specified is the slower of the positive and negative slew rate.

TYPICAL CHARACTERISTICS

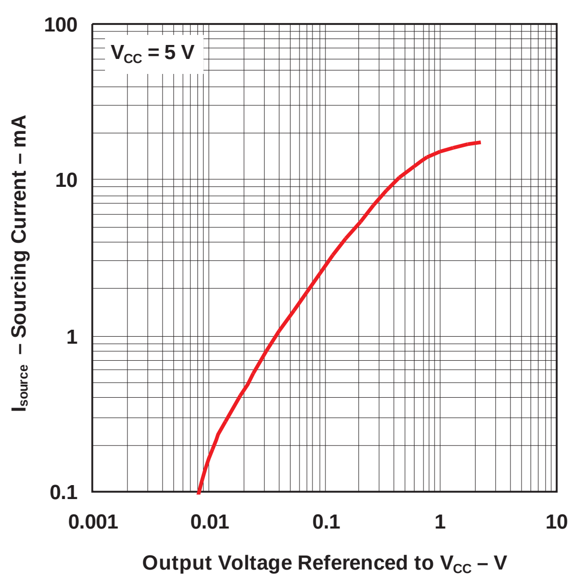
SUPPLY CURRENT
vs
SUPPLY VOLTAGE



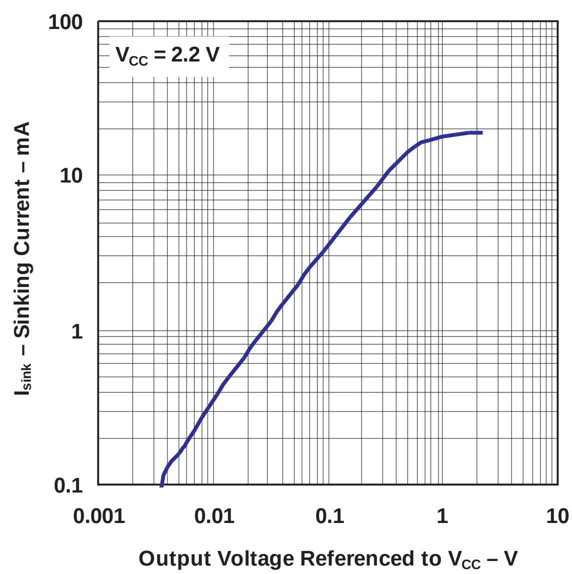
SOURCING CURRENT
vs
OUTPUT VOLTAGE



SOURCING CURRENT
vs
OUTPUT VOLTAGE

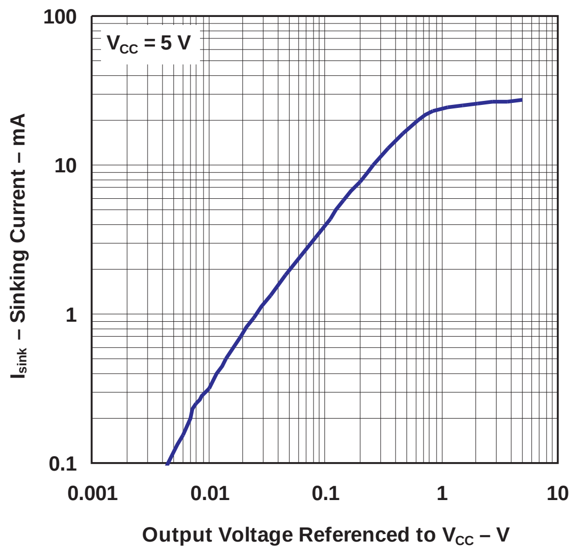


SINKING CURRENT
vs
OUTPUT VOLTAGE

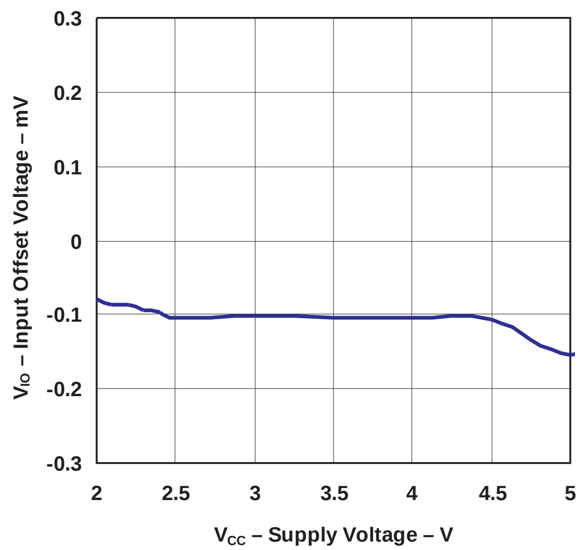


TYPICAL CHARACTERISTICS (continued)

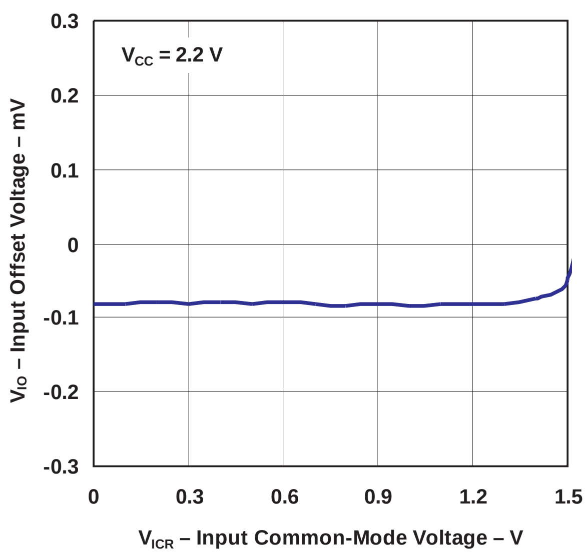
SINKING CURRENT vs OUTPUT VOLTAGE



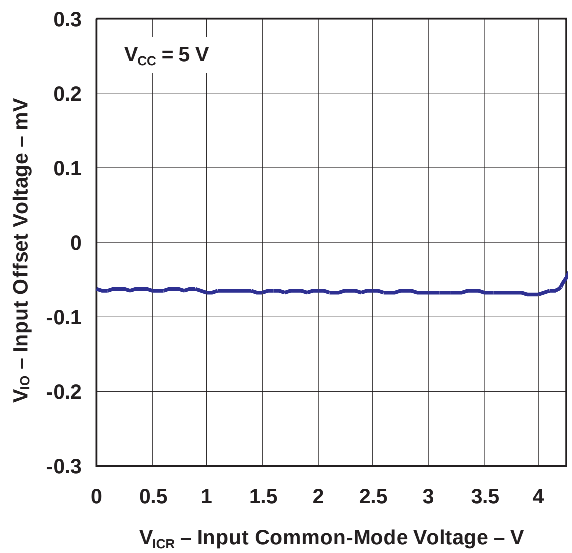
OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE



INPUT OFFSET VOLTAGE vs INPUT COMMON-MODE VOLTAGE

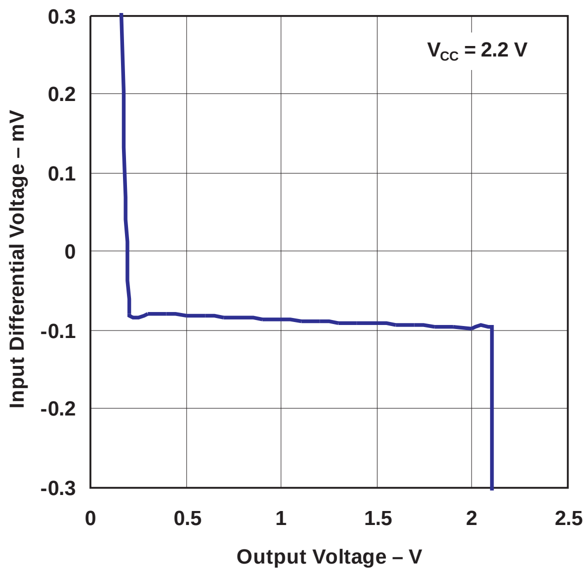


INPUT OFFSET VOLTAGE vs INPUT COMMON-MODE VOLTAGE

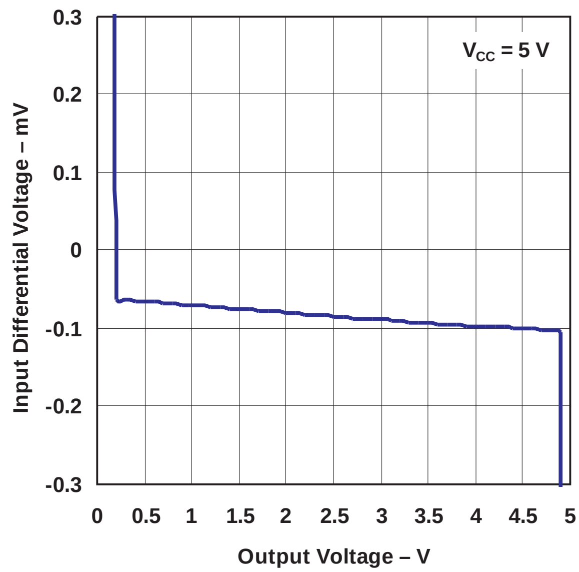


TYPICAL CHARACTERISTICS (continued)

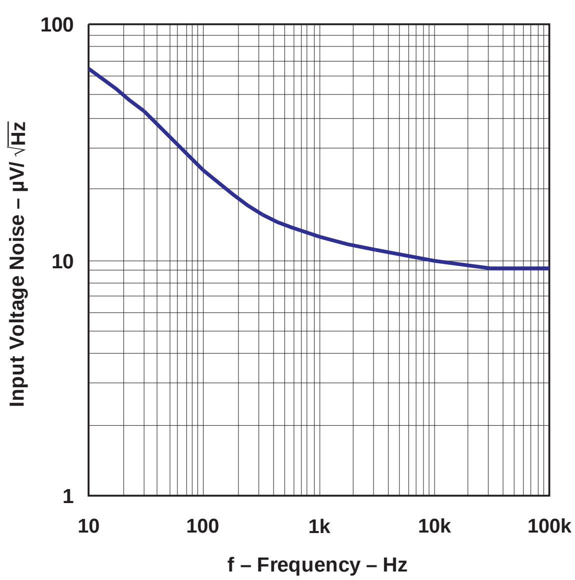
INPUT VOLTAGE vs OUTPUT VOLTAGE



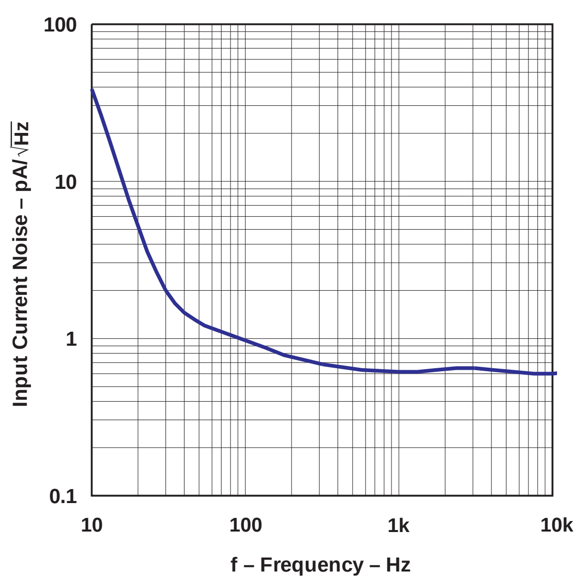
INPUT VOLTAGE vs OUTPUT VOLTAGE



INPUT VOLTAGE NOISE vs FREQUENCY

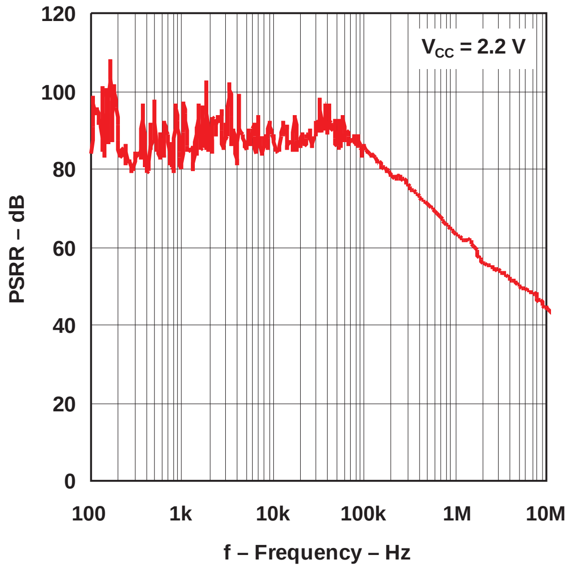


INPUT CURRENT NOISE vs FREQUENCY

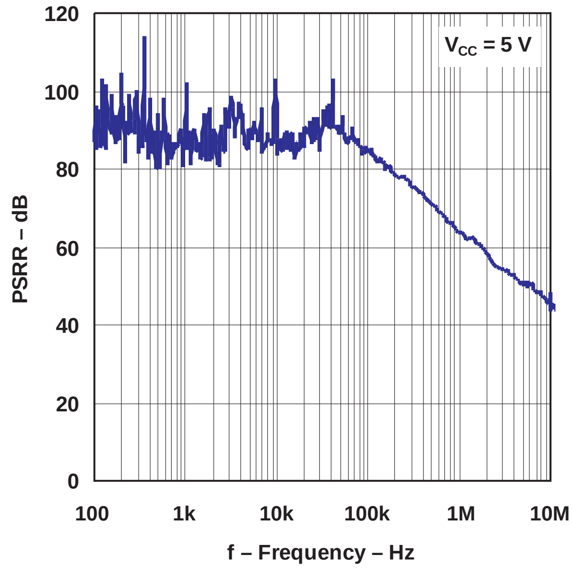


TYPICAL CHARACTERISTICS (continued)

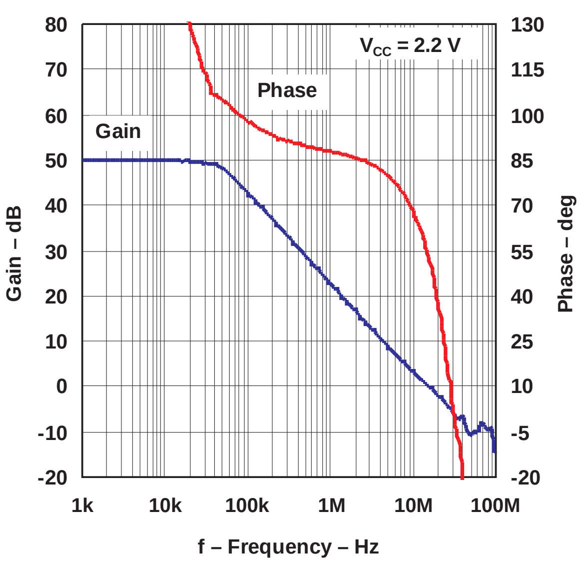
PSRR vs FREQUENCY



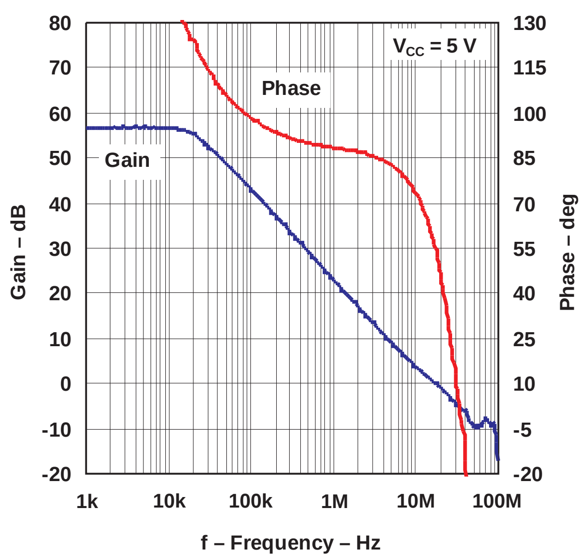
PSRR vs FREQUENCY



GAIN AND PHASE vs FREQUENCY

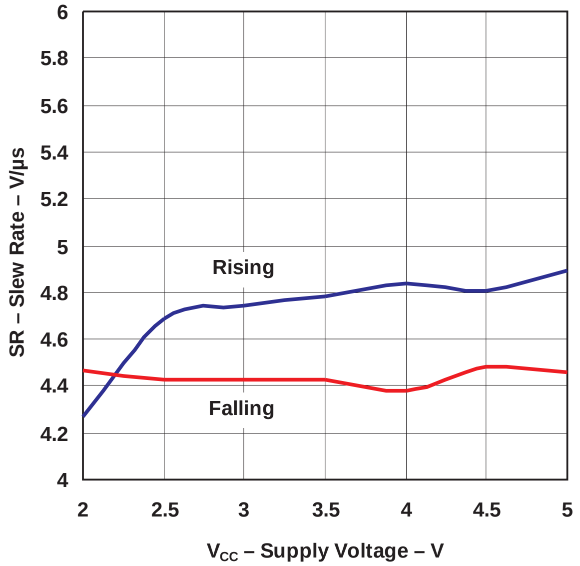


GAIN AND PHASE vs FREQUENCY

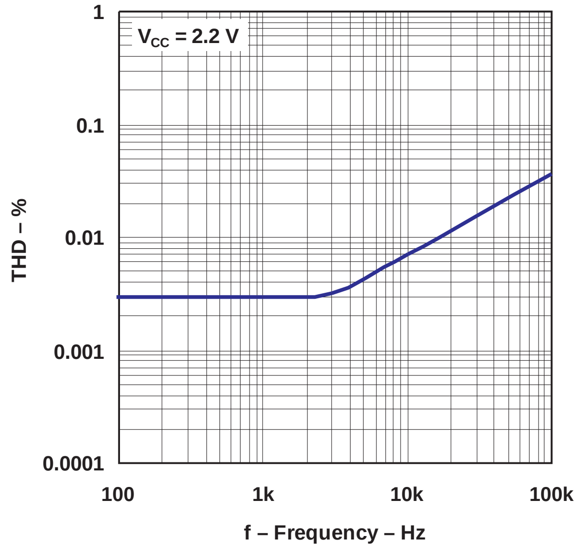


TYPICAL CHARACTERISTICS (continued)

SLEW RATE vs SUPPLY VOLTAGE

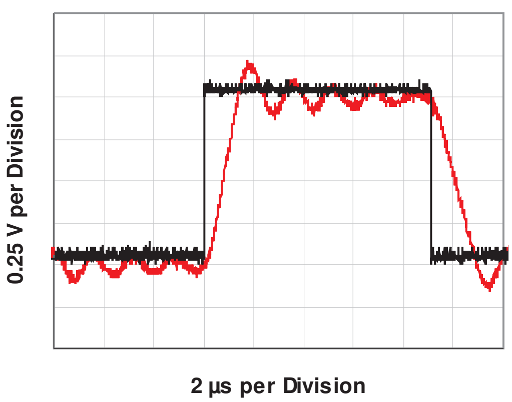


THD vs FREQUENCY



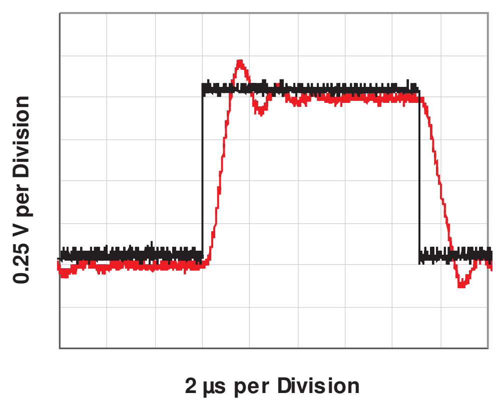
PULSE RESPONSE

V_{CC} = 5 V, R_L = 2 kΩ, C_L = 21.2 nF, R_o = 0 Ω



PULSE RESPONSE

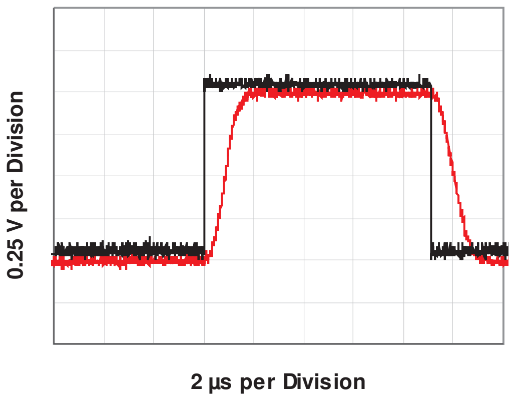
V_{CC} = 5 V, R_L = 2 kΩ, C_L = 21.2 nF, R_o = 2.1 Ω



TYPICAL CHARACTERISTICS (continued)

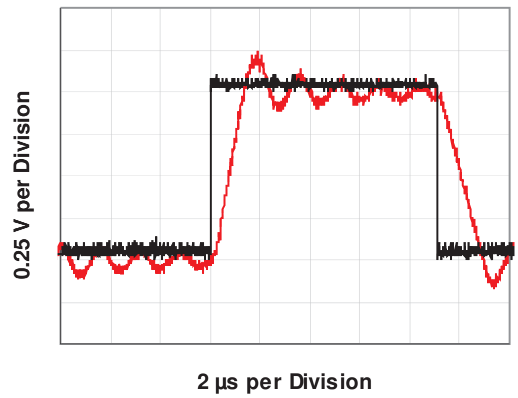
PULSE RESPONSE

V_{CC} = 5 V, R_L = 2 kΩ, C_L = 21.2 nF, R_o = 9.5 Ω



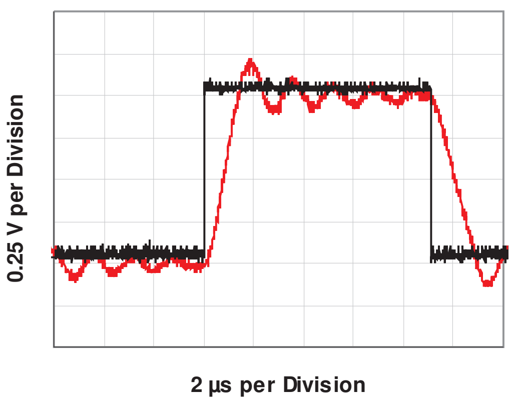
PULSE RESPONSE

V_{CC} = 5 V, R_L = 10 kΩ, C_L = 21.2 nF, R_o = 0 Ω



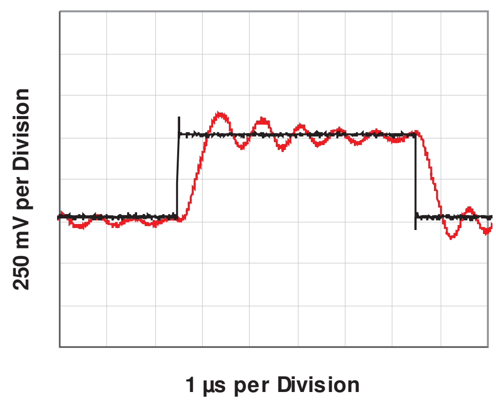
PULSE RESPONSE

V_{CC} = 5 V, R_L = 600 Ω, C_L = 21.2 nF, R_o = 0 Ω



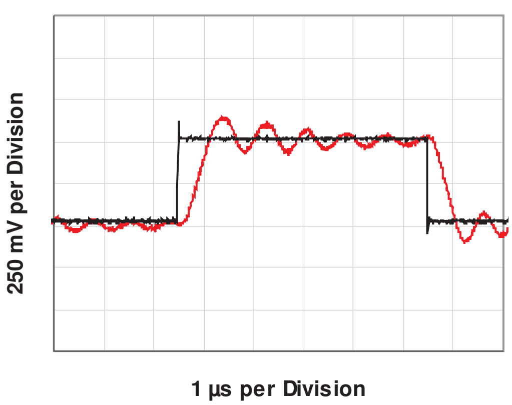
PULSE RESPONSE

V_{CC} = 2.2 V, R_L = 2 Ω, C_L = 2.12 nF, R_o = 0 Ω



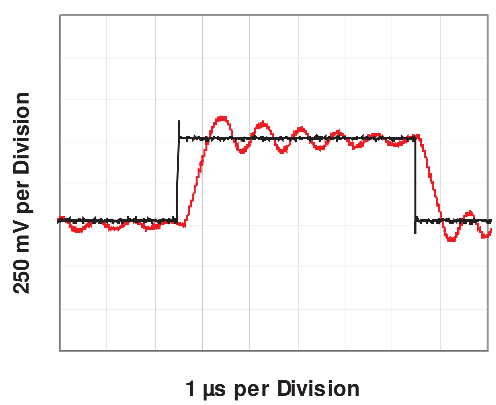
PULSE RESPONSE

V_{CC} = 2.2 V, R_L = 2 kΩ, C_L = 2.12 nF, R_o = 0 Ω



PULSE RESPONSE

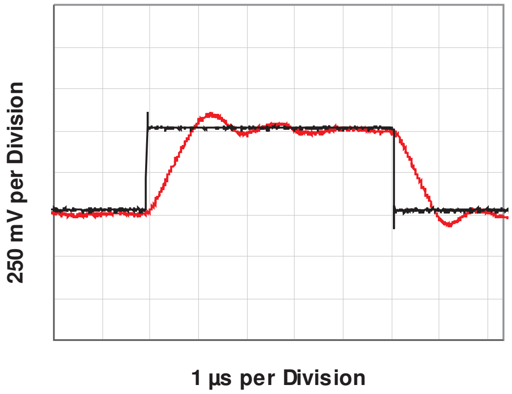
V_{CC} = 2.2 V, R_L = 10 kΩ, C_L = 2.12 nF, R_o = 0 Ω



TYPICAL CHARACTERISTICS (continued)

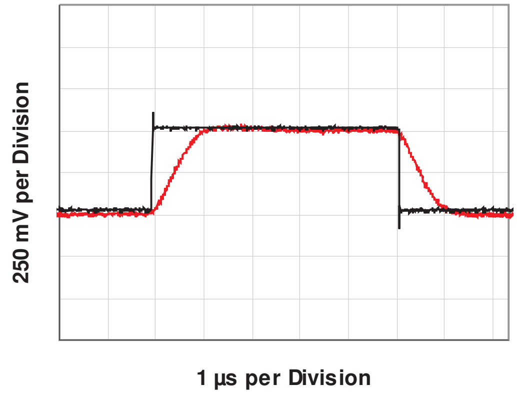
PULSE RESPONSE

V_{cc} = 2.2 V, R_L = 10 kΩ, C_L = 2.12 nF, R_o = 2.2 Ω



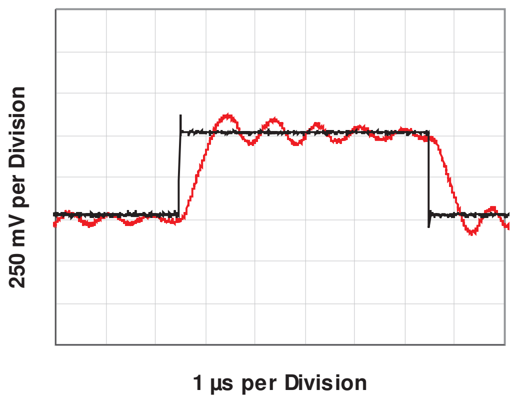
PULSE RESPONSE

V_{cc} = 2.2 V, R_L = 10 kΩ, C_L = 2.12 nF, R_o = 11.5 Ω



PULSE RESPONSE

V_{cc} = 2.2 V, R_L = 600 Ω, C_L = 1.89 nF, R_o = 0 Ω



REVISION HISTORY

Changes from Revision B (August 2010) to Revision C **Page**

- Changed all temperature parameters from max of 85°C to 105°C 1
- Changed supply voltage max value to 6 in Absolute Maximum Ratings table 2
- Changed supply voltage MAX value to 5.5 in Recommended Operating Conditions table 2
- Changed A_{VD}, V_O test conditons for R_L = 600 Ω: 0.75 V to 4.8 V 4
- Changed A_{VD}, V_O test conditons for R_L = 2 kΩ Ω: 0.75 V to 4.8 V 4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV721IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	(RBFA, RBFM)	Samples
LMV721IDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	(RKA, RKM)	Samples
LMV721IDCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	(RKA, RKM)	Samples
LMV722ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	MV722I	Samples
LMV722IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	R6E	Samples
LMV722IDGKRG4	LIFEBUY	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	R6E	
LMV722IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	MV722I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMV722 :

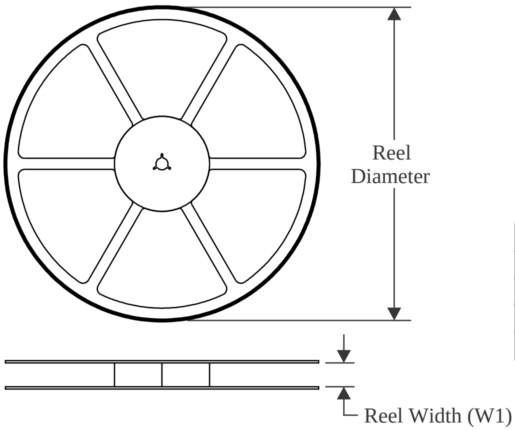
- Automotive : LMV722-Q1

NOTE: Qualified Version Definitions:

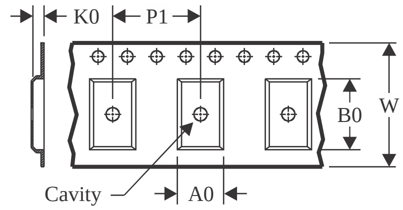
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

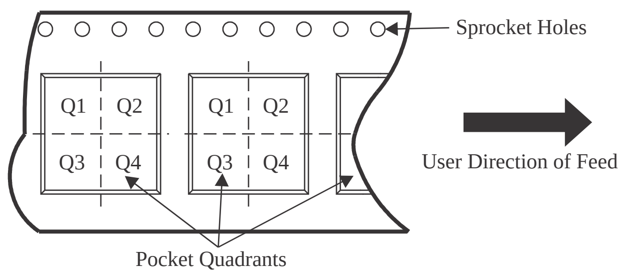


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

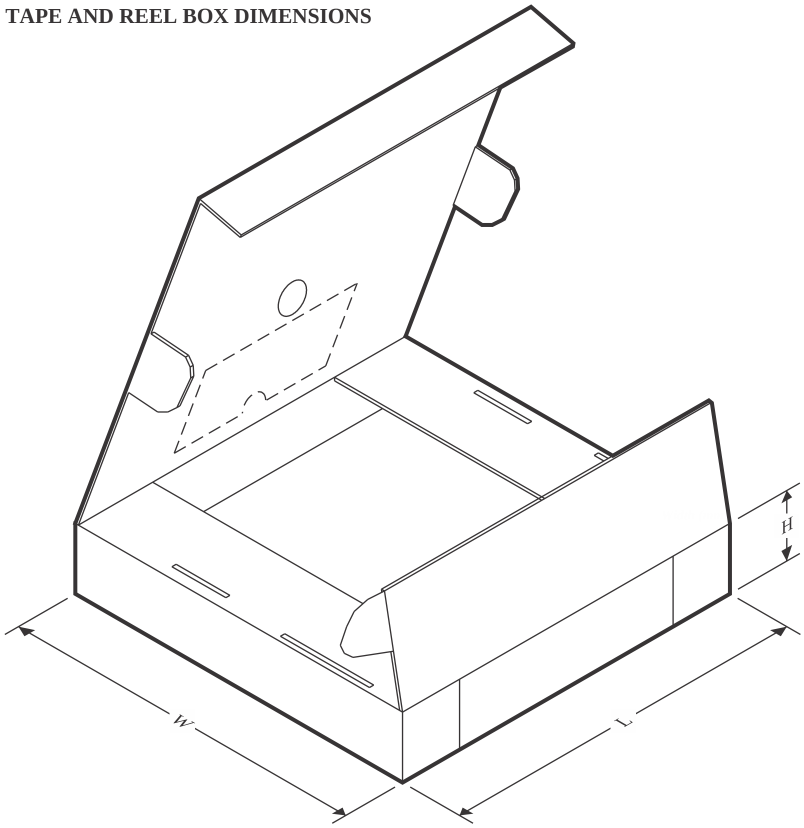
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV721IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
LMV721IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LMV721IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
LMV721IDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
LMV721IDCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
LMV722IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
LMV722IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

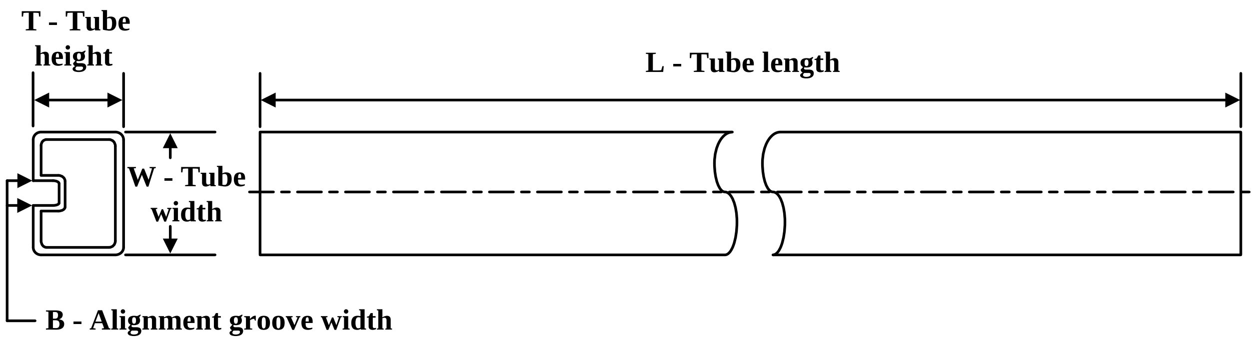
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

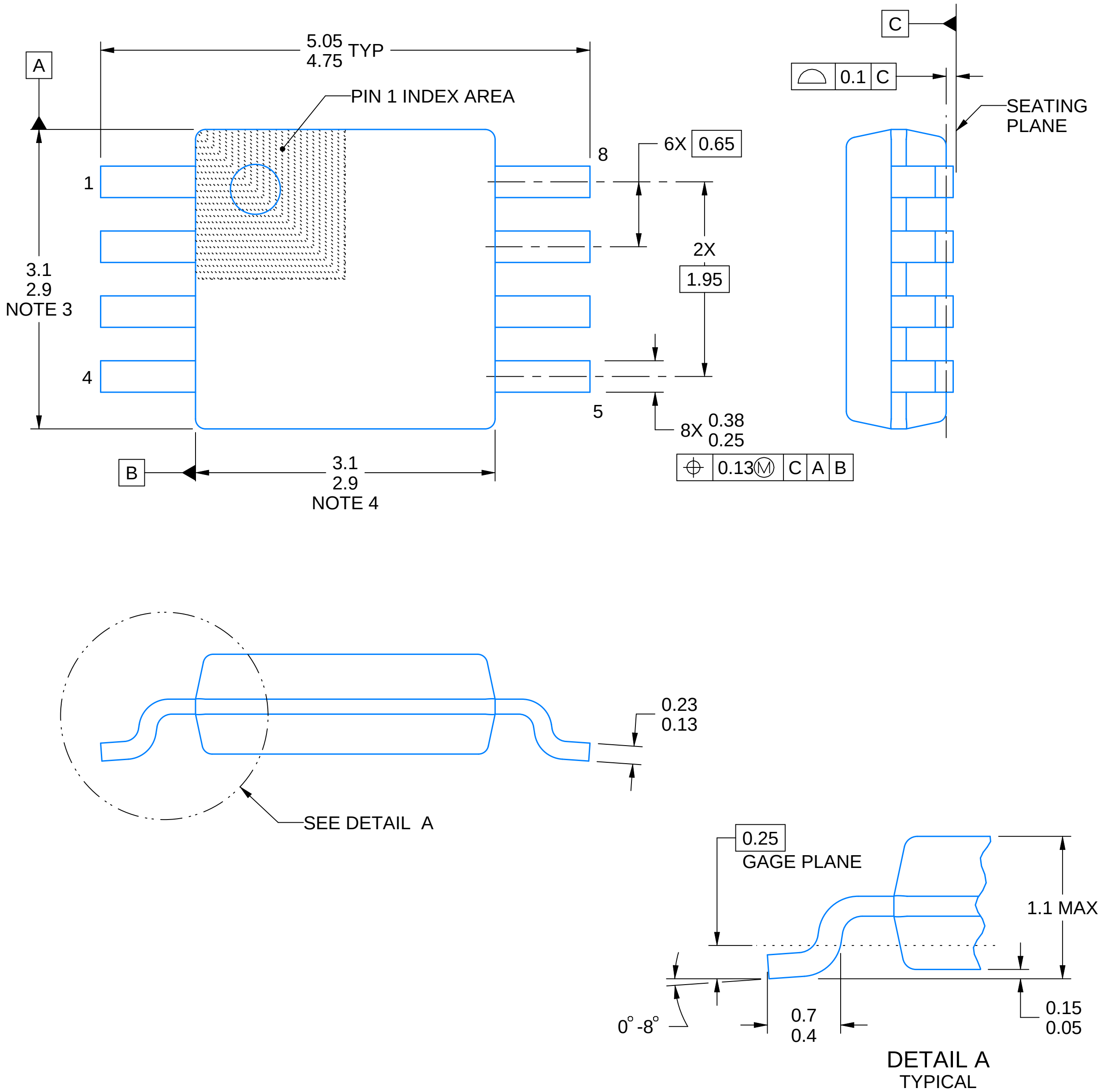
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV721IDBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
LMV721IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LMV721IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
LMV721IDCKT	SC70	DCK	5	250	180.0	180.0	18.0
LMV721IDCKT	SC70	DCK	5	250	202.0	201.0	28.0
LMV722IDGKR	VSSOP	DGK	8	2500	346.0	346.0	35.0
LMV722IDR	SOIC	D	8	2500	340.5	338.1	20.6

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMV722ID	D	SOIC	8	75	507	8	3940	4.32

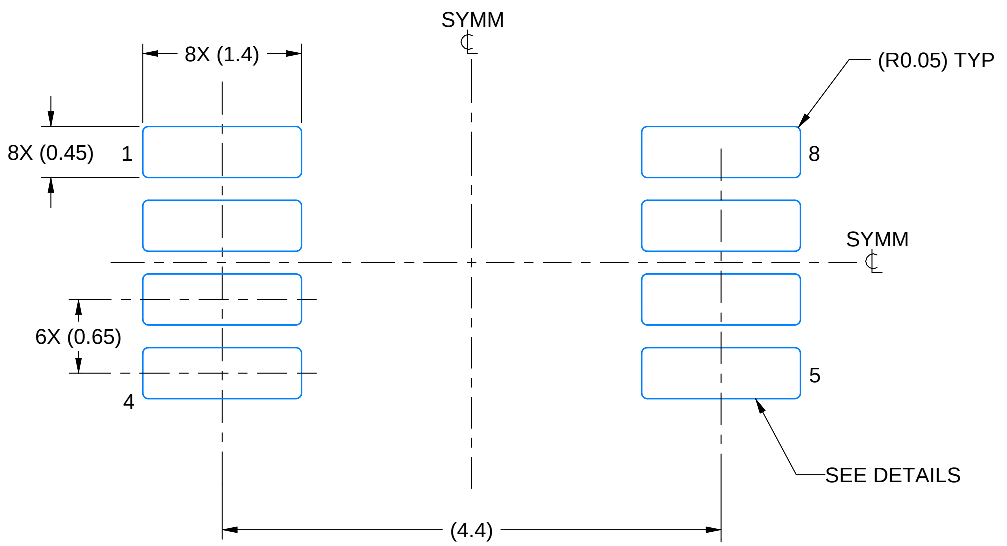


4214862/A 04/2023

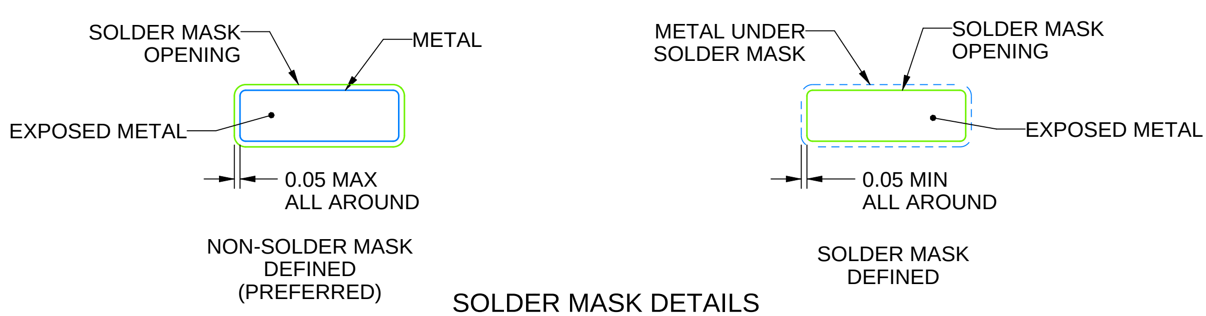
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

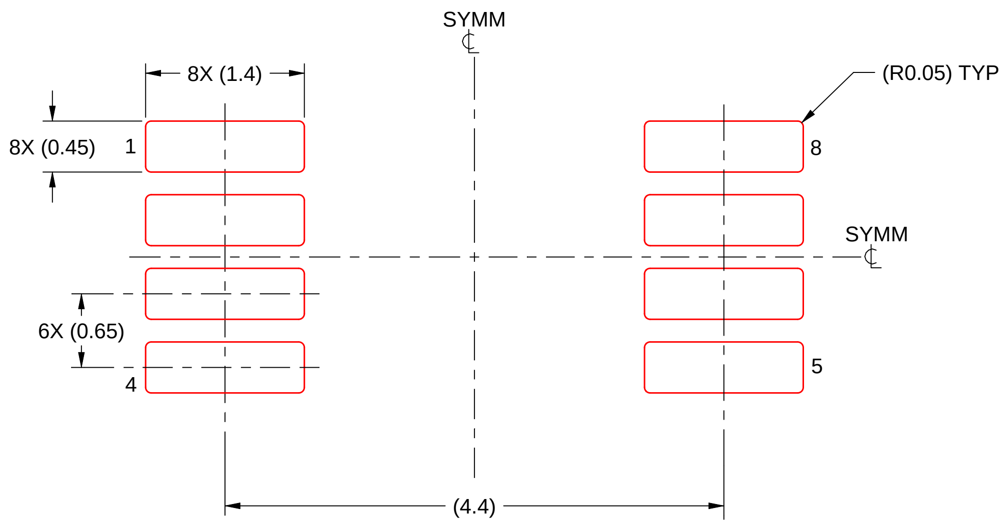


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

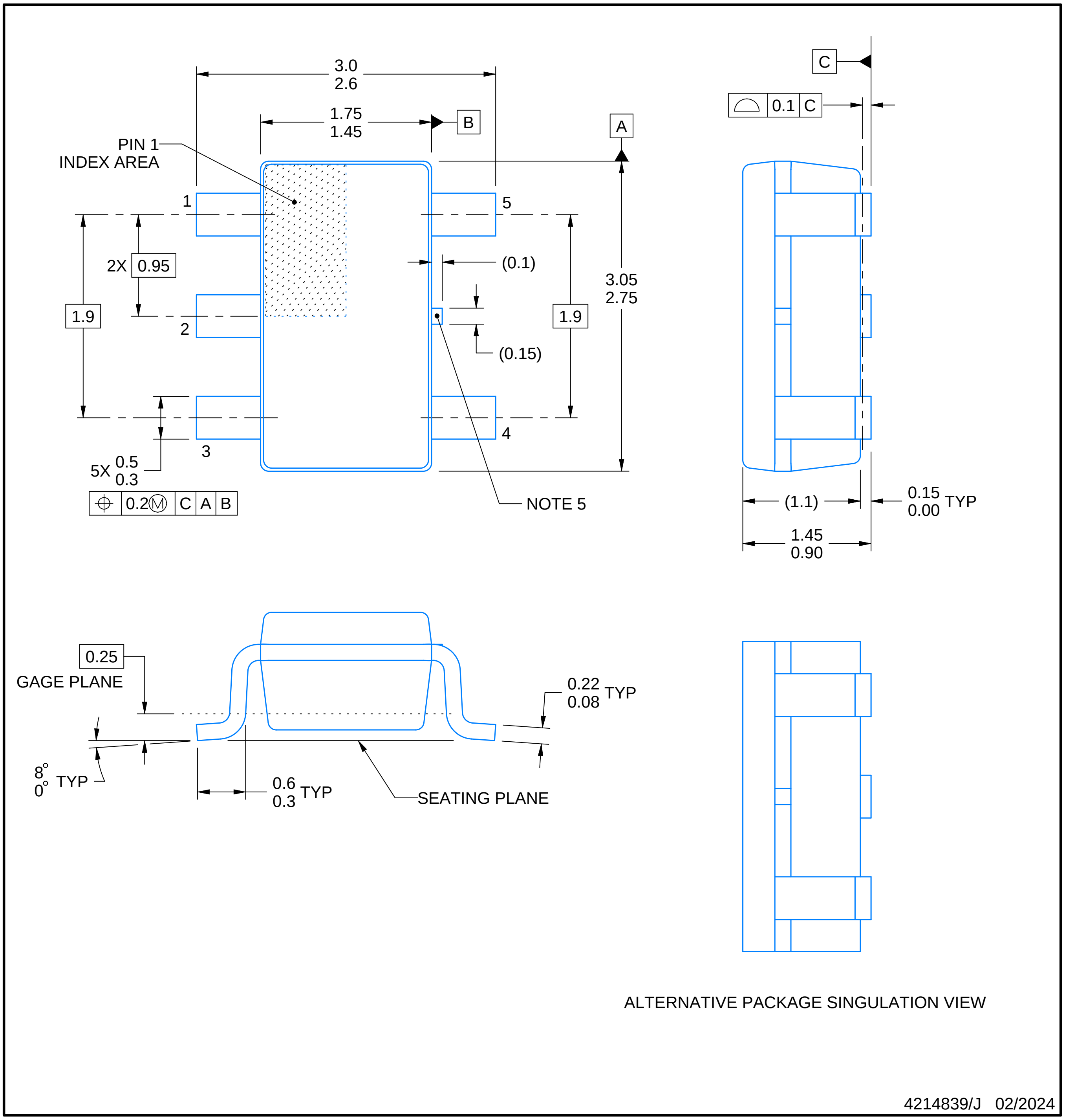


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

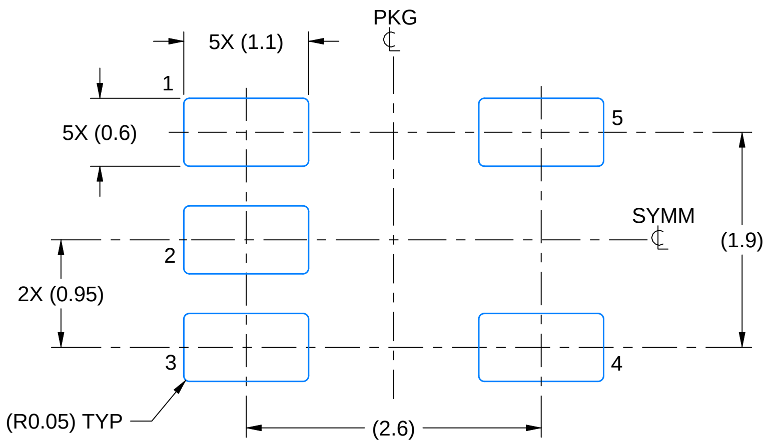
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

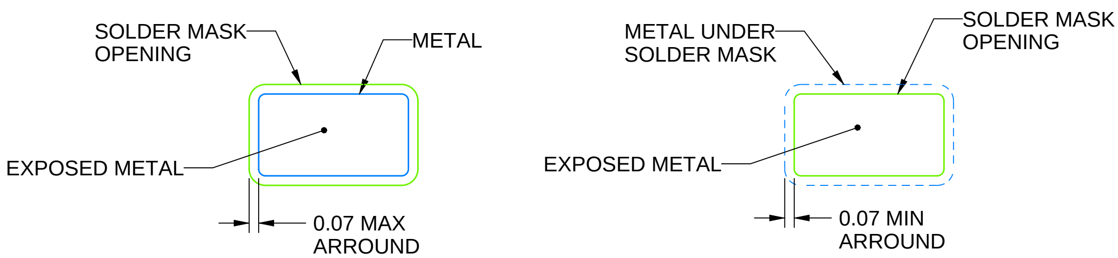


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED (PREFERRED)

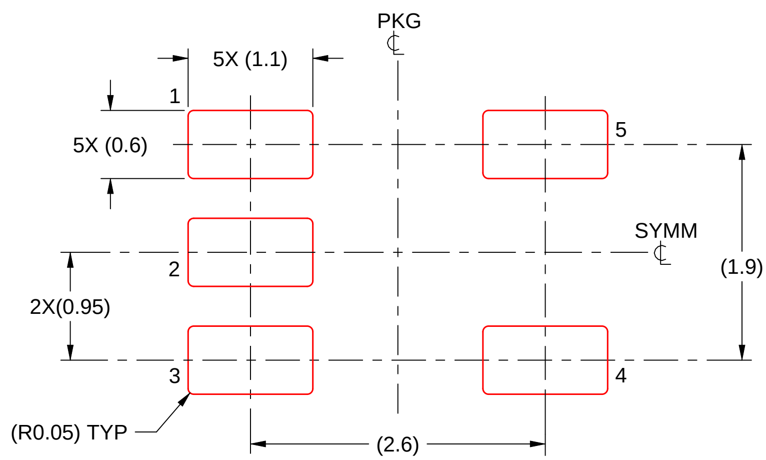
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

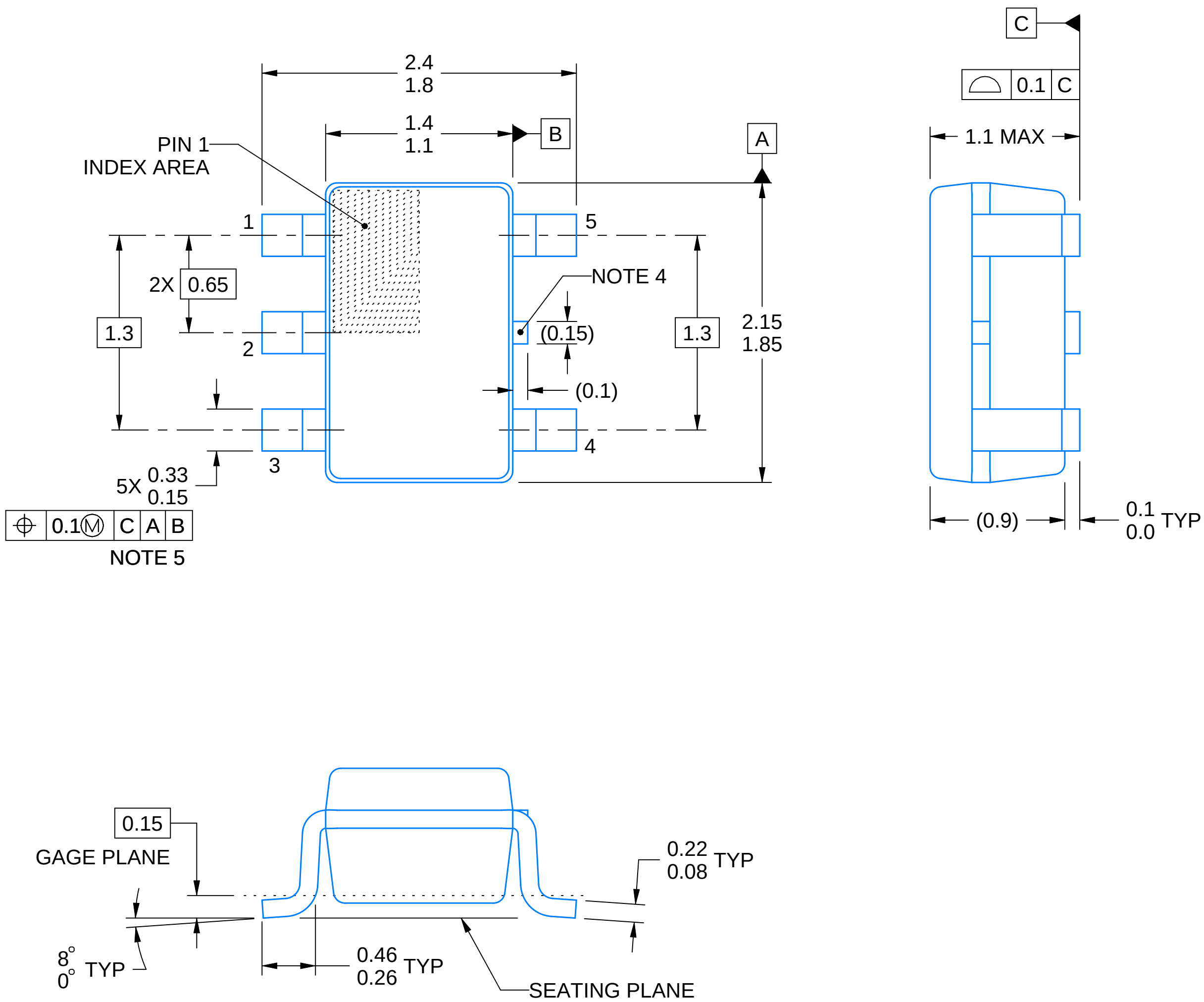


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

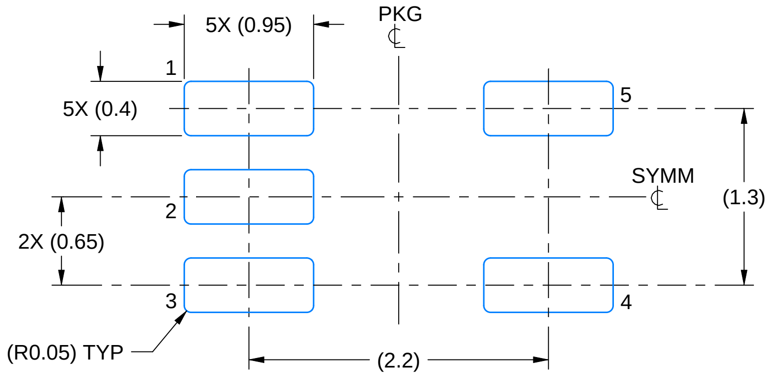
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



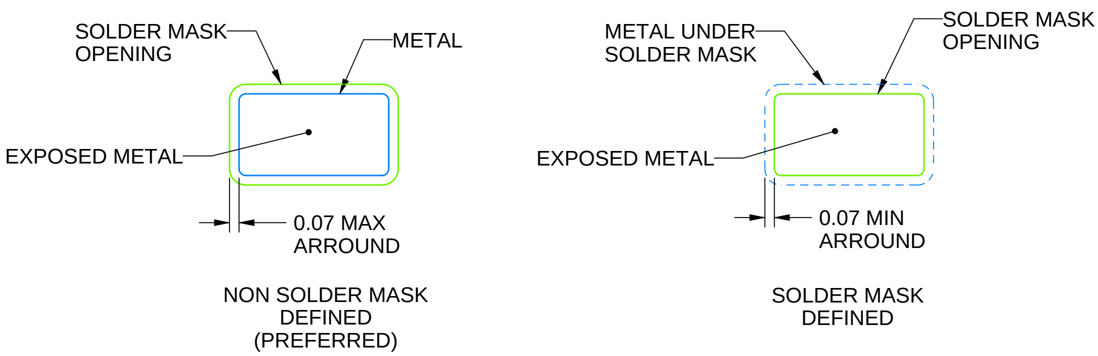
4214834/D 07/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

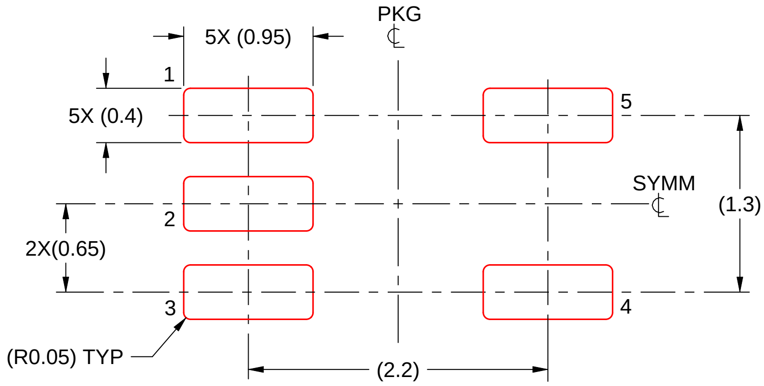


SOLDER MASK DETAILS

4214834/D 07/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

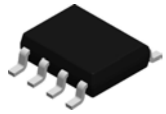


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/D 07/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

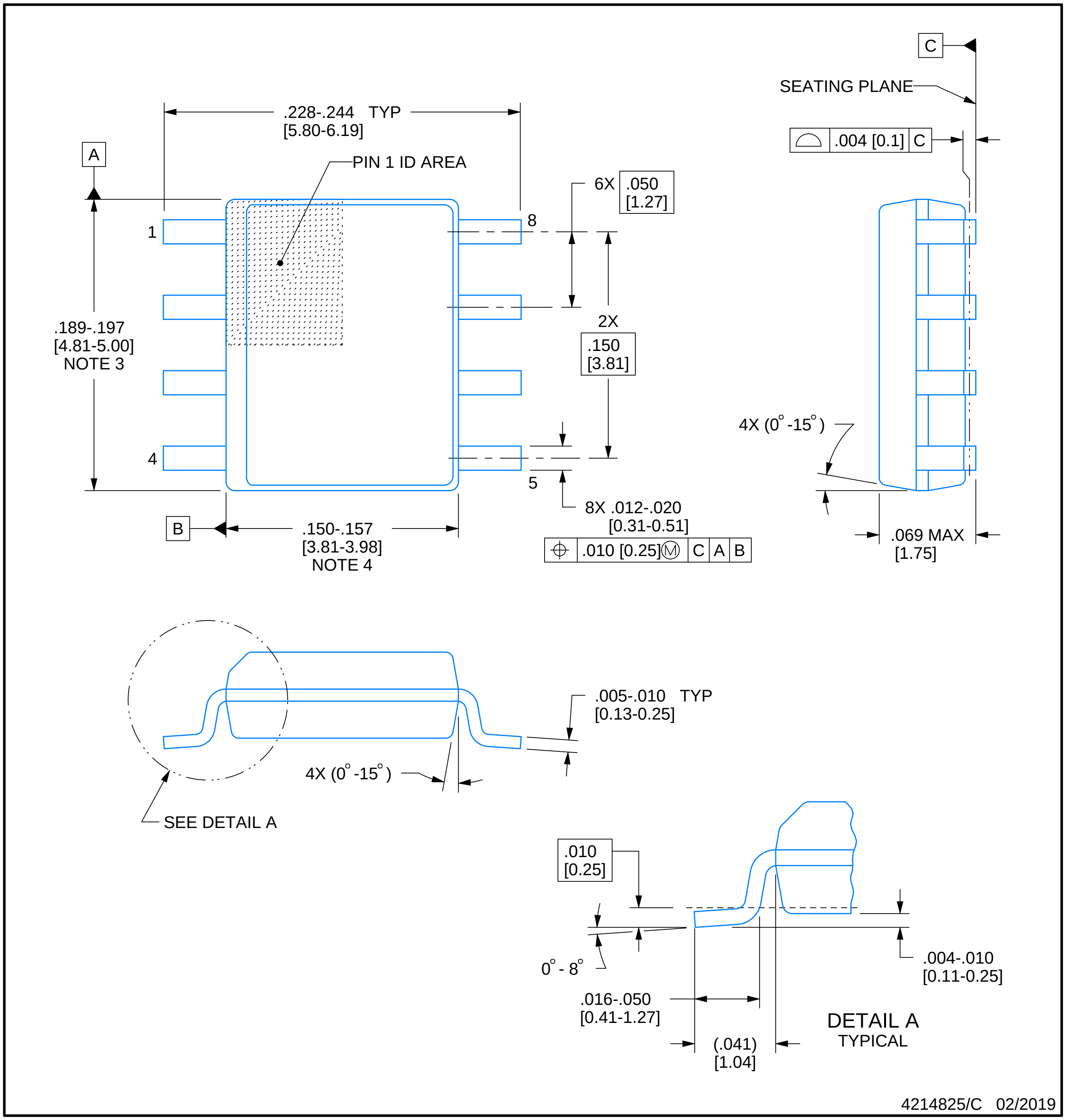


PACKAGE OUTLINE

D0008A

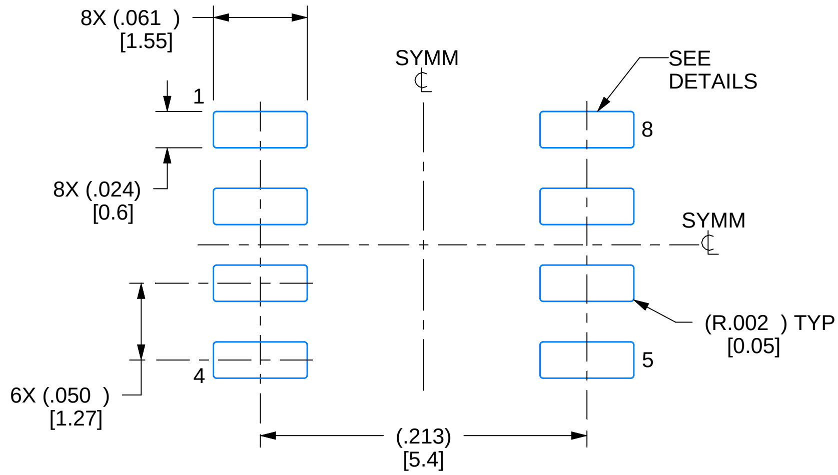
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

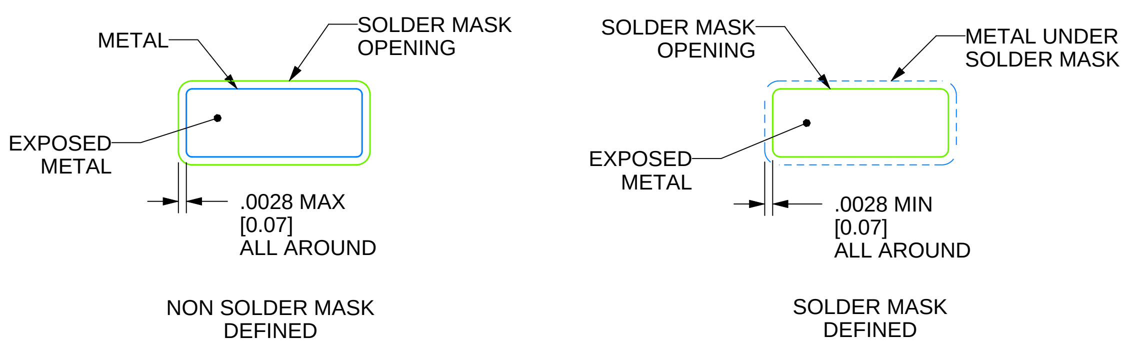


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

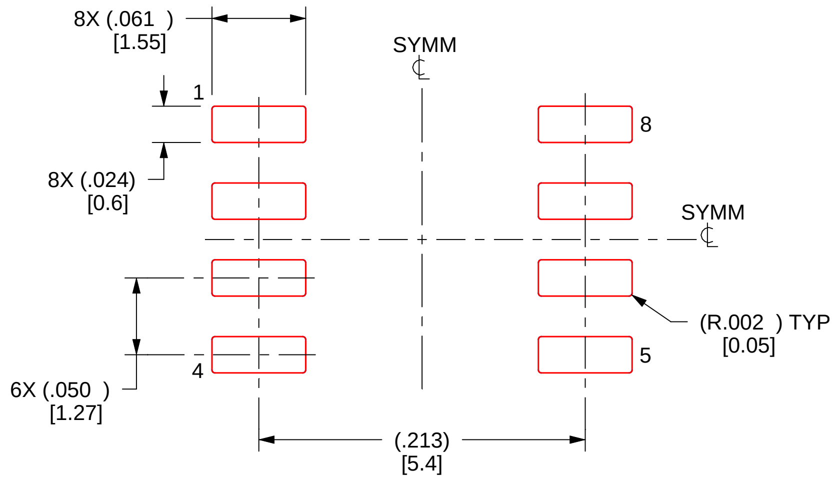


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265