Single-supply diff-in to diff-out AC amplifier circuit



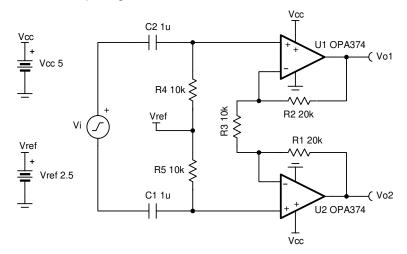
Design Goals

Diff. Input V _i		Diff. Output (V _{o1} – V _{o2})		Supply		
V _{iMin}	V _{iMax}	V _{oMin}	V _{oMax}	V _{cc}	V _{ee}	V _{ref}
-500mV	+500mV	-2.5V	+2.5V	+5	0V	+2.5V

Lower Cutoff Freq.	Upper Cutoff Freq.	
16Hz	> 1MHz	

Design Description

This circuit uses 2 op amps to build a discrete, single-supply diff-in diff-out amplifier. The circuit converts a differential signal to a differential output signal.



Design Notes

- 1. Ensure that R₁ and R₂ are well matched with high accuracy resistors to maintain high DC common-mode rejection performance.
- Increase R₄ and R₅ to match the necessary input impedance at the expense of thermal noise performance.
- 3. Bias for single-supply operation can also be created by a voltage divider from V_{cc} to ground.
- 4. V_{ref} sets the output voltage of the instrumentation amplifier bias at mid-supply to allow the output to swing to both supply rails.
- 5. Choose C_1 and C_2 to select the lower cutoff frequency.
- 6. Linear operation is contingent upon the input common-mode and the output swing ranges of the discrete op amps used. The linear output swing ranges are specified under the AoI test conditions in the op amps data sheets



Design Steps

1. The transfer function of the circuit is shown below.

$$\begin{split} &V_{oDiff} = V_i \times G + V_{ref} \\ &\text{where } V_i = \text{the differential input voltage} \\ &V_{ref} = \text{the reference voltage provided to the amplifier} \\ &G = 1 + 2 \times \left(\frac{R_1}{R_3}\right) \end{split}$$

2. Choose resistors $R_1 = R_2$ to maintain common-mode rejection performance.

Choose
$$R_1 = R_2 = 20 \text{ k}\Omega$$
 (Standard value)

3. Choose resistors R_4 and R_5 to meet the desired input impedance.

Choose
$$R_4 = R_5 = 10 \text{ k}\Omega$$
 (Standard value)

4. Calculate R₃ to set the differential gain.

$$\begin{split} \text{Gain} &= 1 + \left(\frac{2 \times R_1}{R_3}\right) = 5 \, \frac{V}{V} \\ R_1 &= R_2 = -20 \, \text{k} \, \Omega \\ G &= 1 + \frac{2 \times 20 \, \text{k}\Omega}{R_3} = 5 \, \frac{V}{V} \to 5 \, \frac{V}{V} - 1 = \frac{40 \, \text{k}\Omega}{R_3} = 4 \to R_3 = \frac{40 \, \text{k}\Omega}{4} = 10 \, \text{k}\Omega \quad \bigg(\text{Standard value} \bigg) \end{split}$$

5. Set the reference voltage V_{ref} at mid-supply.

$$V_{ref} = \frac{V_{cc}}{2} = \frac{5 \text{ V}}{2} \rightarrow V_{ref} = 2.5 \text{ V}$$

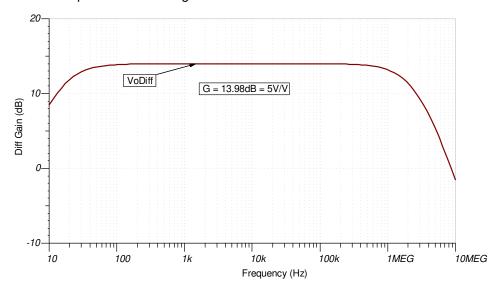
6. Calculate C₁ and C₂ to set the lower cutoff frequency.

$$\begin{split} f_{c} &= \frac{1}{2 \times \pi \times R_{4} \times C_{1}} = 16 \text{ Hz} \\ R_{4} &= R_{5} = 10 \text{ k}\Omega \\ f_{c} &= \frac{1}{2 \times \pi \times 10 \text{ k}\Omega \times C_{1}} = 16 \text{ Hz} \rightarrow C_{1} = \frac{1}{2 \times \pi \times 10 \text{ k}\Omega \times 16 \text{ Hz}} = 0.99 \mu\text{F} \rightarrow C_{1} = C_{2} = 1 \mu\text{F} \quad \Big(\text{Standard value}\Big) \end{split}$$

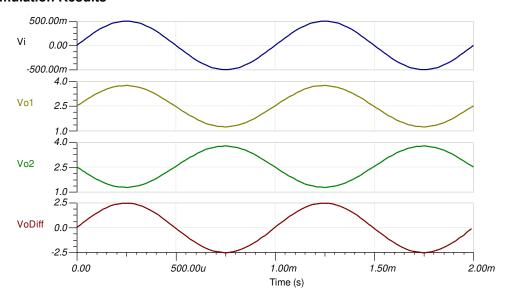
Design Simulations

AC Simulation Results

In the following figure, notice the lower -3-dB cutoff frequency is approximately 16Hz and the upper cutoff frequency is > 1MHz as required for this design.



Transient Simulation Results



References

- 1. Analog Engineer's Circuit Cookbooks
- 2. SPICE Simulation File SBOMAU5.
- 3. TI Precision Labs

Design Featured Op Amp

OPA374				
V _{ss}	2.3V to 5.5V			
V _{inCM}	Rail-to-rail			
V _{out}	Rail-to-rail			
V _{os}	1mV			
I _q	585µA/Ch			
l _b	0.5pA			
UGBW	6.5MHz			
SR	5V/μs			
#Channels	1,2,4			
www.ti.com/product/opa374				

Design Alternate Op Amp

TLV9061				
V _{ss}	1.8V to 5.5V			
V _{inCM}	Rail-to-rail			
V _{out}	Rail-to-rail			
V _{os}	0.3mV			
Iq	0.538mA			
I _b	0.5pA			
UGBW	10MHz			
SR	6.5V/µs			
#Channels	1,2,4			
www.ti.com/product/tlv9061				

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