The Texas Instruments MSP430 family of ultralow-power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency.

The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6 μs.

The MSP430F42x0 is a microcontroller configuration with a 16-bit timer, a high performance 16-bit sigma-delta A/D converter, 12-bit D/A converter, 32 I/O pins, and a liquid crystal display driver.

Typical applications for this device include analog and digital sensor systems, digital motor control, remote controls, thermostats, digital timers, hand-held meters, etc.

### AVAILABLE OPTIONS

<table>
<thead>
<tr>
<th>T&lt;sub&gt;A&lt;/sub&gt;</th>
<th>PLASTIC 48-PIN SSOP (DL)</th>
<th>PLASTIC 48-PIN QFN (RGZ)</th>
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<tbody>
<tr>
<td>−40°C to 85°C</td>
<td>MSP430F4250IDL</td>
<td>MSP430F4250IRGZ</td>
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<tr>
<td></td>
<td>MSP430F4260IDL</td>
<td>MSP430F4260IRGZ</td>
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<tr>
<td></td>
<td>MSP430F4270IDL</td>
<td>MSP430F4270IRGZ</td>
</tr>
</tbody>
</table>

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. These devices have limited built-in ESD protection.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
pin designation, MSP430F42x0

DL PACKAGE
(TOP VIEW)

<table>
<thead>
<tr>
<th>Pin</th>
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<tbody>
<tr>
<td>TDO/TDI</td>
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<td>TDI/TCLK</td>
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<td>3</td>
</tr>
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<td>TCK</td>
<td>4</td>
</tr>
<tr>
<td>RST/NMI</td>
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<td>DVCC</td>
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<td>DVSS</td>
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<td>XIN</td>
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<td>XOUT</td>
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<td>AVSS</td>
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<td>AVCC</td>
<td>11</td>
</tr>
<tr>
<td>VREF</td>
<td>12</td>
</tr>
<tr>
<td>P6.0/A0+</td>
<td>13</td>
</tr>
<tr>
<td>P6.1/A0−</td>
<td>14</td>
</tr>
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<td>P6.2/A1+</td>
<td>15</td>
</tr>
<tr>
<td>P6.3/A1−</td>
<td>16</td>
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<td>P6.4</td>
<td>17</td>
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<td>P6.5</td>
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<td>20</td>
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<tr>
<td>P1.6/A2−</td>
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</tr>
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<td>P1.5/TACLK/ACLK/A3+</td>
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<tr>
<td>P1.4/A3−/DAC0</td>
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<td>P5.4/COM3</td>
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<tr>
<td>P5.3/COM2</td>
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<td>P5.2/COM1</td>
<td>46</td>
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<tr>
<td>COM0</td>
<td>45</td>
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<tr>
<td>P2.0/S13</td>
<td>44</td>
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<tr>
<td>P2.1/S12</td>
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</tr>
<tr>
<td>P2.2/S11</td>
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<tr>
<td>P2.3/S10</td>
<td>41</td>
</tr>
<tr>
<td>P2.4/S9</td>
<td>40</td>
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<td>P2.6/S7</td>
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<tr>
<td>P2.7/S6</td>
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<td>S5</td>
<td>36</td>
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<td>P5.7/S4</td>
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</tr>
<tr>
<td>P5.5/S2</td>
<td>33</td>
</tr>
<tr>
<td>P5.0/S1</td>
<td>32</td>
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<tr>
<td>P5.1/S0</td>
<td>31</td>
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<td>LCDCAP/R23</td>
<td>30</td>
</tr>
<tr>
<td>LCDREF/R13</td>
<td>29</td>
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<td>P1.0/TA0</td>
<td>28</td>
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<tr>
<td>P1.1/TA0/MCLK</td>
<td>27</td>
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<tr>
<td>P1.2/TA1/A4−</td>
<td>26</td>
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<tr>
<td>P1.3/TA2/A4+</td>
<td>25</td>
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</table>
pin designation, MSP430F42x0 (continued)

MSP430F42x0
MIXED SIGNAL MICROCONTROLLER

RGZ PACKAGE
(TOP VIEW)

DVSS  1
XIN   2
XOUT  3
AVSS  4
AVCC  5
VREF  6
P6.0/A0+ 7
P6.1/A0− 8
P6.2/A1+ 9
P6.3/A1− 10
P6.4  11
P6.5  12
P6.6  13
P6.7  14
P1.1/A2+ 15
P1.2/A2− 16
P1.3/A3+ 17
P1.4/A3−/DAC0 18
P1.5/TACLK/ACLK/A3+ 19
P1.6/TACLK/ACLK/A3− 20
P1.7/TACLK/ACLK/A4+ 21
P1.8/TACLK/ACLK/A4− 22
P1.9/TACLK/ACLK/A5+ 23
P1.10/TACLK/ACLK/A5− 24
P1.11/TA0/A5 25
P1.12/TA0/A4 26
P1.13/TA0/A3 27
P1.14/TA0/A2 28
P1.15/TA0/A1 29
P1.16/TA0/A0 30
P5.0/S1 31
P5.1/S0 32
P5.2/COM1 33
P5.3/COM2 34
P5.4/COM3 35
P5.5/S2 36
P5.6/S3 37
P5.7/S4 38
P2.1/S12 39
P2.0/S13 40
P2.6/S7 41
P2.7/S6 42
P2.8/S5 43
P2.9/S4 44
P2.10/S3 45
P2.11/S2 46
P2.12/S1 47
P2.13/S0 48

DVSS  XIN  XOUT  AVSS  AVCC  VREF  P6.0/A0+  P6.1/A0−  P6.2/A1+  P6.3/A1−  P6.4  P6.5  P6.6  P6.7  P1.1/A2+  P1.2/A2−  P1.3/A3+  P1.4/A3−/DAC0  P1.5/TACLK/ACLK/A3+  P1.6/TACLK/ACLK/A3−  P1.7/TACLK/ACLK/A4+  P1.8/TACLK/ACLK/A4−  P1.9/TACLK/ACLK/A5+  P1.10/TACLK/ACLK/A5−  P1.11/TA0/A5  P1.12/TA0/A4  P1.13/TA0/A3  P1.14/TA0/A2  P1.15/TA0/A1  P1.16/TA0/A0  P5.0/S1  P5.1/S0  P5.2/COM1  P5.3/COM2  P5.4/COM3  P5.5/S2  P5.6/S3  P5.7/S4  P2.1/S12  P2.0/S13  P2.6/S7  P2.7/S6  P2.8/S5  P2.9/S4  P2.10/S3  P2.11/S2  P2.12/S1  P2.13/S0

MSP430F42x0IRGZ

RGZ PACKAGE
(TOP VIEW)
MSP430F42x0 functional block diagram
## MSP430F42x0 Terminal Functions

<table>
<thead>
<tr>
<th>TERMINAL</th>
<th>NAME</th>
<th>DL NO</th>
<th>RGZ NO</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TDO/TDI</td>
<td>1</td>
<td>43</td>
<td>I/O</td>
<td>Test data output port. TDO/TDI data output or programming data input terminal</td>
</tr>
<tr>
<td></td>
<td>TDI/TCLK</td>
<td>2</td>
<td>44</td>
<td>I</td>
<td>Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.</td>
</tr>
<tr>
<td></td>
<td>TMS</td>
<td>3</td>
<td>45</td>
<td>I</td>
<td>Test mode select. TMS is used as an input port for device programming and test.</td>
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<tr>
<td></td>
<td>TCK</td>
<td>4</td>
<td>46</td>
<td>I</td>
<td>Test clock. TCK is the clock input port for device programming and test.</td>
</tr>
<tr>
<td></td>
<td>RST/NMI</td>
<td>5</td>
<td>47</td>
<td>I</td>
<td>General-purpose digital I/O / reset input or nonmaskable interrupt input port</td>
</tr>
<tr>
<td></td>
<td>DV_CC</td>
<td>6</td>
<td>48</td>
<td>I</td>
<td>Digital supply voltage, positive terminal</td>
</tr>
<tr>
<td></td>
<td>DV_SS</td>
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<td>1</td>
<td>I</td>
<td>Digital supply voltage, negative terminal</td>
</tr>
<tr>
<td></td>
<td>XIN</td>
<td>8</td>
<td>2</td>
<td>I</td>
<td>Input terminal of crystal oscillator XT1</td>
</tr>
<tr>
<td></td>
<td>XOUT</td>
<td>9</td>
<td>3</td>
<td>O</td>
<td>Output terminal of crystal oscillator XT1</td>
</tr>
<tr>
<td></td>
<td>AV_SS</td>
<td>10</td>
<td>4</td>
<td>I</td>
<td>Analog supply voltage, negative terminal</td>
</tr>
<tr>
<td></td>
<td>AV_CC</td>
<td>11</td>
<td>5</td>
<td>I</td>
<td>Analog supply voltage, positive terminal</td>
</tr>
<tr>
<td></td>
<td>V_REF</td>
<td>12</td>
<td>6</td>
<td>I/O</td>
<td>Analog reference voltage</td>
</tr>
<tr>
<td></td>
<td>P6.0/A0+</td>
<td>13</td>
<td>7</td>
<td>I/O</td>
<td>General-purpose digital I/O / analog input A0+</td>
</tr>
<tr>
<td></td>
<td>P6.1/A0−</td>
<td>14</td>
<td>8</td>
<td>I/O</td>
<td>General-purpose digital I/O / analog input A0−</td>
</tr>
<tr>
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<td>P6.2/A1+</td>
<td>15</td>
<td>9</td>
<td>I/O</td>
<td>General-purpose digital I/O / analog input A1+</td>
</tr>
<tr>
<td></td>
<td>P6.3/A1−</td>
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<td>10</td>
<td>I/O</td>
<td>General-purpose digital I/O / analog input A1−</td>
</tr>
<tr>
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<td>P6.4</td>
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<td>I/O</td>
<td>General-purpose digital I/O</td>
</tr>
<tr>
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<td>I/O</td>
<td>General-purpose digital I/O</td>
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<td>I/O</td>
<td>General-purpose digital I/O</td>
</tr>
<tr>
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<td>I/O</td>
<td>General-purpose digital I/O</td>
</tr>
<tr>
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<td>P1.7/A2+</td>
<td>21</td>
<td>15</td>
<td>I/O</td>
<td>General-purpose digital I/O / analog input A2+</td>
</tr>
<tr>
<td></td>
<td>P1.6/A2−</td>
<td>22</td>
<td>16</td>
<td>I/O</td>
<td>General-purpose digital I/O / analog input A2−</td>
</tr>
<tr>
<td></td>
<td>P1.5/TACLK/ACLK/A3+</td>
<td>23</td>
<td>17</td>
<td>I/O</td>
<td>General-purpose digital I/O / Timer_A, clock signal TACLK input / ACLK output (divided by 1, 2, 4, or 8) / analog input A3+</td>
</tr>
<tr>
<td></td>
<td>P1.4/A3−/DAC0</td>
<td>24</td>
<td>18</td>
<td>I/O</td>
<td>General-purpose digital I/O / analog input A3− / DAC12 output</td>
</tr>
<tr>
<td></td>
<td>P1.3/TA2/A4+</td>
<td>25</td>
<td>19</td>
<td>I/O</td>
<td>General-purpose digital I/O / Timer_A, Capture: CCI2A, compare: Out2 output / analog input A4+</td>
</tr>
<tr>
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<td>P1.2/TA1/A4−</td>
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<td>20</td>
<td>I/O</td>
<td>General-purpose digital I/O / Timer_A, Capture: CCI1A, compare: Out1 output / analog input A4−</td>
</tr>
<tr>
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<td>P1.1/TA0/MCLK</td>
<td>27</td>
<td>21</td>
<td>I/O</td>
<td>General-purpose digital I/O / Timer_A, Capture: CCI0B / MCLK output. Note: TA0 is only an input on this pin / BSL Transmit</td>
</tr>
<tr>
<td></td>
<td>P1.0/TA0</td>
<td>28</td>
<td>22</td>
<td>I/O</td>
<td>General-purpose digital I/O / Timer_A, Capture: CCI0A input, compare: Out0 output / BSL Transmit</td>
</tr>
<tr>
<td></td>
<td>LCDREF/R13</td>
<td>29</td>
<td>23</td>
<td>I/O</td>
<td>External LCD reference voltage input / input port of third most positive analog LCD level (V4 or V3)</td>
</tr>
<tr>
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<td>LCDCAP/R23</td>
<td>30</td>
<td>24</td>
<td>I/O</td>
<td>Capacitor connection for LCD charge pump / input port of second most positive analog LCD level (V2)</td>
</tr>
<tr>
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<td>P5.1/S0</td>
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<td>25</td>
<td>I/O</td>
<td>General-purpose digital I/O / LCD segment output 0</td>
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<td>P5.0/S1</td>
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<td>P5.5/S2</td>
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<td>27</td>
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<td>General-purpose digital I/O / LCD segment output 2</td>
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<tr>
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<td>P5.6/S3</td>
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<td>28</td>
<td>I/O</td>
<td>General-purpose digital I/O / LCD segment output 3</td>
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<tr>
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<td>P5.7/S4</td>
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<td>I/O</td>
<td>General-purpose digital I/O / LCD segment output 4</td>
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<tr>
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<td>S5</td>
<td>36</td>
<td>30</td>
<td>O</td>
<td>LCD segment output 5</td>
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<tr>
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<td>P2.7/S6</td>
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<td>31</td>
<td>I/O</td>
<td>General-purpose digital I/O / LCD segment output 6</td>
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<td>P2.6/S7</td>
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<td>32</td>
<td>I/O</td>
<td>General-purpose digital I/O / LCD segment output 7</td>
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MSP430F42x0 Terminal Functions (Continued)

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<tr>
<th>TERMINAL</th>
<th>DL NO.</th>
<th>RGZ NO.</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
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<tr>
<td>P2.5/S8</td>
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<td>33</td>
<td>I/O</td>
<td>General-purpose digital I/O / LCD segment output 8</td>
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<td>P2.4/S9</td>
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<td>34</td>
<td>I/O</td>
<td>General-purpose digital I/O / LCD segment output 9</td>
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<tr>
<td>P2.3/S10</td>
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<td>35</td>
<td>I/O</td>
<td>General-purpose digital I/O / LCD segment output 10</td>
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<td>P2.2/S11</td>
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<td>36</td>
<td>I/O</td>
<td>General-purpose digital I/O / LCD segment output 11</td>
</tr>
<tr>
<td>P2.1/S12</td>
<td>43</td>
<td>37</td>
<td>I/O</td>
<td>General-purpose digital I/O / LCD segment output 12</td>
</tr>
<tr>
<td>P2.0/S13</td>
<td>44</td>
<td>38</td>
<td>I/O</td>
<td>General-purpose digital I/O / LCD segment output 13</td>
</tr>
<tr>
<td>COM0</td>
<td>45</td>
<td>39</td>
<td>O</td>
<td>Common output, COM0–3 are used for LCD backplanes.</td>
</tr>
<tr>
<td>P5.2/COM1</td>
<td>46</td>
<td>40</td>
<td>I/O</td>
<td>General-purpose digital I/O / common output, COM0–3 are used for LCD backplanes.</td>
</tr>
<tr>
<td>P5.3/COM2</td>
<td>47</td>
<td>41</td>
<td>I/O</td>
<td>General-purpose digital I/O / common output, COM0–3 are used for LCD backplanes.</td>
</tr>
<tr>
<td>P5.4/COM3</td>
<td>48</td>
<td>42</td>
<td>I/O</td>
<td>General-purpose digital I/O / common output, COM0–3 are used for LCD backplanes.</td>
</tr>
<tr>
<td>QFN Pad</td>
<td>NA</td>
<td>None</td>
<td>NA</td>
<td>QFN package pad connection to DVSS recommended.</td>
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</tbody>
</table>
short-form description

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

Table 1. Instruction Word Formats

<table>
<thead>
<tr>
<th>Format Description</th>
<th>Syntax Example</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dual operands, source-destination</td>
<td>e.g. ADD R4,R5</td>
<td>R4 + R5 ----&gt; R5</td>
</tr>
<tr>
<td>Single operands, destination only</td>
<td>e.g. CALL R8</td>
<td>PC ----&gt;(TOS), R8---&gt; PC</td>
</tr>
<tr>
<td>Relative jump, un/conditional</td>
<td>e.g. JNE</td>
<td>Jump-on-equal bit = 0</td>
</tr>
</tbody>
</table>

Table 2. Address Mode Descriptions

<table>
<thead>
<tr>
<th>ADDRESS MODE</th>
<th>S</th>
<th>D</th>
<th>SYNTAX</th>
<th>EXAMPLE</th>
<th>OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register</td>
<td></td>
<td></td>
<td>MOV Rs,Rd</td>
<td>MOV R10,R11</td>
<td>R10 ----&gt; R11</td>
</tr>
<tr>
<td>Indexed</td>
<td></td>
<td></td>
<td>MOV X(Rn),Y(Rm)</td>
<td>MOV 2(R5),6(R6)</td>
<td>M(2+R5) ----&gt; M(6+R6)</td>
</tr>
<tr>
<td>Symbolic (PC relative)</td>
<td></td>
<td></td>
<td>MOV EDE,TONI</td>
<td>M(EDEx) ----&gt; M(TONIX)</td>
<td></td>
</tr>
<tr>
<td>Absolute</td>
<td></td>
<td></td>
<td>MOV &amp; MEM, &amp; TCDAT</td>
<td>M(MEM) ----&gt; M(TCDAT)</td>
<td></td>
</tr>
<tr>
<td>Indirect</td>
<td></td>
<td></td>
<td>MOV @Rn,Y(Rm)</td>
<td>MOV @R10,Tab(R6)</td>
<td>M(R10) ----&gt; M(Tab+R6)</td>
</tr>
<tr>
<td>Indirect autoincrement</td>
<td></td>
<td></td>
<td>MOV @Rn+,Rm</td>
<td>MOV @R10+,R11</td>
<td>M(R10) ----&gt; R11</td>
</tr>
<tr>
<td>Immediate</td>
<td></td>
<td></td>
<td>MOV #X,TONI</td>
<td>MOV #45,TONI</td>
<td>#45 ----&gt; M(TONI)</td>
</tr>
</tbody>
</table>

NOTE: S = source  D = destination
operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- **Active mode (AM)**
  - All clocks are active

- **Low-power mode 0 (LPM0)**
  - CPU is disabled
    - ACLK and SMCLK remain active, MCLK is available to modules
    - FLL+ loop control remains active

- **Low-power mode 1 (LPM1)**
  - CPU is disabled
    - ACLK and SMCLK remain active, MCLK is available to modules
    - FLL+ loop control is disabled

- **Low-power mode 2 (LPM2)**
  - CPU is disabled
    - MCLK, FLL+ loop control, and DCOCLK are disabled
    - DCO’s dc-generator remains enabled
    - ACLK remains active

- **Low-power mode 3 (LPM3)**
  - CPU is disabled
    - MCLK, FLL+ loop control, and DCOCLK are disabled
    - DCO’s dc-generator is disabled
    - ACLK remains active

- **Low-power mode 4 (LPM4);**
  - CPU is disabled
    - ACLK is disabled
    - MCLK, FLL+ loop control, and DCOCLK are disabled
    - DCO’s dc-generator is disabled
    - Crystal oscillator is stopped
### interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh–0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

<table>
<thead>
<tr>
<th>INTERRUPT SOURCE</th>
<th>INTERRUPT FLAG</th>
<th>SYSTEM INTERRUPT</th>
<th>WORD ADDRESS</th>
<th>PRIORITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power-Up</td>
<td>WDTIFG</td>
<td>Reset</td>
<td>0FFFEh</td>
<td>15, highest</td>
</tr>
<tr>
<td>External Reset</td>
<td>KEYV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Watchdog</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Flash Memory</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PC Out-of-Range (see Note 4)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NMI</td>
<td>NMIIFG (see Notes 1 and 3)</td>
<td>(Non)maskable</td>
<td>0FFFCCh</td>
<td>14</td>
</tr>
<tr>
<td>Oscillator Fault</td>
<td>OFIFG (see Notes 1 and 3)</td>
<td>(Non)maskable</td>
<td>0FFFAh</td>
<td>13</td>
</tr>
<tr>
<td>Flash Memory Access Violation</td>
<td>ACCVIFG (see Notes 1 and 3)</td>
<td>(Non)maskable</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SD16_A</td>
<td>SD16CCTLx SD16OVIFG,</td>
<td>Maskable</td>
<td>0FFFAh</td>
<td>13</td>
</tr>
<tr>
<td></td>
<td>SD16CCTLx SD161IFG</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(see Notes 1 and 2)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Watchdog Timer</td>
<td>WDTIFG</td>
<td>Maskable</td>
<td>0FFFAh</td>
<td>13</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Timer_A3</td>
<td>TACCR0 CCIFG0 (see Note 2)</td>
<td>Maskable</td>
<td>0FFFECh</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Timer_A3</td>
<td>TACCR1 CCIFG1 and TACCR2 CCIFG2,</td>
<td>Maskable</td>
<td>0FFEFAh</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>TAIFG (see Notes 1 and 2)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I/O Port P1 (Eight Flags)</td>
<td>P1IFG.0 to P1IFG.7 (see Notes 1 and 2)</td>
<td>Maskable</td>
<td>0FFFAh</td>
<td>13</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DAC12</td>
<td>DAC12_0IFG (see Note 2)</td>
<td>Maskable</td>
<td>0FFE4h</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I/O Port P2 (Eight Flags)</td>
<td>P2IFG.0 to P2IFG.7 (see Notes 1 and 2)</td>
<td>Maskable</td>
<td>0FFE2h</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Basic Timer1</td>
<td>BTIFG</td>
<td>Maskable</td>
<td>0FFE0h</td>
<td>0, lowest</td>
</tr>
</tbody>
</table>

**NOTES:**

1. Multiple source flags
2. Interrupt flags are located in the module.
3. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
4. A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h–01FFh) or from within unused address ranges (MSP430F4270, MSP430F4260: from 0300h to 0BFFh and from 01100h to 07FFFh, MSP430F4250: from 0300h to 0BFFh and from 01100h to 0BFFh).
special function registers

The MSP430 special function registers (SFR) are located in the lowest address space, and are organized as byte mode registers. SFRs should be accessed with byte instructions.

interrupt enable registers 1 and 2

<table>
<thead>
<tr>
<th>Address</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td></td>
<td></td>
<td>ACCVIE</td>
<td>NMIIE</td>
<td>OFIE</td>
<td>WDTIE</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>rw–0</td>
<td>rw–0</td>
<td>rw–0</td>
<td>rw–0</td>
<td>rw–0</td>
<td>rw–0</td>
<td>rw–0</td>
<td>rw–0</td>
</tr>
</tbody>
</table>

WDTIE: Watchdog-timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured as a general-purpose timer.

OFIE: Oscillator-fault-interrupt enable

NMIIE: Nonmaskable-interrupt enable

ACCVIE: Flash access violation interrupt enable

<table>
<thead>
<tr>
<th>Address</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>01h</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>BTIE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>rw–0</td>
<td>rw–0</td>
<td>rw–0</td>
<td>rw–0</td>
<td>rw–0</td>
<td>rw–0</td>
<td>rw–0</td>
<td>rw–0</td>
</tr>
</tbody>
</table>

BTIE: Basic timer interrupt enable

interrupt flag registers 1 and 2

<table>
<thead>
<tr>
<th>Address</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>02h</td>
<td></td>
<td></td>
<td>NMIIFG</td>
<td></td>
<td>OFIFG</td>
<td></td>
<td>WDTIFG</td>
<td></td>
</tr>
<tr>
<td></td>
<td>rw–0</td>
<td>rw–0</td>
<td>rw–0</td>
<td>rw–0</td>
<td>rw–0</td>
<td>rw–0</td>
<td>rw–0</td>
<td>rw–0</td>
</tr>
</tbody>
</table>

WDTIFG: Set on watchdog timer overflow (in watchdog mode) or security key violation
Reset on \( V_{CC} \) power-on or a reset condition at the \( RST/NMI \) pin in reset mode

OFIFG: Flag set on oscillator fault

NMIIFG: Set via \( RST/NMI \) pin

<table>
<thead>
<tr>
<th>Address</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>03h</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>BTIFG</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>rw–0</td>
<td>rw–0</td>
<td>rw–0</td>
<td>rw–0</td>
<td>rw–0</td>
<td>rw–0</td>
<td>rw–0</td>
<td>rw–0</td>
</tr>
</tbody>
</table>

BTIFG: Basic timer flag
module enable registers 1 and 2

<table>
<thead>
<tr>
<th>Address</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>04h</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>05h</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend: rw:
- Bit Can Be Read and Written
- Bit Can Be Read and Written. It Is Reset or Set by PUC.
- Bit Can Be Read and Written. It Is Reset or Set by POR.
- SFR Bit Not Present in Device

memory organization

<table>
<thead>
<tr>
<th></th>
<th>MSP430F4250</th>
<th>MSP430F4260</th>
<th>MSP430F4270</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Main: interrupt vector</td>
<td>Size</td>
<td>16KB</td>
<td>24KB</td>
</tr>
<tr>
<td>Main: code memory</td>
<td>Flash</td>
<td>0FFFh – 0FFE0h</td>
<td>0FFFh – 0FFE0h</td>
</tr>
<tr>
<td></td>
<td>Flash</td>
<td>0FFFh – 0C000h</td>
<td>0FFFh – 0A000h</td>
</tr>
<tr>
<td>Information memory</td>
<td>Size</td>
<td>256 Byte</td>
<td>256 Byte</td>
</tr>
<tr>
<td></td>
<td>Flash</td>
<td>010FFh – 01000h</td>
<td>010FFh – 01000h</td>
</tr>
<tr>
<td>Boot memory</td>
<td>Size</td>
<td>1KB</td>
<td>1KB</td>
</tr>
<tr>
<td></td>
<td>ROM</td>
<td>0FFFh – 0C000h</td>
<td>0FFFh – 0C000h</td>
</tr>
<tr>
<td>RAM</td>
<td>Size</td>
<td>256 Byte</td>
<td>256 Byte</td>
</tr>
<tr>
<td></td>
<td></td>
<td>02FFh – 0200h</td>
<td>02FFh – 0200h</td>
</tr>
<tr>
<td>Peripherals</td>
<td>16-bit</td>
<td>01FFh – 0100h</td>
<td>01FFh – 0100h</td>
</tr>
<tr>
<td></td>
<td>8-bit</td>
<td>0FFh – 010h</td>
<td>0FFh – 010h</td>
</tr>
<tr>
<td></td>
<td>8-bit SFR</td>
<td>0Fh – 00h</td>
<td>0Fh – 00h</td>
</tr>
</tbody>
</table>

bootstrap loader (BSL)

The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the Application report Features of the MSP430 Bootstrap Loader, Literature Number SLAA089.

<table>
<thead>
<tr>
<th>BSL Function</th>
<th>DL Package Pins</th>
<th>RGZ Package Pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Transmit</td>
<td>28 – P1.0</td>
<td>22 – P1.0</td>
</tr>
<tr>
<td>Data Receive</td>
<td>27 – P1.1</td>
<td>21 – P1.1</td>
</tr>
</tbody>
</table>
The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has \( n \) segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to \( n \) may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0–n. Segments A and B are also called *information memory*.
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to the first use.

### Main Memory

<table>
<thead>
<tr>
<th>16KB</th>
<th>24KB</th>
<th>32KB</th>
</tr>
</thead>
<tbody>
<tr>
<td>0FFFFh</td>
<td>0FFFFh</td>
<td>0FFFFh</td>
</tr>
<tr>
<td>0FE00h</td>
<td>0FE00h</td>
<td>0FE00h</td>
</tr>
<tr>
<td>0FDFFh</td>
<td>0FDFFh</td>
<td>0FDFFh</td>
</tr>
<tr>
<td>0FC00h</td>
<td>0FC00h</td>
<td>0FC00h</td>
</tr>
<tr>
<td>0FBFFh</td>
<td>0FBFFh</td>
<td>0FBFFh</td>
</tr>
<tr>
<td>0FA00h</td>
<td>0FA00h</td>
<td>0FA00h</td>
</tr>
<tr>
<td>0F9FFh</td>
<td>0F9FFh</td>
<td>0F9FFh</td>
</tr>
</tbody>
</table>

### Information Memory

- Segments 0 with Interrupt Vectors
- Segment 1
- Segment 2
- Segment \( n \)†
- Segment A
- Segment B

<table>
<thead>
<tr>
<th>16KB</th>
<th>24KB</th>
<th>32KB</th>
</tr>
</thead>
<tbody>
<tr>
<td>0FFFFh</td>
<td>0FFFFh</td>
<td>0FFFFh</td>
</tr>
<tr>
<td>0FE00h</td>
<td>0FE00h</td>
<td>0FE00h</td>
</tr>
<tr>
<td>0FDFFh</td>
<td>0FDFFh</td>
<td>0FDFFh</td>
</tr>
<tr>
<td>0FC00h</td>
<td>0FC00h</td>
<td>0FC00h</td>
</tr>
<tr>
<td>0FBFFh</td>
<td>0FBFFh</td>
<td>0FBFFh</td>
</tr>
<tr>
<td>0FA00h</td>
<td>0FA00h</td>
<td>0FA00h</td>
</tr>
<tr>
<td>0F9FFh</td>
<td>0F9FFh</td>
<td>0F9FFh</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>16KB</th>
<th>24KB</th>
<th>32KB</th>
</tr>
</thead>
<tbody>
<tr>
<td>0C400h</td>
<td>0A400h</td>
<td>08400h</td>
</tr>
<tr>
<td>0C3FFh</td>
<td>0A3FFh</td>
<td>083FFh</td>
</tr>
<tr>
<td>0C200h</td>
<td>0A200h</td>
<td>08200h</td>
</tr>
<tr>
<td>0C1FFh</td>
<td>0A1FFh</td>
<td>081FFh</td>
</tr>
<tr>
<td>0C000h</td>
<td>0A000h</td>
<td>08000h</td>
</tr>
<tr>
<td>010FFh</td>
<td>010FFh</td>
<td>010FFh</td>
</tr>
<tr>
<td>01080h</td>
<td>01080h</td>
<td>01080h</td>
</tr>
<tr>
<td>0107Fh</td>
<td>0107Fh</td>
<td>0107Fh</td>
</tr>
<tr>
<td>01000h</td>
<td>01000h</td>
<td>01000h</td>
</tr>
</tbody>
</table>
peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, refer to the *MSP430x4xx Family User’s Guide*, Literature Number SLAU056.

oscillator and system clock

The clock system in the MSP430F42x0 family of devices is supported by the FLL+ module that includes support for a 32768 Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO) and a high frequency crystal oscillator. The FLL+ clock module is designed to meet the requirements of both low system cost and low-power consumption. The FLL+ features digital frequency locked loop (FLL) hardware which in conjunction with a digital modulator stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6 μs. The FLL+ module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768 Hz watch crystal or a high frequency crystal.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, or ACLK/8.

brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The CPU begins code execution after the brownout circuit releases the device reset. However, VCC may not have ramped to VCC(min) at that time. The user must insure the default FLL+ settings are not changed until VCC reaches VCC(min).

digital I/O

There are four 8-bit I/O ports implemented—ports P1, P2, P5 and P6:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.

Basic Timer1

The Basic Timer1 has two independent 8-bit timers which can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. The Basic Timer1 can be used to generate periodic interrupts.

LCD driver with regulated charge pump

The LCD_A driver generates the segment and common signals required to drive an LCD display. The LCD_A controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2−MUX, 3−MUX, and 4−MUX LCDs are supported by this peripheral. The module can provide a LCD voltage independent of the supply voltage via an integrated charge pump. Furthermore it is possible to control the level of the LCD voltage and thus contrast in software.

watchdog timer

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.
Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compar, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

### Timer_A3 Signal Connections

<table>
<thead>
<tr>
<th>Input Pin Number</th>
<th>Device Input Signal</th>
<th>Module Input Name</th>
<th>Module Block</th>
<th>Module Output Signal</th>
<th>Output Pin Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>23 - P1.5</td>
<td>TACLK</td>
<td>TACLK</td>
<td>Timer</td>
<td>NA</td>
<td></td>
</tr>
<tr>
<td>23 - P1.5</td>
<td>ACLK</td>
<td>ACLK</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>23 - P1.5</td>
<td>SMCLK</td>
<td>SMCLK</td>
<td></td>
<td></td>
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<tr>
<td>28 - P1.0</td>
<td>TACLK</td>
<td>INCLK</td>
<td></td>
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</tr>
<tr>
<td>27 - P1.1</td>
<td>TA0</td>
<td>CCI0A</td>
<td>CCR0</td>
<td>TA0</td>
<td>28 - P1.0</td>
</tr>
<tr>
<td>27 - P1.1</td>
<td>DVSS</td>
<td>GND</td>
<td></td>
<td></td>
<td>22 - P1.0</td>
</tr>
<tr>
<td>26 - P1.2</td>
<td>TA1</td>
<td>CCI1A</td>
<td>CCR1</td>
<td>TA1</td>
<td>26 - P1.2</td>
</tr>
<tr>
<td>26 - P1.2</td>
<td>DVSS</td>
<td>GND</td>
<td></td>
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<td>20 - P1.2</td>
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<tr>
<td>25 - P1.3</td>
<td>TA2</td>
<td>CCI2A</td>
<td>CCR2</td>
<td>TA2</td>
<td>25 - P1.3</td>
</tr>
<tr>
<td></td>
<td>DVSS</td>
<td>GND</td>
<td></td>
<td></td>
<td>19 - P1.3</td>
</tr>
<tr>
<td></td>
<td>ACLK (internal)</td>
<td>CCI2B</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

SD16_A

The SD16_A module supports 16-bit analog-to-digital conversions. The module implements a 16-bit sigma-delta core and reference generator. In addition to external analog inputs, an internal $V_{CC}$ sense and temperature sensor are also available.

DAC12

The DAC12 module is a 12-bit, R-ladder, voltage output DAC. The DAC12 may be used in 8- or 12-bit mode.
### Peripheral File Map

#### Peripheral with Word Access

<table>
<thead>
<tr>
<th>Module</th>
<th>Description</th>
<th>Address</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>Watchdog</td>
<td>Watchdog timer control</td>
<td>WDTCTL</td>
<td>0120h</td>
</tr>
<tr>
<td>Timer_A3</td>
<td>Capture/compare register 2</td>
<td>TACCR2</td>
<td>0176h</td>
</tr>
<tr>
<td></td>
<td>Capture/compare register 1</td>
<td>TACCR1</td>
<td>0174h</td>
</tr>
<tr>
<td></td>
<td>Capture/compare register 0</td>
<td>TACCR0</td>
<td>0172h</td>
</tr>
<tr>
<td></td>
<td>Timer_A register</td>
<td>TAR</td>
<td>0170h</td>
</tr>
<tr>
<td></td>
<td>Capture/compare control 2</td>
<td>TACCTL2</td>
<td>0166h</td>
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<td></td>
<td>Capture/compare control 1</td>
<td>TACCTL1</td>
<td>0164h</td>
</tr>
<tr>
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<td>Capture/compare control 0</td>
<td>TACCTL0</td>
<td>0162h</td>
</tr>
<tr>
<td></td>
<td>Timer_A control</td>
<td>TACTL</td>
<td>0160h</td>
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<tr>
<td></td>
<td>Timer_A interrupt vector</td>
<td>TAIV</td>
<td>012Eh</td>
</tr>
<tr>
<td>Flash</td>
<td>Flash control 3</td>
<td>FCTL3</td>
<td>012Ch</td>
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<tr>
<td></td>
<td>Flash control 2</td>
<td>FCTL2</td>
<td>012Ah</td>
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<tr>
<td></td>
<td>Flash control 1</td>
<td>FCTL1</td>
<td>0128h</td>
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<tr>
<td>DAC12</td>
<td>DAC12_0 data</td>
<td>DAC12_0DAT</td>
<td>01C8h</td>
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<td></td>
<td>DAC12_0 control</td>
<td>DAC12_0CTL</td>
<td>01C0h</td>
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<tr>
<td>SD16_A (see also: Peripherals with Byte Access)</td>
<td>General Control</td>
<td>SD16CTL</td>
<td>0100h</td>
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<tr>
<td></td>
<td>Channel 0 Control</td>
<td>SD16CCTL0</td>
<td>0102h</td>
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<tr>
<td></td>
<td>Interrupt vector word register</td>
<td>SD16IV</td>
<td>0110h</td>
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<tr>
<td></td>
<td>Channel 0 conversion memory</td>
<td>SD16MEM0</td>
<td>0112h</td>
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#### Peripheral with Byte Access

<table>
<thead>
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<th>Module</th>
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<th>Offset</th>
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<tbody>
<tr>
<td>SD16_A (see also: Peripherals with Word Access)</td>
<td>Channel 0 Input Control</td>
<td>SD16INCTL0</td>
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<tr>
<td></td>
<td>Analog Enable</td>
<td>SD16AE</td>
<td>0B7h</td>
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<td>LCD_A</td>
<td>LCD Voltage Control 1</td>
<td>LCDAVCTL1</td>
<td>0AFh</td>
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<tr>
<td></td>
<td>LCD Voltage Control 0</td>
<td>LCDAVCTL0</td>
<td>0AEh</td>
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<td>LCD Voltage Port Control 1</td>
<td>LCDAPCTL1</td>
<td>0ADh</td>
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<tr>
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<td>LCD Voltage Port Control 0</td>
<td>LCDAPCTL0</td>
<td>0ACH</td>
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<tr>
<td></td>
<td>LCD memory 20</td>
<td>LCDM20</td>
<td>0A4h</td>
</tr>
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<td>LCD memory 16</td>
<td>LCDM16</td>
<td>0A0h</td>
</tr>
<tr>
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<td>LCD memory 15</td>
<td>LCDM15</td>
<td>09Fh</td>
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<tr>
<td></td>
<td>LCD memory 1</td>
<td>LCDM1</td>
<td>091h</td>
</tr>
<tr>
<td></td>
<td>LCD control and mode</td>
<td>LCDACL</td>
<td>090h</td>
</tr>
<tr>
<td>FLL+ Clock</td>
<td>FLL+ Control 1</td>
<td>FLL_CTL1</td>
<td>054h</td>
</tr>
<tr>
<td></td>
<td>FLL+ Control 0</td>
<td>FLL_CTL0</td>
<td>053h</td>
</tr>
<tr>
<td></td>
<td>System clock frequency control</td>
<td>SCFOCTL</td>
<td>052h</td>
</tr>
<tr>
<td></td>
<td>System clock frequency integrator</td>
<td>SCFI1</td>
<td>051h</td>
</tr>
<tr>
<td></td>
<td>System clock frequency integrator</td>
<td>SCFI0</td>
<td>050h</td>
</tr>
<tr>
<td>Basic Timer1</td>
<td>BT counter 2</td>
<td>BTCNT2</td>
<td>047h</td>
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<tr>
<td></td>
<td>BT counter 1</td>
<td>BTCNT1</td>
<td>046h</td>
</tr>
<tr>
<td></td>
<td>BT control</td>
<td>BTCTL</td>
<td>040h</td>
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## Peripheral File Map (Continued)

<table>
<thead>
<tr>
<th>Port</th>
<th>Function</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port P6</td>
<td>Port P6 selection</td>
<td>P6SEL 037h</td>
</tr>
<tr>
<td>Port P6</td>
<td>Port P6 direction</td>
<td>P6DIR 036h</td>
</tr>
<tr>
<td>Port P6</td>
<td>Port P6 output</td>
<td>P6OUT 035h</td>
</tr>
<tr>
<td>Port P6</td>
<td>Port P6 input</td>
<td>P6IN 034h</td>
</tr>
<tr>
<td>Port P5</td>
<td>Port P5 selection</td>
<td>P5SEL 033h</td>
</tr>
<tr>
<td>Port P5</td>
<td>Port P5 direction</td>
<td>P5DIR 032h</td>
</tr>
<tr>
<td>Port P5</td>
<td>Port P5 output</td>
<td>P5OUT 031h</td>
</tr>
<tr>
<td>Port P5</td>
<td>Port P5 input</td>
<td>P5IN 030h</td>
</tr>
<tr>
<td>Port P2</td>
<td>Port P2 selection</td>
<td>P2SEL 02Eh</td>
</tr>
<tr>
<td>Port P2</td>
<td>Port P2 interrupt enable</td>
<td>P2IE 02Dh</td>
</tr>
<tr>
<td>Port P2</td>
<td>Port P2 interrupt-edge select</td>
<td>P2IES 02Ch</td>
</tr>
<tr>
<td>Port P2</td>
<td>Port P2 interrupt flag</td>
<td>P2IFG 02Bh</td>
</tr>
<tr>
<td>Port P2</td>
<td>Port P2 direction</td>
<td>P2DIR 02Ah</td>
</tr>
<tr>
<td>Port P2</td>
<td>Port P2 output</td>
<td>P2OUT 029h</td>
</tr>
<tr>
<td>Port P2</td>
<td>Port P2 input</td>
<td>P2IN 028h</td>
</tr>
<tr>
<td>Port P1</td>
<td>Port P1 selection</td>
<td>P1SEL 026h</td>
</tr>
<tr>
<td>Port P1</td>
<td>Port P1 interrupt enable</td>
<td>P1IE 025h</td>
</tr>
<tr>
<td>Port P1</td>
<td>Port P1 interrupt-edge select</td>
<td>P1IES 024h</td>
</tr>
<tr>
<td>Port P1</td>
<td>Port P1 interrupt flag</td>
<td>P1IFG 023h</td>
</tr>
<tr>
<td>Port P1</td>
<td>Port P1 direction</td>
<td>P1DIR 022h</td>
</tr>
<tr>
<td>Port P1</td>
<td>Port P1 output</td>
<td>P1OUT 021h</td>
</tr>
<tr>
<td>Port P1</td>
<td>Port P1 input</td>
<td>P1IN 020h</td>
</tr>
<tr>
<td>Special functions</td>
<td>SFR module enable 2</td>
<td>ME2 005h</td>
</tr>
<tr>
<td>Special functions</td>
<td>SFR module enable 1</td>
<td>ME1 004h</td>
</tr>
<tr>
<td>Special functions</td>
<td>SFR interrupt flag 2</td>
<td>IFC2 003h</td>
</tr>
<tr>
<td>Special functions</td>
<td>SFR interrupt flag 1</td>
<td>IFC1 002h</td>
</tr>
<tr>
<td>Special functions</td>
<td>SFR interrupt enable 2</td>
<td>IE2 001h</td>
</tr>
<tr>
<td>Special functions</td>
<td>SFR interrupt enable 1</td>
<td>IE1 000h</td>
</tr>
</tbody>
</table>
absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

| Voltage applied at VCC to VSS | −0.3 V to 4.1 V |
| Voltage applied to any pin (see Note) | −0.3 V to VCC + 0.3 V |
| Diode current at any device terminal | ±2 mA |
| Storage temperature, Tstg: (unprogrammed device) | −55°C to 150°C |
| (programmed device) | −40°C to 85°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltages referenced to VSS. The JTAG fuse-blow voltage, VFB, is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.

recommended operating conditions

| Supply voltage during program execution (see Note 1), VCC (AVCC = DVCC = VCC) | MIN | NOM | MAX | UNITS |
| Supply voltage during flash memory programming (see Note 1), VCC (AVCC = DVCC = VCC) | 1.8 | 3.6 | V |
| Supply voltage, VSS (AVSS = DVSS = VSS) | 0 | 0 | V |
| Operating free-air temperature range, TA | −40 | 85 | °C |

| LFXT1 crystal frequency, f(LFXT1) (see Note 2) | Watch crystal | 32.768 | kHz |
| LF selected, XTSES_FLL=0 | Ceramic resonator | 450 | 8000 | kHz |
| XT1 selected, XTSES_FLL=1 | Crystal | 1000 | 8000 | kHz |

| Processor frequency (signal MCLK), f(System) | VCC = 1.8 V | DC | 4.15 | MHz |
| VCC = 3.6 V | DC | 8 | |

NOTES:
1. It is recommended to power AVCC and DVCC from the same source. A maximum difference of 0.3 V between AVCC and DVCC can be tolerated during power up and operation.
2. In LF mode, the LFXT1 oscillator requires a watch crystal. In XT1 mode, LFXT1 accepts a ceramic resonator or a crystal.

Figure 1. Frequency vs Supply Voltage, typical characteristic
electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

supply current into AVCC + DVCC excluding external current

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{(AM)}$</td>
<td>Active mode, (see Note 1)</td>
<td>$T_A = -40°C$ to $85°C$</td>
<td>$V_{CC} = 2.2$</td>
<td>250</td>
<td>370</td>
</tr>
<tr>
<td></td>
<td>$f_{(MCLK)} = f_{(SMCLK)} = 1$ MHz,</td>
<td></td>
<td>$V_{CC} = 3$</td>
<td>400</td>
<td>520</td>
</tr>
<tr>
<td></td>
<td>$f_{(ACLK)} = 32.768$ Hz</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>XT$S=0$, SELM=(0,1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{(LPM0)}$</td>
<td>Low-power mode, (LPM0) (see Note 1 and Note 4)</td>
<td>$T_A = -40°C$ to $85°C$</td>
<td>$V_{CC} = 2.2$</td>
<td>55</td>
<td>70</td>
</tr>
<tr>
<td></td>
<td>$f_{(MCLK)} = f_{(SMCLK)} = 1$ MHz</td>
<td></td>
<td>$V_{CC} = 3$</td>
<td>95</td>
<td>110</td>
</tr>
<tr>
<td></td>
<td>$f_{(ACLK)} = 32.768$ Hz, SCG0 = 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{(LPM2)}$</td>
<td>Low-power mode, (LPM2), (LPM3) (see Note 2 and Note 4)</td>
<td>$T_A = -40°C$ to $85°C$</td>
<td>$V_{CC} = 2.2$</td>
<td>11</td>
<td>14</td>
</tr>
<tr>
<td></td>
<td>$f_{(MCLK)} = f_{(SMCLK)} = 0$ MHz</td>
<td></td>
<td>$V_{CC} = 3$</td>
<td>17</td>
<td>22</td>
</tr>
<tr>
<td>$I_{(LPM3)}$</td>
<td>Low-power mode, (LPM3), (LPM4) (see Note 2 and Note 4)</td>
<td>$T_A = -40°C$</td>
<td>$V_{CC} = 2.2$</td>
<td>1.0</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td>$f_{(MCLK)} = f_{(SMCLK)} = 0$ MHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_{(ACLK)} = 32.768$ Hz, SCG0 = 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Basic Timer1 enabled, ACLK selected</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LCD_A enabled, LCDCPEN = 0: (static mode; $f_{LCD} = f_{(ACLK)}/32$)</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
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<tr>
<td>$I_{(LPM4)}$</td>
<td>Low-power mode, (LPM4) (see Note 2 and Note 4)</td>
<td>$T_A = -40°C$</td>
<td>$V_{CC} = 2.2$</td>
<td>0.1</td>
<td>0.5</td>
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<tr>
<td></td>
<td>$f_{(MCLK)} = 0$ MHz, $f_{(SMCLK)} = 0$ MHz,</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_{(ACLK)} = 0$ Hz, SCG0 = 1</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

NOTES:
1. Timer_A is clocked by $f_{(DCOCLK)} = f_{(DCO)} = 1$ MHz. All inputs are tied to 0 V or to VCC. Outputs do not source or sink any current.
2. All inputs are tied to 0 V or to VCC. Outputs do not source or sink any current.
3. The LPM3 currents are characterized with a Micro Crystal CC4V−T1A (9pF) crystal and OSCCAPx=01h.

Current consumption of active mode versus system frequency

$I_{(AM)} = I_{(AM)} [1 MHz] \times f_{(System)} [MHz]$

Current consumption of active mode versus supply voltage

$I_{(AM)} = I_{(AM)} [3 V] + 175 \mu A/V \times (V_{CC} - 3 V)$
electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

**SCHMITT-trigger inputs – Ports P1, P2, P5, and P6; RST/NMI; JTAG: TCK, TMS, TDI/TCLK, TDO/TDI**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IT+}$ Positive-going input threshold voltage</td>
<td>$V_{CC} = 2.2 \text{ V}$</td>
<td>1.1</td>
<td>1.55</td>
<td>1.98</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{CC} = 3 \text{ V}$</td>
<td>1.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IT-}$ Negative-going input threshold voltage</td>
<td>$V_{CC} = 2.2 \text{ V}$</td>
<td>0.4</td>
<td>0.9</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{CC} = 3 \text{ V}$</td>
<td>0.9</td>
<td>1.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{hys}$ Input voltage hysteresis ($V_{IT+} - V_{IT-}$)</td>
<td>$V_{CC} = 2.2 \text{ V}$</td>
<td>0.3</td>
<td>1.1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{CC} = 3 \text{ V}$</td>
<td>0.5</td>
<td>1.0</td>
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</table>

**inputs Px.x, TAx**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$V_{CC}$</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{(int)}$ External interrupt timing</td>
<td>Port P1, P2: P1.x to P2.x, external trigger signal for the interrupt flag, (see Note 1)</td>
<td>$2.2 \text{ V}$</td>
<td>62</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$3 \text{ V}$</td>
<td>50</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{(cap)}$ Timer_A capture timing</td>
<td>TA0, TA1, TA2</td>
<td>$2.2 \text{ V}$</td>
<td>62</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$3 \text{ V}$</td>
<td>50</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f_{(TAext)}$ Timer_A clock frequency externally applied to pin</td>
<td>TACLK, INCLK: $t(H) = t(L)$</td>
<td>$2.2 \text{ V}$</td>
<td>8</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$3 \text{ V}$</td>
<td>10</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>$f_{(TAint)}$ Timer_A, clock frequency</td>
<td>SMCLK or ACLK signal selected</td>
<td>$2.2 \text{ V}$</td>
<td>8</td>
<td></td>
<td></td>
<td>MHz</td>
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<tr>
<td></td>
<td></td>
<td>$3 \text{ V}$</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**leakage current – Ports P1, P2, P5, and P6 (see Note 1)**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$V_{CC}$</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{kgi(Px,y)}$ Leakage current</td>
<td>Port Px</td>
<td>$V_{P(x,y)}$ (see Note 2)</td>
<td>$2.2 \text{ V}/3 \text{ V}$</td>
<td>±50</td>
<td></td>
<td>nA</td>
</tr>
</tbody>
</table>

**NOTES:**
1. The external signal sets the interrupt flag every time the minimum $t_{(int)}$ parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$.

- **leakage current**
  - The leakage current is measured with $V_{SS}$ or $V_{CC}$ applied to the corresponding pin(s), unless otherwise noted.
  - The port pin must be selected as input.
electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

outputs – Ports P1, P2, P5, and P6

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>VOH</strong></td>
<td><strong>High-level output voltage</strong></td>
<td>$I_{OH\text{(max)}} = -1.5, mA,\ V_{CC} = 2.2, V,\ $</td>
<td>$V_{CC} - 0.25\ V$</td>
<td></td>
<td>$V_{CC}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{OH\text{(max)}} = -6, mA,\ V_{CC} = 2.2, V,\ $</td>
<td>$V_{CC} - 0.6\ V$</td>
<td></td>
<td>$V_{CC}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{OH\text{(max)}} = -1.5, mA,\ V_{CC} = 3, V,\ $</td>
<td>$V_{CC} - 0.25\ V$</td>
<td></td>
<td>$V_{CC}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{OH\text{(max)}} = -6, mA,\ V_{CC} = 3, V,\ $</td>
<td>$V_{CC} - 0.6\ V$</td>
<td></td>
<td>$V_{CC}$</td>
</tr>
</tbody>
</table>

| **VOL**   | **Low-level output voltage** | $I_{OL\text{(max)}} = 1.5\, mA,\ V_{CC} = 2.2\, V,\ $ | $V_{SS}\ V$ | $V_{SS} + 0.25\ V$ | 
|           |                  | $I_{OL\text{(max)}} = 6\, mA,\ V_{CC} = 2.2\, V,\ $ | $V_{SS}\ V$ | $V_{SS} + 0.6\ V$ | 
|           |                  | $I_{OL\text{(max)}} = 1.5\, mA,\ V_{CC} = 3\, V,\ $ | $V_{SS}\ V$ | $V_{SS} + 0.25\ V$ | 
|           |                  | $I_{OL\text{(max)}} = 6\, mA,\ V_{CC} = 3\, V,\ $ | $V_{SS}\ V$ | $V_{SS} + 0.6\ V$ | 

NOTES:  
1. The maximum total current, $I_{OH\text{(max)}}$ and $I_{OL\text{(max)}}$, for all outputs combined, should not exceed $\pm 12\, mA$ to satisfy the maximum specified voltage drop.  
2. The maximum total current, $I_{OH\text{(max)}}$ and $I_{OL\text{(max)}}$, for all outputs combined, should not exceed $\pm 48\, mA$ to satisfy the maximum specified voltage drop.

output frequency

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{(P_{x,y})}$</td>
<td>$(x = 1, 2, 5, 6; 0 \leq y \leq 7)$</td>
<td>$C_L = 20, pF,$ $I_L = \pm 1.5, mA$</td>
<td>$V_{CC} = 2.2, V / 3, V$</td>
<td>$f_{\text{System}}$</td>
<td>MHz</td>
</tr>
<tr>
<td>$f_{(MCLK)}$</td>
<td>P1.1/TA0/MCLK</td>
<td>$C_L = 20, pF$</td>
<td>$f_{(MCLK)} = f_{(XT1)}$</td>
<td>40%</td>
<td>60%</td>
</tr>
<tr>
<td>$t_{(Xdc)}$</td>
<td>Duty cycle of output frequency</td>
<td>P1.1/TA0/MCLK, $C_L = 20, pF,$ $V_{CC} = 2.2, V / 3, V$</td>
<td>$f_{(MCLK)} = f_{(DCOCLK)}$</td>
<td>50%− 15 ns</td>
<td>50% 15 ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>50%+ 15 ns</td>
<td></td>
</tr>
</tbody>
</table>
electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

outputs – Ports P1, P2, P5, and P6 (continued)

![Graph of Typical Low-Level Output Current vs Low-Level Output Voltage](image1)

![Graph of Typical High-Level Output Current vs High-Level Output Voltage](image2)

![Graph of Typical Low-Level Output Current vs Low-Level Output Voltage](image3)

![Graph of Typical High-Level Output Current vs High-Level Output Voltage](image4)
wake-up LPM3

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{d\text{(LPM3)}} ) Delay time</td>
<td>( f = 1 \text{ MHz} )</td>
<td>( V_{\text{CC}} = 2.2 \text{ V/3 V} )</td>
<td>6</td>
<td></td>
<td>( \mu\text{s} )</td>
</tr>
<tr>
<td></td>
<td>( f = 2 \text{ MHz} )</td>
<td></td>
<td>6</td>
<td></td>
<td>( \mu\text{s} )</td>
</tr>
<tr>
<td></td>
<td>( f = 3 \text{ MHz} )</td>
<td></td>
<td>6</td>
<td></td>
<td>( \mu\text{s} )</td>
</tr>
</tbody>
</table>

RAM

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{RAMh}} )</td>
<td>CPU halted (see Note 1)</td>
<td>1.6</td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

**NOTE 1:** This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

LCD_A

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>VCC</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{CC(LCD)}} ) Supply Voltage Range</td>
<td>Charge pump enabled ( (\text{LCDCPEN} = 1; \ V_{\text{LCDCx}} &gt; \ 0000) )</td>
<td>2.2</td>
<td>3.6</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( C_{\text{LCD}} ) Capacitor on LCDCAP (see Note 1)</td>
<td>Charge pump enabled ( (\text{LCDCPEN} = 1; \ V_{\text{LCDCx}} &gt; 0000) )</td>
<td>4.7</td>
<td></td>
<td></td>
<td>( \mu\text{F} )</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{CC(LCD)}} ) Average Supply Current (see Note 2)</td>
<td>( V_{\text{CC(LCD)}} = 3 \text{ V}; \ \text{LCDCPEN} = 1; \ V_{\text{LCDCx}} = 1000, \text{ all segments on} ) ( I_{\text{LCLC}} = \frac{f_{ACLK}}{32} \text{ no LCD connected (see Note 3)} ) ( T_{A} = 25 \text{ °C} )</td>
<td>2.2</td>
<td>3.8</td>
<td></td>
<td>( \mu\text{A} )</td>
<td></td>
</tr>
<tr>
<td>( f_{\text{LCD}} ) LCD frequency</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.1</td>
<td>kHz</td>
</tr>
<tr>
<td>( V_{\text{LCD}} ) LCD voltage</td>
<td>( V_{\text{LCDCx}} = 0000 )</td>
<td></td>
<td></td>
<td></td>
<td>VCC</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{LCD}} ) LCD voltage</td>
<td>( V_{\text{LCDCx}} = 0001 )</td>
<td></td>
<td></td>
<td></td>
<td>2.60</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{LCD}} ) LCD voltage</td>
<td>( V_{\text{LCDCx}} = 0010 )</td>
<td></td>
<td></td>
<td></td>
<td>2.66</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{LCD}} ) LCD voltage</td>
<td>( V_{\text{LCDCx}} = 0011 )</td>
<td></td>
<td></td>
<td></td>
<td>2.72</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{LCD}} ) LCD voltage</td>
<td>( V_{\text{LCDCx}} = 0100 )</td>
<td></td>
<td></td>
<td></td>
<td>2.78</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{LCD}} ) LCD voltage</td>
<td>( V_{\text{LCDCx}} = 0101 )</td>
<td></td>
<td></td>
<td></td>
<td>2.84</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{LCD}} ) LCD voltage</td>
<td>( V_{\text{LCDCx}} = 0110 )</td>
<td></td>
<td></td>
<td></td>
<td>2.90</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{LCD}} ) LCD voltage</td>
<td>( V_{\text{LCDCx}} = 0111 )</td>
<td></td>
<td></td>
<td></td>
<td>2.96</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{LCD}} ) LCD voltage</td>
<td>( V_{\text{LCDCx}} = 1000 )</td>
<td></td>
<td></td>
<td></td>
<td>3.02</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{LCD}} ) LCD voltage</td>
<td>( V_{\text{LCDCx}} = 1001 )</td>
<td></td>
<td></td>
<td></td>
<td>3.08</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{LCD}} ) LCD voltage</td>
<td>( V_{\text{LCDCx}} = 1010 )</td>
<td></td>
<td></td>
<td></td>
<td>3.14</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{LCD}} ) LCD voltage</td>
<td>( V_{\text{LCDCx}} = 1011 )</td>
<td></td>
<td></td>
<td></td>
<td>3.20</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{LCD}} ) LCD voltage</td>
<td>( V_{\text{LCDCx}} = 1100 )</td>
<td></td>
<td></td>
<td></td>
<td>3.26</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{LCD}} ) LCD voltage</td>
<td>( V_{\text{LCDCx}} = 1101 )</td>
<td></td>
<td></td>
<td></td>
<td>3.32</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{LCD}} ) LCD voltage</td>
<td>( V_{\text{LCDCx}} = 1110 )</td>
<td></td>
<td></td>
<td></td>
<td>3.38</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{LCD}} ) LCD voltage</td>
<td>( V_{\text{LCDCx}} = 1111 )</td>
<td></td>
<td></td>
<td></td>
<td>3.44</td>
<td>3.60</td>
</tr>
<tr>
<td>( R_{\text{LCD}} ) LCD Driver Output impedance</td>
<td>( V_{\text{LCD}} = 3 \text{ V}; \ \text{LCDCPEN} = 1; \ V_{\text{LCDCx}} = 1000, \</td>
<td>I_{\text{LOAD}}</td>
<td>= \pm 10 \mu\text{A} )</td>
<td>2.2</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
1. Enabling the internal charge pump with an external capacitor smaller than the minimum specified might damage the device.
2. Refer to the supply current specifications \( I_{\text{LPM3}} \) for additional current specifications with the LCD_A module active.
3. Connecting an actual display will increase the current consumption depending on the size of the LCD.
electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

**POR/brownout reset (BOR) (see Note 1)**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_d(BOR)$</td>
<td></td>
<td>2000</td>
<td>μs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CC(start)}$</td>
<td>$dV_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 6)</td>
<td>0.7</td>
<td>$V_{(B.IT-)}$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V(B.IT-)$</td>
<td>$dV_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 6 through Figure 8)</td>
<td>1.71</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{hys(B.IT-)}$</td>
<td>$dV_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 6)</td>
<td>70</td>
<td>130</td>
<td>180</td>
<td>mV</td>
</tr>
<tr>
<td>$t_{(reset)}$</td>
<td>Pulse length needed at RST/NMI pin to accepted reset internally, $V_{CC} = 2.2 \text{ V/3 V}$</td>
<td>2</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
</tbody>
</table>

NOTES:
1. The current consumption of the brownout module is already included in the $I_{CC}$ current consumption data. The voltage level $V(B.IT-)$ + $V_{hys(B.IT-)}$ is $\leq 1.8\text{V}$.
2. During power up, the CPU begins code execution following a period of $t_d(BOR)$ after $V_{CC} = V(B.IT-)$ + $V_{hys(B.IT-)}$. The default FLL+ settings must not be changed until $V_{CC} \geq V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency. See the MSP430x4xx Family User’s Guide (SLAU056) for more information on the brownout.

**typical characteristics**

![Figure 6. POR/Brownout Reset (BOR) vs Supply Voltage](image-url)
electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

typical characteristics (continued)

Figure 7. \( V_{\text{CC(min)}} \) Level With a Square Voltage Drop to Generate a POR/Brownout Signal

Figure 8. \( V_{\text{CC(drop)}} \) Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal
### Electrical Characteristics Over Recommended Operating Free-Air Temperature

#### DCO

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>V&lt;sub&gt;CC&lt;/sub&gt;</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>f(DCOCLK)</td>
<td>N(DCO)=01Eh, FN_8=FN_4=FN_3=FN_2=0; DCOPLUS=0, f&lt;sub&gt;Crystal&lt;/sub&gt; = 32.768 kHz</td>
<td>2.2 V/3 V</td>
<td>1</td>
<td>1 MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>f(DCO=2)</td>
<td>FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1</td>
<td>2.2 V</td>
<td>0.3</td>
<td>0.65</td>
<td>1.25</td>
<td>MHz</td>
</tr>
<tr>
<td>f(DCO=2)</td>
<td>FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1</td>
<td>2.2 V</td>
<td>0.3</td>
<td>0.7</td>
<td>1.3</td>
<td>MHz</td>
</tr>
<tr>
<td>f(DCO=2)</td>
<td>FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1</td>
<td>2.2 V</td>
<td>0.8</td>
<td>1.5</td>
<td>2.5</td>
<td>MHz</td>
</tr>
<tr>
<td>f(DCO=2)</td>
<td>FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1</td>
<td>2.2 V</td>
<td>1.2</td>
<td>2</td>
<td>3</td>
<td>MHz</td>
</tr>
<tr>
<td>f(DCO=2)</td>
<td>FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1</td>
<td>2.2 V</td>
<td>2.5</td>
<td>5.6</td>
<td>10.5</td>
<td>MHz</td>
</tr>
<tr>
<td>f(DCO=2)</td>
<td>FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1</td>
<td>2.2 V</td>
<td>2.7</td>
<td>6.1</td>
<td>11.3</td>
<td>MHz</td>
</tr>
<tr>
<td>f(DCO=2)</td>
<td>FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1</td>
<td>2.2 V</td>
<td>3</td>
<td>6.5</td>
<td>12.1</td>
<td>20 MHz</td>
</tr>
<tr>
<td>f(DCO=2)</td>
<td>FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1</td>
<td>2.2 V</td>
<td>3</td>
<td>6.5</td>
<td>12.1</td>
<td>20 MHz</td>
</tr>
<tr>
<td>f(DCO=2)</td>
<td>FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1</td>
<td>2.2 V</td>
<td>5.7</td>
<td>10.8</td>
<td>18 MHz</td>
<td></td>
</tr>
<tr>
<td>f(DCO=2)</td>
<td>FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1</td>
<td>2.2 V</td>
<td>6.5</td>
<td>12.1</td>
<td>20 MHz</td>
<td></td>
</tr>
<tr>
<td>f(DCO=2)</td>
<td>FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1</td>
<td>2.2 V</td>
<td>1.3</td>
<td>2.2</td>
<td>3.5</td>
<td>MHz</td>
</tr>
<tr>
<td>f(DCO=2)</td>
<td>FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1</td>
<td>3</td>
<td>2.2</td>
<td>3.5</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>f(DCO=2)</td>
<td>FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1</td>
<td>3</td>
<td>2.2</td>
<td>3.5</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>f(DCO=2)</td>
<td>FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1</td>
<td>3</td>
<td>2.2</td>
<td>3.5</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>f(DCO=2)</td>
<td>FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1</td>
<td>3</td>
<td>2.2</td>
<td>3.5</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>f(DCO=2)</td>
<td>FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1</td>
<td>3</td>
<td>2.2</td>
<td>3.5</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>f(DCO=2)</td>
<td>FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1</td>
<td>3</td>
<td>2.2</td>
<td>3.5</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>f(DCO=2)</td>
<td>FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1</td>
<td>3</td>
<td>2.2</td>
<td>3.5</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>f(DCO=2)</td>
<td>FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1</td>
<td>3</td>
<td>2.2</td>
<td>3.5</td>
<td>MHz</td>
<td></td>
</tr>
</tbody>
</table>

#### Notes
- **Step Size Between Adjacent DCO Taps:**
  \[ S_n = \frac{f(DCO_{n+1})}{f(DCO_n)} \] (see Figure 10 for taps 21 to 27)
- **Temperature Drift:**
  \[ N(DCO) = 01Eh, FN_8=FN_4=FN_3=FN_2=0; D = 2; DCOPLUS = 0, (see Note 2) \]
- **Drift with V<sub>CC</sub> Variation:**

#### Figure 9: DCO Frequency vs Supply Voltage V<sub>CC</sub> and vs Ambient Temperature
electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Figure 10. DCO Tap Step Size

Figure 11. Five Overlapping DCO Ranges Controlled by FN_x Bits
electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

crystal oscillator, LFXT1 oscillator (see Notes 1 and 2)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>C(_{\text{XIN}})</td>
<td>Integrated input capacitance (see Note 4)</td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td>OSCCAP(<em>{\text{x}}) = 0h, V(</em>{\text{CC}}) = 2.2 V / 3 V</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>OSCCAP(<em>{\text{x}}) = 1h, V(</em>{\text{CC}}) = 2.2 V / 3 V</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>OSCCAP(<em>{\text{x}}) = 2h, V(</em>{\text{CC}}) = 2.2 V / 3 V</td>
<td>14</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>OSCCAP(<em>{\text{x}}) = 3h, V(</em>{\text{CC}}) = 2.2 V / 3 V</td>
<td>18</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>C(_{\text{XOUT}})</td>
<td>Integrated output capacitance (see Note 4)</td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
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<td>OSCCAP(<em>{\text{x}}) = 0h, V(</em>{\text{CC}}) = 2.2 V / 3 V</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>OSCCAP(<em>{\text{x}}) = 1h, V(</em>{\text{CC}}) = 2.2 V / 3 V</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>OSCCAP(<em>{\text{x}}) = 2h, V(</em>{\text{CC}}) = 2.2 V / 3 V</td>
<td>14</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>OSCCAP(<em>{\text{x}}) = 3h, V(</em>{\text{CC}}) = 2.2 V / 3 V</td>
<td>18</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V(_{\text{IL}})</td>
<td>Input levels at XIN</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>V(_{\text{CC}}) = 2.2 V/3 V (see Note 3)</td>
<td>V(_{\text{SS}})</td>
<td>0.2×V(_{\text{CC}})</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V(_{\text{IH}})</td>
<td>Input levels at XIN</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>V(_{\text{CC}}) = 2.2 V/3 V (see Note 3)</td>
<td>0.8×V(_{\text{CC}})</td>
<td>V(_{\text{CC}})</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTES:
1. The parasitic capacitance from the package and board may be estimated to be 2 pF. The effective load capacitor for the crystal is \((C_{\text{XIN}} \times C_{\text{XOUT}}) / (C_{\text{XIN}} + C_{\text{XOUT}})\). This is independent of XTS_FLL.
2. To improve EMI on the low-power LFXT1 oscillator, particularly in the LF mode (32 kHz), the following guidelines should be observed.
   - Keep as short of a trace as possible between the F42x0 and the crystal.
   - Design a good ground plane around the oscillator pins.
   - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
3. Applies only when using an external logic-level clock source. XTS_FLL must be set. Not applicable when using a crystal or resonator.
4. External capacitance is recommended for precision real-time clock applications; OSCCAP\(_{\text{x}}\) = 0h.
electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

### SD16_A, power supply and recommended operating conditions

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$V_{CC}$</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVCC</td>
<td>Analog supply voltage</td>
<td>$AV_{CC} = DV_{CC}$ $AV_{SS} = DV_{SS} = 0V$</td>
<td>2.5</td>
<td>3.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{SD16}$</td>
<td>Analog supply current including internal reference</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SD16LP = 0, $f_{SD16} = 1$ MHz, SD16OSR = 256</td>
<td>$SD16BUF_x = 00$; GAIN: 1,2</td>
<td>3 $V$</td>
<td>650</td>
<td>950</td>
<td></td>
<td>$\mu A$</td>
</tr>
<tr>
<td>SD16LP = 1, $f_{SD16} = 0.5$ MHz, SD16OSR = 256</td>
<td>$SD16BUF_x = 00$; GAIN: 1,2</td>
<td>3 $V$</td>
<td>800</td>
<td>1100</td>
<td></td>
<td>$\mu A$</td>
</tr>
<tr>
<td>SD16LP = 0, $f_{SD16} = 1$ MHz, SD16OSR = 256</td>
<td>$SD16BUF_x = 00$; GAIN: 1</td>
<td>3 $V$</td>
<td>620</td>
<td>930</td>
<td></td>
<td>$\mu A$</td>
</tr>
</tbody>
</table>

### SD16_A, input range

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$V_{CC}$</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{ID,FSR}$</td>
<td>Differential full scale input voltage range</td>
<td>Bipolar Mode, SD16UNI = 0</td>
<td>$-V_{REF}/2GAIN$</td>
<td>$+V_{REF}/2GAIN$</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>Unipolar Mode, SD16UNI = 1</td>
<td>0</td>
<td>$+V_{REF}/2GAIN$</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>$V_{ID}$</td>
<td>Differential input voltage range for specified performance (see Note 1)</td>
<td>SD16REFON = 1</td>
<td></td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>$SD16GAIN_x = 1$</td>
<td></td>
<td></td>
<td></td>
<td>500</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$SD16GAIN_x = 2$</td>
<td></td>
<td></td>
<td></td>
<td>250</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$SD16GAIN_x = 4$</td>
<td></td>
<td></td>
<td></td>
<td>125</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$SD16GAIN_x = 8$</td>
<td></td>
<td></td>
<td></td>
<td>62</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$SD16GAIN_x = 16$</td>
<td></td>
<td></td>
<td></td>
<td>31</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$SD16GAIN_x = 32$</td>
<td></td>
<td></td>
<td></td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>$Z_{I}$</td>
<td>Input impedance (one input pin to $AV_{SS}$)</td>
<td>$f_{SD16} = 1$ MHz, $SD16BUF_x = 00$</td>
<td>$SD16GAIN_x = 1$</td>
<td></td>
<td></td>
<td>k$\Omega$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>700</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{SD16} = 1$ MHz, $SD16BUF_x = 01$</td>
<td>$SD16GAIN_x = 1$</td>
<td></td>
<td></td>
<td>k$\Omega$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>$Z_{ID}$</td>
<td>Differential Input impedance (IN+ to IN–)</td>
<td>$f_{SD16} = 1$ MHz, $SD16BUF_x = 00$</td>
<td>$SD16GAIN_x = 1$</td>
<td></td>
<td></td>
<td>k$\Omega$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>300</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{SD16} = 1$ MHz, $SD16BUF_x &gt; 00$</td>
<td>$SD16GAIN_x = 1$</td>
<td></td>
<td></td>
<td>k$\Omega$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>$V_{I}$</td>
<td>Absolute input voltage range</td>
<td>$SD16BUF_x = 00$</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$AV_{SS} - 0.1V$</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$AV_{CC}$</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IC}$</td>
<td>Common-mode input voltage range</td>
<td>$SD16BUF_x = 00$</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$AV_{SS} - 0.1V$</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$AV_{CC}$</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

NOTES: 1. The analog input range depends on the reference voltage applied to $V_{REF}$. If $V_{REF}$ is sourced externally, the full-scale range is defined by $V_{FSR+} = +(V_{REF}/2)/GAIN$ and $V_{FSR–} = -(V_{REF}/2)/GAIN$. The analog input range should not exceed 80% of $V_{FSR+}$ or $V_{FSR–}$.
electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

**SD16_A, performance (fSD16 = 30kHz, SD16REFON = 1, SD16BUFx = 01)**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$V_{CC}$</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>SINAD</td>
<td>$f_{IN} = 2.8Hz$</td>
<td>3 V</td>
<td>84</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>$f_{IN} = 50Hz$, $f_{IN} = 100Hz$</td>
<td>3 V</td>
<td>84</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Nominal gain</td>
<td>SD16GAINx = 1; SD16OSRx = 1024</td>
<td>3 V</td>
<td>0.97</td>
<td>1.00</td>
<td>1.02</td>
<td></td>
</tr>
<tr>
<td>dG/dT</td>
<td>Gain temperature drift</td>
<td>3 V</td>
<td>15</td>
<td>ppm/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>dG/dVCC</td>
<td>Gain supply voltage drift</td>
<td>3 V</td>
<td>0.35</td>
<td>ppm/V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
1. Calculated using the box method: $(\text{MAX}(-40...85°C) − \text{MIN}(-40...85°C))/\text{MIN}(-40...85°C)/(85°C − (-40°C))$
2. Calculated using the box method: $(\text{MAX}(2.5...3.6V) − \text{MIN}(2.5...3.6V))/\text{MIN}(2.5...3.6V)/(3.6V − 2.5V)$

**SD16_A, performance (fSD16 = 1MHz, SD16OSRx = 256, SD16REFON = 1, SD16BUFx = 00)**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$V_{CC}$</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>SINAD</td>
<td>$f_{IN} = 50Hz$, $f_{IN} = 100Hz$</td>
<td>3 V</td>
<td>83.5</td>
<td>85</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>$f_{IN} = 50Hz$, $f_{IN} = 100Hz$</td>
<td>3 V</td>
<td>81.5</td>
<td>84</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>$f_{IN} = 50Hz$, $f_{IN} = 100Hz$</td>
<td>3 V</td>
<td>76</td>
<td>79.5</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>$f_{IN} = 50Hz$, $f_{IN} = 100Hz$</td>
<td>3 V</td>
<td>73</td>
<td>76.5</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>$f_{IN} = 50Hz$, $f_{IN} = 100Hz$</td>
<td>3 V</td>
<td>69</td>
<td>73</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>$f_{IN} = 50Hz$, $f_{IN} = 100Hz$</td>
<td>3 V</td>
<td>62</td>
<td>69</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>G</td>
<td>Nominal gain</td>
<td>3 V</td>
<td>0.97</td>
<td>1.00</td>
<td>1.02</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_{IN} = 50Hz$, $f_{IN} = 100Hz$</td>
<td>3 V</td>
<td>1.90</td>
<td>1.96</td>
<td>2.02</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_{IN} = 50Hz$, $f_{IN} = 100Hz$</td>
<td>3 V</td>
<td>3.76</td>
<td>3.86</td>
<td>3.96</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_{IN} = 50Hz$, $f_{IN} = 100Hz$</td>
<td>3 V</td>
<td>7.36</td>
<td>7.62</td>
<td>7.84</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_{IN} = 50Hz$, $f_{IN} = 100Hz$</td>
<td>3 V</td>
<td>14.56</td>
<td>15.04</td>
<td>15.52</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$f_{IN} = 50Hz$, $f_{IN} = 100Hz$</td>
<td>3 V</td>
<td>27.20</td>
<td>28.35</td>
<td>29.76</td>
<td></td>
</tr>
<tr>
<td>EOS</td>
<td>Offset error</td>
<td>3 V</td>
<td>±0.2</td>
<td>%FSR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>dEOS/dT</td>
<td>Offset error temperature coefficient</td>
<td>3 V</td>
<td>±4</td>
<td>ppm FSR/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-mode rejection ratio</td>
<td>3 V</td>
<td>&gt;90</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AC PSRR</td>
<td>AC power supply rejection ratio</td>
<td>3 V</td>
<td>&gt;80</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

### SD16_A, temperature sensor

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>Vcc</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>TC&lt;sub&gt;Sensor&lt;/sub&gt;</td>
<td>Sensor temperature coefficient</td>
<td></td>
<td>1.18</td>
<td>1.32</td>
<td>1.46</td>
<td>mV/K</td>
</tr>
<tr>
<td>V&lt;sub&gt;Offset,sensor&lt;/sub&gt;</td>
<td>Sensor offset voltage</td>
<td></td>
<td>−100</td>
<td>100</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>V&lt;sub&gt;sensor&lt;/sub&gt;</td>
<td>Sensor output voltage (see Note 2)</td>
<td>3 V</td>
<td>435</td>
<td>475</td>
<td>515</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>Temperature sensor voltage at TA = 85°C</td>
<td></td>
<td>3 V</td>
<td>355</td>
<td>395</td>
<td>435</td>
</tr>
<tr>
<td></td>
<td>Temperature sensor voltage at TA = 25°C</td>
<td></td>
<td>3 V</td>
<td>320</td>
<td>360</td>
<td>400</td>
</tr>
<tr>
<td></td>
<td>Temperature sensor voltage at TA = 0°C</td>
<td></td>
<td>3 V</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
1. The following formula can be used to calculate the temperature sensor output voltage:
   
   \[ V_{sensor,typ} = TCSensor \times (273 + T [°C]) + V_{offset,sensor} [mV] \]
2. Results based on characterization and/or production test, not TC<sub>Sensor</sub> or V<sub>offset,sensor</sub>.

### SD16_A, built-in voltage reference

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>Vcc</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;REF&lt;/sub&gt;</td>
<td>Internal reference voltage</td>
<td>3 V</td>
<td>1.14</td>
<td>1.20</td>
<td>1.26</td>
<td>V</td>
</tr>
<tr>
<td>I&lt;sub&gt;REF&lt;/sub&gt;</td>
<td>Reference supply current</td>
<td>3 V</td>
<td>175</td>
<td>260</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>TC</td>
<td>Temperature coefficient</td>
<td>3 V</td>
<td>18</td>
<td>50</td>
<td></td>
<td>ppm/K</td>
</tr>
<tr>
<td>C&lt;sub&gt;REF&lt;/sub&gt;</td>
<td>V&lt;sub&gt;REF&lt;/sub&gt; load capacitance</td>
<td>100</td>
<td></td>
<td></td>
<td></td>
<td>nF</td>
</tr>
<tr>
<td>I&lt;sub&gt;LOAD&lt;/sub&gt;</td>
<td>V&lt;sub&gt;REF&lt;/sub&gt;(O) maximum load current</td>
<td>3 V</td>
<td>±200</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>t&lt;sub&gt;ON&lt;/sub&gt;</td>
<td>Turn on time</td>
<td>3 V</td>
<td>5</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>DC PSR</td>
<td>DC power supply rejection, ( ΔV_{REF}/ΔV_{CC} )</td>
<td>3 V</td>
<td>100</td>
<td></td>
<td></td>
<td>uV/V</td>
</tr>
</tbody>
</table>

**NOTES:**
1. There is no capacitance required on V<sub>REF</sub>. However, a capacitance of at least 100nF is recommended to reduce any reference voltage noise.

### SD16_A, reference output buffer

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>Vcc</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;REF,BUF&lt;/sub&gt;</td>
<td>Reference buffer output voltage</td>
<td>3 V</td>
<td>1.2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>I&lt;sub&gt;REF,BUF&lt;/sub&gt;</td>
<td>Reference Supply + Reference output buffer quiescent current</td>
<td>3 V</td>
<td>385</td>
<td>600</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>C&lt;sub&gt;REF(O)&lt;/sub&gt;</td>
<td>Required load capacitance on V&lt;sub&gt;REF&lt;/sub&gt;</td>
<td>470</td>
<td></td>
<td></td>
<td></td>
<td>nF</td>
</tr>
<tr>
<td>I&lt;sub&gt;LOAD,Max&lt;/sub&gt;</td>
<td>Maximum load current on V&lt;sub&gt;REF&lt;/sub&gt;</td>
<td>3 V</td>
<td>±1</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Maximum voltage variation vs. load current</td>
<td>3 V</td>
<td>−15</td>
<td>15</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>t&lt;sub&gt;ON&lt;/sub&gt;</td>
<td>Turn on time</td>
<td>3 V</td>
<td>100</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
</tbody>
</table>
### SD16_A, external reference input

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>V&lt;sub&gt;CC&lt;/sub&gt;</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;REF(I)&lt;/sub&gt;</td>
<td>Input voltage range</td>
<td>SD16REFON = 0</td>
<td>3 V</td>
<td>1.0</td>
<td>1.25</td>
<td>1.5</td>
</tr>
<tr>
<td>I&lt;sub&gt;REF(I)&lt;/sub&gt;</td>
<td>Input current</td>
<td>SD16REFON = 0</td>
<td>3 V</td>
<td>50</td>
<td></td>
<td>nA</td>
</tr>
</tbody>
</table>
electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, supply specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$V_{CC}$</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$AV_{CC}$</td>
<td>Analog supply voltage $AV_{CC} = DV_{CC}$, $AV_{SS} = DV_{SS} = 0$ V</td>
<td>2.20</td>
<td>3.60</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{DD}$</td>
<td>Supply Current $DAC12_{AMPx}=2$, $DAC12IR=0$, $DAC12_{xDAT}=0800h$</td>
<td>2.2V/3V</td>
<td>50</td>
<td>110</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>$DAC12_{AMPx}=2$, $DAC12IR=1$, $DAC12_{xDAT}=0800h$, $V_{REF,DAC12} = AV_{CC}$</td>
<td>2.2V/3V</td>
<td>50</td>
<td>110</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>$DAC12_{AMPx}=5$, $DAC12IR=1$, $DAC12_{xDAT}=0800h$, $V_{REF,DAC12} = AV_{CC}$</td>
<td>2.2V/3V</td>
<td>200</td>
<td>440</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>$DAC12_{AMPx}=7$, $DAC12IR=1$, $DAC12_{xDAT}=0800h$, $V_{REF,DAC12} = AV_{CC}$</td>
<td>2.2V/3V</td>
<td>700</td>
<td>1500</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>$PSRR$</td>
<td>Power supply rejection ratio $DAC12_{xDAT} = 800h$, $V_{REF,DAC12} = 1.2V$ $\Delta AV_{CC} = 100mV$</td>
<td>2.7V</td>
<td>70</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>

NOTES:  
1. No load at the output pin assuming that the control bits for the shared pins are set properly.  
2. Current into reference terminals not included. If $DAC12IR = 1$ current flows through the input divider; see Reference Input specifications.  
3. $PSRR = 20^{\log}(\Delta AV_{CC}/\Delta V_{DAC12_{xOUT}})$.  
4. $V_{REF}$ is applied externally. The internal reference is not used.
electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

### 12-bit DAC, linearity specifications (see Figure 12)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$V_{CC}$</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>(12-bit Monotonic)</td>
<td>2.7V</td>
<td>±2.0</td>
<td>±8.0</td>
<td>LSB</td>
<td></td>
</tr>
<tr>
<td>INL</td>
<td>Integral nonlinearity (see Note 1)</td>
<td>$V_{REF,DAC12} = 1.2V$</td>
<td>DAC12AMPx = 7, DAC12IR = 1</td>
<td>2.7V</td>
<td>±20</td>
<td>mV</td>
</tr>
<tr>
<td>DNL</td>
<td>Differential nonlinearity (see Note 1)</td>
<td>$V_{REF,DAC12} = 1.2V$</td>
<td>DAC12AMPx = 7, DAC12IR = 1</td>
<td>2.7V</td>
<td>±2.5</td>
<td></td>
</tr>
<tr>
<td>$E_O$</td>
<td>Offset voltage w/o calibration (see Notes 1, 2)</td>
<td>$V_{REF,DAC12} = 1.2V$</td>
<td>DAC12AMPx = 7, DAC12IR = 1</td>
<td>2.7V</td>
<td>±30</td>
<td>μV/C</td>
</tr>
<tr>
<td>$dE_O/dT$</td>
<td>Offset error temperature coefficient (see Note 1)</td>
<td>2.7V</td>
<td>10</td>
<td>ppm of FSR/C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$E_G$</td>
<td>Gain error (see Note 1)</td>
<td>$V_{REF,DAC12} = 1.2V$</td>
<td>2.7V</td>
<td>±3.50</td>
<td>% FSR</td>
<td></td>
</tr>
<tr>
<td>$dE_G/dT$</td>
<td>Gain temperature coefficient (see Note 1)</td>
<td>2.7V</td>
<td>10</td>
<td>ppm of FSR/C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{Offset_Cal}$</td>
<td>Time for offset calibration (see Note 3)</td>
<td>DAC12AMPx=2</td>
<td>2.7V</td>
<td>100</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DAC12AMPx=3,5</td>
<td>2.7V</td>
<td>32</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DAC12AMPx=4,6,7</td>
<td>2.7V</td>
<td>6</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
1. Parameters calculated from the best-fit curve from 0x0A to 0xFFF. The best-fit curve method is used to deliver coefficients “a” and “b” of the first order equation: $y = a + b \cdot x$. $V_{DAC12_{xOUT}} = E_O + (1 + E_G) \cdot (V_{REF,DAC12/4095}) \cdot DAC12_{xDAT}$, DAC12IR = 1.
2. The offset calibration works on the output operational amplifier. Offset Calibration is triggered setting bit DAC12CALON.
3. The offset calibration can be done if DAC12AMPx = {2, 3, 4, 5, 6, 7}. The output operational amplifier is switched off with DAC12AMPx = {0, 1}. It is recommended that the DAC12 module be configured prior to initiating calibration. Port activity during calibration may affect accuracy and is not recommended.

![Diagram of DAC Output](image)

**Figure 12. Linearity Test Load Conditions and Gain/Offset Definition**
electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, linearity specifications (continued)

![TYPICAL INL ERROR vs DIGITAL INPUT DATA](image)

![TYPICAL DNL ERROR vs DIGITAL INPUT DATA](image)
### 12-bit DAC, output specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>V(_{CC})</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_O) Output voltage range (see Note 1, Figure 15)</td>
<td>No Load, (V_{REF(DAC12)} = AV_{CC}), (DAC12_x,D,A,T = 0h), (DAC12RIR = 1), (DAC12_A,M,P,x = 7)</td>
<td>2.2V/3V</td>
<td>0</td>
<td>0.005</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>No Load, (V_{REF(DAC12)} = AV_{CC}), (DAC12_x,D,A,T = 0FF,h), (DAC12,R,I,R = 1), (DAC12_A,M,P,x = 7)</td>
<td>2.2V/3V</td>
<td>AV(_{CC})−0.05</td>
<td>AV(_{CC})</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(R_{Load} = 3,k\Omega), (V_{REF(DAC12)} = AV_{CC}), (DAC12_x,D,A,T = 0h), (DAC12RIR = 1), (DAC12_A,M,P,x = 7)</td>
<td>2.2V/3V</td>
<td>0</td>
<td>0.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(R_{Load} = 3,k\Omega), (V_{REF(DAC12)} = AV_{CC}), (DAC12_x,D,A,T = 0FF,h), (DAC12_R,I,R = 1), (DAC12_A,M,P,x = 7)</td>
<td>2.2V/3V</td>
<td>AV(_{CC})−0.13</td>
<td>AV(_{CC})</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(C_{L,(DAC12)}) Max DAC12 load capacitance</td>
<td></td>
<td>2.2V/3V</td>
<td>100</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>(I_{L,(DAC12)}) Max DAC12 load current</td>
<td>(R_{Load} = 3,k\Omega), (V_{O/P(DAC12)} &lt; 0.3,V), (DAC12_A,M,P,x = 2), (DAC12_x,D,A,T = 0h)</td>
<td>2.2V/3V</td>
<td>−0.5</td>
<td>+0.5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>(R_{Load} = 3,k\Omega), (V_{O/P(DAC12)} = AV_{CC}−0.3,V), (DAC12_x,D,A,T = 0FF,h)</td>
<td>3V</td>
<td>−1.0</td>
<td>+1.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(R_{O/P(DAC12)}) Output Resistance (see Figure 15)</td>
<td>(R_{Load} = 3,k\Omega), (\min,I_{Load} = 1,mA), (V_{O/P(DAC12)} = AV_{CC}−0.3,V), (DAC12_x,D,A,T = 0FF,h)</td>
<td>2.2V/3V</td>
<td>150</td>
<td>250</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>(R_{Load} = 3,k\Omega), (0.3,V ≤ V_{O/P(DAC12)} ≤ AV_{CC}−0.3,V), (DAC12_x,D,A,T = 0FF,h)</td>
<td>2.2V/3V</td>
<td>1</td>
<td>4</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
1. Data is valid after the offset calibration of the output amplifier.

---

**Figure 15. DAC12\_x Output Resistance Tests**
electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

### 12-bit DAC, reference input specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>VCC</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{REF}$</td>
<td>Reference input voltage range</td>
<td>$2.2V/3V$</td>
<td>$AV_{CC}/0.2$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_i(V_{REF})$</td>
<td>Reference input resistance</td>
<td>$2.2V/3V$</td>
<td>$40/48/56$</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
</tbody>
</table>

**NOTES:**
1. For a full-scale output, the reference input voltage can be as high as $1/3$ of the maximum output voltage swing ($AV_{CC}$).
2. The maximum voltage applied at reference input voltage terminal $V_{REF} = [AV_{CC} - V_{EO}] / [3*(1 + EG)]$.
3. For a full-scale output, the reference input voltage can be as high as the maximum output voltage swing ($AV_{CC}$).
4. The maximum voltage applied at reference input voltage terminal $V_{REF} = [AV_{CC} - V_{EO}] / (1 + EG)$.

### 12-bit DAC, dynamic specifications; $V_{REF,DAC12} = AV_{CC}$, $DAC12IR = 1$ (see Figure 16 and Figure 17)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>VCC</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{ON}$</td>
<td>DAC12 on-time</td>
<td>$2.2V/3V$</td>
<td>$60/120$</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>$I_{S(FS)}$</td>
<td>Settling time, full-scale</td>
<td>$2.2V/3V$</td>
<td>$100/200$</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>$I_{S(C-C)}$</td>
<td>Settling time, code to code</td>
<td>$2.2V/3V$</td>
<td>$0.05/0.12$</td>
<td></td>
<td></td>
<td>nV-s</td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate</td>
<td>$2.2V/3V$</td>
<td>$0.05/0.12$</td>
<td></td>
<td></td>
<td>V/μs</td>
</tr>
<tr>
<td>Glitch energy: full-scale</td>
<td>$2.2V/3V$</td>
<td>$10$</td>
<td></td>
<td></td>
<td></td>
<td>nV-s</td>
</tr>
</tbody>
</table>

**NOTES:**
1. $R_{Load}$ and $C_{Load}$ connected to $AV_{SS}$ (not $AV_{CC}/2$) in Figure 16.
2. Slew rate applies to output voltage steps $\geq 200$mV.

---

**Figure 16.** Settling Time and Glitch Energy Testing
electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

![Slew Rate Testing](image)

**Figure 17. Slew Rate Testing**

12-bit DAC, dynamic specifications continued (T<sub>A</sub> = 25°C unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>V&lt;sub&gt;CC&lt;/sub&gt;</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>BW&lt;sub&gt;3 dB&lt;/sub&gt;</td>
<td>3-dB bandwidth, V&lt;sub&gt;DC&lt;/sub&gt;=1.5V, V&lt;sub&gt;AC&lt;/sub&gt;=0.1V&lt;sub&gt;PP&lt;/sub&gt; (see Figure 18)</td>
<td>2.2V/3V</td>
<td>40</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td>DAC12AMP&lt;sub&gt;x&lt;/sub&gt; = {2, 3, 4}, DAC12SREF&lt;sub&gt;x&lt;/sub&gt; = 2, DAC12IR = 1, DAC12_xDAT = 800h</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>DAC12AMP&lt;sub&gt;x&lt;/sub&gt; = {5, 6}, DAC12SREF&lt;sub&gt;x&lt;/sub&gt; = 2, DAC12IR = 1, DAC12_xDAT = 800h</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>DAC12AMP&lt;sub&gt;x&lt;/sub&gt; = 7, DAC12SREF&lt;sub&gt;x&lt;/sub&gt; = 2, DAC12IR = 1, DAC12_xDAT = 800h</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
1. R<sub>LOAD</sub> = 3 kΩ, C<sub>LOAD</sub> = 100 pF

![Test Conditions for 3-dB Bandwidth Specification](image)

**Figure 18. Test Conditions for 3-dB Bandwidth Specification**
electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

### Flash Memory

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>Vcc</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC(PGM/ERASE)</td>
<td>Program and Erase supply voltage</td>
<td></td>
<td>2.5</td>
<td>3.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>fFTG</td>
<td>Flash Timing Generator frequency</td>
<td></td>
<td>257</td>
<td>476</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>IPGM</td>
<td>Supply current from DVCC during program</td>
<td></td>
<td>2.5V/3.6V</td>
<td>3</td>
<td>5</td>
<td>mA</td>
</tr>
<tr>
<td>IERASE</td>
<td>Supply current from DVCC during erase</td>
<td></td>
<td>2.5V/3.6V</td>
<td>3</td>
<td>7</td>
<td>mA</td>
</tr>
<tr>
<td>tCPT</td>
<td>Cumulative program time</td>
<td></td>
<td>2.5V/3.6V</td>
<td>10</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>tCMerase</td>
<td>Cumulative mass erase time</td>
<td></td>
<td>2.5V/3.6V</td>
<td>200</td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>tRetention</td>
<td>Program/Erase endurance</td>
<td></td>
<td>10^4</td>
<td>10^5</td>
<td>cycles</td>
<td></td>
</tr>
<tr>
<td>tWord</td>
<td>Word or byte program time</td>
<td></td>
<td></td>
<td>35</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tBlock, 0</td>
<td>Block program time for 1st byte or word</td>
<td></td>
<td></td>
<td>30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tBlock, 1-63</td>
<td>Block program time for each additional byte or word</td>
<td></td>
<td></td>
<td>21</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tBlock, End</td>
<td>Block program end-sequence wait time</td>
<td></td>
<td></td>
<td>6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tMass Erase</td>
<td>Mass erase time</td>
<td></td>
<td></td>
<td>5297</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tSeg Erase</td>
<td>Segment erase time</td>
<td></td>
<td></td>
<td>4819</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. The mass erase duration generated by the flash timing generator is at least 11.1ms ( = 5297x1/f_{FTG, max} = 5297x1/476kHz). To achieve the required cumulative mass erase time the Flash Controller’s mass erase operation can be repeated until this time is met. (A worst case minimum of 19 cycles are required).
3. These values are hardwired into the Flash Controller’s state machine (t_{FTG} = 1/f_{FTG}).

### JTAG Interface

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>Vcc</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>fTCK</td>
<td>TCK input frequency</td>
<td></td>
<td>2.2 V</td>
<td>0</td>
<td>5</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3 V</td>
<td>0</td>
<td>10</td>
<td>MHz</td>
</tr>
<tr>
<td>RInternal</td>
<td>Internal pull-up resistance on TMS, TCK, TDI/TCLK</td>
<td></td>
<td>2.2 V</td>
<td>25</td>
<td>60</td>
<td>90</td>
</tr>
</tbody>
</table>

**NOTES:**
1. fTCK may be restricted to meet the timing requirements of the module selected.
2. TMS, TDI/TCLK, and TCK pull-up resistors are implemented in all versions.

### JTAG Fuse (see Note 1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>Vcc</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC(FB)</td>
<td>Supply voltage during fuse-blow condition</td>
<td>T_A = 25°C</td>
<td>2.5</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_FB</td>
<td>Voltage level on TDI/TCLK for fuse-blow: F versions</td>
<td></td>
<td>6</td>
<td>7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I_FB</td>
<td>Supply current into TDI/TCLK during fuse blow</td>
<td></td>
<td>100</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>tFB</td>
<td>Time to blow fuse</td>
<td></td>
<td>1</td>
<td></td>
<td>ms</td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
1. Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.
input/output schematics

Port P1 pin schematic: P1.0, P1.1, input/output with Schmitt–trigger

Port P1 (P1.0, P1.1) pin functions

<table>
<thead>
<tr>
<th>PIN NAME (P1.X)</th>
<th>X</th>
<th>FUNCTION</th>
<th>CONTROL BITS / SIGNALS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>P1DIR.x</td>
</tr>
<tr>
<td>P1.0/TA0</td>
<td>0</td>
<td>P1.0† Input/Output</td>
<td>0/1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Timer_A3.CC10A</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Timer_A3.TA0</td>
<td>1</td>
</tr>
<tr>
<td>P1.1/TA0/MCLK</td>
<td>1</td>
<td>P1.1† Input/Output</td>
<td>0/1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Timer_A3.CC10B</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MCLK</td>
<td>1</td>
</tr>
</tbody>
</table>

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don’t care.
Port P1 pin schematic: P1.2, input/output with Schmitt-trigger and analog functions

**Port P1 (P1.2) pin functions**

<table>
<thead>
<tr>
<th>PIN NAME (P1.X)</th>
<th>X</th>
<th>FUNCTION</th>
<th>CONTROL BITS / SIGNALS</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1.2/TA1/A4−</td>
<td>2</td>
<td>P1.2† Input/Output</td>
<td>P1DIR.x  P1SEL.x SD16AE.x</td>
</tr>
<tr>
<td>Timer_A3.CCI1A</td>
<td>1</td>
<td>Timer_A3.CCI1A</td>
<td>0 1 0</td>
</tr>
<tr>
<td>Timer_A3.TA1</td>
<td>X</td>
<td>Timer_A3.TA1</td>
<td>1 1 0</td>
</tr>
<tr>
<td>A4− (see Notes 3, 4)</td>
<td>X</td>
<td>A4− (see Notes 3, 4)</td>
<td>X X 1</td>
</tr>
</tbody>
</table>

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don’t care.
3. Setting the SD16AE.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
4. Negative input to SD16_A (A4−) connected to VSS if corresponding SD16AE.x bit is cleared.
Port P1 pin schematic: P1.3, P1.5, P1.7, input/output with Schmitt–trigger and analog functions

INCH=y

Ay+

SD16AE.x

P1DIR.x

0
1

Direction

0: Input
1: Output

Module X OUT

P1OUT.x

1
0

Module X IN

P1IN.x

P1SEL.x

Interrupt

Edge

Select

Pad Logic

P1.3/TA2/A4+
P1.5/TACLK/ACLK/A3+
P1.7/A2+

Note: x = 3, 5, 7
y = 4, 3, 2
## Port P1 (P1.3, P1.5, P1.7) pin functions

<table>
<thead>
<tr>
<th>PIN NAME (P1.X)</th>
<th>X</th>
<th>FUNCTION</th>
<th>CONTROL BITS / SIGNALS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>P1DIR.x</td>
</tr>
<tr>
<td>P1.3/TA2/A4+</td>
<td>3</td>
<td>P1.3† Input/Output</td>
<td>0/1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Timer_A3.CCI2A</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Timer_A3.TA2</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A4+ (see Note 3)</td>
<td>X</td>
</tr>
<tr>
<td>P1.5/TACLK/ACLK/A3+</td>
<td>5</td>
<td>P1.5† Input/Output</td>
<td>0/1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Timer_A3.TACLK/INCLK</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ACLK</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A3+ (see Note 3)</td>
<td>X</td>
</tr>
<tr>
<td>P1.7/A2+</td>
<td>7</td>
<td>P1.5† Input/Output</td>
<td>0/1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>N/A</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DVSS</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A2+ (see Note 3)</td>
<td>X</td>
</tr>
</tbody>
</table>

† Default after reset (PUC/POR)

NOTES:
1. N/A: Not available or not applicable.
2. X: Don’t care.
3. Setting the SD16AE.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
Port P1 pin schematic: P1.4, input/output with Schmitt–trigger and analog functions

Port P1 (P1.4) pin functions

<table>
<thead>
<tr>
<th>PIN NAME (P1.X)</th>
<th>X</th>
<th>FUNCTION</th>
<th>CONTROL BITS / SIGNALS</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1.4/A3−/DAC0</td>
<td>4</td>
<td>P1.4† Input/Output</td>
<td>P1DIR.x</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0/1</td>
<td>0/1</td>
</tr>
<tr>
<td>N/A</td>
<td></td>
<td>0/1</td>
<td>0/1</td>
</tr>
<tr>
<td>DVSS</td>
<td></td>
<td>1</td>
<td>1/0</td>
</tr>
<tr>
<td>A3− (see Notes 3, 4)</td>
<td></td>
<td>X</td>
<td>X/1</td>
</tr>
<tr>
<td>DAC0 (see Note 5)</td>
<td></td>
<td>X</td>
<td>X/1</td>
</tr>
</tbody>
</table>

† Default after reset (PUC/POR)

NOTES:
1. N/A: Not available or not applicable.
2. X: Don't care.
3. Setting the SD16AE.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
4. Negative input to SD16_A (A3−) connected to AVSS if corresponding SD16AE.x bit is cleared.
5. Setting the DAC12OPS bit also disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
Port P1 pin schematic: P1.6, input/output with Schmitt-trigger and analog functions

Port P1 (P1.6) pin functions

<table>
<thead>
<tr>
<th>PIN NAME (P1.X)</th>
<th>X</th>
<th>FUNCTION</th>
<th>CONTROL BITS / SIGNALS</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1.6/A2−</td>
<td>6</td>
<td>P1.6† Input/Output</td>
<td>P1DIR.x</td>
</tr>
<tr>
<td></td>
<td></td>
<td>N/A</td>
<td>0/1</td>
</tr>
<tr>
<td>DVSS</td>
<td></td>
<td>DVSS</td>
<td>1</td>
</tr>
<tr>
<td>A2− (see Notes 3, 4)</td>
<td></td>
<td>A2−</td>
<td>X</td>
</tr>
</tbody>
</table>

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don’t care.
3. Setting the SD16AE.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
4. Negative input to SD16_A (A2−) connected to AVSS if corresponding SD16AE.x bit is cleared.
Port P2 pin schematic: P2.0 to P2.7, input/output with Schmitt–trigger, LCD and analog functions

Note: x = 0 to 7
    y = 13 to 6
## Port P2 (P2.0 to P2.7) pin functions

<table>
<thead>
<tr>
<th>PIN NAME (P2.X)</th>
<th>X</th>
<th>FUNCTION</th>
<th>CONTROL BITS / SIGNALS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>P2DIR.x</td>
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<tr>
<td>P2.0/S13</td>
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<td>P2.0† Input/Output</td>
<td>0/1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>N/A</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DVSS</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>S13</td>
<td>X</td>
</tr>
<tr>
<td>P2.1/S12</td>
<td>1</td>
<td>P2.1† Input/Output</td>
<td>0/1</td>
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<tr>
<td></td>
<td></td>
<td>N/A</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DVSS</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>S12</td>
<td>X</td>
</tr>
<tr>
<td>P2.2/S11</td>
<td>2</td>
<td>P2.2† Input/Output</td>
<td>0/1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>N/A</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DVSS</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>S11</td>
<td>X</td>
</tr>
<tr>
<td>P2.3/S10</td>
<td>3</td>
<td>P2.3† Input/Output</td>
<td>0/1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>N/A</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DVSS</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>S10</td>
<td>X</td>
</tr>
<tr>
<td>P2.4/S9</td>
<td>4</td>
<td>P2.4† Input/Output</td>
<td>0/1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>N/A</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DVSS</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>S9</td>
<td>X</td>
</tr>
<tr>
<td>P2.5/S8</td>
<td>5</td>
<td>P2.5† Input/Output</td>
<td>0/1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>N/A</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DVSS</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>S8</td>
<td>X</td>
</tr>
<tr>
<td>P2.6/S7</td>
<td>6</td>
<td>P2.6† Input/Output</td>
<td>0/1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>N/A</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DVSS</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>S7</td>
<td>X</td>
</tr>
<tr>
<td>P2.7/S6</td>
<td>7</td>
<td>P2.7† Input/Output</td>
<td>0/1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>N/A</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DVSS</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>S6</td>
<td>X</td>
</tr>
</tbody>
</table>

† Default after reset (PUC/POR)

NOTES:
1. N/A: Not available or not applicable.
2. X: Don’t care.
Port P5 pin schematic: P5.0, P5.1, P5.5 to P5.7, input/output with Schmitt−trigger and LCD functions

Note: x = 0, 1, 5, 6, 7
y = 1, 0, 2, 3, 4
Port P5 (P5.0, P5.1, P5.5, P5.6) pin functions

<table>
<thead>
<tr>
<th>PIN NAME (P5.X)</th>
<th>X</th>
<th>FUNCTION</th>
<th>CONTROL BITS / SIGNALS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>P5DIR.x</td>
</tr>
<tr>
<td>P5.0/S1</td>
<td>0</td>
<td>P5.0† Input/Output</td>
<td>0/1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>N/A</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DVSS</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>S1</td>
<td>X</td>
</tr>
<tr>
<td>P5.1/S0</td>
<td>1</td>
<td>P5.1† Input/Output</td>
<td>0/1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>N/A</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DVSS</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>S0</td>
<td>X</td>
</tr>
<tr>
<td>P5.5/S2</td>
<td>5</td>
<td>P5.5† Input/Output</td>
<td>0/1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>N/A</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DVSS</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>S2</td>
<td>X</td>
</tr>
<tr>
<td>P5.6/S3</td>
<td>6</td>
<td>P5.6† Input/Output</td>
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<td></td>
<td></td>
<td>N/A</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DVSS</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>S3</td>
<td>X</td>
</tr>
</tbody>
</table>

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
        2. X: Don’t care.

Port P5 (P5.7) pin functions

<table>
<thead>
<tr>
<th>PIN NAME (P5.X)</th>
<th>X</th>
<th>FUNCTION</th>
<th>CONTROL BITS / SIGNALS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>P5DIR.x</td>
</tr>
<tr>
<td>P5.7/S4</td>
<td>7</td>
<td>P5.7† Input/Output</td>
<td>0/1</td>
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<tr>
<td></td>
<td></td>
<td>N/A</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DVSS</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>S4</td>
<td>X</td>
</tr>
</tbody>
</table>

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
        2. X: Don’t care.
Port P5 pin schematic: P5.2 to P5.4, input/output with Schmitt–trigger and LCD functions

Note: x = 2 to 4

Port P5 (P5.2 to P5.4) pin functions

<table>
<thead>
<tr>
<th>PIN NAME (P5.X)</th>
<th>X</th>
<th>FUNCTION</th>
<th>CONTROL BITS / SIGNALS</th>
</tr>
</thead>
<tbody>
<tr>
<td>P5.2/COM1</td>
<td>2</td>
<td>P5.2† Input/Output</td>
<td>P5DIR.x</td>
</tr>
<tr>
<td></td>
<td></td>
<td>COM1</td>
<td>0/1</td>
</tr>
<tr>
<td>P5.3/COM2</td>
<td>3</td>
<td>P5.3† Input/Output</td>
<td>P5DIR.x</td>
</tr>
<tr>
<td></td>
<td></td>
<td>COM2</td>
<td>0/1</td>
</tr>
<tr>
<td>P5.4/COM3</td>
<td>4</td>
<td>P5.4† Input/Output</td>
<td>P5DIR.x</td>
</tr>
<tr>
<td></td>
<td></td>
<td>COM3</td>
<td>0/1</td>
</tr>
</tbody>
</table>

† Default after reset (PUC/POR)

NOTES:
1. N/A: Not available or not applicable.
2. X: Don’t care.
Port P6 pin schematic: P6.0, P6.2, input/output with Schmitt–trigger and analog functions

Note: x = 0, 2
y = 0, 1
#Signal from or to SD16

Port P6 (P6.0, P6.2) pin functions

<table>
<thead>
<tr>
<th>PIN NAME (P6.X)</th>
<th>X</th>
<th>FUNCTION</th>
<th>CONTROL BITS / SIGNALS</th>
</tr>
</thead>
<tbody>
<tr>
<td>P6.0/A0+</td>
<td>0</td>
<td>P6.0† Input/Output</td>
<td>P6DIR.x</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A0+ (see Note 3)</td>
<td>0/1</td>
</tr>
<tr>
<td>P6.2/A1+</td>
<td>2</td>
<td>P6.2† Input/Output</td>
<td>P6DIR.x</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A1+ (see Note 3)</td>
<td>0/1</td>
</tr>
</tbody>
</table>

† Default after reset (PUC/POR)

NOTES:  1. N/A: Not available or not applicable.
        2. X: Don’t care.
        3. Setting the P6SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
Port P6 pin schematic: P6.1, P6.3, input/output with Schmitt–trigger and analog functions

Note: x = 1,3  
y = 0,1  
†Signal from or to SD16

Port P6 (P6.1, P6.3) pin functions

<table>
<thead>
<tr>
<th>PIN NAME (P6.X)</th>
<th>X</th>
<th>FUNCTION</th>
<th>CONTROL BITS / SIGNALS</th>
</tr>
</thead>
<tbody>
<tr>
<td>P6.1/A0−</td>
<td>1</td>
<td>P6.1† Input/Output</td>
<td>0/1 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A0− (see Note 3)</td>
<td>0/1 0</td>
</tr>
<tr>
<td>P6.3/A1−</td>
<td>3</td>
<td>P6.3† Input/Output</td>
<td>0/1 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A1− (see Note 3)</td>
<td>0/1 0</td>
</tr>
</tbody>
</table>

† Default after reset (PUC/POR)  
NOTES: 1. N/A: Not available or not applicable.  
2. X: Don’t care.  
3. Setting the P6SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
Port P6 pin schematic: P6.4 to P6.7, input/output with Schmitt-trigger and analog functions

**Note:** x = 4 to 7

**Port P6 (P6.4 to P6.7) pin functions**

<table>
<thead>
<tr>
<th>PIN NAME (P6.X)</th>
<th>X</th>
<th>FUNCTION</th>
<th>CONTROL BITS / SIGNALS</th>
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<tr>
<td>P6.4</td>
<td>4</td>
<td>P6.4† Input/Output</td>
<td>P6DIR.x 0/1 P6SEL.x 0</td>
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<td></td>
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<td>P6.5</td>
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<td>P6DIR.x 0/1 P6SEL.x 0</td>
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<td></td>
<td>N/A</td>
<td>DVSS 0 1</td>
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<td>P6.6† Input/Output</td>
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<tr>
<td>P6.7</td>
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<td>P6.7† Input/Output</td>
<td>P6DIR.x 0/1 P6SEL.x 0</td>
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<td></td>
<td>N/A</td>
<td>DVSS 0 1</td>
</tr>
</tbody>
</table>

† Default after reset (PUC/POR)

NOTES:
1. N/A: Not available or not applicable.
2. X: Don’t care.
JTAG pins TMS, TCK, TDI/TCLK, TDO/TDI, input/output with Schmitt-trigger or output

---

**JTAG pins**

- **TMS**
- **TCK**
- **TDI/TCLK**
- **TDO/TDI**

Controlled by JTAG

---

**Test and Emulation Module**

- **TDI**
- **TDI/TCLK**
- **TD/CC**
- **TMS**

**Burn and Test Fuse**

---

**Burn and Test Fuse**

- **DV_CC**
- **TMS**

---

**Brownout**

- **TCK**
- **TCK**

**RST/NMI**

- **Tau ~ 50 ns**
- **Brownout**
- **G**

---

**Texas Instruments**

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JTAG fuse check mode

MSP430 devices that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current ($I_{TF}$) of 1 mA at 3 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current only flows when the fuse check mode is active and the TMS pin is in a low state (see Figure 19). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition). The JTAG pins are terminated internally and therefore do not require external termination.

\[\text{Time TMS Goes Low After POR} \]

\[\begin{array}{c}
\text{TMS} \\
I_{TF} \\
I_{TDI/TCLK}
\end{array} \]

Figure 19. Fuse Check Mode Current
## Data Sheet Revision History

<table>
<thead>
<tr>
<th>Literature Number</th>
<th>Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLAS455D</td>
<td>Updated functional block diagram (page 4)</td>
</tr>
<tr>
<td></td>
<td>Clarified test conditions in recommended operating conditions table (page 17)</td>
</tr>
<tr>
<td></td>
<td>Clarified test conditions in electrical characteristics table (page 18)</td>
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<tr>
<td></td>
<td>Clarified test conditions in DCO table (page 25)</td>
</tr>
<tr>
<td></td>
<td>Changed PSRR to AC PSRR in SD16_A, performance table (page 29)</td>
</tr>
<tr>
<td></td>
<td>Changed PSRR to DC PSR in SD16_A, built-in voltage reference table; corrected typical value from 10 to 100 μV/V (page 30)</td>
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**NOTE:** Page and figure numbers refer to the respective document revision.
Document Being Updated: *MSP430F42x0 Mixed Signal Microcontroller*

Literature Number Being Updated: SLAS455D

<table>
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<tr>
<th>Page</th>
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</thead>
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<td>46</td>
<td>The table includes <em>LCDS12</em> in the &quot;CONTROL BITS / SIGNALS&quot; column. This is correct for P2.0/S13 and P2.1/S12. For P2.2/S11, P2.3/S10, P2.4/S9, and P2.5/S8, the correct control bit is <em>LCDS8</em>. For P2.6/S7 and P2.7/S6, the correct control bit is <em>LCDS4</em>.</td>
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## Packaging Information

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<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/Ball material (3)</th>
<th>MSL Peak Temp (°C)</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
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<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>M430F4250</td>
<td>Samples</td>
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<td>MSP430F4270</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE**: Product device recommended for new designs.

**LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, “RoHS” products are suitable for use in specified lead-free processes. TI may reference these types of products as “Pb-Free”.

**RoHS Exempt**: TI defines “RoHS Exempt” to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**

- Reel Diameter
- Reel Width (W1)

**TAPE DIMENSIONS**

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- Pocket Quadrants
- Sprocket Holes
- User Direction of Feed

*All dimensions are nominal*

<table>
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<th>Device</th>
<th>Package Type</th>
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<th>Pins</th>
<th>SPQ</th>
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<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
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# TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

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<th>Device</th>
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<th>Package Drawing</th>
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<th>Width (mm)</th>
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</table>
TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

<table>
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<th>Package Name</th>
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<th>Pins</th>
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NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
D. Falls within JEDEC MO-118.

www.ti.com
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

4219044/D 02/2022
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
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