TEXAS INSTRUMENTS
AMC3301-Q1
ZHCSLI8A – JULY 2020 – REVISED MAY 2021

AMC3301-Q1 具有集成直流/直流转换器的 精密、±250mV 输入、增强型隔离放大器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 温度等级 1: –40°C 至 125°C，T_A
- 3.3V 或 5V 单电源，具有集成直流/直流转换器
- ±250mV 输入电压范围，针对使用分流电阻器测量电流进行了优化
- 固定增益：8.2
- 低直流误差：
  - 失调电压：±150µV（最大值）
  - 温漂：±1µV/°C（最大值）
  - 增益误差：±0.2%（最大值）
  - 增益误差漂移：±40ppm/°C（最大值）
  - 非线性度：±0.04%（最大值）
- 高 CMTI：85kV/µs（最小值）
- 系统级诊断功能
- 符合 CISPR-11 和 CISPR-25 EMI 标准
- 安全相关认证：
  - 符合 DIN VDE V 0884-11 标准的 6000V_{PK} 增强型隔离
  - 符合 UL1577 标准且长达 1 分钟的 4250V_{RMS} 隔离

2 应用

- 基于分流器的隔离式电流检测，用于：
  - HEV/EV 充电桩
  - HEV/EV 车载充电器 (OBC)
  - HEV/EV 直流/直流转换器
  - HEV/EV 牵引逆变器

3 说明

AMC3301-Q1 是一款精密的隔离放大器，针对基于分流器的电流测量进行了优化。这款完全集成的隔离式直流/直流转换器可实现器件低侧的单电源运行，使该器件成为空间受限应用的独特解决方案。增强型电容式隔离栅已通过 VDE V 0884-11 和 UL1577 认证，并支持高达 1.2kV_{RMS} 的工作电压。

该隔离栅可将系统中以不同共模电压电平运行的各器件隔开，并保护电压较低的器件免受高电压冲击。

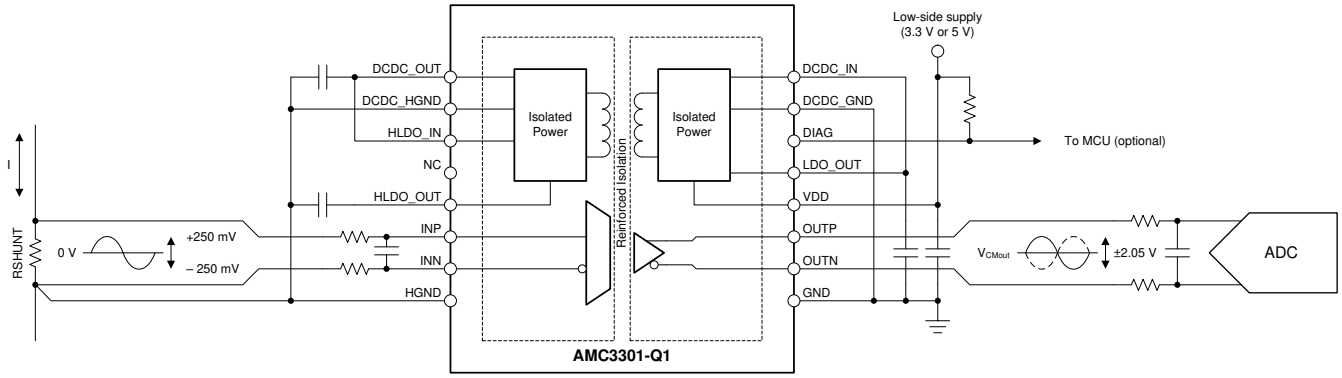
AMC3301-Q1 的输入针对直接连接低阻抗分流电阻器或其他具有低信号电平的低阻抗电压源的情况进行了优化。出色的直流精度和低温漂支持在 –40°C 至 +125°C 的温度范围内进行精确的电流测量。

AMC3301-Q1 的集成直流/直流转换器故障检测和诊断输出引脚可简化系统级设计和诊断。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
AMC3301-Q1	SOIC (16)	10.30mm × 7.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型应用

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (July 2020) to Revision A (May 2021)	Page
• Changed *Pin Configuration and Functions* section	3
• Changed A*bsolute Maximum Ratings*: changed max for *DIAG* pin from 5.5 V to 6.5 V	4
• Changed overvoltage category for rated mains voltage ≤ 600 V from I-IV to I-III and for rated mains voltage ≤1000 V from I-III to I-II	6
• Changed *output bandwidth (BW) (min)* from 250 kHz to 290 kHz	8
• Changed *Typical Characteristics* section. Removed histograms, editorial changes	12
• Changed *Functional Block Diagram* figure	18
• Changed *Data Isolation Channel Signal Transmission* section	19
• Changed *Analog Output* section	20
• Changed *Diagnostic Output* section: added *DIAG Output Under Different Operating Conditions* figure	21
• Changed *Typical Application* section: changed *The AMC3301-Q1 in an OBC Application* figure	22
• Changed *Input Filter Design* section: changed *Differential Input Filter* figure	23
• Added *Differential to Single-Ended Output Conversion* section	24
• Changed *Step Response of the AMC3301-Q1* figure	24
• Changed *Power Supply Recommendations* section: changed nominal value in the first sentence from *3.3 V (or 5 V) ± 10 V* to *3.3 V or 5 V*, changed *primary-side* to *low-side*, *seconday-side* to *high-side*, and *Decoupling the AMC3301-Q1* figure	26
• Changed *Recommended Layout of the AMC3301-Q1* figure	27

5 Pin Configuration and Functions

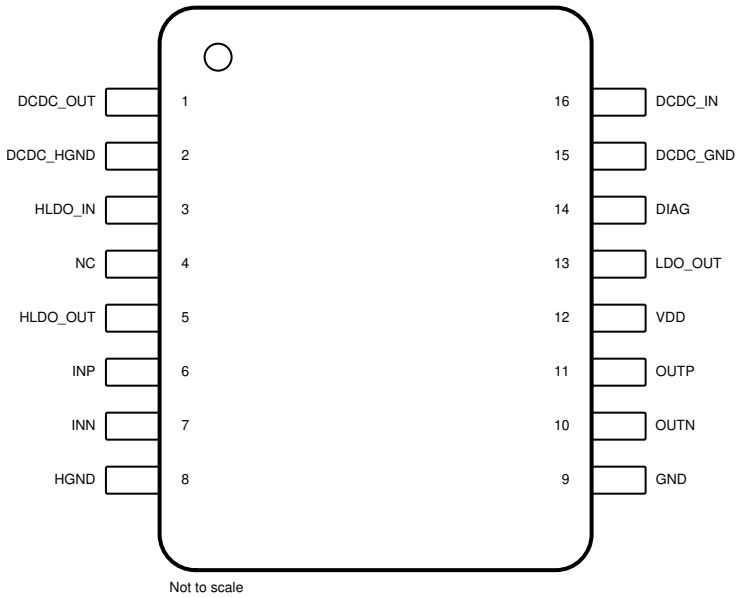


图 5-1. DWE Package, 16-Pin SOIC, Top View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	DCDC_OUT	Power	High-side output of the isolated DC/DC converter; connect this pin to the HLDO_IN pin.(1)
2	DCDC_HGND	High-side power ground	High-side ground reference for the isolated DC/DC converter; connect this pin to the HGND pin.
3	HLDO_IN	Power	Input of the high-side LDO; connect this pin to the DCDC_OUT pin.(1)
4	NC	—	No internal connection; connect this pin to HGND or leave this pin unconnected.
5	HLDO_OUT	Power	Output of the high-side LDO.(1)
6	INP	Analog input	Noninverting analog input. Either INP or INN must have a DC current path to HGND to define the common-mode input voltage.(2)
7	INN	Analog input	Inverting analog input. Either INP or INN must have a DC current path to HGND to define the common-mode input voltage.(2)
8	HGND	High-side signal ground	High-side analog ground; connect this pin to the DCDC_HGND pin.
9	GND	Low-side signal ground	Low-side analog ground; connect this pin to the DCDC_GND pin.
10	OUTN	Analog output	Inverting analog output.
11	OUTP	Analog output	Noninverting analog output.
12	VDD	Low-side power	Low-side power supply.(1)
13	LDO_OUT	Power	Output of the low-side LDO; connect this pin to the DCDC_IN pin. The output of the LDO must not be loaded by external circuitry.(1)
14	DIAG	Digital output	Active-low, open-drain status indicator output; connect this pin to the pullup supply (for example, VDD) using a resistor or leave this pin floating if not used.
15	DCDC_GND	Low-side power ground	Low-side ground reference for the isolated DC/DC converter; connect this pin to the GND pin.
16	DCDC_IN	Power	Low-side input of the isolated DC/DC converter; connect this pin to the LDO_OUT pin.(1)

(1) See the *Power Supply Recommendations* section for power-supply decoupling recommendations.
(2) See the *Layout* section for details.

6 Specifications

6.1 Absolute Maximum Ratings

see (1)

		MIN	MAX	UNIT
Power-supply voltage	VDD to GND	–0.3	6.5	V
Analog input voltage	INP, INN	HGND – 6	V_{HLDO_OUT} + 0.5	V
Analog output voltage	OUTP, OUTN	GND – 0.5	VDD + 0.5	V
Digital output voltage	DIAG	GND – 0.5	6.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1), HBM ESD classification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011, CDM ESD classification Level C6	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
VDD	Low-side power supply	VDD to GND	3	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Differential input voltage before clipping output	$V_{IN} = V_{INP} – V_{INN}$		±320		mV
V_{FSR}	Specified linear differential full-scale voltage	$V_{IN} = V_{INP} – V_{INN}$	–250		250	mV
	Absolute common-mode input voltage (1)	$(V_{INP} + V_{INN}) / 2$ to HGND	–2		V_{HLDO_OUT}	V
V_{CM}	Operating common-mode input voltage	$(V_{INP} + V_{INN}) / 2$ to HGND	–0.16		1	V
TEMPERATURE RANGE						
T_A	Specified ambient temperature		–40		125	°C

(1) Steady-state voltage supported by the device in case of a system failure. See specified common-mode input voltage V_{CM} for normal operation. Observe analog input voltage range as specified in the *Absolute Maximum Ratings* table.

6.4 Thermal Information

THERMAL METRIC(1)		AMC3301-Q1 DWE (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation	VDD = 5.5 V			231	mW
		VDD = 3.6 V			151	

6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance (1)	Shortest pin-to-pin distance through air	≥ 8	mm
CPG	External creepage (1)	Shortest pin-to-pin distance across the package surface	≥ 8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance - capacitive signal isolation)	≥ 21	µm
		Minimum internal gap (internal clearance - transformer power isolation)	≥ 120	
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I-III	
		Rated mains voltage ≤ 1000 V_{RMS}	I-II	
DIN VDE V 0884-11 (VDE V 0884-11): 2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage (bipolar)	1700	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test	1200	V_{RMS}
		At DC voltage	1700	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test)	6000	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test)	7200	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 60065, 1.2/50-µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 10000\ V_{PK}$ (qualification)	6250	V_{PK}
q_{pd}	Apparent charge(4)	Method a, after input/output safety test subgroup 2 / 3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.5 V_{PP} at 1 MHz	~3.5	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		40/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 4250 V_{RMS} or 6000 V_{DC}, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	4250	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings must be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier are tied together, creating a two-pin device.

6.7 Safety-Related Certifications

VDE	UL
Certified according to DIN VDE V 0884-11 (VDE V 0884-11): 2017-01, DIN EN 60950-1 (VDE 0805 Teil 1): 2014-08, and DIN EN 60065 (VDE 0860): 2005-11	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: 40040142	File number: E181974

6.8 Safety Limiting Values

Safety limiting (1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure ofthe I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 73.5°C/W, VDD = 5.5 V, T_J = 150°C, T_A = 25°C			309	mA
		$R_{\theta JA}$ = 73.5°C/W, VDD = 3.6 V, T_J = 150°C, T_A = 25°C			472	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 73.5°C/W, T_J = 150°C, T_A = 25°C			1700	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum low-side voltage.

6.9 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD = 3.0 V to 5.5 V, INP = –250 mV to +250 mV, INN = HGND = 0 V, and the external components listed in the *Typical Application* section; typical specifications are at T_A = 25°C, and VDD = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
R_{IN}	Single-ended input resistance	INN = HGND		19		kΩ
R_{IND}	Differential input resistance			22		
I_{IB}	Input bias current	INP = INN = HGND; I_{IB} = (I_{IBP} + I_{IBN}) / 2	–41	–30	–24	µA
TCI_{IB}	Input bias current drift			0.8		nA/°C
I_{IO}	Input offset current	I_{IO} = |I_{IBP} – I_{IBN}|		1.4		nA
C_{IN}	Single-ended input capacitance	INN = HGND, f_{IN} = 275 kHz		2		pF
C_{IND}	Differential input capacitance	f_{IN} = 275 kHz		1		
ANALOG OUTPUT						
	Nominal gain			8.2		V/V
V_{CMout}	Common-mode output voltage		1.39	1.44	1.49	V
$V_{CLIPout}$	Clipping differential output voltage	V_{OUT} = (V_{OUTP} – V_{OUTN}); |V_{IN}| = |V_{INP} – V_{INN}| > $V_{Clipping}$		±2.49		V
$V_{Failsafe}$	Failsafe differential output voltage	V_{OUT} = (V_{OUTP} – V_{OUTN}); V_{DCDC_OUT} ≤ V_{DCDCUV}, or V_{HLDO_OUT} ≤ V_{HLDOUV}		–2.57	-2.5	V
BW	Output bandwidth		290	334		kHz
R_{OUT}	Output resistance	On OUTP or OUTN		0.2		Ω
	Output short-circuit current	On OUTP or OUTN, sourcing or sinking, INP = INN = HGND, outputs shorted to either GND or VDD		14		mA
CMTI	Common-mode transient immunity	|HGND – GND| = 2 kV	85	135		kV/µs
ACCURACY						
V_{OS}	Input offset voltage(1) (2)	T_A = 25°C, INP = INN = HGND	–0.15	±0.02	0.15	mV
TCV_{OS}	Input offset drift(1) (2) (4)		–1	±0.15	1	uV/°C
E_G	Gain error(1)	T_A = 25°C	–0.2%	±0.04%	0.2%	
TCE_G	Gain error drift(1) (5)		–40	±6	40	ppm/°C
	Nonlinearity(1)		–0.04%	±0.002%	0.04%	
	Nonlinearity drift(1)			0.9		ppm/°C
SNR	Signal-to-noise ratio	V_{IN} = 0.5 V_{PP}, f_{IN} = 1 kHz, BW = 10 kHz, 10 kHz filter	80	85		dB
		V_{IN} = 0.5 V_{PP}, f_{IN} = 10 kHz, BW = 100 kHz, 1 MHz filter	67	71		
THD	Total harmonic distortion(3)	V_{IN} = 0.5 Vpp, f_{IN} = 10 kHz, BW = 100 kHz		–85		dB
	Output noise	INP = INN = HGND, f_{IN} = 0 Hz, BW = 100 kHz		300		$µV_{RMS}$
CMRR	Common-mode rejection ratio	f_{IN} = 0 Hz, $V_{CM\ min}$ ≤ V_{CM} ≤$V_{CM\ max}$		–97		dB
		f_{IN} = 10 kHz, $V_{CM\ min}$ ≤ V_{CM} ≤$V_{CM\ max}$		–98		
PSRR	Power-supply rejection ratio	VDD from 3.0 V to 5.5 V, at dc, input referred		–109		dB
		INP = INN = HGND, VDD from 3.0 V to 5.5 V, 10 kHz / 100 mV ripple, input referred		–98		

6.9 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD = 3.0 V to 5.5 V, INP = –250 mV to +250 mV, INN = HGND = 0 V, and the external components listed in the *Typical Application* section; typical specifications are at T_A = 25°C, and VDD = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
IDD	Low-side supply current	no external load on HLDO		27.5	40	mA
		1 mA external load on HLDO		29.5	42	
V_{DCDC_OUT}	DCDC output voltage	DCDC_OUT to HGND	3.1	3.5	4.65	V
V_{DCDCUV}	DCDC output undervoltage detection threshold voltage	DCDC output falling	2.1	2.25		V
V_{HLDO_OUT}	High-side LDO output voltage	HLDO to HGND, up to 1 mA external load	3	3.2	3.4	V
V_{HLDOUV}	High-side LDO output undervoltage detection threshold voltage	HLDO output falling	2.4	2.6		V
I_H	High-side supply current for auxiliary circuitry	Load connected from HLDO_OUT to HGND, non-switching			1	mA
t_{AS}	Analog settling time	VDD step to 3.0 V, to OUTP and OUTN valid, 0.1% settling		0.9	1.4	ms

(1) The typical value includes one standard deviation ("sigma") at nominal operating conditions.
(2) This parameter is input referred.
(3) THD is the ratio of the rms sum of the amplitues of first five higher harmonics to the amplitude of the fundamental.
(4) Offset error temperature drift is calculated using the box method, as described by the following equation:
$TCV_{OS} = (Value_{MAX} - Value_{MIN}) / TempRange$
(5) Gain error temperature drift is calculated using the box method, as described by the following equation:
$TCE_G\ (ppm) = (Value_{MAX} - Value_{MIN}) / (Value_{(T=25°C)} \times TempRange) \times 10^6$

6.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output signal rise time			1.3		µs
t_f	Output signal fall time			1.3		µs
	V_{INx} to V_{OUTx} signal delay (50% – 10%)	Unfiltered output		1	1.5	µs
	V_{INx} to V_{OUTx} signal delay (50% – 50%)	Unfiltered output		1.6	2.1	µs
	V_{INx} to V_{OUTx} signal delay (50% – 90%)	Unfiltered output		2.5	3	µs

6.11 Timing Diagram

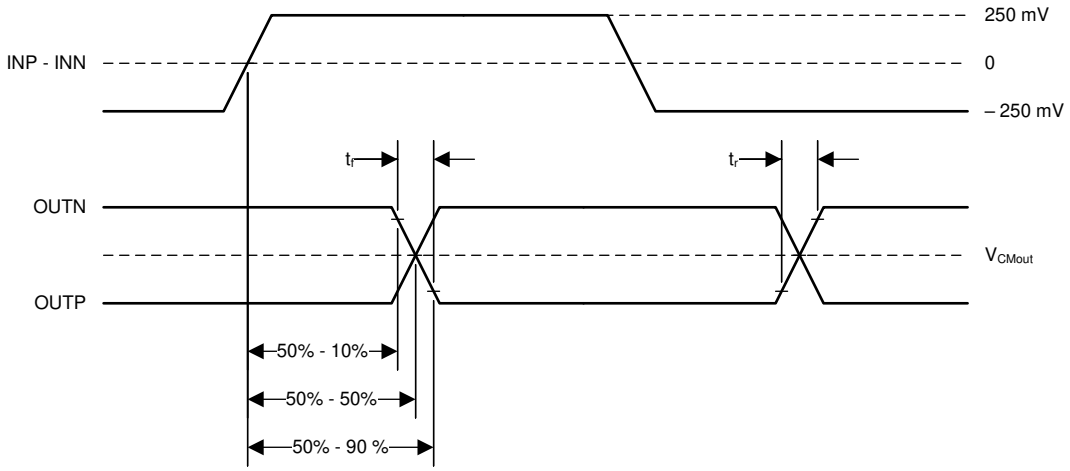


图 6-1. Rise, Fall, and Delay Time Waveforms

6.12 Insulation Characteristics Curves

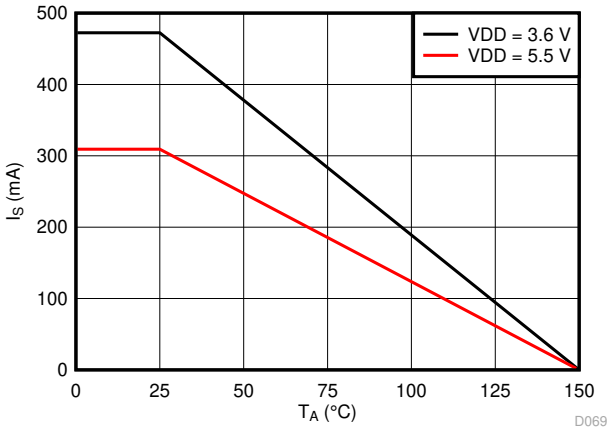


图 6-2. Thermal Derating Curve for Safety-Limiting Current per VDE

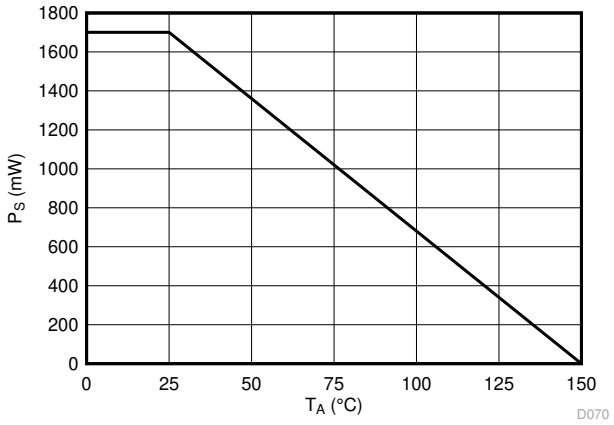
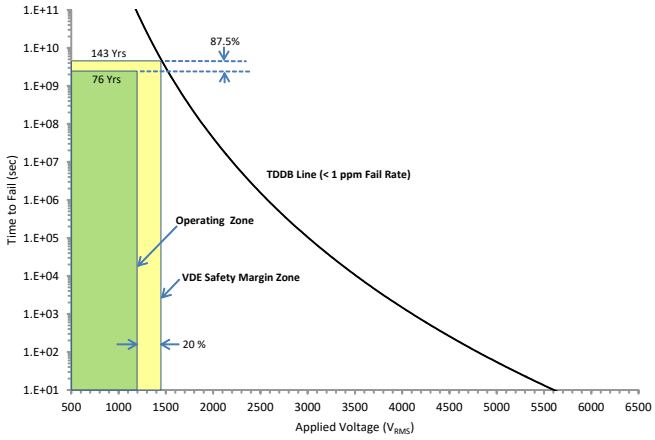


图 6-3. Thermal Derating Curve for Safety-Limiting Power per VDE



T_A up to 150°C, stress-voltage frequency = 60 Hz,
isolation working voltage = 1200 V_{RMS}, operating lifetime = 76 years

图 6-4. Reinforced Isolation Capacitor Lifetime Projection

6.13 Typical Characteristics

at VDD = 3.3 V, INP = –250 mV to +250 mV, INN = HGND = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

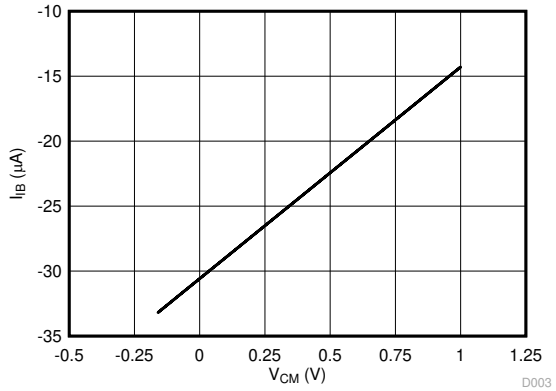


图 6-5. Input Bias Current vs Common-Mode Input Voltage

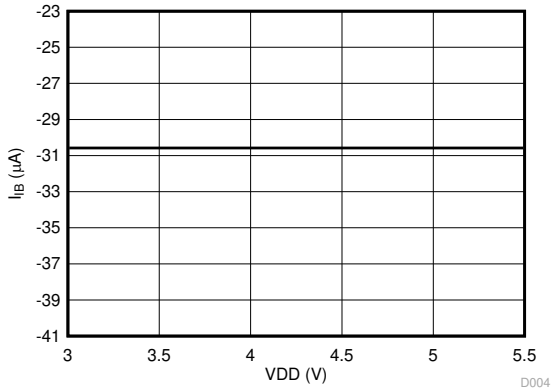


图 6-6. Input Bias Current vs Supply Voltage

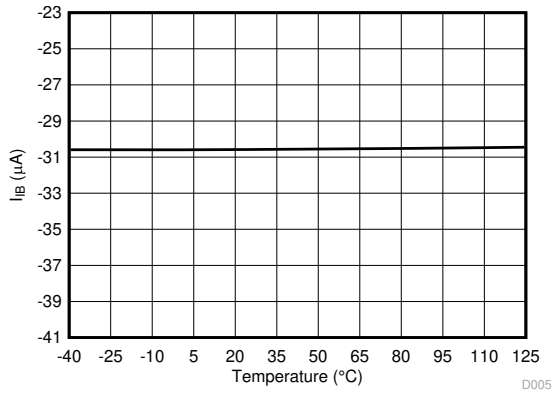


图 6-7. Input Bias Current vs Temperature

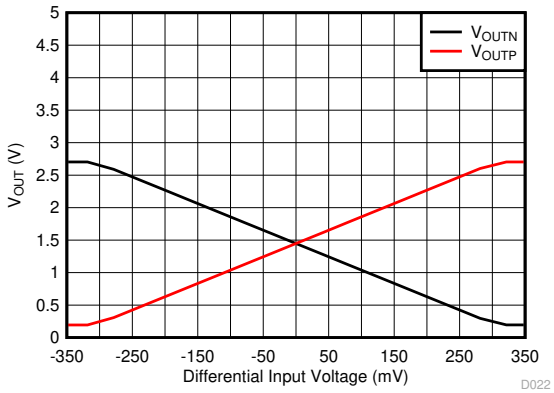


图 6-8. Output Voltage vs Input Voltage

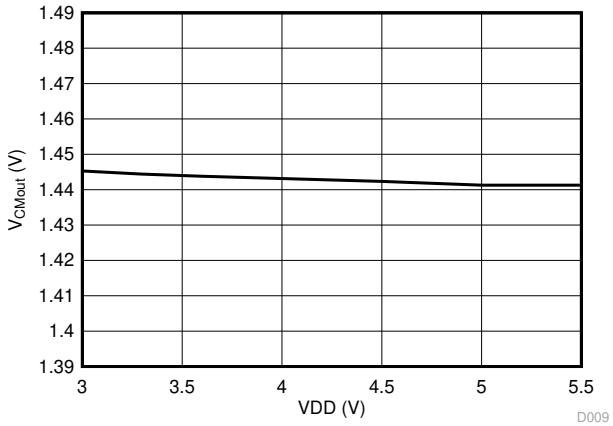


图 6-9. Output Common-Mode Voltage vs Supply Voltage

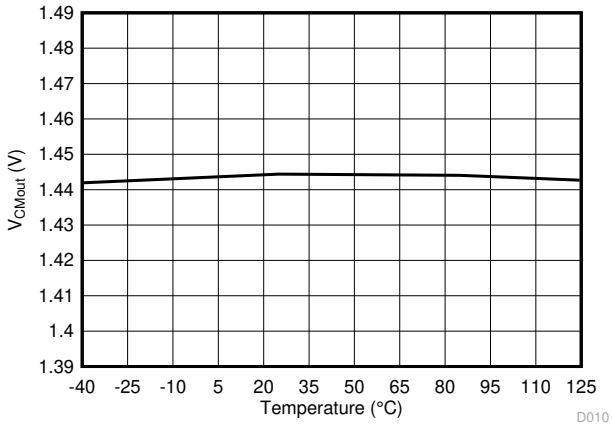


图 6-10. Output Common-Mode Voltage vs Temperature

6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = –250 mV to +250 mV, INN = HGND = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

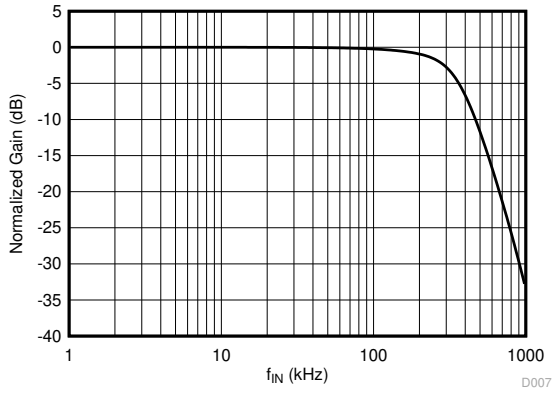


图 6-11. Normalized Gain vs Input Frequency

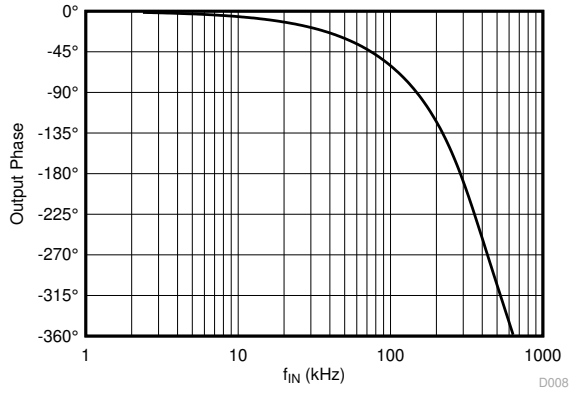


图 6-12. Output Phase vs Input Frequency

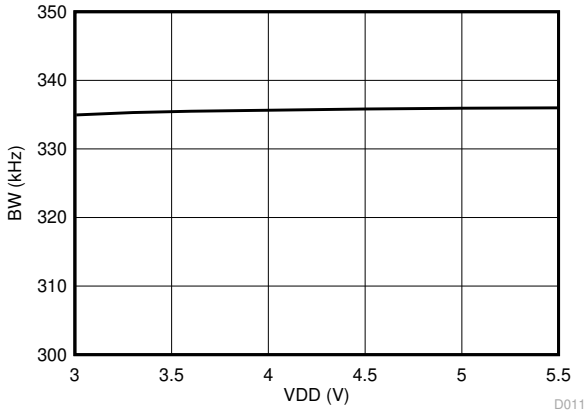


图 6-13. Output Bandwidth vs Supply Voltage

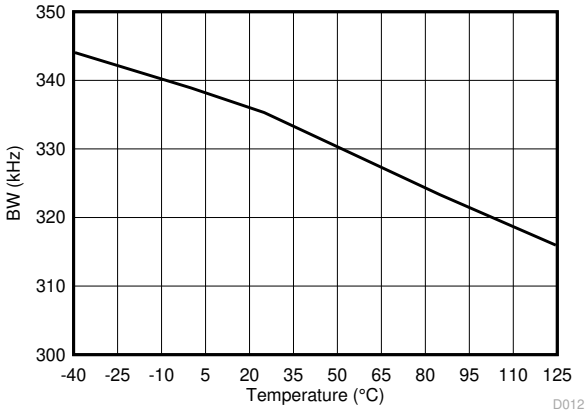


图 6-14. Output Bandwidth vs Temperature

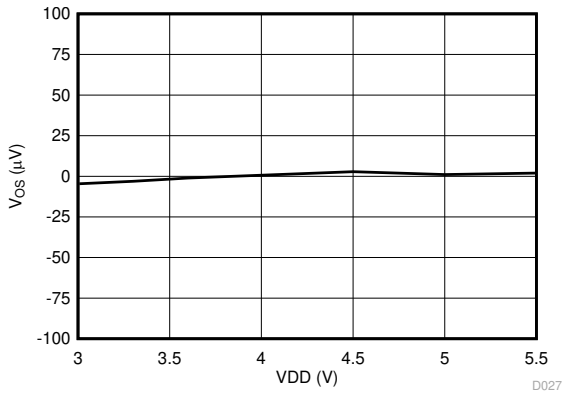


图 6-15. Input Offset Voltage vs Supply Voltage

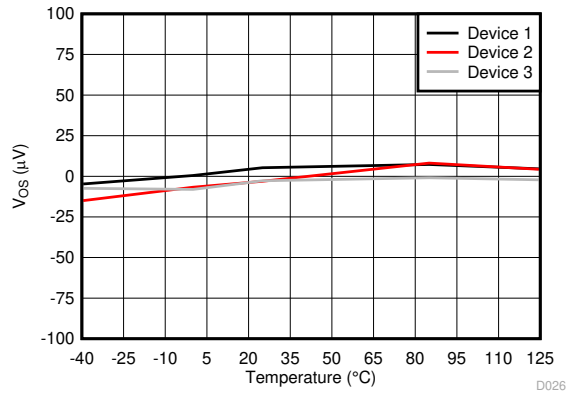


图 6-16. Input Offset Voltage vs Temperature

6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = –250 mV to +250 mV, INN = HGND = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

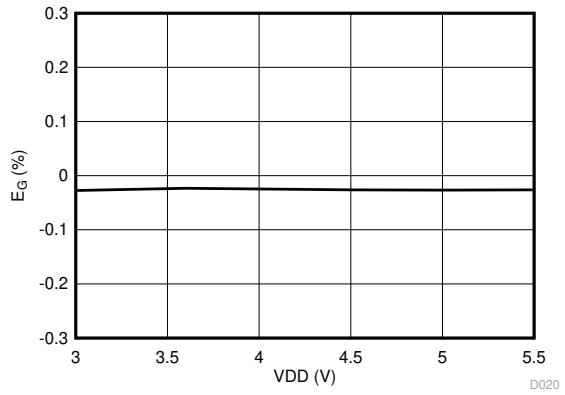


图 6-17. Gain Error vs Supply Voltage

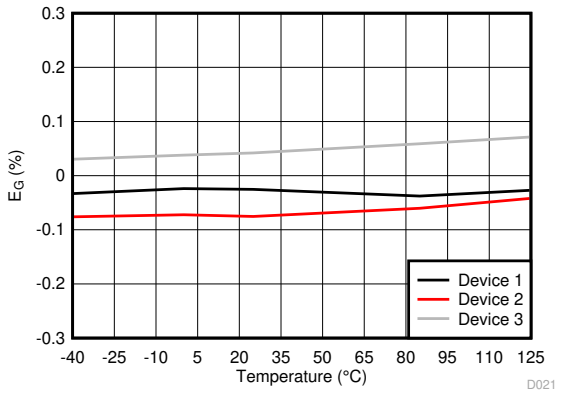


图 6-18. Gain Error vs Temperature

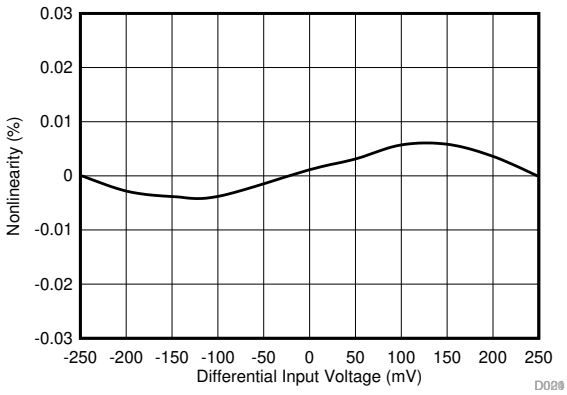


图 6-19. Nonlinearity vs Input Voltage

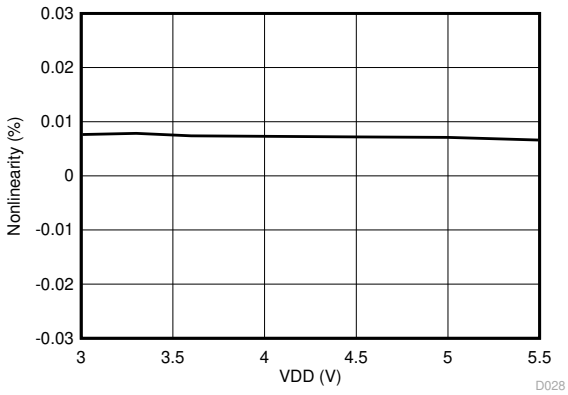


图 6-20. Nonlinearity vs Supply Voltage

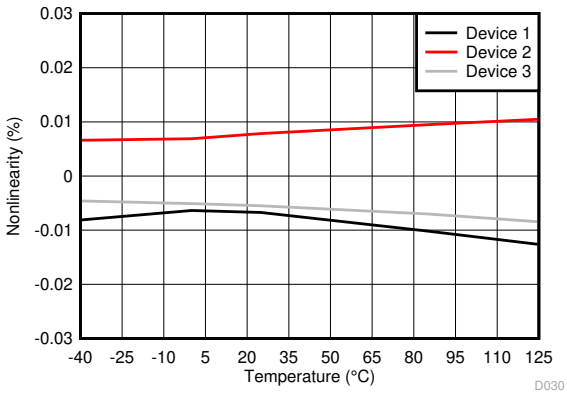
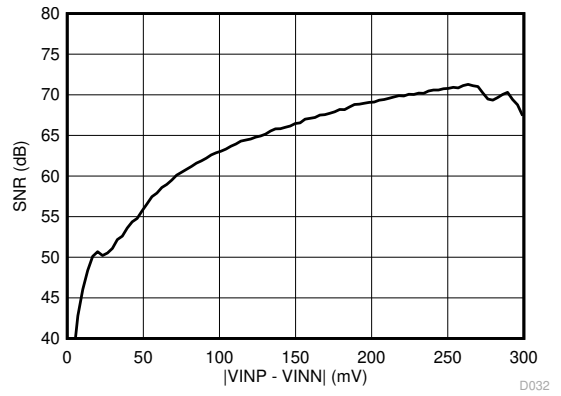


图 6-21. Nonlinearity vs Temperature

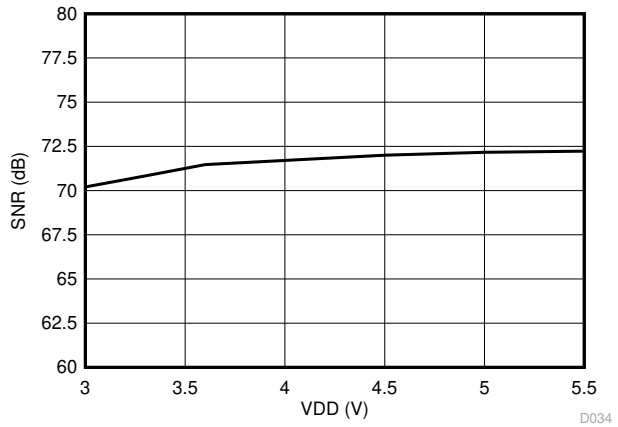


V_{IN} = 0.5 V_{pp}, f_{IN} = 10 kHz

图 6-22. Signal-to-Noise Ratio vs Input Voltage

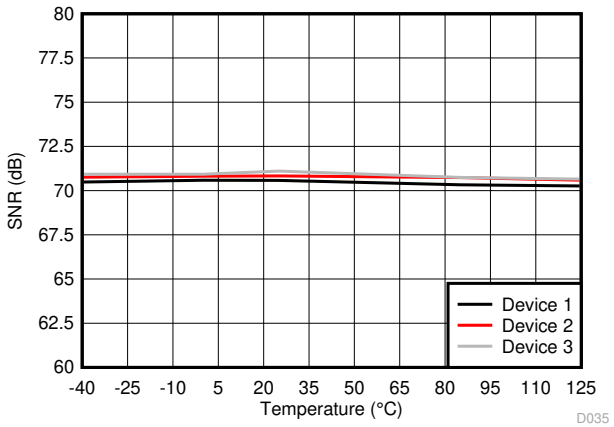
6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = –250 mV to +250 mV, INN = HGND = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)



V_{IN} = 0.5 V_{pp}, f_{IN} = 10 kHz

图 6-23. Signal-to-Noise Ratio vs Supply Voltage



V_{IN} = 0.5 V_{pp}, f_{IN} = 10 kHz

图 6-24. Signal-to-Noise Ratio vs Temperature

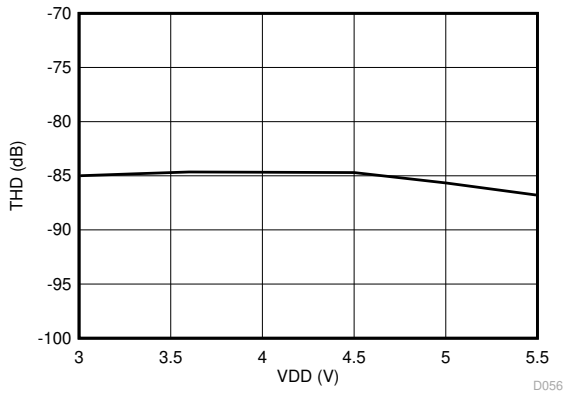


图 6-25. Total Harmonic Distortion vs Supply Voltage

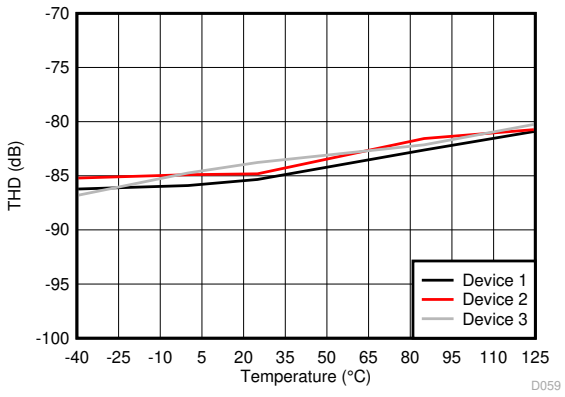


图 6-26. Total Harmonic Distortion vs Temperature

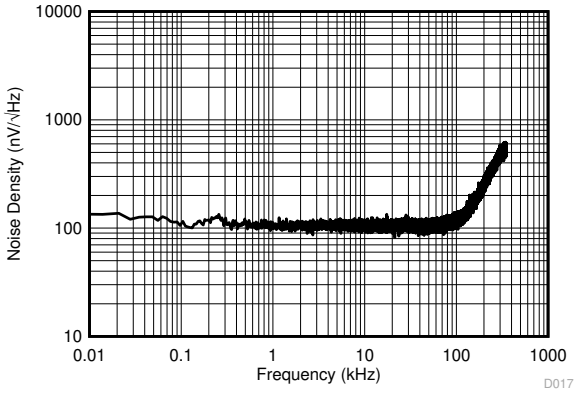


图 6-27. Input-Referred Noise Density vs Frequency

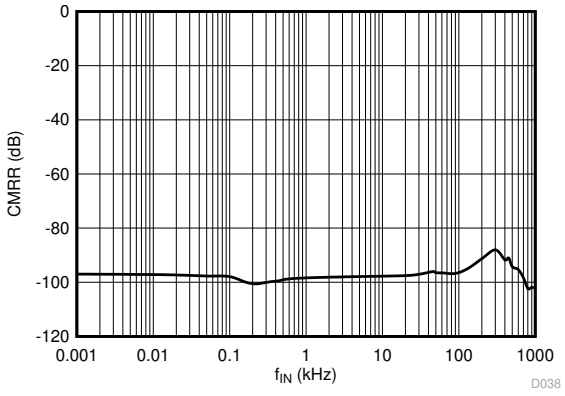


图 6-28. Common-Mode Rejection Ratio vs Input Frequency

6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = –250 mV to +250 mV, INN = HGND = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

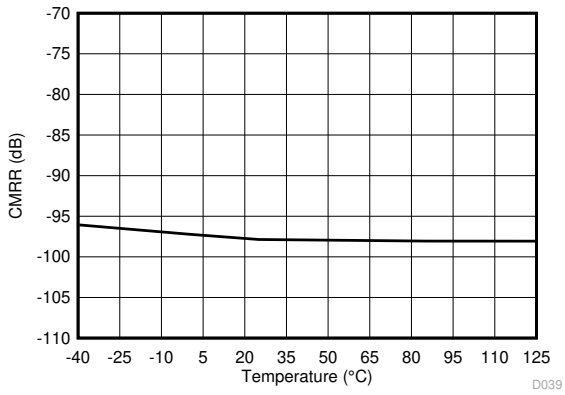


图 6-29. Common-Mode Rejection Ratio vs Temperature

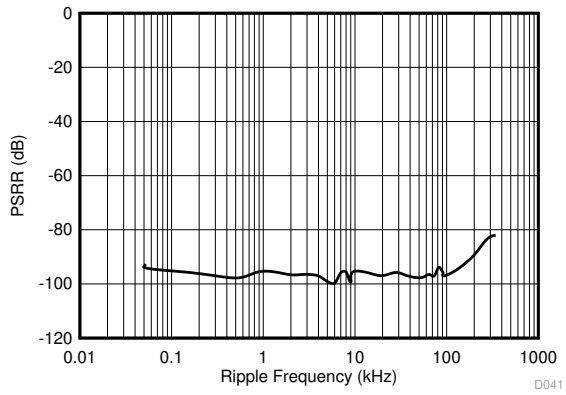


图 6-30. Power-Supply Rejection Ratio vs Ripple Frequency

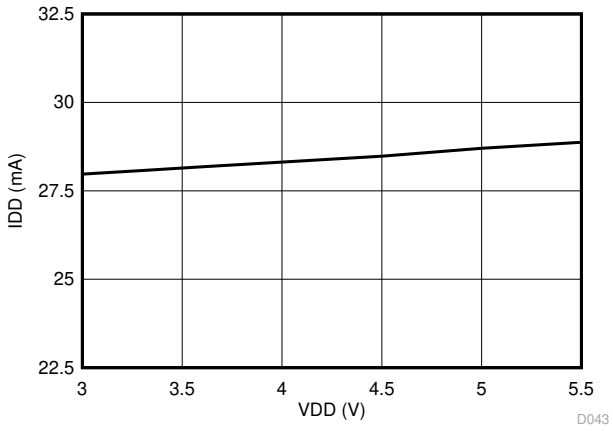


图 6-31. Supply Current vs Supply Voltage

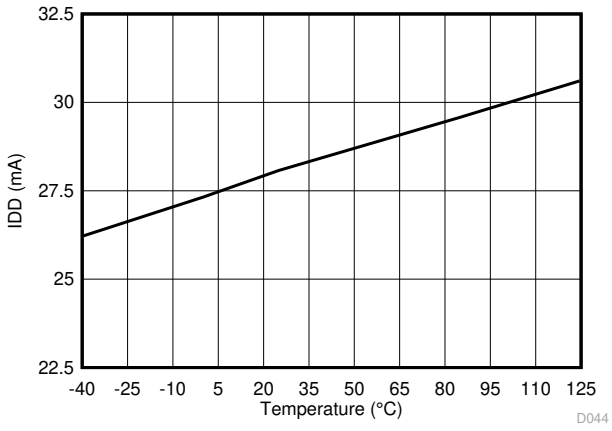


图 6-32. Supply Current vs Temperature

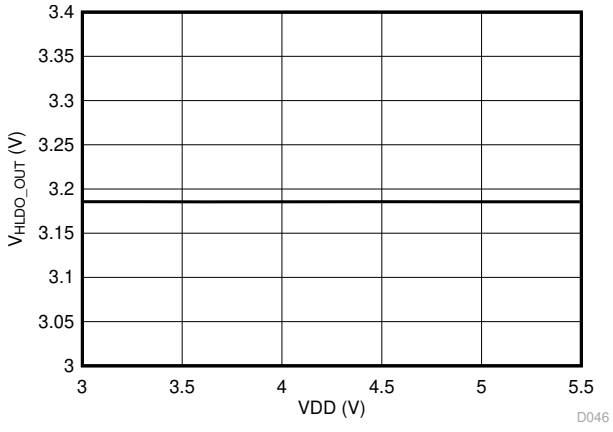


图 6-33. High-Side LDO Line Regulation

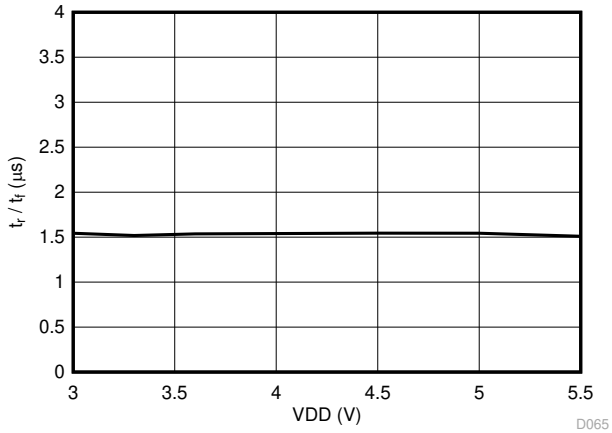


图 6-34. Output Rise and Fall time vs Supply Voltage

6.13 Typical Characteristics (continued)

at VDD = 3.3 V, INP = –250 mV to +250 mV, INN = HGND = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

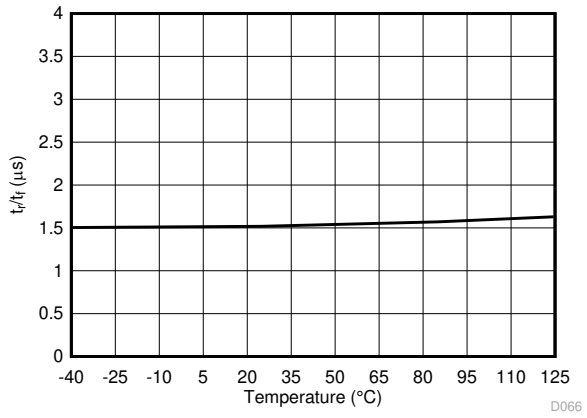


图 6-35. Output Rise and Fall Time vs Temperature

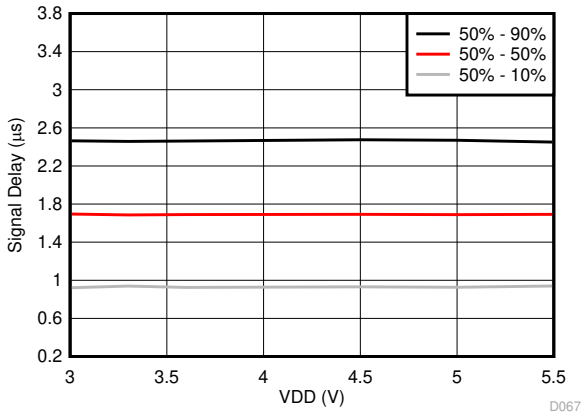


图 6-36. V_{IN} to V_{OUT} Signal Delay vs Supply Voltage

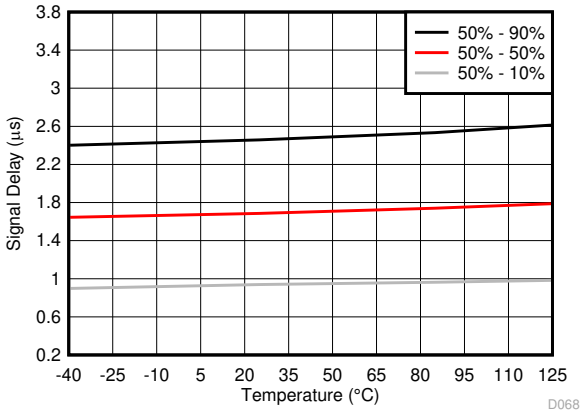


图 6-37. V_{IN} to V_{OUT} Signal Delay vs Temperature

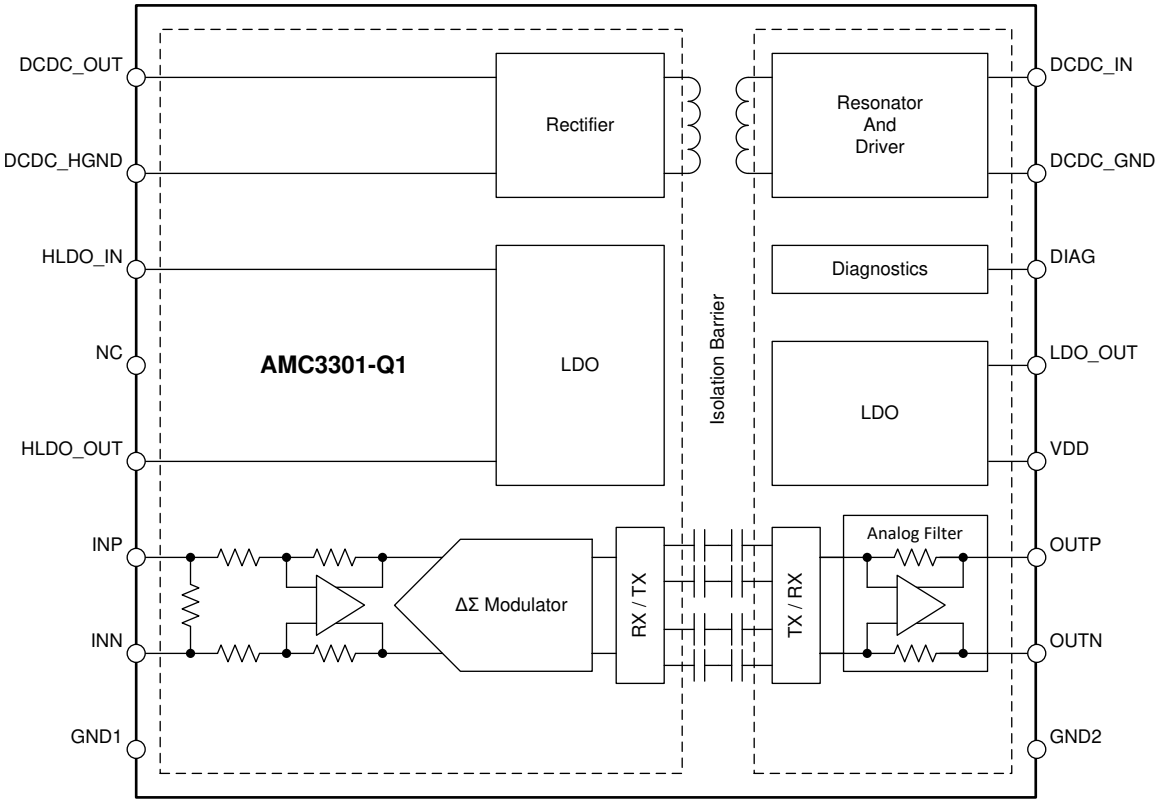
7 Detailed Description

7.1 Overview

The AMC3301-Q1 is a fully differential, precision, isolated amplifier with a fully integrated DC/DC converter that can supply the device from a single 3.3-V or 5-V voltage supply on the low-side. The input stage of the device consists of a fully differential amplifier that drives a second-order, delta-sigma (ΔΣ) modulator. The modulator uses an internal voltage reference and clock generator to convert the analog input signal to a digital bitstream. The drivers (termed *TX* in the *Functional Block Diagram*) transfer the output of the modulator across the isolation barrier that separates the high-side and low-side voltage domains. As shown in the *Functional Block Diagram*, the received bitstream and clock are synchronized and processed by a fourth-order analog filter on the low-side and presented as a differential output of the device

The signal path is isolated by a double capacitive silicon dioxide (SiO_2) insuation barrier, whereas power isolation uses an on-chip transformer separated by a thin-film polymer as the insulating material.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input

The differential amplifier input stage of the AMC3301-Q1 feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The gain of the differential amplifier is set by internal precision resistors with a differential input impedance of R_{IND}. The modulator converts the analog signal into a bitstream that is transferred across the isolation barrier, as described in the *Data Isolation Channel Signal Transmission* section.

There are two restrictions on the analog input signals (INP and INN). First, if the input voltages V_{INP} or V_{INN} exceed the range specified in the *Absolute Maximum Ratings* table, the input current must be limited to the absolute maximum value, because the device input electrostatic discharge (ESD) diodes turns on. In addition, the linearity and parametric performance of the device are ensured only when the analog input voltage remains within linear full-scale range (V_{FSR}) and within the common-mode input voltage range (V_{CM}) as specified in the *Recommended Operating Conditions* table.

7.3.2 Data Isolation Channel Signal Transmission

The AMC3301-Q1 uses an on-off keying (OOK) modulation scheme, as shown in 图 7-1, to transmit the modulator output bitstream across the capacitive SiO_2-based isolation barrier. The transmit driver (TX) shown in the *Functional Block Diagram* transmits an internally generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC3301-Q1 is 480 MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and produces the output. The AMC3301-Q1 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and lowest level of radiated emissions caused by the high-frequency carrier and RX/TX buffer switching.

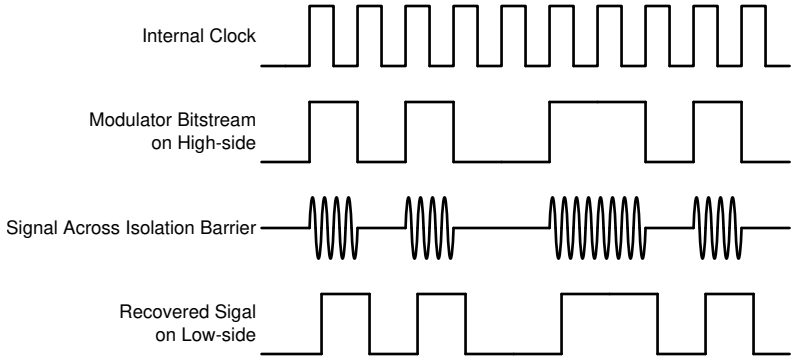


图 7-1. OOK-Based Modulation Scheme

7.3.3 Analog Output

The AMC3301-Q1 offers a differential analog output comprised of the OUTP and OUTN pins. For differential input voltages ($V_{INP} – V_{INN}$) in the range from –250 mV to +250 mV, the device provides a linear response with a nominal gain of 8.2. For example, for a differential input voltage of 250 mV, the differential output voltage ($V_{OUTP} – V_{OUTN}$) is 2.05 V. At zero input (INP shorted to INN), both pins output the same common-mode output voltage V_{CMout}, as specified in the *Electrical Characteristics* table. For absolute differential input voltages greater than 250 mV but less than 320 mV, the differential output voltage continues to increase in magnitude but with reduced linearity performance. The outputs saturate at a differential output voltage of $V_{CLIPout}$ as shown in 图 7-2 if the differential input voltage exceeds the $V_{Clipping}$ value.

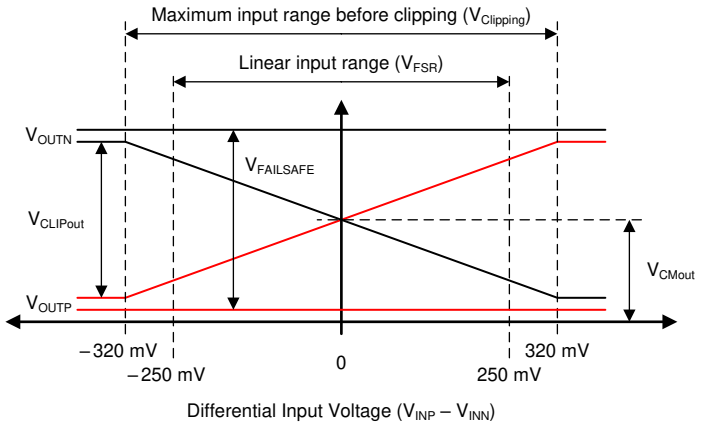


图 7-2. Output Behavior of the AMC3301-Q1

The AMC3301-Q1 provides a fail-safe output that simplifies diagnostics on system level. 图 7-2 shows the fail-safe mode, in which the AMC3301-Q1 outputs a negative differential output voltage that does not occur under normal operating conditions. The fail-safe output is active in two cases:

- The low-side does not receive data from the high-side (for example, because of a loss of power on the high side).
- The high-side DC/DC output voltage (DCDC_OUT) or the high-side LDO output voltage (HLDO_OUT) drop below their respective undervoltage detection thresholds (brown-out).

Use the maximum $V_{FAILSAFE}$ voltage specified in the *Electrical Characteristics* table as a reference value for the fail-safe detection on the system level.

7.3.4 Isolated DC/DC Converter

The AMC3301-Q1 offers a fully integrated isolated DC/DC converter that includes the following components as illustrated in the *Functional Block Diagram*:

- Low-dropout regulator (LDO) on the low-side to stabilize the supply voltage VDD that drives the low-side of the converter. This circuit does not output a constant voltage and is not intended for driving any external load.
- Low-side full-bridge inverter and drivers
- Laminate-based, air-core transformer for high-immunity to magnetic fields
- High-side full-bridge rectifier
- High-side LDO to stabilize the output voltage of the DC/DC converter for high analog performance of the signal path. The high-side LDO outputs a constant voltage and can provide a limited amount of current to power external circuitry.

The DC/DC converter uses a spread-spectrum clock generation technique to reduce the spectral density of the electromagnetic radiation. The resonator frequency is synchronized to the operation of the ΔΣ modulator to minimize the interference with data transmission and support the high analog performance of the device.

The architecture of the DC/DC converter is optimized to drive the high-side circuitry of the AMC3301-Q1 and can source up to I_H of additional DC current for an optional auxiliary circuit such as an active filter, preamplifier, or comparator. I_H is specified in the *Electrical Characteristics* table as a DC, non-switching current.

7.3.5 Diagnostic Output

The open-drain DIAG pin can be monitored to confirm the device is operational and the output voltage is valid. As shown in 图 7-3, during power-up, the DIAG pin is actively held low until the high-side supply is in regulation and the device operates properly. During normal operation, the DIAG pin is in high-impedance (Hi-Z) state and is pulled high through an external pullup resistor. The DIAG pin is actively pulled low if:

- The low-side does not receive data from the high-side (for example, because of a loss of power on the high side). In this case, the amplifier outputs are driven to the $V_{FAILSAFE}$ value that is shown in 图 7-2.
- The high-side DC/DC output voltage (DCDC_OUT) or the high-side LDO output voltage (HLDO_OUT) drop below their respective undervoltage detection thresholds (brown-out). In this case, the low-side may still receive data from the high-side but the data may not be valid. The amplifier outputs are driven to the $V_{FAILSAFE}$ value that is shown in 图 7-2.

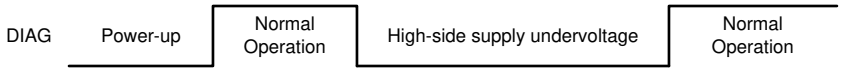


图 7-3. DIAG Output Under Different Operating Conditions

During normal operation, the DIAG pin is in a high-impedance state. Connect the DIAG pin to a pullup resistor or leave open if not used.

7.4 Device Functional Modes

The AMC3301-Q1 is operational when the power supply VDD is applied, as specified in the *Recommended Operating Conditions* table.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The low input voltage range, low nonlinearity, and low temperature drift make the AMC3301-Q1 a high-performance solution for automotive applications where shunt-based current sensing with high common-mode voltage levels is required.

8.2 Typical Application

The AMC3301-Q1 is ideally suited for shunt-based current sensing applications where accurate current monitoring is required in the presence of high common-mode voltages. The AMC3301-Q1 integrates an isolated power supply for the high-voltage side and therefore makes the device particularly easy to use in applications that do not have a high-side supply readily available or where a high-side supply is referenced to a different ground potential than the signal to be measured.

图 8-1 shows a simplified schematic using the AMC3301-Q1 to measure the output current of a PFC stage of an onboard charger (OBC). At this location in the system, there is no supply readily available for powering the high-side of the isolated amplifier. The integrated isolated power supply solves this problem and, together with its bipolar input voltage range, makes the AMC3301-Q1 ideally suited for bidirectional current sensing. In this example, the AC line-voltage is sensed by the AMC3330-Q1 on the grid-side where there is also no suitable supply available for powering the high-side of the isolated amplifier. The integrated power supply, high input impedance, and bipolar input voltage range of the AMC3330-Q1 make the device ideally suited for AC voltage-sensing applications.

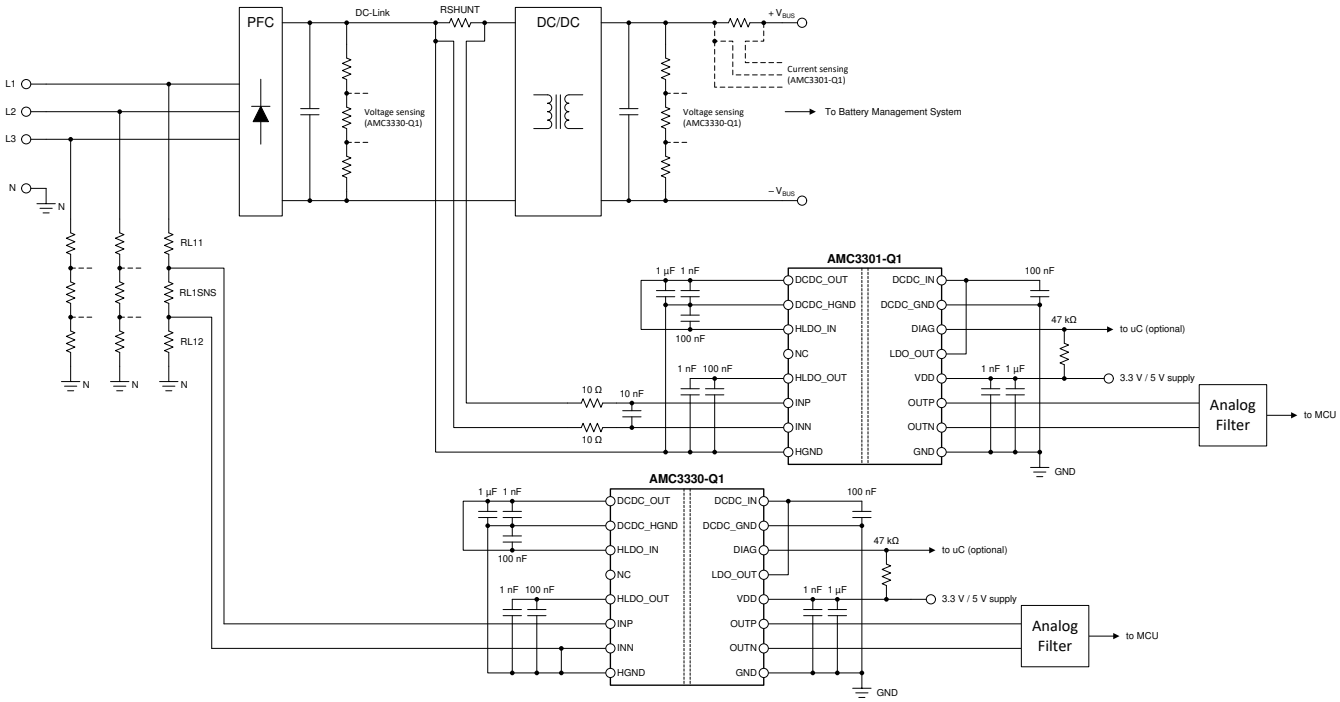


图 8-1. The AMC3301-Q1 in an OBC Application

8.2.1 Design Requirements

表 8-1 lists the parameters for this typical application.

表 8-1. Design Requirements

PARAMETER	VALUE
Supply voltage	3.3 V or 5 V
Voltage drop across the shunt for a linear response (V_{SHUNT})	±250 mV (maximum)

8.2.2 Detailed Design Procedure

The AMC3301-Q1 requires a single 3.3-V or 5-V supply on its low-side. The high-side supply is internally generated by an integrated DC/DC converter as explained in the *Isolated DC/DC Converter* section.

The ground reference (HGND) is derived from the terminal of the shunt resistor that is connected to the negative input of the AMC3301-Q1 (INN). If a four-pin shunt is used, the inputs of the AMC3301-Q1 are connected to the inner leads and HGND is connected to one of the outer shunt leads. To minimize offset and improve accuracy, set the ground connection to a separate trace that connects directly to the shunt resistor rather than shorting HGND to INN directly at the input to the device. See the *Layout* section for more details.

8.2.2.1 Shunt Resistor Sizing

Use Ohm's Law to calculate the voltage drop across the shunt resistor (V_{SHUNT}) for the desired measured current: $V_{SHUNT} = I \times R_{SHUNT}$.

Consider the following two restrictions to choose the proper value of the shunt resistor, R_{SHUNT}:

- The voltage drop caused by the nominal current range must not exceed the recommended differential input voltage range: $|V_{SHUNT}| \leq |V_{FSR}|$
- The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $|V_{SHUNT}| \leq |V_{Clipping}|$

8.2.2.2 Input Filter Design

TI recommends placing an RC filter in front of the isolated amplifier to improve signal-to-noise performance of the signal path. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (20 MHz) of the ΔΣ modulator
- The input bias current does not generate significant voltage drop across the DC impedance of the input filter
- The impedances measured from the analog inputs are equal

For most applications, the structure shown in 图 8-2 achieves excellent performance.

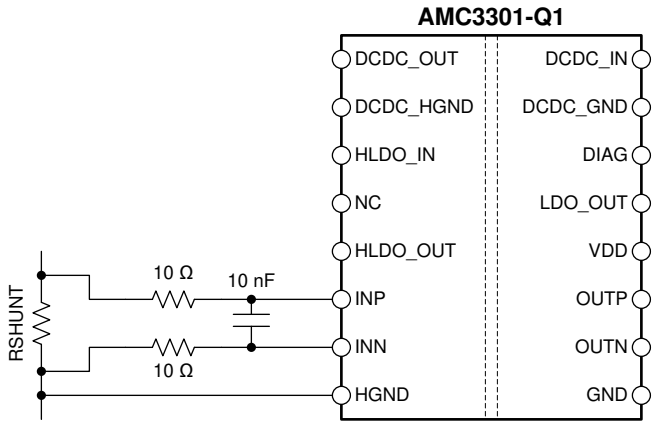


图 8-2. Differential Input Filter

8.2.3 Differential to Single-Ended Output Conversion

图 8-3 shows an example of a TLV313-Q1 based signal conversion and filter circuit for systems using single-ended-input ADCs to convert the analog output voltage into digital. With R1 = R2 = R3 = R4, the output voltage equals (V_{OUTP} – V_{OUTN}) + V_{REF}. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system. For most applications, R1 = R2 = R3 = R4 = 3.3 kΩ and C1 = C2 = 330 pF yields good performance.

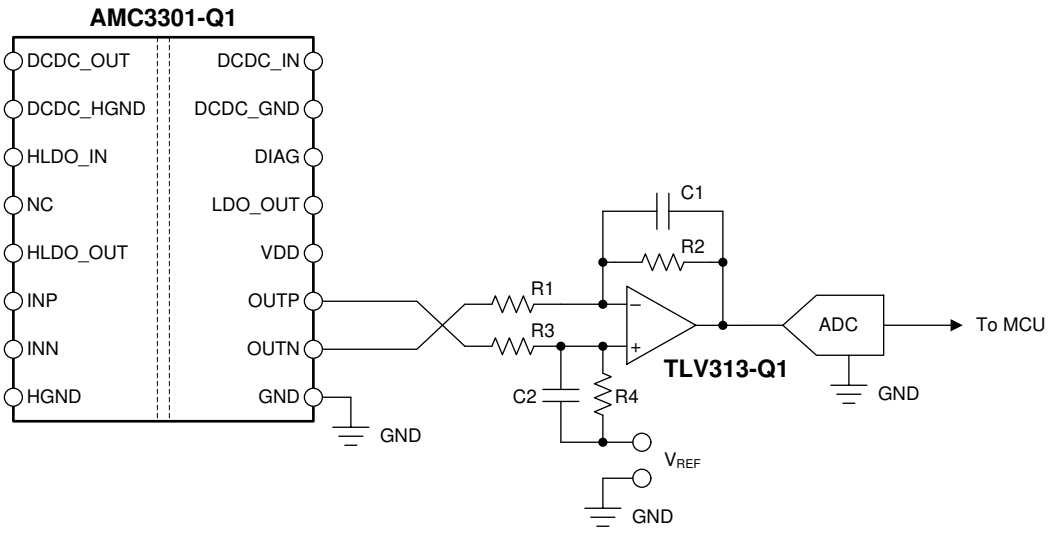


图 8-3. Connecting the AMC3301-Q1 Output to a Single-Ended Input ADC

For more information on the general procedure to design the filtering and driving stages of successive-approximation-register (SAR) ADCs, see the *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* reference guide and *18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guide, available for download at www.ti.com.

8.2.4 Application Curve

In frequency inverter applications, the power switches must be protected in case of an overcurrent condition. To allow for fast powering off of the system, a low delay caused by the isolated amplifier is required. 图 8-4 shows the typical full-scale step response of the AMC3301-Q1. Consider the delay of the required window comparator and the MCU to calculate the overall response time of the system.

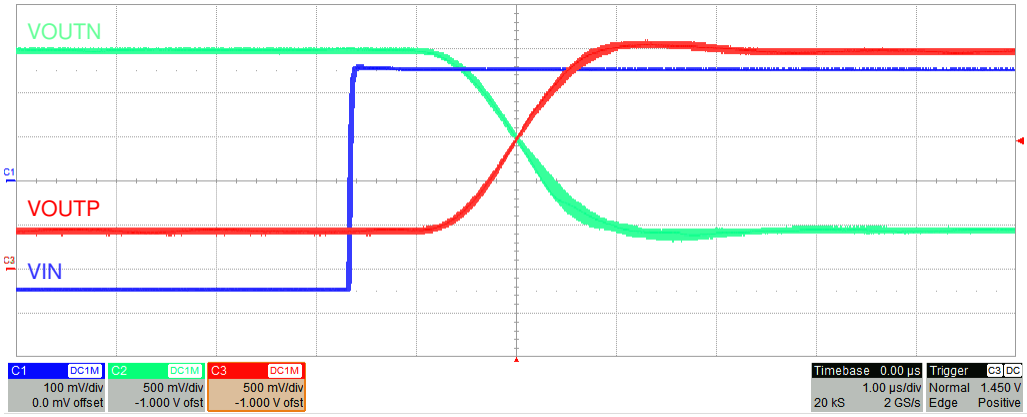


图 8-4. Step Response of the AMC3301-Q1

8.3 What To Do and What Not To Do

Do not leave the analog inputs INP and INN of the AMC3301-Q1 unconnected (floating) when the device is powered up. If the device inputs are left floating, the input bias current may drive the inputs to a positive value that exceeds the operating common-mode input voltage and the output of the device is undetermined.

Connect the negative input (INN) to the high-side ground (HGND), either by a hard short or through a resistive path. A DC current path between INN and HGND is required to define the input common-mode voltage. Take care not to exceed the input common-mode range as specified in the *Recommended Operating Conditions* table. For best accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor rather than shorting AGND to INN directly at the input to the device. See the *Layout* section for more details.

The high-side LDO can source a limited amount of current (I_H) to power external circuitry. Take care not to overload the high-side LDO.

The low-side LDO does not output a constant voltage and is not intended for powering any external circuitry. Do not connect any external load to the HLDO_OUT pin.

9 Power Supply Recommendations

The AMC3301-Q1 is powered from the low-side power supply (VDD) with a nominal value of 3.3 V or 5 V. TI recommends a low-ESR decoupling capacitor of 1 nF (C8 in 图 9-1) placed as close as possible to the VDD pin, followed by a 1-µF capacitor (C9) to filter this power-supply path.

The low-side of the DC/DC converter is decoupled with a low-ESR 100-nF capacitor (C4) positioned close to the device between the DCDC_IN and DCDC_GND pins. Use a 1-µF capacitor (C2) to decouple the high side in addition to a low-ESR, 1-nF capacitor (C3) placed as close as possible to the device and connected to the DCDC_OUT and DCDC_HGND pins.

For the high-side LDO, use low-ESR capacitors of 1-nF (C6), placed as close as possible to the AMC3301-Q1, followed by a 100-nF decoupling capacitor (C5).

The ground reference for the high-side (HGND) is derived from the terminal of the shunt resistor which is connected to the negative input (INN) of the device. For best DC accuracy, use a separate trace to make this connection instead of shorting HGND to INN directly at the device input. The high-side DC/DC ground terminal (DCDC_HGND) is shorted to HGND directly at the device pins.

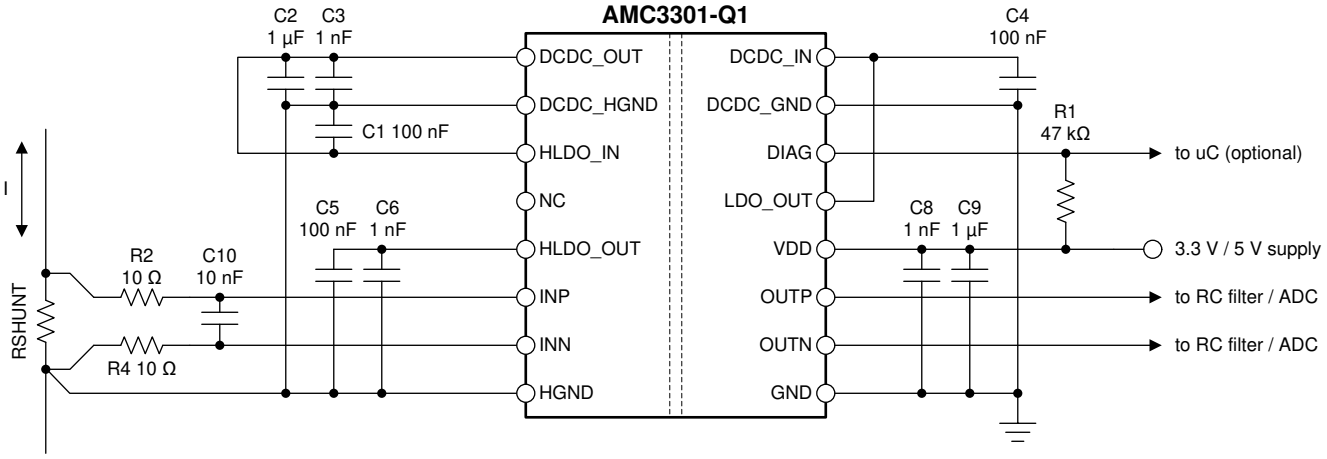


图 9-1. Decoupling the AMC3301-Q1

Capacitors must provide adequate *effective* capacitance under the applicable DC bias conditions they experience in the application. Multilayer ceramic capacitors (MLCC) typically exhibit only a fraction of their nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

表 9-1 lists components suitable for use with the AMC3301-Q1. This list is not exhaustive. Other components may exist that are equally suitable (or better), however these listed components have been validated during the development of the AMC3301-Q1.

表 9-1. Recommended External Components

DESCRIPTION		PART NUMBER	MANUFACTURER	SIZE (EIA, L x W)
VDD				
C8	1 nF ± 10%, X7R, 50 V	12065C102KAT2A	AVX	1206, 3.2 mm x 1.6 mm
C9	1 µF ± 10%, X7R, 25 V	12063C105KAT2A	AVX	1206, 3.2 mm x 1.6 mm
DC/DC CONVERTER				
C4	100 nF ± 10%, X7R, 50 V	C0603C104K5RACAUTO	Kemet	0603, 1.6 mm x 0.8 mm
C3	1 nF ± 10%, X7R, 50 V	C0603C102K5RACTU	Kemet	0603, 1.6 mm x 0.8 mm
C2	1 µF ± 10%, X7R, 25 V	CGA3E1X7R1E105K080AC	TDK	0603, 1.6 mm x 0.8 mm
HLDO				
C1	100 nF ± 10%, X7R, 50 V	C0603C104K5RACAUTO	Kemet	0603, 1.6 mm x 0.8 mm
C5	100 nF ± 5%, NP0, 50 V	C3216NP01H104J160AA	TDK	1206, 3.2 mm x 1.6 mm
C6	1 nF ± 10%, X7R, 50 V	12065C102KAT2A	AVX	1206, 3.2 mm x 1.6 mm

10 Layout

10.1 Layout Guidelines

图 10-1 shows a layout recommendation with the critical placement of the decoupling capacitors. The same component reference designators are used as in the *Power Supply Recommendations* section. Decoupling capacitors are placed as close as possible to the AMC3301-Q1 supply pins. For best performance, place the shunt resistor close to the INP and INN inputs of the AMC3301-Q1 and keep the layout of both connections symmetrical.

To avoid causing errors in the measurement by the input bias currents of the AMC3301-Q1, connect the high-side ground pin (HGND) to the INN-side of the shunt resistor. Use a separate trace in the layout to make this connection to maintain equal currents in the INN and INP traces.

10.2 Layout Example

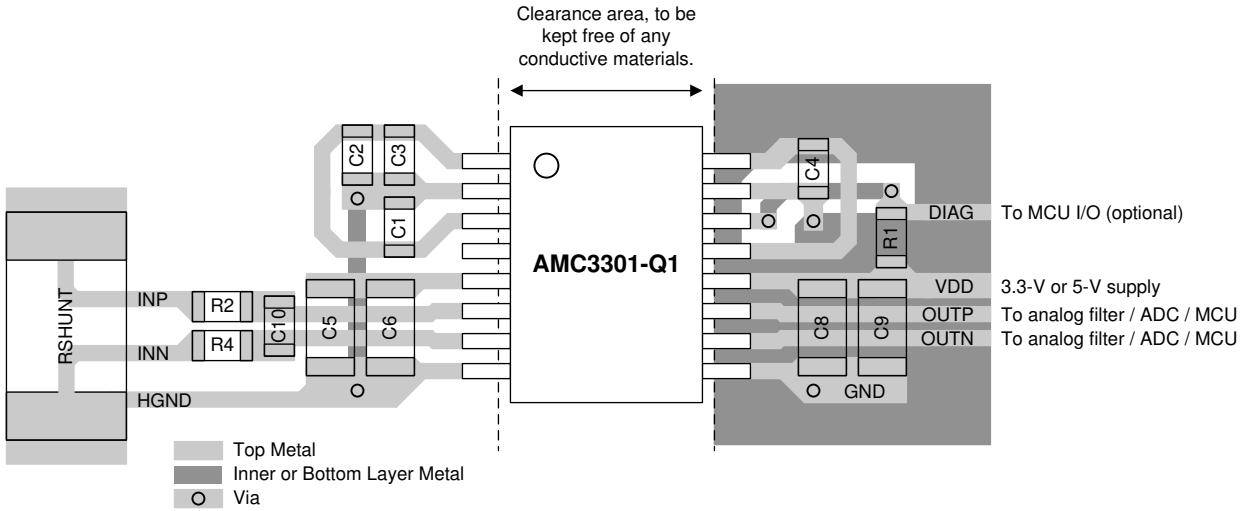


图 10-1. Recommended Layout of the AMC3301-Q1

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

Texas Instruments, *Isolation Glossary*

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application report
- Texas Instruments, *AMC3330-Q1 Precision, ±1-V Input, Reinforced Isolated Amplifier* data sheet
- Texas Instruments, *TLVx313-Q1 Low-Power, Rail-to-Rail In/Out, 750-µV Typical Offset, 1-MHz Operational Amplifier for Cost-Sensitive Systems* data sheet
- Texas Instruments, *18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* reference guide
- Texas Instruments, *18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guide

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 支持资源

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AMC3301QDWERQ1	Active	Production	SOIC (DWE) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC3301Q
AMC3301QDWERQ1.A	Active	Production	SOIC (DWE) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC3301Q
AMC3301QDWERQ1.B	Active	Production	SOIC (DWE) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF AMC3301-Q1 :

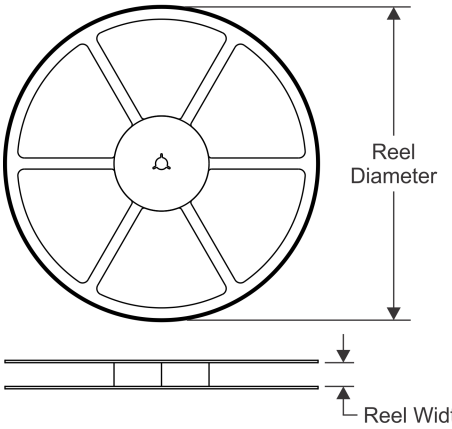
- Catalog : AMC3301

NOTE: Qualified Version Definitions:

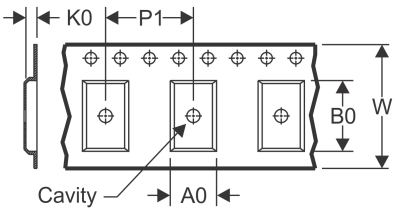
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

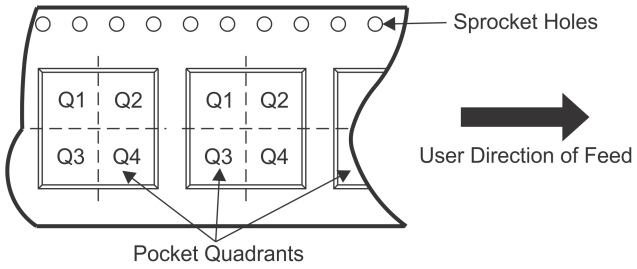


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

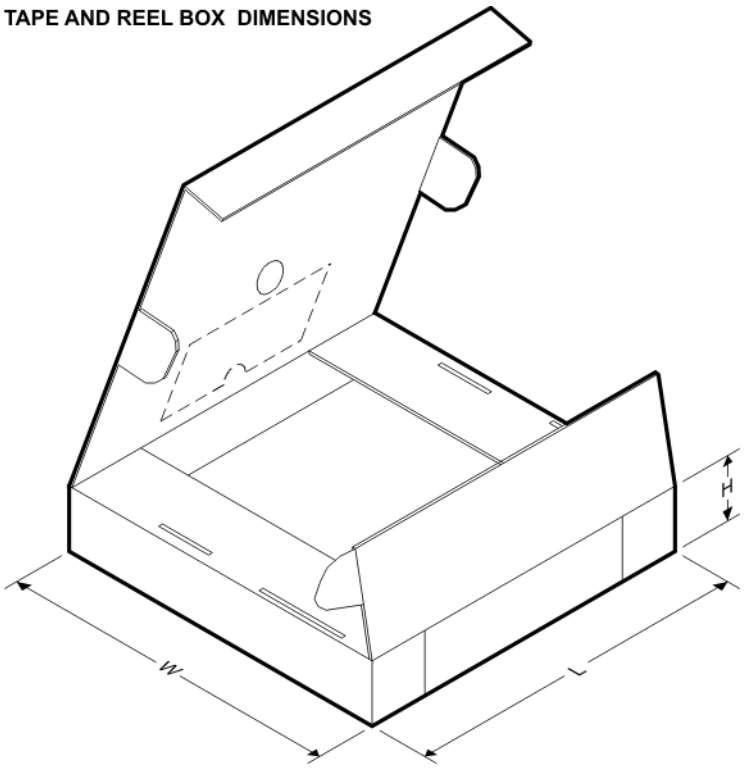
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

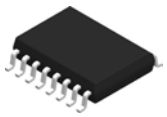
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC3301QDWERQ1	SOIC	DWE	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC3301QDWERQ1	SOIC	DWE	16	2000	350.0	350.0	43.0

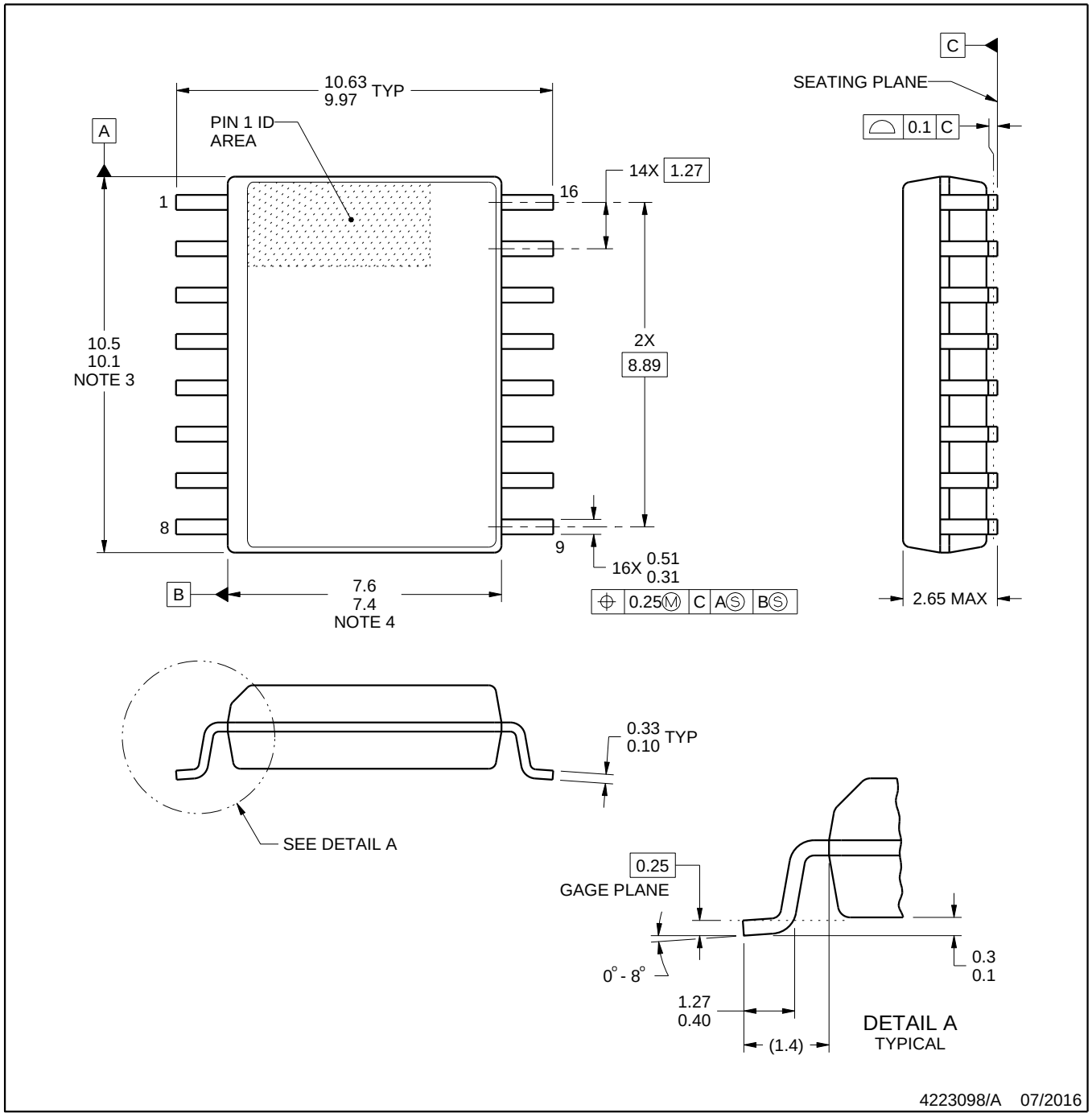


PACKAGE OUTLINE

DWE0016A

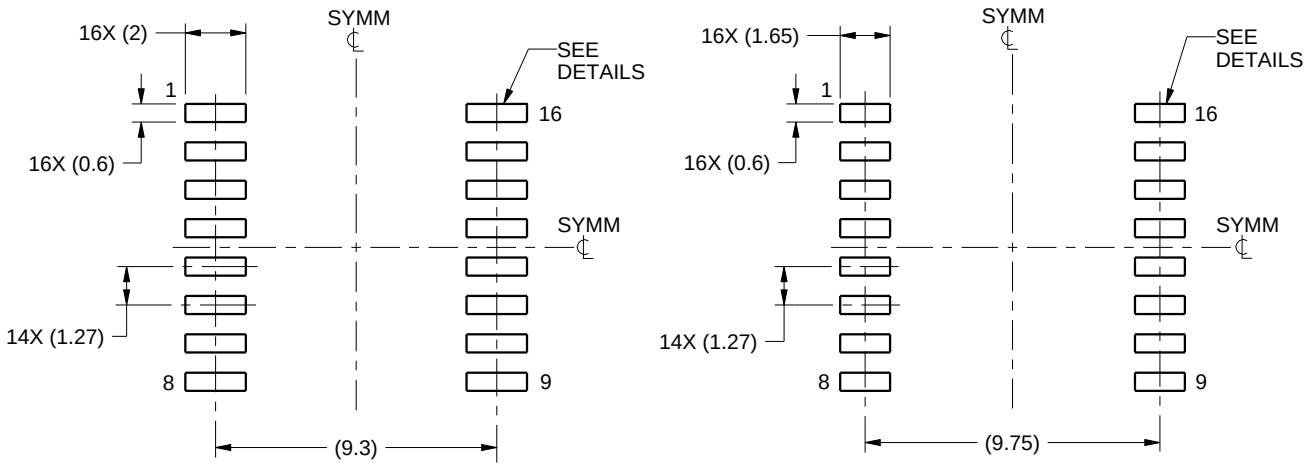
SOIC - 2.65 mm max height

SOIC



NOTES:

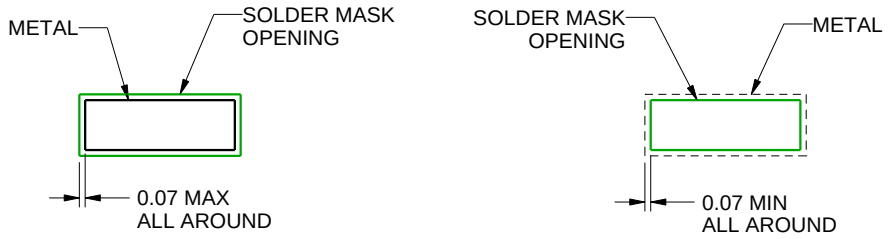
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

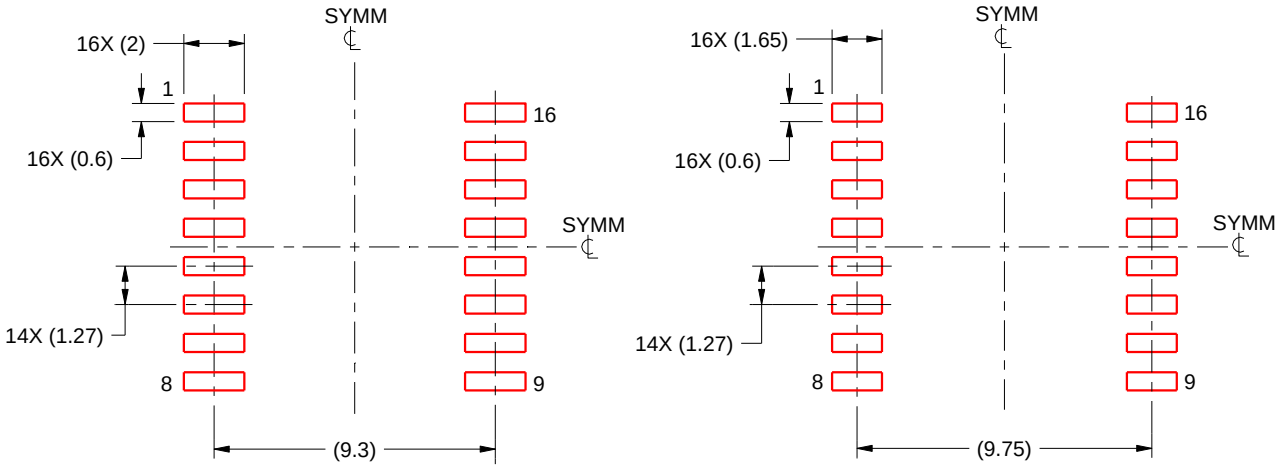
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4223098/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4223098/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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