

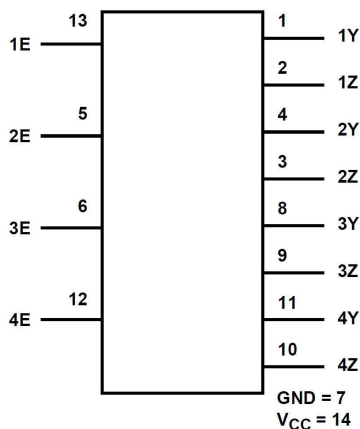
高速 CMOS 逻辑四路双向开关

1 特性

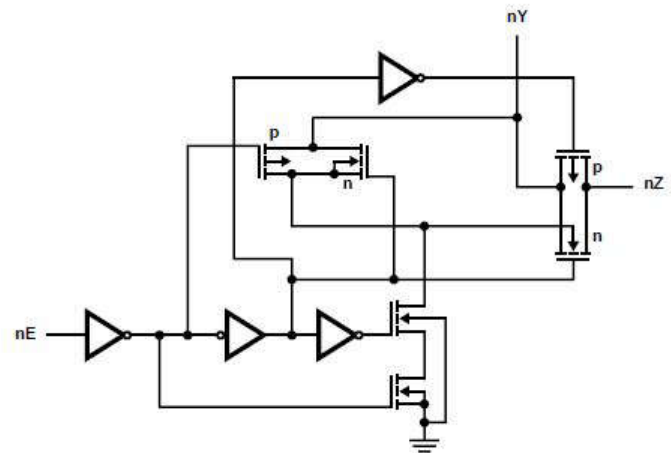
- 宽模拟输入电压范围：
0V 至 10V
- 低导通电阻：
 - $V_{CC} = 4.5V$: 25Ω
 - $V_{CC} = 9V$: 15Ω
- 快速开关和传播延迟时间
- 低关断漏电流
- 宽工作温度范围：
-55°C 至 125°C
- HC 类型：
 - 工作电压为 2 V 至 10 V
 - 高抗噪性：当 $V_{CC} = 5V$ 和 10V 时， $N_{IL} = 30\%$ ， $N_{IH} = V_{CC}$ 的 30%
- HCT 类型：
 - 直接 LSTTL 输入逻辑兼容性， $V_{IL} = 0.8V$ (最大值)， $V_{IH} = 2V$ (最小值)
 - CMOS 输入兼容性，在 V_{OL} 、 V_{OH} 时， $I_I \leq 1\mu A$

2 应用

- 模拟信号开关和多路复用：信号门控、调制器、静噪控制、解调器、斩波器、换向开关
- 数字信号开关和多路复用：模数和数模转换
- 频率、阻抗、相位和模拟信号增益的数字控制
- 楼宇自动化



功能方框图



逻辑图

3 说明

HC4066 和 CD74HCT4066 器件包含四个独立的数控模拟开关，这些开关使用硅栅 CMOS 技术并借助标准 CMOS 集成电路的低功耗特性来实现与 LSTTL 接近的运行速度。

这些开关具有金属栅 CD4066B 器件的线性导通电阻特性。每个开关由其控制输入端的高电平电压进行开通。

器件信息

器件型号	温度范围 (°C)	封装 ⁽¹⁾
CD74HC4066	-55 至 125	D (SOIC, 14)
	-55 至 125	PW (TSSOP, 14)
CD74HCT4066	-55 至 125	D (SOIC, 14)

(1) 有关更多信息，请参阅节 19。



Table of Contents

1 特性	1	15 Test Circuits and Waveforms	11
2 应用	1	16 Detailed Description	12
3 说明	1	16.1 Functional Block Diagram.....	12
4 Pin Configuration and Functions	3	16.2 Device Functional Modes.....	12
5 Absolute Maximum Ratings	4	17 Device and Documentation Support	13
6 ESD Ratings	4	17.1 接收文档更新通知.....	13
7 Thermal Information	4	17.2 支持资源.....	13
8 Recommended Operating Conditions	5	17.3 Trademarks.....	13
9 Electrical Characteristics: HC Devices	6	17.4 静电放电警告.....	13
10 Electrical Characteristics: HCT Devices	8	17.5 术语表.....	13
11 Switching Characteristics HC	9	18 Revision History	13
12 Switching Characteristics HCT	10	19 Mechanical, Packaging, and Orderable Information	13
13 Analog Channel Specifications	10		
14 Analog Test Circuits	11		

4 Pin Configuration and Functions

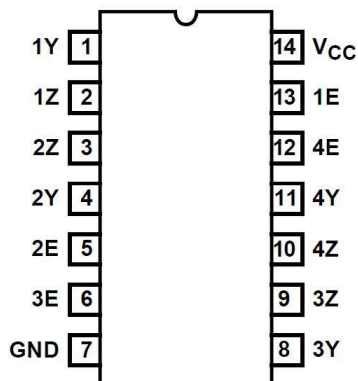


图 4-1. CD74HC4066 D or PW Package, 14-Pin SOIC or TSSOP CD74HCT4066 r D Package, 14-Pin SOIC (Top View)

表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
1Y	1	I/O	Input/Output for Switch 1
1Z	2	I/O	Input/Output for Switch 1
2Z	3	I/O	Input/Output for Switch 2
2Y	4	I/O	Input/Output for Switch 2
2E	5	I	Control pin for Switch 2
3E	6	I	Control pin for Switch 3
GND	7	-	Ground Pin
3Y	8	I/O	Input/Output for Switch 3
3Z	9	I/O	Input/Output for Switch 3
4Z	10	I/O	Input/Output for Switch 4
4Y	11	I/O	Input/Output for Switch 4
4E	12	I	Control pin for Switch 4
1E	13	I	Control pin for Switch 1
V _{CC}	14	-	Power Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

			MIN	MAX	UNIT
V _{CC} HCT	DC Supply voltage		- 0.5	7	V
V _{CC} HC ⁽¹⁾			-0.5	10.5	V
I _{IK}	DC input diode current	For V _I < -0.5V or V _I > V _{CC} + 0.5V	- 20	20	mA
I _O	DC switch current ⁽²⁾	For V _I < -0.5V or V _I > V _{CC} + 0.5V	-20	20	mA
I _{OK}	DC Output diode current	For V _O < -0.5V or V _O > V _{CC} + -0.5V	-25	25	mA
DC Output Source or Sink Current per Output Pin, I _O	For V _O > -0.5V or V _O < V _{CC} + -0.5V		- 25	25	mA
I _{CC}	DC V _{CC} or ground current		- 50	50	mA
T _{JMAX}	Maximum junction temperature (Plastic Package)			150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) In certain applications, the external load-resistor current may include both VCC and signal-line components. To avoid drawing VCC current when switch current flows into the transmission gate inputs, (terminals 1, 4, 8 and 11) the voltage drop across the bidirectional switch must not exceed 0.6V (calculated from RON values shown in the DC Electrical Specifications Table). No VCC current will flow through RL if the switch current flows into terminals 2, 3, 9 and 10. 2.

6 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	±500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±200	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7 Thermal Information

THERMAL METRIC		CD74HCx4066		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	108.4	133.9	°C/W

8 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage range (T _A = full package temperature range)(2)	CD54 and 74HC types	2		10	V
		CD54 and 74HCT types	4.5		5.5	
V _{IS}	Analog switch I/O voltage		0		V _{CC}	V
T _A	Ambient temperature		– 55		125	°C
t _r , t _f	Input rise and fall times	2 V	0		1000	ns
		4.5 V	0		500	
		6 V	0		400	

9 Electrical Characteristics: HC Devices

Over operating free-air temperature range, $V_{\text{SUPPLY}} = \pm 5 \text{ V}$, and $R_L = 100 \ \Omega$, (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
SIGNAL INPUTS (V _{IS}) AND OUTPUTS (V _{OS})									
		V _{IS} (V)	V _I (V)	V _{CC} (V)	T _A				
High Level Input Voltage	V _{IH}			2	25°C			1.5	V
					– 40°C to +85°C			1.5	
					– 55°C to +125°C			1.5	
				4.5	25°C			3.15	
					– 40°C to +85°C			3.15	
					– 55°C to +125°C			3.15	
				9	25°C			6.3	
					– 40°C to +85°C			6.3	
					– 55°C to +125°C			6.3	
Low Level Input Voltage	V _{IL}			2	25°C	0.5		V	
					– 40°C to +85°C	0.5			
					– 55°C to +125°C	0.5			
				4.5	25°C	1.35			
					– 40°C to +85°C	1.35			
					– 55°C to +125°C	1.35			
				9	25°C	2.7			
					– 40°C to +85°C	2.7			
					– 55°C to +125°C	2.7			

Over operating free-air temperature range, $V_{SUPPLY} = \pm 5\text{ V}$, and $R_L = 100\ \Omega$, (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
"ON" Resistance IO = 1mA	RON	VCC or GND	VCC	4.5	25°C		25	80	Ω
					– 40°C to +85°C		106		
					– 55°C to +125°C		128		
				6	25°C		20	75	
					– 40°C to +85°C		94		
					– 55°C to +125°C		113		
				9	25°C		15	60	
					– 40°C to +85°C		78		
					– 55°C to +125°C		95		
		VCC to GND	VCC	4.5	25°C		35	95	Ω
					– 40°C to +85°C		118		
					– 55°C to +125°C		142		
				6	25°C		24	84	
					– 40°C to +85°C		105		
					– 55°C to +125°C		126		
				9	25°C		31	70	
					– 40°C to +85°C		88		
					– 55°C to +125°C		105		
"ON" Resistance Between Any Two Switches	▲ RON		VCC	4.5	25°C		1	Ω	
			VCC	6	25°C		0.75		
			VCC	9	25°C		0.5		
Off-Switch Leakage Current	IZ	VCC or GND	VIL	10	25°C		±0.1	μA	
					– 55°C to 85°C		±1		
					– 55°C to 125°C		±1		
Input Leakage Current (Any Control)	IIL		VCC or GND	10	25°C		±0.1	μA	
					– 55°C to 85°C		±1		
					– 55°C to 125°C		±1		
Quiescent Device Current	ICC		VCC or GND	6	25°C		18.5	μA	
					– 55°C to 85°C		20		
					– 55°C to 125°C		40		
				10	25°C		35		
					– 55°C to 85°C		160		
					– 55°C to 125°C		320		
CONTROL (ADDRESS OR INHIBIT), VC									

(1) Peak-to-Peak voltage symmetrical about $(V_{DD} - V_{EE}) / 2$.

10 Electrical Characteristics: HCT Devices

Over operating free-air temperature range, $V_{\text{SUPPLY}} = \pm 5 \text{ V}$, and $R_L = 100 \, \Omega$, (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
SIGNAL INPUTS (V _{IS}) AND OUTPUTS (V _{OS})									
		V _{IS} (V)	V _I (V)	V _{CC} (V)	T _A				
High Level Input Voltage	V _{IH}			4.5 to 5.5	25°C	2		V	
					- 40°C to +85°C	2			
					- 55°C to +125°C	2			
Low Level Input Voltage	V _{IL}				25°C	0.8		V	
					- 40°C to +85°C	0.8			
					- 55°C to +125°C	0.8			
"ON" Resistance IO = 1mA	R _{ON}	V _{CC} or GND	V _{CC}	4.5	25°C	25	80	Ω	
					- 40°C to +85°C	106			
					- 55°C to +125°C	128			
		V _{CC} to GND			25°C	35	95	Ω	
					- 40°C to +85°C	118			
					- 55°C to +125°C	142			
"ON" Resistance Between Any Two Switches	▲ R _{ON}		V _{CC}	4.5	25°C	1		Ω	
Off-Switch Leakage Current	I _Z	V _{CC} or GND	V _{IL}	5.5	25°C	±0.1		μA	
					- 55°C to 85°C	±1			
					- 55°C to 125°C	±1			
Input Leakage Current (Any Control)	I _{IL}		V _{CC} or GND	5.5	25°C	±0.1		μA	
					- 55°C to 85°C	±1			
					- 55°C to 125°C	±1			
Quiescent Device Current	I _{CC}		V _{CC} or GND	5.5	25°C	2		μA	
					- 55°C to 85°C	20			
					- 55°C to 125°C	40			
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	▲ I _{CC}		V _{CC} - 2.1	4.5 to 5.5	25°C	100	360		
					- 55°C to 85°C	450			
					- 55°C to 125°C	490			
CONTROL (ADDRESS OR INHIBIT), V _C									

(1) Peak-to-Peak voltage symmetrical about $(V_{\text{DD}} - V_{\text{EE}}) / 2$.

11 Switching Characteristics HC

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions		C_L (pF)	MIN	NOM	MAX	UNIT
Propagation Delay Time Switch In to Out	t_{PHL}, t_{PLH}	2	25°C	50			60	ns
			-40°C to 85°C				75	ns
			-55°C to 125°C				90	ns
		4.5	25°C				12	ns
			-40°C to 85°C				15	ns
			-55°C to 125°C				18	ns
		9	25°C				8	ns
			-40°C to 85°C				11	ns
			-55°C to 125°C				13	ns
		5	25°C	15		4		ns
Propagation Delay Time Switch Turn On Delay	t_{PZH}, t_{PZL}	2	25°C	50			100	ns
			-40°C to 85°C				125	ns
			-55°C to 125°C				150	ns
		4.5	25°C				20	ns
			-40°C to 85°C				25	ns
			-55°C to 125°C				30	ns
		9	25°C				12	ns
			-40°C to 85°C				15	ns
			-55°C to 125°C				18	ns
		5	25°C	15		4		ns
Propagation Delay Time Switch Turn Off Delay	t_{PHZ}, t_{PLZ}	2	25°C	50			150	ns
			-40°C to 85°C				190	ns
			-55°C to 125°C				225	ns
		4.5	25°C				30	ns
			-40°C to 85°C				38	ns
			-55°C to 125°C				45	ns
		9	25°C				24	ns
			-40°C to 85°C				30	ns
			-55°C to 125°C				36	ns
		5	25°C	15		9.5		ns
Input (Control) Capacitance	C_i		25°C				10	pF
			-40°C to 85°C				10	
			-55°C to 125°C				10	
C_{PD} Power dissipation capacitance(1)	C_{PD}	5	25°C			25		

12 Switching Characteristics HCT

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions		C _L (pF)	MIN	NOM	MAX	UNIT
Propagation Delay Time Switch In to Out	t _{PHL} , t _{PLH}	4.5	25°C	50			12	ns
			-40°C to 85°C				15	ns
			-55°C to 125°C				18	ns
		5	25°C	15		1.3		ns
Propagation Delay Time Switch Turn On Delay	t _{PZH} , t _{PZL}	4.5	25°C	50			24	ns
			-40°C to 85°C				30	ns
			-55°C to 125°C				36	ns
		5	25°C	15		5		ns
Propagation Delay Time Switch Turn Off Delay	t _{PHZ} , t _{PLZ}	4.5	25°C	50			35	ns
			-40°C to 85°C				44	ns
			-55°C to 125°C				53	ns
		5	25°C	15		5.5		ns
Input (Control) Capacitance	C _I		25°C				10	pF
			-40°C to 85°C				10	
			-55°C to 125°C				10	
C _{PD} Power dissipation capacitance(1)	C _{PD}	5	25°C			38		

13 Analog Channel Specifications

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions		V _{CC} (V)	HC	HCT	UNIT
Switch Frequency Response Bandwidth at -3dB				4.5	200	200	MHz
Cross Talk Between Any Two Switches				4.5	-72	-72	dB
Total Harmonic Distortion		1kHz, V _{IS} =4V _{PP}		4.5	0.022	0.023	%
		1kHz, V _{IS} =8V _{PP}		9	0.019	N/A	%
Control to Switch Feedthrough Noise	Control to Switch Feedthrough Noise			4.5	200	130	mV
Control to Switch Feedthrough Noise				4.5	200	130	mV
				9	550	N/A	
Switch "OFF" signal feedthrough				4.5	-72	-72	dB
C _I Switch input capacitance					5	5	pF

14 Analog Test Circuits

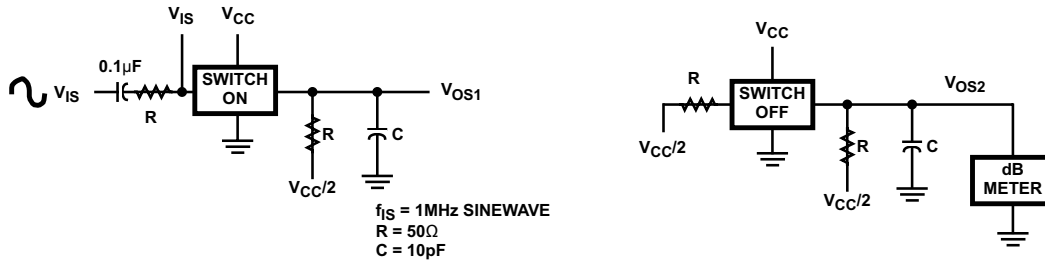


图 14-1. Crosstalk Between Two Switches Test Circuit

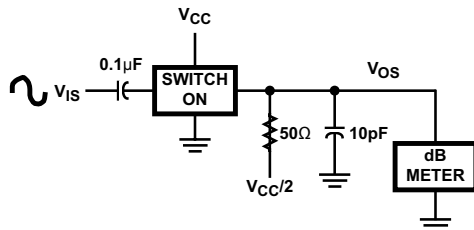


图 14-2. Frequency Response Test Circuit

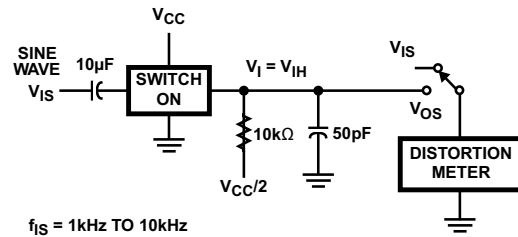


图 14-3. Total Harmonic Distortion Test Circuit

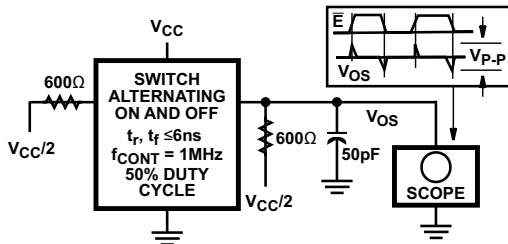


图 14-4. Control-To-Switch Feedthrough Noise Test Circuit

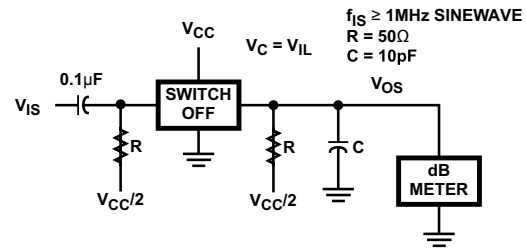


图 14-5. Switch OFF Signal Feedthrough

15 Test Circuits and Waveforms

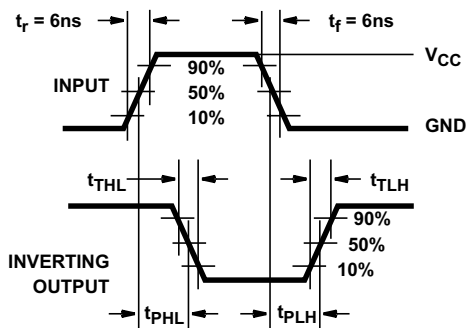


图 15-1. HC Transition Times and Propagation Delay Times, Combination Logic

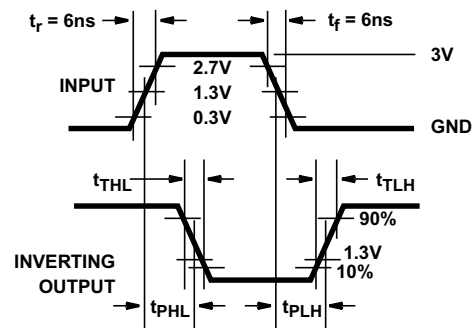


图 15-2. HCT Transition Times and Propagation Delay Times, Combination Logic

16 Detailed Description

16.1 Functional Block Diagram

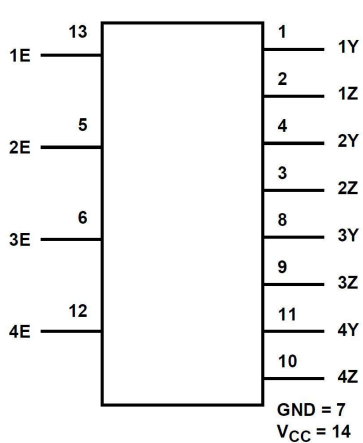


图 16-1. Functional Block Diagram

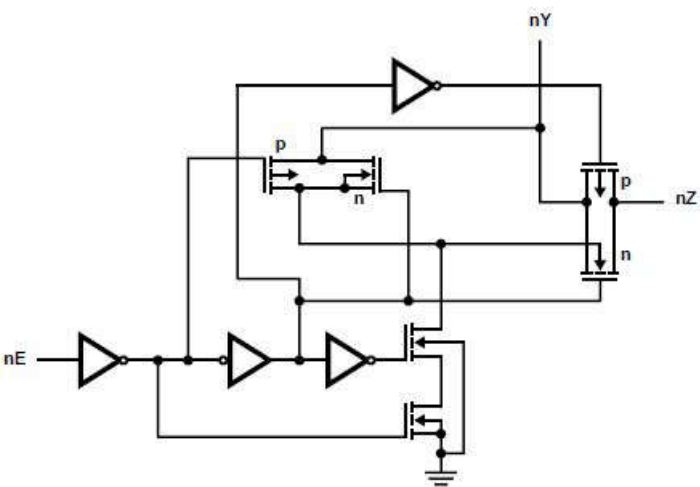


图 16-2. Logic Diagram

16.2 Device Functional Modes

表 16-1. Truth Table

INPUTnE	SWITCH
L ⁽²⁾	Off
H ⁽¹⁾	On

- (1) H = High Level
(2) L = Low Level

17 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

17.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

17.2 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

17.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

17.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

17.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

18 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (August 2003) to Revision E (July 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• Updated thermal information.....	4
• Updated electrical specifications.....	6
• Updated switching specifications.....	9
• Updated analog channel specifications.....	10
• Updated ordering information.....	13

19 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8950701CA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8950701CA CD54HC4066F3A
CD54HC4066F3A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8950701CA CD54HC4066F3A
CD54HC4066F3A.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8950701CA CD54HC4066F3A
CD74HC4066E	NRND	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4066E
CD74HC4066E.A	NRND	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4066E
CD74HC4066EE4	NRND	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4066E
CD74HC4066M	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-55 to 125	HC4066M
CD74HC4066M96	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4066M
CD74HC4066M96.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4066M
CD74HC4066M96E4	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4066M
CD74HC4066MT	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-55 to 125	HC4066M
CD74HC4066PWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HP4066
CD74HC4066PWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HP4066
CD74HC4066PWT	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-55 to 125	HP4066
CD74HCT4066E	NRND	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4066E
CD74HCT4066E.A	NRND	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4066E
CD74HCT4066M	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-55 to 125	HCT4066M
CD74HCT4066M96	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4066M
CD74HCT4066M96.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4066M
CD74HCT4066MT	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-55 to 125	HCT4066M

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

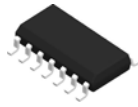
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC4066, CD74HC4066, CD74HCT4066 :

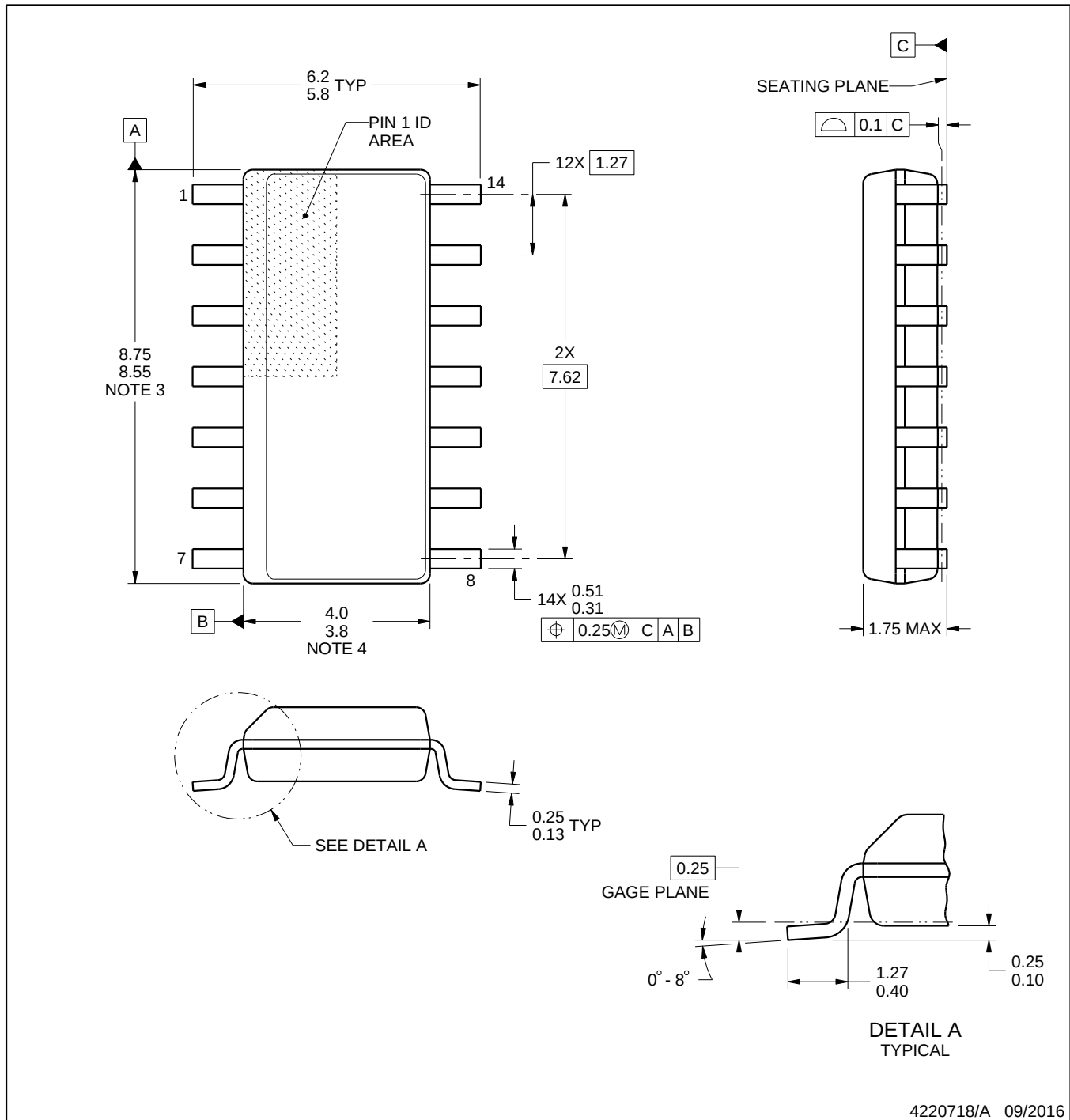
- Catalog : [CD74HC4066](#)
- Automotive : [CD74HCT4066-Q1](#)
- Military : [CD54HC4066](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT

**NOTES:**

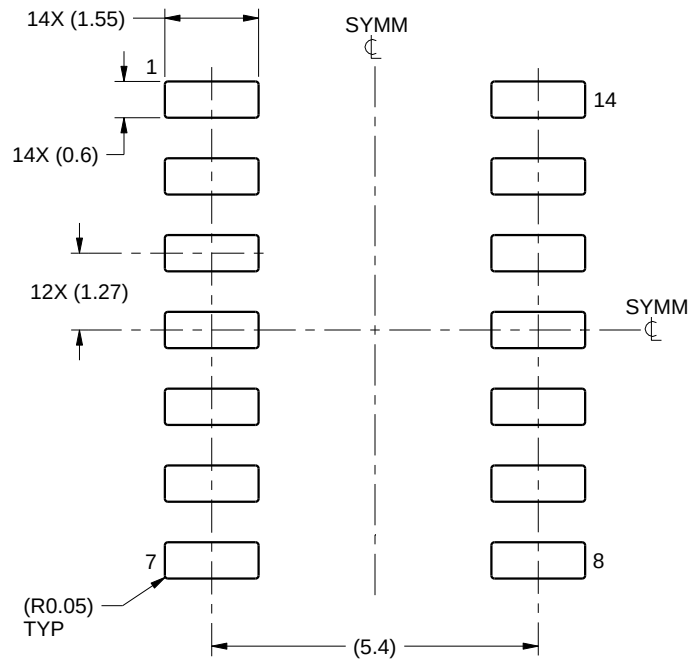
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

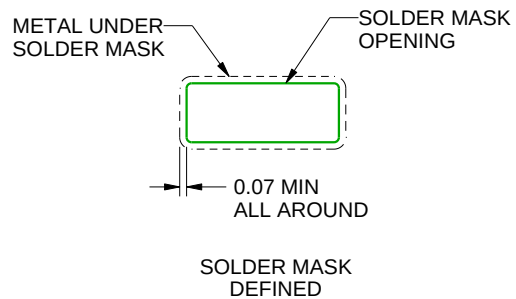
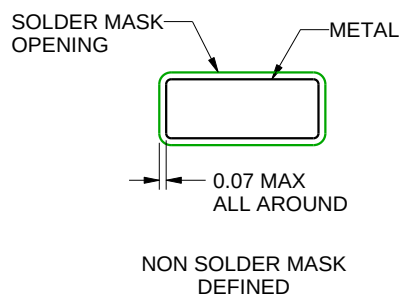
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

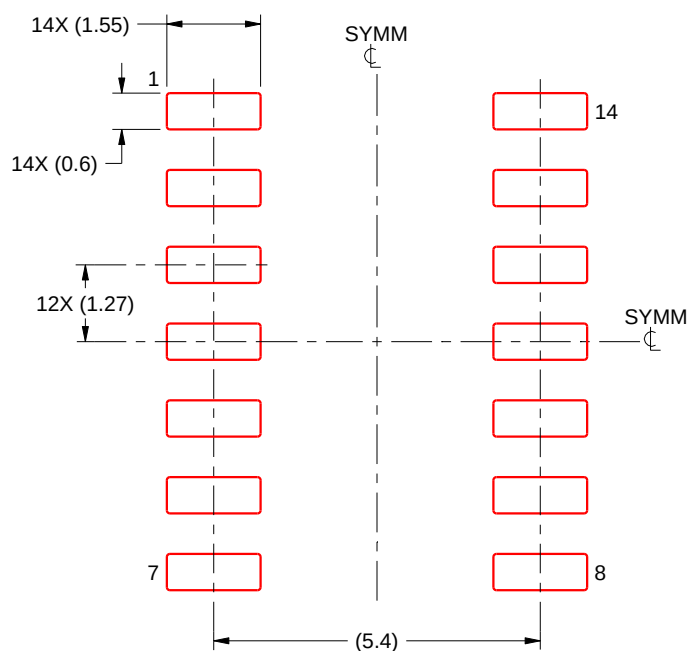
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

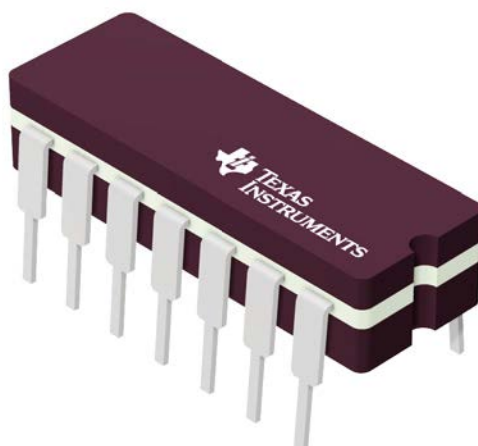
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

J 14

GENERIC PACKAGE VIEW

CDIP - 5.08 mm max height

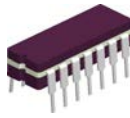
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

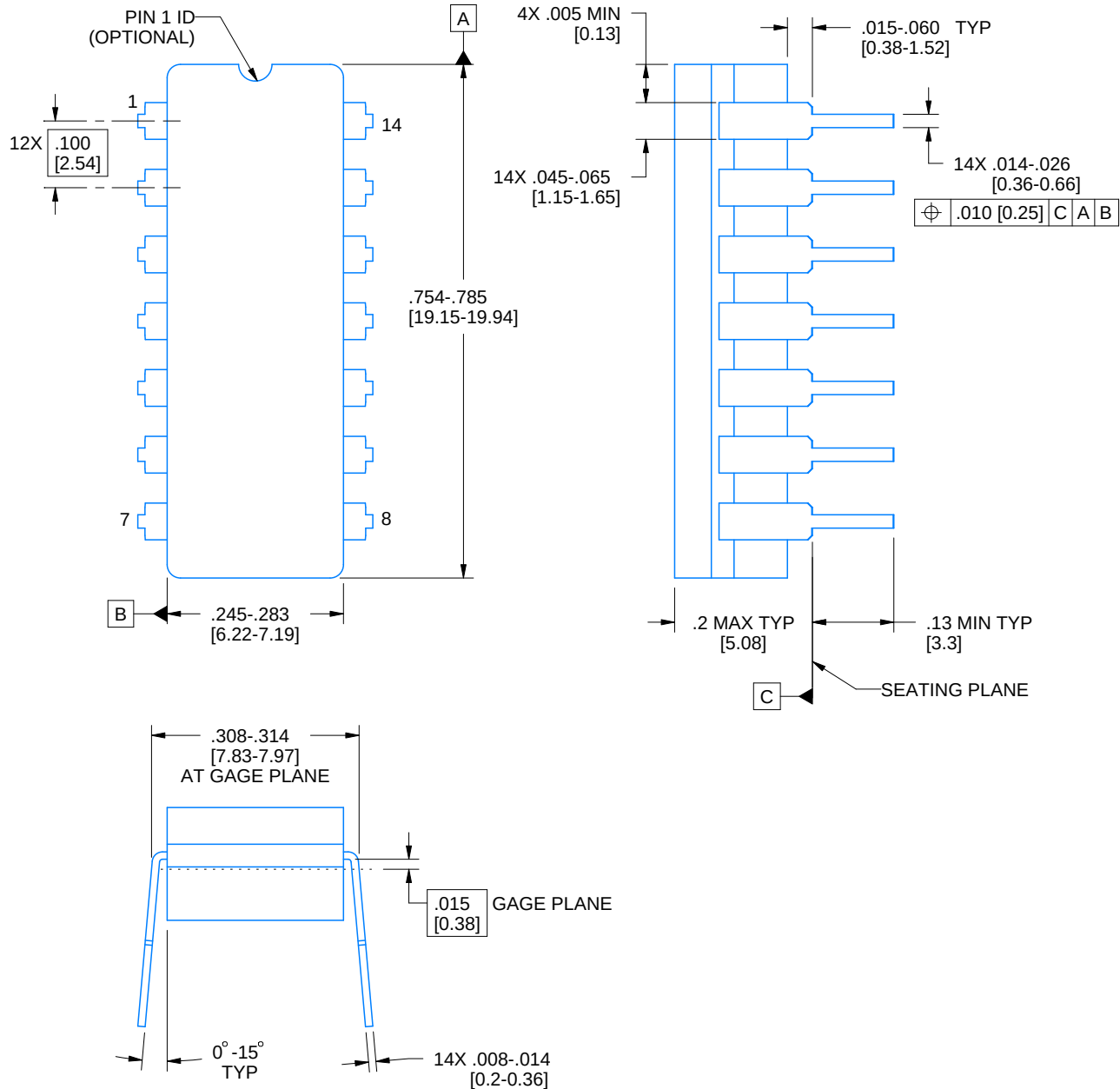
J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

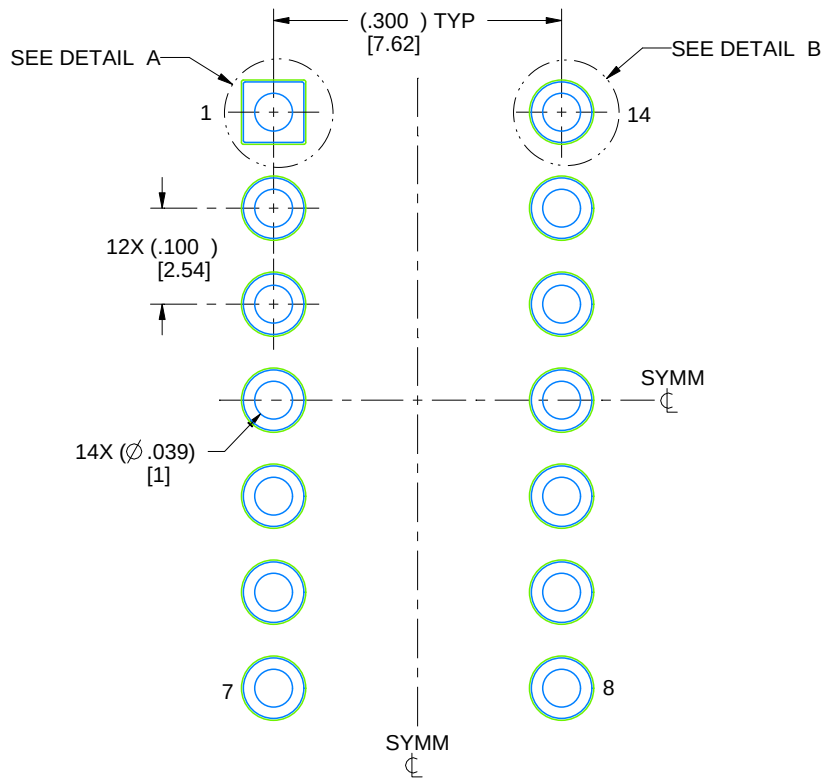
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

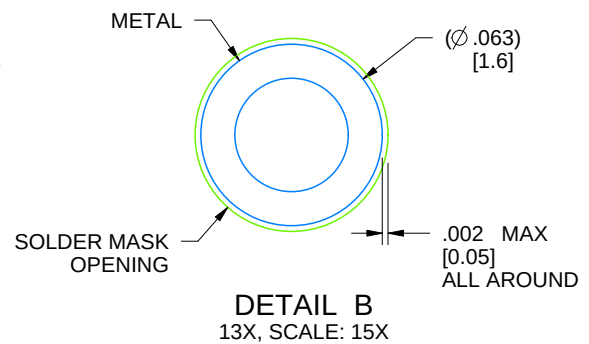
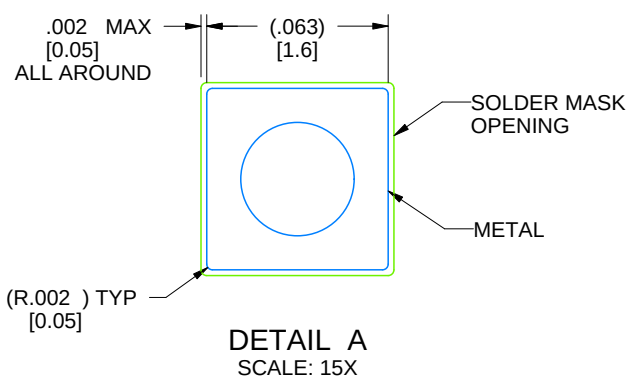
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

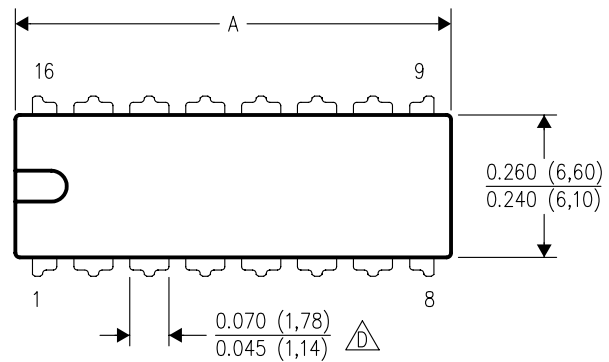


4214771/A 05/2017

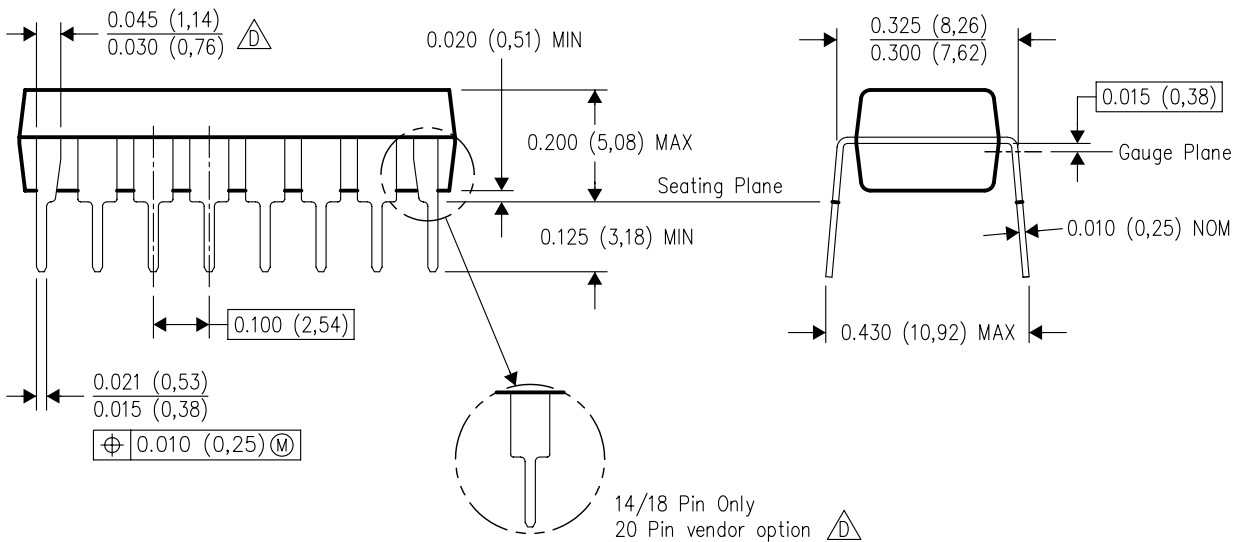
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

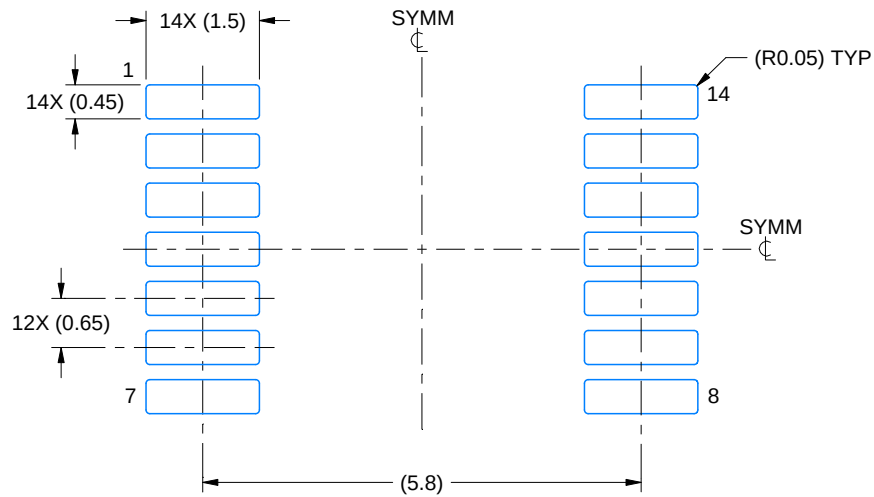
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

EXAMPLE BOARD LAYOUT

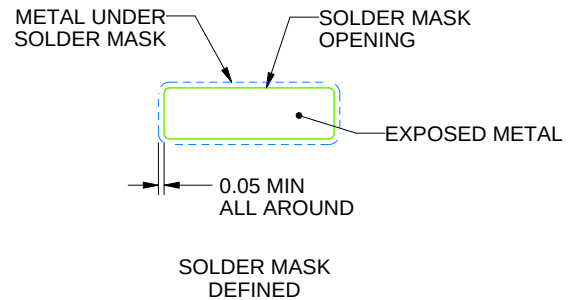
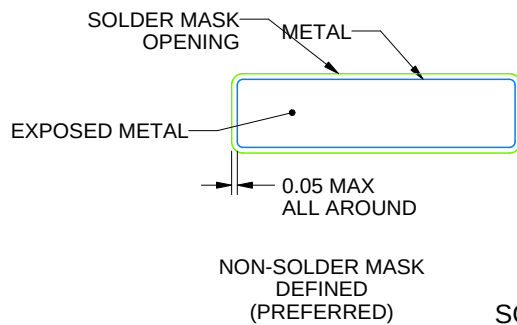
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

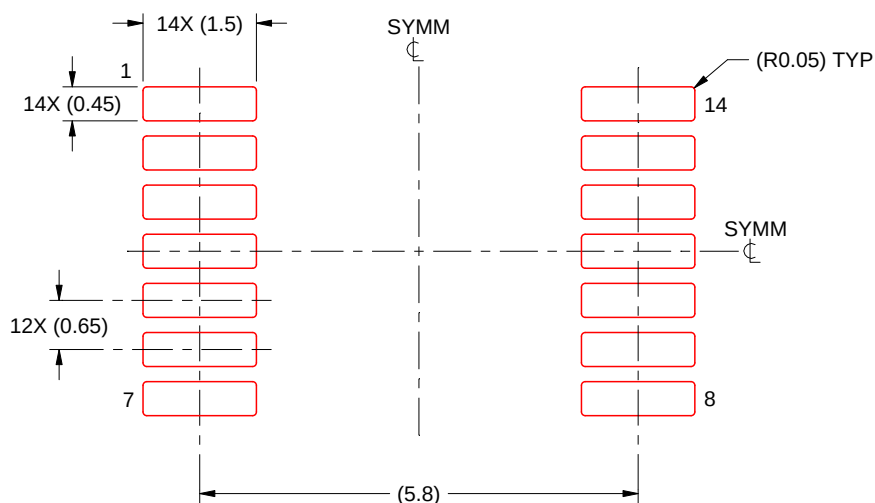
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 [TI 销售条款](#)、[TI 通用质量指南](#) 或 [ti.com](#) 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2026，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月