

# LM5161 100V 宽输入、1A 同步降压/Fly-Buck™ 转换器

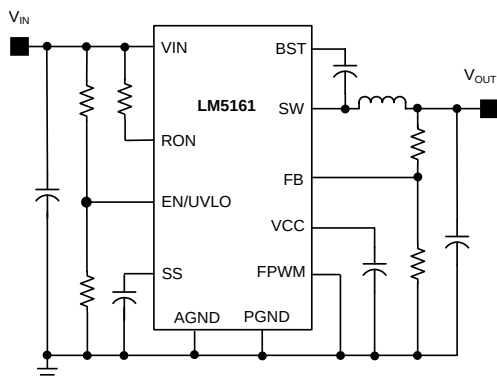
## 1 特性

- 4.5V 至 100V 宽输入电压范围
- 集成高侧和低侧开关
  - 无需肖特基二极管
- 1A 最大负载电流
- 恒定导通时间控制
  - 无外部环路补偿
  - 快速瞬态响应
- 轻载条件下可选择 DCM 降压操作
- CCM 选项支持多输出 Fly-Buck™
- 无需外部纹波电路 (FPWM = 0 时)
- 近似恒定的开关频率
- 频率最高可调节至 1MHz
- 可编程软启动时间
- 预偏置启动
- 峰值电流限制保护
- 可调输入欠压闭锁 (UVLO) 和滞后
- $\pm 1\%$  反馈电压基准
- 热关断保护
- 使用 LM5161 并借助 [WEBENCH® 电源设计器](#) 创建定制设计方案

## 2 应用

- 工业可编程逻辑控制器
- IGBT 栅极驱动偏置电源
- 电信直流/直流的初级侧和次级侧偏置
- 电子电表电力线通信
- 低功耗 (< 12W) 隔离式 DC-DC (Fly-Buck)

典型降压应用电路



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## 3 说明

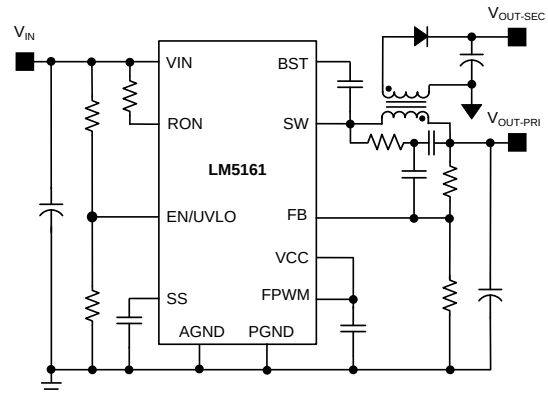
LM5161 是一款集成高侧和低侧金属氧化物半导体场效应晶体管 (MOSFET) 的 100V、1A 同步降压转换器。恒定导通时间控制方案无需环路补偿，支持快速瞬态响应下的高降压比。内部反馈放大器在完整工作温度范围保持  $\pm 1\%$  的输出电压调节率。导通时间与输入电压成反比，产生近似恒定的开关频率。峰谷电流限制电路可防止发生过载。欠压锁定 (EN/UVLO) 电路独立提供可调节输入欠电压阈值和迟滞。LM5161 通过其 FPWM 输入引脚可选择在所有负载水平下以强制连续导通模式 (CCM) 运行，或在轻载或空载条件下以断续导通模式 (DCM) 运行。在强制 CCM 下运行时，LM5161 支持多输出和隔离式 Fly-Buck 应用中，低功耗是一个关键问题。当通过编程实现 DCM 操作时，LM5161 提供严格稳压的降压输出，无需使用任何外部纹波反馈注入电路。

器件信息(1)

| 器件型号   | 封装          | 封装尺寸 (标称值)        |
|--------|-------------|-------------------|
| LM5161 | HTSSOP (14) | 5.00 mm × 4.40 mm |

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

典型 Fly-Buck 应用电路



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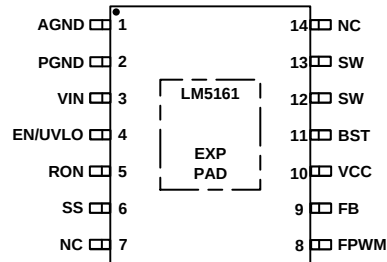
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## 4 修订历史记录

| Changes from Revision A (August 2016) to Revision B |                                                                  | Page |
|-----------------------------------------------------|------------------------------------------------------------------|------|
| •                                                   | 已添加 WEBENCH 链接; TI Designs 的顶部导航图标 .....                         | 1    |
| •                                                   | Deleted the lead temperature from the <i>Abs Max</i> table ..... | 4    |
| Changes from Original (March 2016) to Revision A    |                                                                  | Page |
| •                                                   | “产品预览”至“量产数据”版本 .....                                            | 1    |

## 5 Pin Configuration and Functions

**PWP Package  
14-Pin HTSSOP With Exposed Pad  
Top View**



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### Pin Functions

| PIN     |        | I/O | DESCRIPTION                                                                                                                                                                                        |
|---------|--------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME    | HTSSOP |     |                                                                                                                                                                                                    |
| AGND    | 1      | -   | Analog ground. Ground connection of internal control circuits.                                                                                                                                     |
| PGND    | 2      | -   | Power ground. Ground connection of the internal synchronous rectifier FET.                                                                                                                         |
| VIN     | 3      | I   | Input supply connection. Operating input range is 4.5-V to 100-V.                                                                                                                                  |
| EN/UVLO | 4      | I   | Precision enable. Input pin of undervoltage lockout (UVLO) comparator.                                                                                                                             |
| RON     | 5      | I   | On-time programming pin. A resistor between this pin and VIN sets the switch ON-time as a function of input voltage.                                                                               |
| SS      | 6      | I   | Soft start. Connect a capacitor from SS to AGND to control output rise time and limit overshoot.                                                                                                   |
| FPWM    | 8      | I   | Forced PWM logic input pin. Connect to AGND for discontinuous conduction mode (DCM) with light loads. Connect to VCC for continuous conduction mode (CCM) at all loads and Fly-Buck configuration. |
| FB      | 9      | I   | Feedback input of voltage regulation comparator.                                                                                                                                                   |
| VCC     | 10     | O   | Internal high voltage start-up regulator bypass capacitor pin.                                                                                                                                     |
| BST     | 11     | I   | Bootstrap capacitor pin. Connect a capacitor between BST and SW to bias gate driver of high-side buck FET.                                                                                         |
| SW      | 12,13  | O   | Switch node. Source connection of high side buck FET and drain connection of low-side synchronous rectifier FET.                                                                                   |
| NC      | 7,14   |     | No connection                                                                                                                                                                                      |
| EP      | -      |     | Exposed pad. Connect to AGND and printed-circuit board ground plane to improve power dissipation.                                                                                                  |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

|                                             |                              | MIN  | MAX | UNIT |
|---------------------------------------------|------------------------------|------|-----|------|
| Input voltage                               | VIN to AGND                  | −0.3 | 100 | V    |
|                                             | EN/UVLO to AGND              | −0.3 | 100 |      |
|                                             | RON to AGND                  | −0.3 | 100 |      |
|                                             | BST to AGND                  | −0.3 | 114 |      |
|                                             | VCC to AGND                  | −0.3 | 14  |      |
|                                             | FPWM to AGND                 | −0.3 | 14  |      |
|                                             | SS to AGND                   | −0.3 | 7   |      |
|                                             | FB to AGND                   | −0.3 | 7   |      |
| Output voltage                              | BST to SW                    | −0.3 | 14  | V    |
|                                             | BST to VCC                   |      | 100 |      |
|                                             | SW to AGND                   | −1.5 | 100 |      |
|                                             | SW to AGND (20-ns transient) | −3   |     |      |
| Maximum junction temperature <sup>(3)</sup> |                              | −40  | 150 | °C   |
| Storage temperature T <sub>stg</sub>        |                              | −65  | 150 | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

### 6.2 ESD Ratings

|                    |                         | VALUE                                                                          | UNIT  |
|--------------------|-------------------------|--------------------------------------------------------------------------------|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±750  |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                               | MIN | NOM | MAX | UNIT |
|-----------------------------------------------|-----|-----|-----|------|
| V <sub>IN</sub> input voltage                 | 4.5 |     | 100 | V    |
| I <sub>O</sub> output current                 |     |     | 1   | A    |
| External V <sub>CC</sub> bias voltage         | 9   |     | 13  | V    |
| Operating junction temperature <sup>(2)</sup> | −40 |     | 125 | °C   |

- (1) Recommended Operating Ratings are conditions under the device is intended to be functional. For specifications and test conditions, see [Electrical Characteristics](#).
- (2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

## 6.4 Thermal Information

See <sup>(1)</sup>

| THERMAL METRIC     |                                                             | LM5161       | UNIT |
|--------------------|-------------------------------------------------------------|--------------|------|
|                    |                                                             | PWP (HTSSOP) |      |
|                    |                                                             | 14 PINS      |      |
| $R_{\theta JA}$    | Junction-to-ambient thermal resistance <sup>(1)</sup>       | 39.3         | °C/W |
| $R_{\theta JCbot}$ | Junction-to-case (bottom) thermal resistance <sup>(1)</sup> | 2.0          | °C/W |
| $\Psi_{JB}$        | Junction-to-board thermal characteristic parameter          | 19.3         | °C/W |
| $R_{\theta JB}$    | Junction-to-board thermal resistance                        | 19.6         | °C/W |
| $R_{\theta JCTop}$ | Junction-to-case (top) thermal resistance                   | 22.8         | °C/W |
| $\Psi_{JT}$        | Junction-to-top thermal characteristic parameter            | 0.5          | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

Typical values correspond to  $T_J = 25^\circ\text{C}$ . Minimum and maximum limits apply over  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ <sup>(1)(2)</sup> for LM5161.

Unless otherwise stated,  $V_{IN} = 48\text{ V}$ .

| PARAMETER                      |                                   | TEST CONDITIONS                                         | MIN | TYP  | MAX | UNIT |
|--------------------------------|-----------------------------------|---------------------------------------------------------|-----|------|-----|------|
| <b>SUPPLY CURRENT</b>          |                                   |                                                         |     |      |     |      |
| $I_{SD}$                       | Input shutdown current            | $V_{IN} = 48\text{ V}$ , EN/UVLO = 0 V                  |     | 50   | 90  | μA   |
| $I_{OP}$                       | Input operating current           | $V_{IN} = 48\text{ V}$ , FB = 3 V, Non-switching        |     | 2.3  | 2.8 | mA   |
| <b>VCC SUPPLY</b>              |                                   |                                                         |     |      |     |      |
| $V_{CC}$                       | Bias regulator output             | $V_{IN} = 48\text{ V}$ , $I_{CC} = 20\text{ mA}$        | 6.3 | 7.3  | 8.5 | V    |
| $V_{CC}$                       | Bias regulator current limit      | $V_{IN} = 48\text{ V}$                                  | 30  |      |     | mA   |
| $V_{CC(UV)}$                   | VCC undervoltage threshold        | $V_{CC}$ rising                                         |     | 3.98 | 4.1 | V    |
| $V_{CC(HYS)}$                  | VCC undervoltage hysteresis       | $V_{CC}$ falling                                        |     | 185  |     | mV   |
| $V_{CC(LDO)}$                  | VIN - VCC dropout voltage         | $V_{IN} = 4.5\text{ V}$ , $I_{CC} = 20\text{ mA}$       |     | 200  | 340 | mV   |
| <b>HIGH-SIDE FET</b>           |                                   |                                                         |     |      |     |      |
| $R_{DS(ON)}$                   | High-side on resistance           | $V_{(BST - SW)} = 7\text{ V}$ , $I_{SW} = 0.5\text{ A}$ |     | 0.58 |     | Ω    |
| $BST_{(UV)}$                   | Bootstrap gate drive UV           | $V_{(BST - SW)}$ rising                                 |     | 2.93 | 3.6 | V    |
| $BST_{(HYS)}$                  | Gate drive UV hysteresis          | $V_{(BST - SW)}$ falling                                |     | 200  |     | mV   |
| <b>LOW-SIDE FET</b>            |                                   |                                                         |     |      |     |      |
| $R_{DS(ON)}$                   | Low-side on resistance            | $I_{SW} = 0.5\text{ A}$                                 |     | 0.24 |     | Ω    |
| <b>HIGH-SIDE CURRENT LIMIT</b> |                                   |                                                         |     |      |     |      |
| $I_{LIM(HS)}$                  | High-side current limit threshold |                                                         | 1.3 | 1.61 | 1.9 | A    |
| $T_{RES}$                      | Current limit response time       | $I_{LIM(HS)}$ threshold detect to FET turn-off          |     | 100  |     | ns   |
| $T_{OFF}$                      | Current limit forced off-time     | FB = 0 V, $V_{IN} = 72\text{ V}$                        | 13  | 16.5 | 21  | μs   |
| $T_{OFF1}$                     | Current limit forced off-time     | FB = 0.1 V, $V_{IN} = 72\text{ V}$                      | 10  | 13   | 17  | μs   |
| $T_{OFF2}$                     | Current limit forced off-time     | FB = 1 V, $V_{IN} = 72\text{ V}$                        | 2   | 2.7  | 4.1 | μs   |
| <b>LOW-SIDE CURRENT LIMIT</b>  |                                   |                                                         |     |      |     |      |
| $I_{SOURCE(LS)}$               | Sourcing current limit            |                                                         | 1.3 | 1.6  | 1.9 | A    |
| $I_{SINK(LS)}$                 | Sinking current limit             |                                                         |     | 3    |     |      |

## Electrical Characteristics (接下页)

Typical values correspond to  $T_J = 25^\circ\text{C}$ . Minimum and maximum limits apply over  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}^{(1)(2)}$  for LM5161. Unless otherwise stated,  $V_{IN} = 48\text{ V}$ .

| PARAMETER                                        |                                 | TEST CONDITIONS                     | MIN   | TYP  | MAX   | UNIT             |
|--------------------------------------------------|---------------------------------|-------------------------------------|-------|------|-------|------------------|
| <b>DIODE EMULATION</b>                           |                                 |                                     |       |      |       |                  |
| $V_{FPWM(LOW)}$                                  | FPWM input logic low            | $V_{IN} = 48\text{ V}$              |       |      | 1     | V                |
| $V_{FPWM(HIGH)}$                                 | FPWM input logic high           | $V_{IN} = 48\text{ V}$              | 3     |      |       |                  |
| $I_{ZX}$                                         | Zero cross detect current       | FPWM = 0 (Diode emulation)          |       | 22.5 |       | mA               |
| <b>REGULATION COMPARATOR</b>                     |                                 |                                     |       |      |       |                  |
| $V_{REF}$                                        | FB regulation level             | $V_{IN} = 48\text{ V}$              | 1.975 | 2    | 2.015 | V                |
| $I_{(BIAS)}$                                     | FB input bias current           | $V_{IN} = 48\text{ V}$              |       |      | 100   | nA               |
| <b>ERROR CORRECTION AMPLIFIER AND SOFT START</b> |                                 |                                     |       |      |       |                  |
| $G_M$                                            | Error amp transconductance      | FB = $V_{REF} (\pm) 10\text{ mV}$   |       | 100  |       | $\mu\text{A/V}$  |
| $I_{EA(SOURCE)}$                                 | Error amp source current        | FB = 1 V, SS = 1 V                  | 7.5   | 10   | 12.5  | $\mu\text{A}$    |
| $I_{EA(SINK)}$                                   | Error amp sink current          | FB = 5 V, SS = 2.25 V               | 7.5   | 10   | 12.5  |                  |
| $V_{(SS-FB)}$                                    | $V_{SS} - V_{FB}$ clamp voltage | FB = 1.75 V, $C_{SS} = 1\text{ nF}$ |       | 135  |       | mV               |
| $I_{SS}$                                         | Soft-start charging current     | SS = 0.5 V                          | 7.5   | 10   | 12.5  | $\mu\text{A}$    |
| <b>ENABLE/UVLO</b>                               |                                 |                                     |       |      |       |                  |
| $V_{UVLO(TH)}$                                   | UVLO threshold                  | EN/UVLO rising                      | 1.195 | 1.24 | 1.272 | V                |
| $I_{UVLO(HYS)}$                                  | UVLO hysteresis current         | EN/UVLO = 1.4 V                     | 15    | 20   | 25    | $\mu\text{A}$    |
| $V_{SD(TH)}$                                     | Shutdown mode threshold         | EN/UVLO falling                     | 0.29  | 0.35 |       | V                |
| $V_{SD(HYS)}$                                    | Shutdown threshold hysteresis   | EN/UVLO rising                      |       | 50   |       | mV               |
| <b>THERMAL SHUTDOWN</b>                          |                                 |                                     |       |      |       |                  |
| $T_{SD}$                                         | Thermal shutdown threshold      |                                     |       | 175  |       | $^\circ\text{C}$ |
| $T_{SD(HYS)}$                                    | Thermal shutdown hysteresis     |                                     |       | 20   |       | $^\circ\text{C}$ |

(1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

(2) The junction temperature ( $T_J$  in  $^\circ\text{C}$ ) is calculated from the ambient temperature ( $T_A$  in  $^\circ\text{C}$ ) and power dissipation ( $P_D$  in Watts) as follows:  $T_J = T_A + (P_D \cdot R_{\theta JA})$  where  $R_{\theta JA}$  (in  $^\circ\text{C/W}$ ) is the package thermal impedance provided in the Thermal Information section.

## 6.6 Switching Characteristics<sup>(1)</sup>

Typical values correspond to  $T_J = 25^\circ\text{C}$ . Minimum and maximum limits apply over  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$  for LM5161. Unless otherwise stated,  $V_{IN} = 48\text{ V}$ .

| PARAMETER                |                                                        | TEST CONDITIONS | MIN  | TYP  | MAX  | UNIT |
|--------------------------|--------------------------------------------------------|-----------------|------|------|------|------|
| <b>MINIMUM OFF-TIME</b>  |                                                        |                 |      |      |      |      |
| $T_{OFF-MIN}$            | Minimum off-time, FB = 0 V                             |                 |      | 170  |      | ns   |
| $T_{OFF-MIN}$            | Minimum off-time, FB = 0 V, $V_{IN} = 4.5\text{ V}$    |                 |      | 200  |      | ns   |
| <b>ON-TIME GENERATOR</b> |                                                        |                 |      |      |      |      |
| $T_{ON}$ Test 1          | $V_{IN} = 24\text{ V}$ , $R_{ON} = 100\text{ k}\Omega$ |                 | 420  | 540  | 665  | ns   |
| $T_{ON}$ Test 2          | $V_{IN} = 48\text{ V}$ , $R_{ON} = 100\text{ k}\Omega$ |                 |      | 270  |      | ns   |
| $T_{ON}$ Test 3          | $V_{IN} = 8\text{ V}$ , $R_{ON} = 100\text{ k}\Omega$  |                 | 1150 | 1325 | 1500 | ns   |
| $T_{ON}$ Test 4          | $V_{IN} = 72\text{ V}$ , $R_{ON} = 150\text{ k}\Omega$ |                 |      | 285  |      | ns   |

(1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

## 6.7 Typical Characteristics

At  $T_A = 25^\circ\text{C}$  and applicable to LM5161 unless otherwise noted.

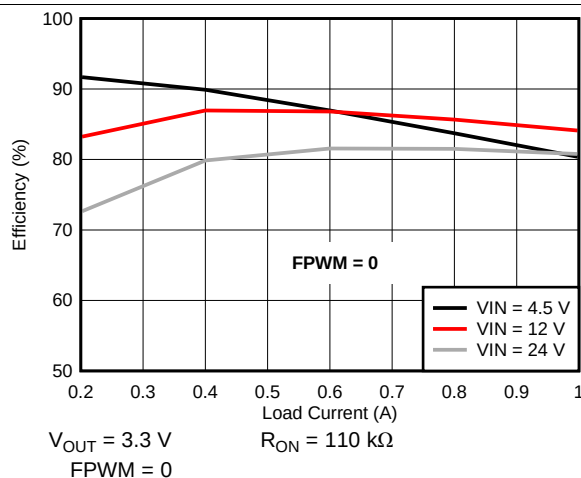


图 1. Efficiency at 300 kHz

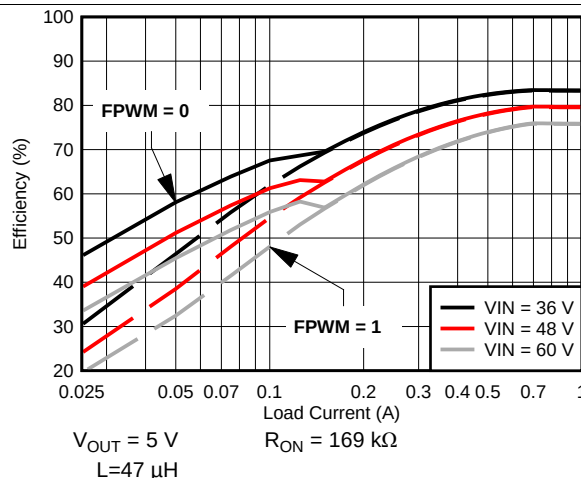


图 2. Efficiency at 300 kHz

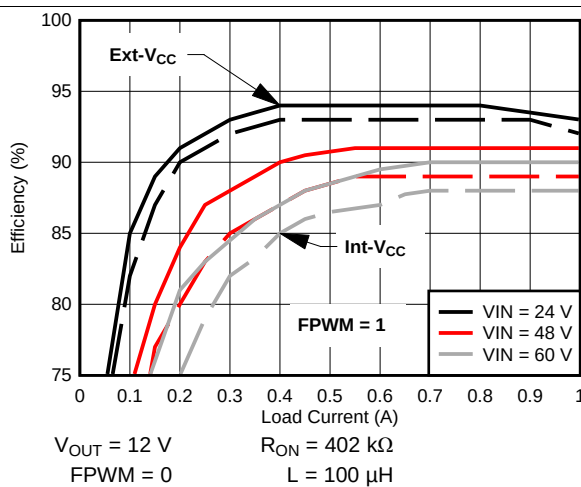


图 3. Efficiency at 300 kHz

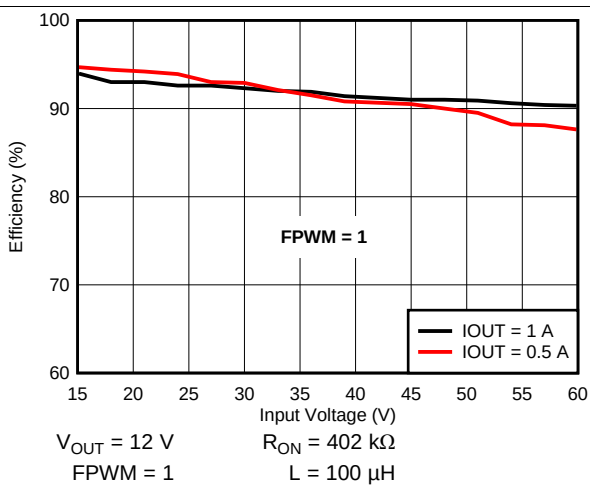


图 4. Efficiency at 300 kHz

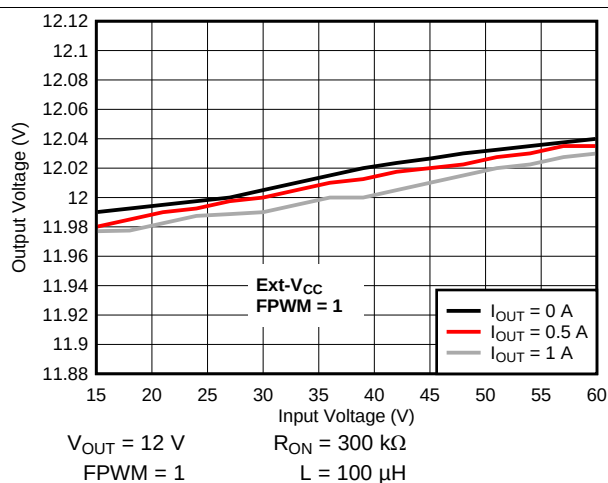


图 5. Line Regulation

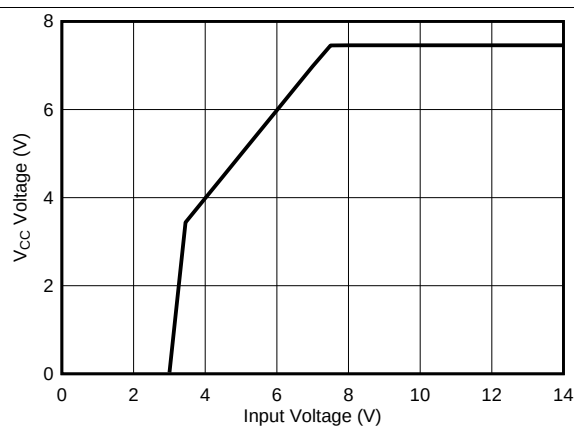


图 6.  $V_{CC}$  vs  $V_{IN}$

## Typical Characteristics (接下页)

At  $T_A = 25^\circ\text{C}$  and applicable to LM5161 unless otherwise noted.

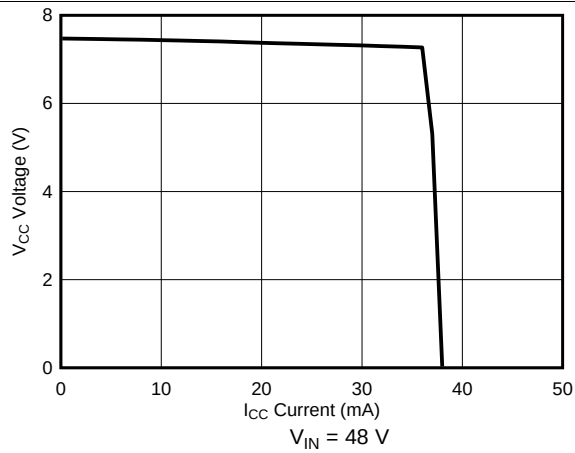


图 7.  $V_{CC}$  vs  $I_{CC}$

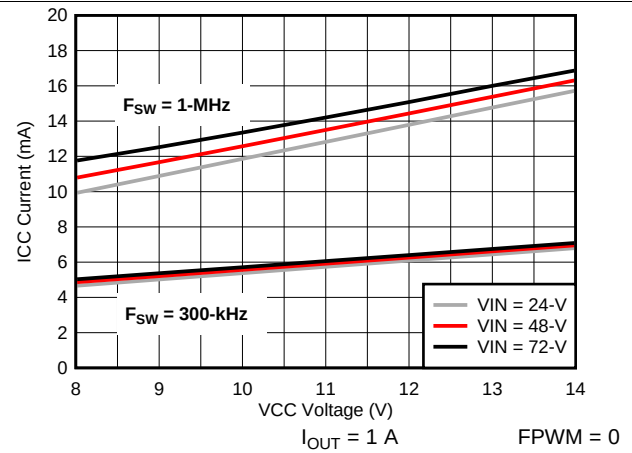


图 8.  $I_{CC}$  vs External  $V_{CC}$

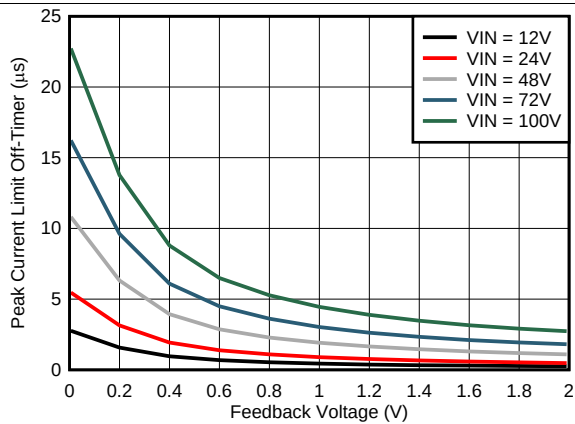


图 9.  $T_{OFF} (I_{LIM})$  vs  $V_{FB}$

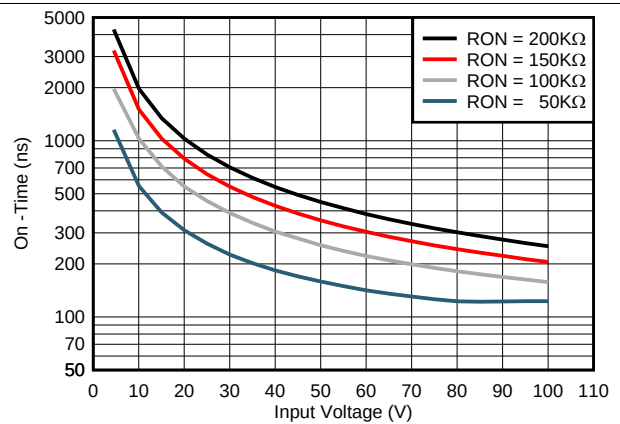


图 10.  $T_{ON}$  vs  $V_{IN}$

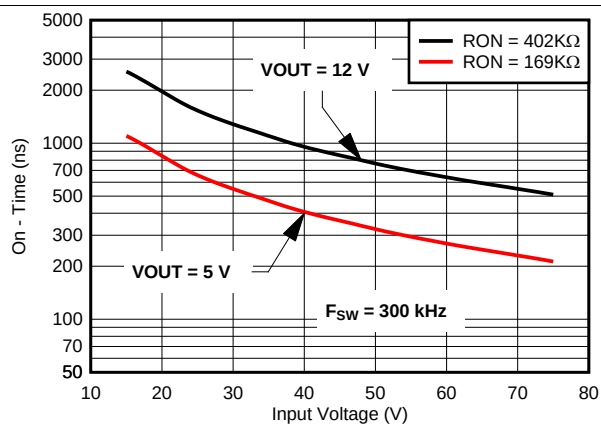


图 11.  $T_{ON}$  vs  $V_{IN}$

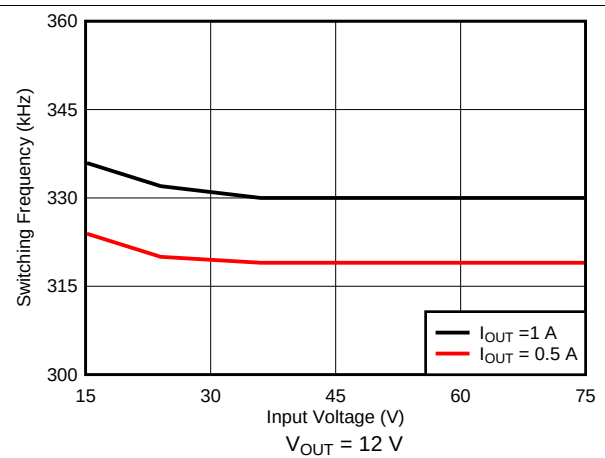


图 12.  $F_{SW}$  vs  $V_{IN}$

## Typical Characteristics (接下页)

At  $T_A = 25^\circ\text{C}$  and applicable to LM5161 unless otherwise noted.

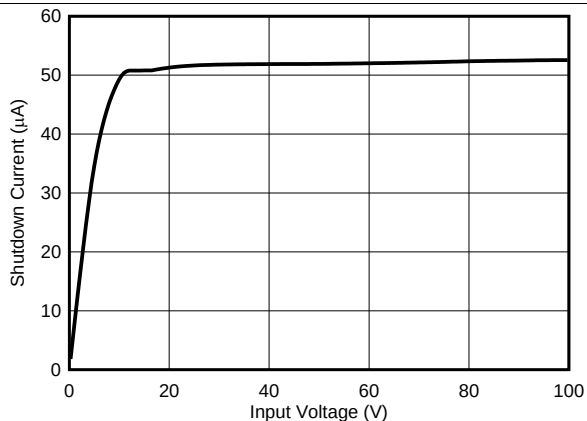


图 13. Shutdown Current vs  $V_{IN}$

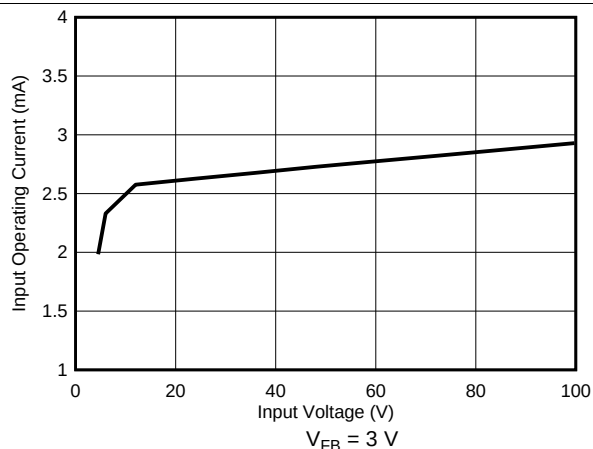


图 14.  $I_{IN}$  vs  $V_{IN}$  (Operating, Non Switching)

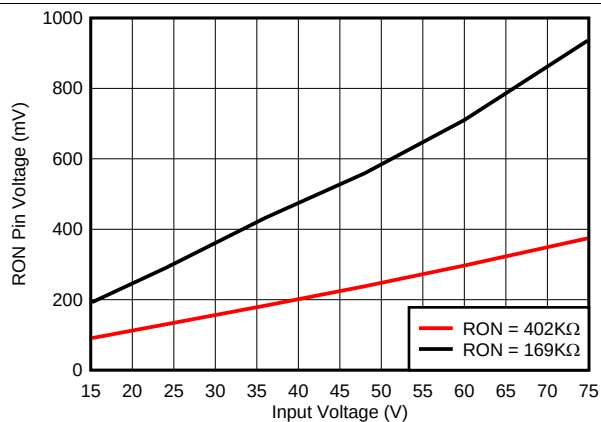


图 15. Voltage at RON pin vs Input Voltage

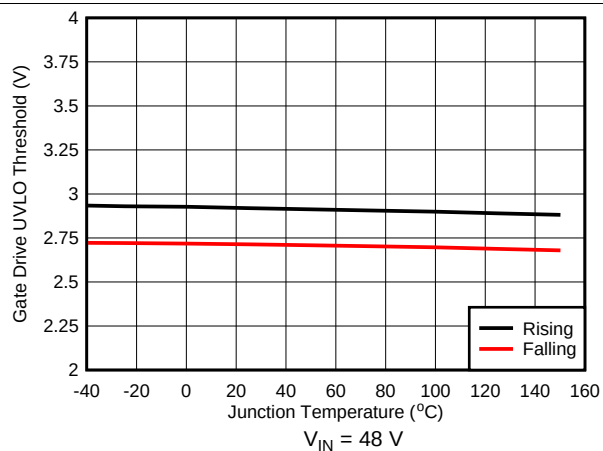


图 16. Gate Drive UVLO vs Temperature

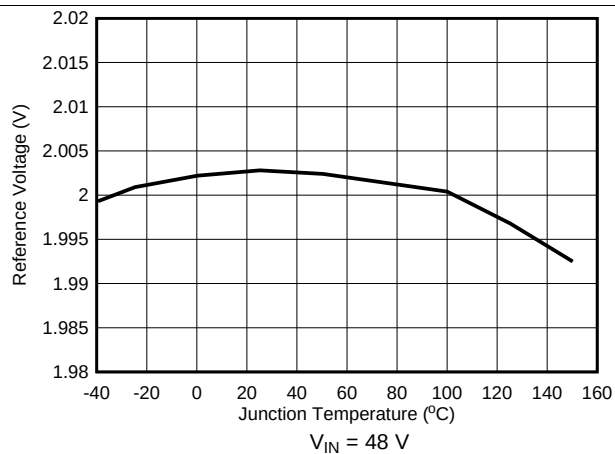


图 17. Reference Voltage vs Temperature

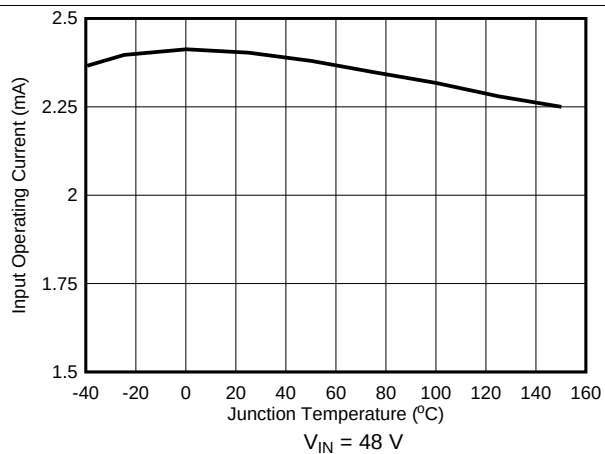


图 18. Input Operating Current vs Temperature

## Typical Characteristics (接下页)

At  $T_A = 25^\circ\text{C}$  and applicable to LM5161 unless otherwise noted.

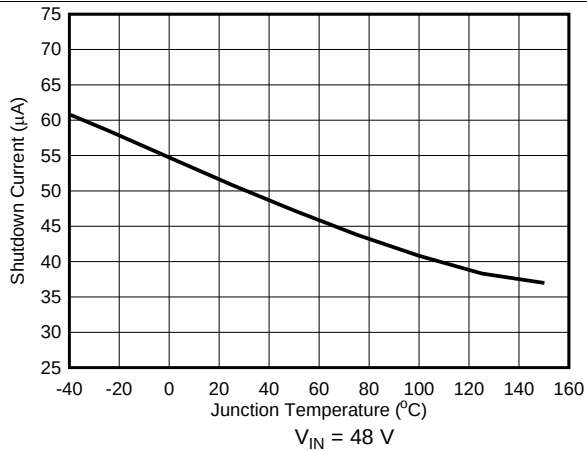


图 19. Input Shutdown Current vs Temperature

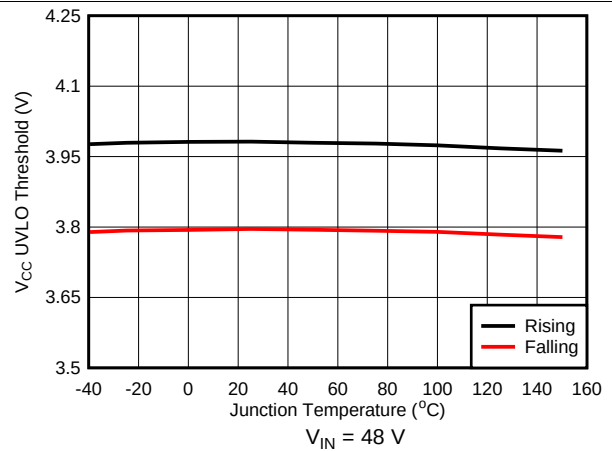


图 20.  $V_{CC}$  UVLO vs Temperature

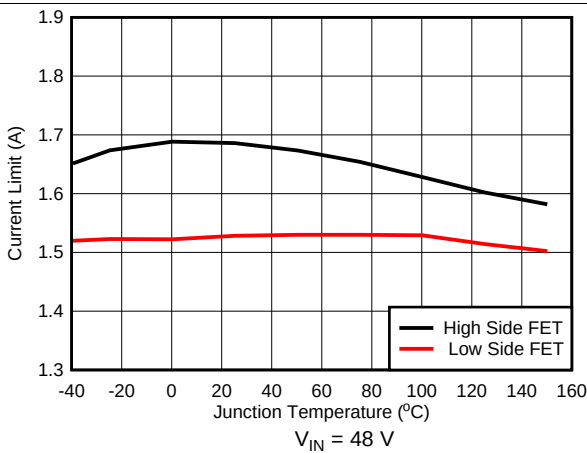


图 21. Current Limit vs Temperature

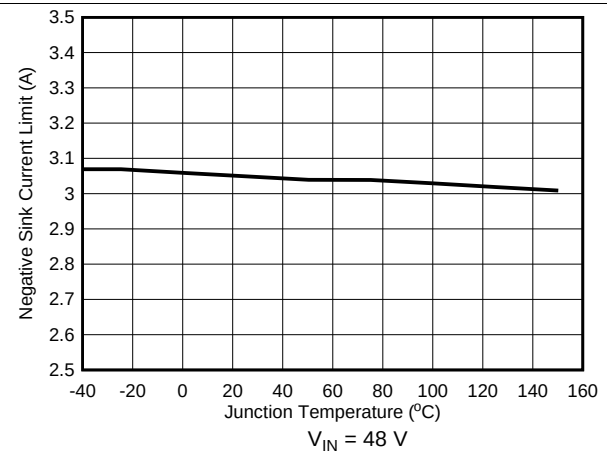


图 22. Sink Current Limit vs Temperature

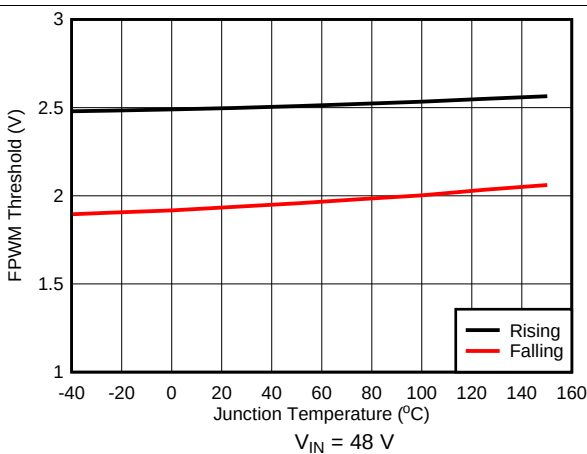


图 23. FPWM Threshold vs Temperature

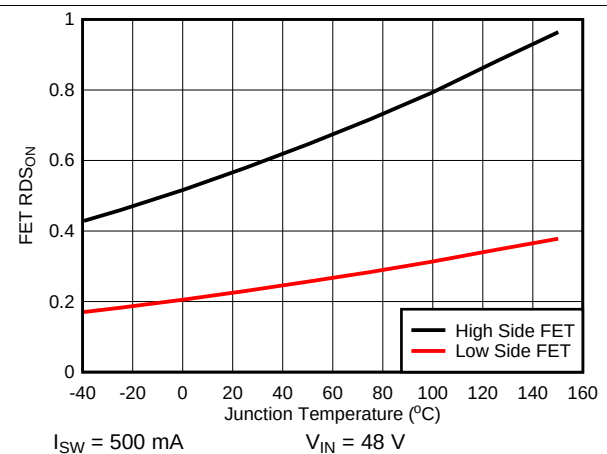


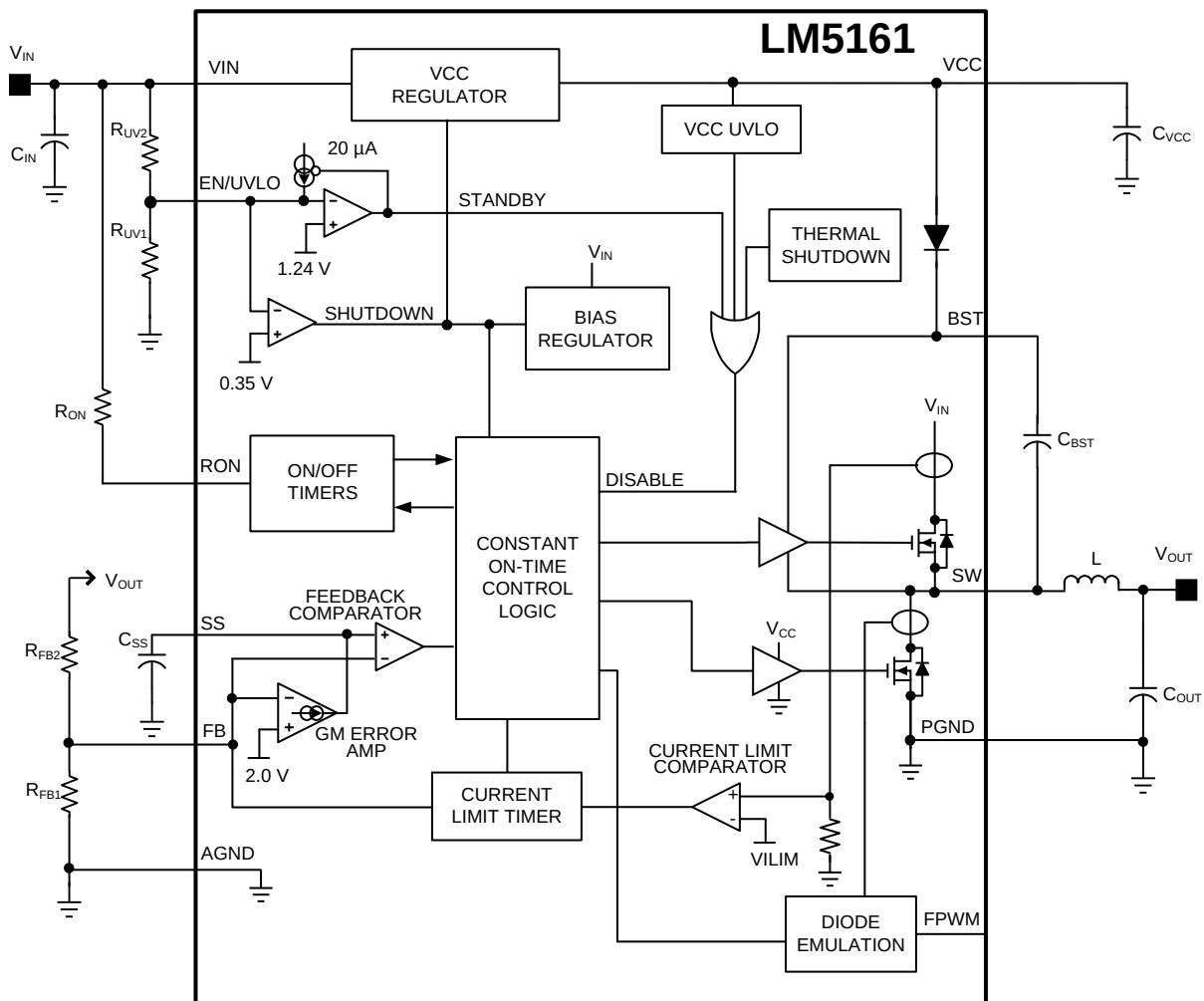
图 24. Switch Resistance vs Temperature

## 7 Detailed Description

### 7.1 Overview

The LM5161 step-down switching regulator features all the functions needed to implement a low-cost, efficient buck converter capable of supplying 1-A to the load. This high voltage regulator contains 100-V N-channel buck and synchronous rectifier switches and is available in the 14-pin HTSSOP package. The regulator operation is based on constant ON-time control where the ON-time is inversely proportional to input voltage  $V_{IN}$ . This feature maintains a relatively constant operating frequency with load and input voltage variations. A constant on-time switching regulator requires no loop compensation resulting in fast load transient response. Peak current limit detection circuit is implemented with a forced OFF-time during current limiting which is inversely proportional to voltage at the feedback pin,  $V_{FB}$  and directly proportional to  $V_{IN}$ . Varying the current limit OFF-time with  $V_{FB}$  and  $V_{IN}$  ensures short circuit protection with minimal current limit foldback. The LM5161 can be applied in numerous end equipment systems requiring efficient step-down regulation from higher input voltages. This regulator is well suited for 24 V industrial systems as well as for 48 V telecom and PoE voltage ranges. The LM5161 integrates an under-voltage lockout (EN/UVLO) circuit to prevent faulty operation of the device at low input voltages and features intelligent current limit and thermal shutdown to protect the device during overload or short circuit.

### 7.2 Functional Block Diagram



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## 7.3 Feature Description

### 7.3.1 Control Circuit

The LM5161 step-down switching regulator employs a control principle based on a comparator and a one-shot ON-timer, with the output voltage feedback (FB) compared to the voltage at the Soft-Start (SS) pin ( $V_{SS}$ ). If the FB voltage is below  $V_{SS}$ , the internal buck switch is turned on for a time period determined by the input voltage and one-shot programming resistor ( $R_{ON}$ ). Following the ON-time, the buck switch must remain off for the minimum OFF-time forced by the minimum OFF-time one-shot. The buck switch remains off until the FB voltage falls below  $V_{SS}$  again, when it turns on for another ON-time one-shot period.

During a rapid start-up or when the load current increases suddenly, the regulator operates with minimum off-time per cycle. When regulating the output in steady state operation, the off-time automatically adjusts to produce the SW pin duty cycle required for output voltage regulation.

When in regulation, the LM5161 operates in continuous conduction mode at heavy load currents. If the FPWM pin is connected to ground or left floating, the regulator operates in discontinuous conduction mode at light load with the synchronous rectifier FET emulating a diode. With sufficient load, the LM5161 operates in continuous conduction mode with the inductor current never reaching zero during the OFF-time of the high-side FET. In this mode the operating frequency remains relatively constant with load and line variations. The minimum load current for continuous conduction mode is one-half the inductor's ripple current amplitude. The operating frequency (in Hz) is programmed by the  $R_{ON}$  pin resistor and can be calculated from 公式 1 with  $R_{ON}$  expressed in ohms.

$$F_{SW} = \frac{V_{OUT}}{1.008 \times 10^{-10} \times R_{ON}} \text{ Hz} \quad (1)$$

In discontinuous conduction mode, current through the inductor ramps up from zero to a peak value during the ON-time, then ramps back to zero before the end of the OFF-time. The next ON-time period starts when the voltage at FB falls below  $V_{SS}$ . When the inductor current is zero during the high side FET off-time, the load current is supplied by the output capacitor. In this mode, the operating switching frequency is lower than the continuous conduction mode switching frequency and the frequency varies with load. The discontinuous conduction mode maintains higher conversion efficiency at light loads because the switching losses decrease with the decrease in load and frequency.

The output voltage is set by two external resistors ( $R_{FB1}$ ,  $R_{FB2}$ ). The regulated output voltage is calculated from 公式 2, where  $V_{REF} = 2 \text{ V}$  (typ) is the feedback reference voltage.

$$V_{OUT} = \frac{V_{REF} \times (R_{FB2} + R_{FB1})}{R_{FB1}} \text{ V} \quad (2)$$

### 7.3.2 VCC Regulator

The LM5161 contains an internal high voltage linear regulator with a nominal output voltage of 7.3 V (typical). The VCC regulator is internally current limited to 30 mA (minimum). This regulator supplies power to internal circuit blocks including the synchronous FET gate driver and the logic circuits. When the voltage on the VCC pin reaches the undervoltage lockout ( $V_{CC(UV)}$ ) threshold of 3.98 V (typical), the IC is enabled. An external capacitor at the VCC pin stabilizes the regulator and supplies transient VCC current to the gate drivers. An internal diode connected from VCC to the BST pin replenishes the charge in the high-side gate drive bootstrap capacitor when the SW pin is low.

In high input voltage applications, the power dissipated in the regulator is significant and can limit the efficiency and maximum achievable output power. The LM5161 allows the internal VCC regulator power loss to be reduced by supplying the VCC voltage via a diode from an external voltage source regulated between 9 V and 13 V. The external VCC bias can be supplied from the LM5161 converter output rail if the regulation voltage is within this range. When the VCC pin of the LM5161 is raised above the regulation voltage (7.3 V typical), the internal regulator is disabled and the power dissipation in the IC is reduced.

## Feature Description (接下页)

### 7.3.3 Regulation Comparator

The feedback voltage at the FB pin is compared to the SS pin voltage  $V_{SS}$ . In normal operation when the output voltage is in regulation, an ON-time period is initiated when the voltage at FB pin falls below  $V_{SS}$ . The high-side buck switch stays on for the ON-time one-shot period causing the FB voltage to rise. After the on-time period expires, the high-side switch will remain off until the FB voltage falls below  $V_{SS}$ . During start-up, the FB voltage is below  $V_{SS}$  at the end of each on-time period and the high-side switch turns on again after the minimum forced off-time of 170 ns (typical). When the output is shorted to ground (FB = 0 V), the high side peak current limit is triggered, the high-side FET is turned off, and remains off for a period determined by the current limit OFF-time one-shot. See the [Current Limit](#) section for additional information.

### 7.3.4 Soft-Start

The soft-start feature of the LM5161 allows the converter to gradually reach a steady-state operating point, thereby reducing start-up stresses and current surges. When the EN/UVLO pin is above the EN/UVLO standby threshold  $V_{UVLO(TH)} = 1.24$  V (typ) and VCC exceeds the VCC undervoltage  $V_{CC(UV)} = 3.98$  V (typ) threshold, an internal 10- $\mu$ A current source charges the external capacitor at the SS pin ( $C_{SS}$ ) from 0 V to 2 V. The voltage at the SS pin is connected to the noninverting input of the internal FB comparator. The soft-start interval ends when the SS capacitor is charged to the 2 V reference level. The ramping voltage at the SS pin produces a controlled, monotonic output voltage start-up. A minimum 1-nF soft-start capacitor must be used in all applications.

### 7.3.5 Error Transconductance ( $G_M$ ) Amplifier

The LM5161 provides a trans-conductance ( $G_M$ ) error amplifier that minimizes the difference between the reference voltage ( $V_{REF}$ ) and the average feedback (FB) voltage. This amplifier reduces the load and line regulation errors that are common in constant-on-time regulators. The soft-start capacitor ( $C_{SS}$ ) provides compensation for this error correction loop. The soft-start capacitor should be greater than 1 nF to ensure stability.

### 7.3.6 On-Time Generator

The ON-time of the LM5161 high-side FET is determined by the  $R_{ON}$  resistor and is inversely proportional to the input voltage ( $V_{IN}$ ). The inverse relationship with  $V_{IN}$  results in a nearly constant frequency as  $V_{IN}$  is varied. The ON-time can be calculated from [公式 3](#) with  $R_{ON}$  expressed in ohms.

$$T_{ON} = \frac{1.008 \times 10^{-10} \times R_{ON}}{V_{IN}} \text{ s} \quad (3)$$

To set a specific continuous conduction mode switching frequency ( $F_{SW}$  expressed in Hz), the  $R_{ON}$  resistor is determined from [公式 4](#):

$$R_{ON} = \frac{V_{OUT}}{1.008 \times 10^{-10} \times F_{SW}} \Omega \quad (4)$$

$R_{ON}$  must be selected for a minimum on-time (at maximum  $V_{IN}$ ) greater than 150 ns for proper operation. This minimum ON-time requirement limits the maximum switching frequency of applications with relatively high  $V_{IN}$  and low  $V_{OUT}$ .

### 7.3.7 Current Limit

The LM5161 provides an intelligent current limit OFF-timer that adjusts the OFF-time to reduce foldback of the current limit. If the peak value of the current in the buck switch exceeds 1.6 A (typical) the present ON-time period is immediately terminated, and a non-resettable OFF-timer is initiated. The length of the OFF-time is controlled by the FB voltage and the input voltage  $V_{IN}$ . As an example, when  $V_{FB} = 0.1$ -V and  $V_{IN} = 72$ -V, the OFF-time is set to 13  $\mu$ s (typical). This condition would occur if the output is shorted or during the initial phase of start-up. In cases of output overload where the FB voltage is greater than zero volts (a soft short), the current limit OFF-time is reduced. Reducing the OFF-time during less severe overloads reduces the current limit foldback, overload recovery time, and start-up time. The current limit off-time,  $T_{OFF(CL)}$  is calculated from [公式 5](#):

$$T_{OFF(CL)} = \frac{V_{IN}}{20 V_{FB} + 4.35} \mu\text{s} \quad (5)$$

## Feature Description (接下页)

### 7.3.8 N-Channel Buck Switch and Driver

The LM5161 integrates an N-channel buck switch and associated floating high-side gate driver. The gate driver circuit works in conjunction with an external bootstrap capacitor and an internal high voltage bootstrap diode. A 10-nF or larger ceramic capacitor connected between the BST pin and the SW pin provides the voltage to the high-side driver during the buck switch ON-time. During the OFF-time, the SW node is pulled down to approximately 0 V and the bootstrap capacitor charges from VCC through the internal bootstrap diode. The minimum OFF-time of 170 ns (typical) provides a minimum time each cycle to recharge the bootstrap capacitor.

### 7.3.9 Synchronous Rectifier

The LM5161 provides an internal low-side synchronous rectifier N-channel FET. This low-side FET provides a low resistance path for the inductor current when the high-side FET is turned off.

With the FPWM pin connected to ground or left floating, the LM5161 synchronous rectifier operates in diode emulation mode. Diode emulation enables the pulse-skipping during light load conditions. This leads to a reduction in the average switching frequency at light loads. Switching losses and FET gate driver losses, both of which are proportional to switching frequency, are significantly reduced and efficiency is improved. This pulse-skipping mode also reduces the circulating inductor currents and losses associated with a continuous conduction mode (CCM). When the FPWM pin is grounded or left floating, an internal ripple injection circuit is enabled. With the internal ripple injection enabled, the typical external feedback ripple injection circuit is no longer required. This feature reduces the component count in the buck applications. For more details see [Forced Pulse Width Modulation \(FPWM\) Mode](#).

When the FPWM pin is pulled high, diode emulation is disabled. The inductor current can flow in either direction through the low-side FET resulting in CCM operation with nearly constant switching frequency. A negative sink current limit circuit limits the current that can flow into the SW pin and through the low-side FET to ground. In a buck regulator application, large negative current will only flow from V<sub>OUT</sub> to the SW pin if V<sub>OUT</sub> is lifted above the output regulation set-point.

### 7.3.10 Enable / Undervoltage Lockout (EN/UVLO)

The LM5161 contains a dual level undervoltage lockout (EN/UVLO) circuit. When the EN/UVLO pin voltage is below 0.35 V (typical), the regulator is in a low current shutdown mode. When the EN/UVLO pin voltage is greater than 0.35 V (typical) but less than 1.24 V (typical), the regulator is in standby mode. In standby mode, the VCC bias regulator is active but converter switching remains disabled. When the voltage at the VCC pin exceeds the VCC rising threshold V<sub>CC(UV)</sub> = 3.98 V (typ) and the EN/UVLO pin voltage is greater than 1.24 V, normal switching operation begins. An external resistor voltage divider from VIN to GND can be used to set the minimum operating voltage of the regulator.

EN/UVLO hysteresis is accomplished with an internal 20-μA (typical) current source (I<sub>UVLO(HYS)</sub>) that is switched on or off into the impedance of the EN/UVLO pin resistor divider. When the EN/UVLO threshold is exceeded, the current source is activated to effectively raise the voltage at the EN/UVLO pin. The hysteresis is equal to the value of this current times the upper resistance of the resistor divider, (R<sub>UV2</sub>) (See [Functional Block Diagram](#) .)

### 7.3.11 Thermal Protection

The LM5161 must be operated such that the junction temperature does not exceed 150°C during normal operation. An internal thermal shutdown circuit is provided to protect the LM5161 in the event of a higher than normal junction temperature. When activated, typically at 175°C, the controller is forced into a low-power reset state, disabling the high side buck switch and the VCC regulator. This feature prevents catastrophic failures due to device overheating. When the junction temperature falls below 155 °C (typical hysteresis = 20°C), the VCC regulator is enabled, and operation resumes.

## 7.4 Device Functional Modes

### 7.4.1 Forced Pulse Width Modulation (FPWM) Mode

The [Synchronous Rectifier](#) section gives a brief introduction to the LM5161 diode emulation feature. The FPWM pin allows the power supply designer to select either CCM or DCM mode of operation at light loads. When the FPWM pin is connected to ground or left floating (FPWM = 0), a pulse-skipping mode and the zero-cross current detector circuit is enabled. The zero-cross detector turns off the low-side FET when the inductor current falls close to zero ( $I_{ZX}$ , see [Electrical Characteristics](#)). This feature allows the LM5161 regulator to operate in DCM mode at light loads. In the DCM state, the switching frequency decreases with lighter loads.

When the FPWM pin is left open or shorted to ground, the user can take the advantage of the internal ripple injection circuit, enabled in this mode, for a typical Buck application circuit. This feature is applicable over the entire load and input voltage ranges. It eliminates the need for an external feedback ripple injection circuit.

For wide VIN applications where  $V_{IN} > 72\text{ V}$ , an external VCC supply is commonly used to minimize the power dissipation in the IC. In such applications at  $T_J > 125^\circ\text{C}$ , it is recommended to add a BST resistor ( $> 3\Omega$ ) in series with the BST capacitor, in order to protect the internal VCC-BST diode during a full load transient operation. The addition of the external resistor will reduce the fast (dv/dt) of the switch node that can impact the normal IC operation.

If the FPWM pin is pulled high, the LM5161 will operate in CCM mode regardless of the load conditions. The CCM operation reduces efficiency at light load but improves the output transient response to step load changes and provides nearly constant switching frequency. Moreover, the Fly-Buck topology always requires the continuous conduction mode during its operation.

The internal ripple injection circuit is disabled in the CCM mode. An external ripple injection circuit or an additional ESR resistor in series with the output capacitor is required to generate the optimal ripple at the FB node. Also, there is no need to add any BST resistor in series with the BST capacitor in either forced CCM Buck or Fly-Buck application.

**表 1. FPWM Pin Mode Summary**

| FPWM PIN CONNECTION      | LOGIC STAGE | DESCRIPTION                                                                                                                                                  |
|--------------------------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GND or Floating (High Z) | 0           | The FPWM pin is grounded or left floating. DCM enabled at light loads. Internal Ripple circuit is enabled. No external ripple circuit/ addition required.    |
| $V_{CC}$                 | 1           | The FPWM pin is connected to VCC. The LM5161 then operates in CCM mode at light loads. Internal ripple injection disabled. External ripple injection needed. |

### 7.4.2 Undervoltage Detector

表 2 summarizes the dual threshold levels of the under-voltage lockout (EN/UVLO) circuit explained in [Enable / Undervoltage Lockout \(EN/UVLO\)](#).

**表 2. UVLO Pin Mode Summary**

| EN/UVLO PIN VOLTAGE              | VCC REGULATOR         | MODE      | DESCRIPTION                                                   |
|----------------------------------|-----------------------|-----------|---------------------------------------------------------------|
| $< 0.35\text{ V}$                | Off                   | Shutdown  | $V_{CC}$ regulator disabled. High and low side FETs disabled. |
| $0.35\text{ V to }1.24\text{ V}$ | On                    | Standby   | $V_{CC}$ regulator enabled. High and low side FETs disabled.  |
| $> 1.24\text{ V}$                | $V_{CC} < V_{CC(UV)}$ | Standby   | $V_{CC}$ regulator enabled. High and low side FETs disabled.  |
|                                  | $V_{CC} > V_{CC(UV)}$ | Operating | $V_{CC}$ regulator enabled. Switching enabled.                |

If an EN/UVLO setpoint is not required, the EN/UVLO pin can be driven by a logic signal as an enable input or connected directly to the VIN pin. If the EN/UVLO is directly connected to the VIN pin, the regulator will begin switching when the  $V_{CC}$  UVLO is satisfied.



## Typical Applications (接下页)

### 8.2.1.1 Design Requirements

A typical synchronous-buck application introduced in [LM5161 Synchronous Buck \(15-V to 95-V Input, 12-V Output, 1-A Load\)](#), 表 3 summarizes the operating parameters:

**表 3. Design Parameters**

| DESIGN PARAMETER            | EXAMPLE VALUE      |
|-----------------------------|--------------------|
| Input voltage range         | 15-V to 80-V       |
| output                      | 12-V               |
| Full load current           | 1-A                |
| Nominal switching frequency | 300 kHz            |
| Light load operating mode   | CCM, FPWM=1        |
| Jumper JP1                  | Pins 1-2 connected |

### 8.2.1.2 Detailed Design Procedure

#### 8.2.1.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the LM5161 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ( $V_{IN}$ ), output voltage ( $V_{OUT}$ ), and output current ( $I_{OUT}$ ) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at [www.ti.com/WEBENCH](http://www.ti.com/WEBENCH).

#### 8.2.1.2.2 Output Resistor Divider Selection

With the required output voltage set point at 12 V and  $V_{FB} = 2$  V (typical), the ratio of R8 ( $R_{FB1}$ ) to R7 ( $R_{FB2}$ ) can be calculated using 公式 6:

$$\frac{R_{FB2}}{R_{FB1}} = \frac{V_{OUT}}{V_{REF}} - 1 \quad (6)$$

The resistor ratio calculates to be 5:1. Standard values of R8 ( $R_{FB1}$ ) = 2 kΩ and R7 ( $R_{FB2}$ ) = 10 kΩ are chosen. Higher or lower resistor values could be used as long as the ratio of 5:1 is maintained.

#### 8.2.1.2.3 Frequency Selection

The duty cycle required to maintain output regulation at the minimum input voltage restricts the maximum switching frequency of LM5161. The maximum value of the minimum forced OFF-time  $T_{OFF,min}(max)$ , limits the duty cycle and therefore the switching frequency. The maximum frequency that avoids output dropout at minimum input voltage can be calculated from 公式 7.

$$F_{SW,max}(@V_{IN,min}) = \frac{V_{IN,min} - V_{OUT}}{V_{IN,min} \times T_{OFF,min}(ns)} \quad (7)$$

For this design example, the maximum frequency based on the minimum OFF-time limitation for  $T_{OFF,min}(typ) = 170$  ns is calculated to be  $F_{SW,max}(@V_{IN,min}) = 1.2$  MHz. This value is above 1 MHz, the maximum possible operating frequency of the LM5161. Therefore, the minimum OFF-time parameter restricts the maximum achievable switching frequency calculation in this application.

At the maximum input voltage, the maximum switching frequency of LM5161 is restricted by the minimum ON-time,  $T_{ON,min}$  which limits the minimum duty cycle of the converter. The maximum frequency at maximum input voltage can be calculated using [公式 8](#).

$$F_{SW,max} (@ V_{IN,max}) = \frac{V_{OUT}}{V_{IN,max} \times T_{ON,min} (ns)} \quad (8)$$

Using [公式 8](#) and  $T_{ON,min}$  (typ) = 150 ns, the maximum achievable switching frequency is  $F_{SW,max}(@V_{IN,min}) = 1000$  kHz. Taking this value as the maximum possible operational switching frequency over the input voltage range in this application, a nominal switching frequency of  $F_{SW} = 300$  kHz is chosen for this design.

The value of the resistor,  $R_{ON}$  sets the nominal switching frequency based on [公式 9](#).

$$R_{ON} = \frac{V_{OUT}}{1.008 \times 10^{-10} \times F_{SW}} \Omega \quad (9)$$

For this particular application with  $F_{SW} = 300$  kHz,  $R_{ON}$  calculates to be 396 k $\Omega$ . Selecting a standard value for  $R_1$  ( $R_{ON}$ ) = 402 k $\Omega$  ( $\pm 1\%$ ) results in a nominal frequency of 296 kHz. The resistor value may need to be adjusted further in order to achieve the required switching frequency as the switching frequency in Constant ON-Time converters varies slightly ( $\pm 10\%$ ) with input voltage and/or output current. Operation at a lower nominal switching frequency will result in higher efficiency but increase in the inductor and capacitor values leading to a larger total solution size.

#### 8.2.1.2.4 Inductor Selection

The inductor is selected to limit the inductor ripple current to a value between 20 and 40 percent of the maximum load current. The minimum value of the inductor required in this application can be calculated from [公式 10](#):

$$L_{min} = \frac{V_O \times (V_{IN,max} - V_O)}{V_{IN,max} \times F_{SW} \times I_{O,max} \times 0.4} \quad (10)$$

Based on [公式 10](#), the minimum value of the inductor is calculated to be 85  $\mu$ H for  $V_{IN} = 80$ -V (max) and inductor current ripple will be 40 percent of the maximum load current. Allowing some margin for inductance variation and inductor saturation, a higher standard value of  $L_1$  ( $L$ ) = 100  $\mu$ H is selected for this design.

The peak inductor current at maximum load must be smaller than the minimum current limit threshold of the high side FET as given in [Electrical Characteristics](#) table. The inductor current ripple at any input voltage is given by:

$$\Delta I_L = \frac{V_O \times (V_{IN} - V_O)}{V_{IN} \times F_{SW} \times L} \quad (11)$$

The peak-to-peak inductor current ripple is calculated to be 81 mA and 341 mA at the minimum and maximum input voltages respectively. The maximum peak inductor current in the buck FET is given by [公式 12](#):

$$I_{L(peak)} = I_{O,max} + \frac{\Delta I_{L,max}}{2} \quad (12)$$

In this design with maximum output current of 1-A, the maximum peak inductor current is calculated to be approximately 1.17 A at  $V_{IN,max} = 80$  V, which is less than the minimum high-side FET current limit threshold.

The saturation current of the inductor must also be carefully considered. The peak value of the inductor current will be bound by the high side FET current limit during overload or short circuit conditions. Based on the high side FET current limit specification in the [Electrical Characteristics](#), an inductor with saturation current rating above 1.9 A (max) should be selected.

### 8.2.1.2.5 Output Capacitor Selection

The output capacitor is selected to limit the capacitive ripple at the output of the regulator. Maximum capacitive ripple is observed at maximum input voltage. The output capacitance required for a ripple voltage  $\Delta V_O$  across the capacitor is given by [公式 13](#).

$$C_{OUT} = \frac{\Delta I_{L,max}}{8 \times F_{SW} \times \Delta V_{O,ripple}} \quad (13)$$

Substituting  $\Delta V_{O,ripple} = 10 \text{ mV}$  gives  $C_{OUT} = 15 \text{ } \mu\text{F}$ . Two standard  $10 \text{ } \mu\text{F}$  ceramic capacitors in parallel (C11, C12) are selected. An X7R type capacitor with a voltage rating  $25 \text{ V}$  or higher should be used for  $C_{OUT}$  (C11, C12) to limit the reduction of capacitance due to dc bias voltage.

### 8.2.1.2.6 Series Ripple Resistor - $R_{ESR}$ (FPWM = 1)

If the FPWM = 1, i.e. the FPWM pin is pulled high as when connected to  $V_{CC}$ , a series resistor in series with the output capacitor or the external ripple injection circuit must be selected such that sufficient ripple injection ( $> 25\text{mV}$ ) is ensured at the feedback pin FB. The ripple produced by  $R_{ESR}$  is proportional to the inductor current ripple, and therefore,  $R_{ESR}$  should be chosen for minimum inductor current ripple which occurs at minimum input voltage. The  $R_{ESR}$  is calculated by [公式 14](#).

$$R_{ESR} \geq \frac{25 \text{ mV} \times V_O}{V_{REF} \times \Delta I_{L,min}} \quad (14)$$

With  $V_O = 12 \text{ V}$ ,  $V_{REF} = 2 \text{ V}$  and  $\Delta I_{L,min} = 81 \text{ mA}$  (at  $V_{IN,min} = 15 \text{ V}$ ) as calculated in [公式 11](#), [公式 14](#) requires an  $R_{ESR}$  greater than or equal to  $1.87 \text{ } \Omega$ . Selecting R4 ( $R_{ESR}$ ) =  $2 \text{ } \Omega$  results in approximately  $700 \text{ mV}$  of maximum output voltage ripple at  $V_{IN,max}$ . However due to the internal DC Error correction loop, the load and line regulation will be much improved, despite the addition of a large  $R_{ESR}$  in the circuit. For applications which require even lower output voltage ripple, Type 2 or Type 3 ripple injection circuits must be used, as described in [Ripple Configuration](#). In this design example, with the FPWM = 1 (i.e. the FPWM pin is pulled up to  $V_{CC}$ ) a  $0 \text{ } \Omega$  ESR resistor is selected and the external Type 3 ripple injection circuit is used.

### 8.2.1.2.7 VCC and Bootstrap Capacitor

The VCC capacitor charges the bootstrap capacitor during the OFF-time of the high-side switch and powers internal logic circuits and the low side sync FET gate driver. The bootstrap capacitor biases the high-side gate driver during the high-side FET ON-time. A good value for C13 ( $C_{VCC}$ ) is  $1 \text{ } \mu\text{F}$ . A good choice for C1 ( $C_{BST}$ ) is  $10 \text{ nF}$ . Both must be high quality X7R ceramic capacitors.

### 8.2.1.2.8 Input Capacitor Selection

The input capacitor must be large enough to limit the input voltage ripple to an acceptable level. [公式 15](#) provides the input capacitance  $C_{IN}$  required for a worst case input ripple of  $\Delta V_{IN,ripple}$ .

$$C_{IN} = \frac{I_{O,max} \times D \times (1-D)}{\Delta V_{IN,ripple} \times F_{SW}} \quad (15)$$

$C_{IN}$  (C4, C6) supplies most of the switch current during the ON-time to limit the voltage ripple at the VIN pin. At maximum load current, when the buck switch turns on, the current into the VIN pin quickly increases to the valley current of the inductor ripple and then ramps up to the peak of the inductor ripple during the ON-time of the high-side FET. The average current during the ON-time is the output load current. For a worst-case calculation,  $C_{IN}$  must supply this average load current during the maximum ON-time, without letting the voltage at VIN drop more than the desired input ripple. For this design, the input voltage drop is limited to  $0.5 \text{ V}$  and the value of  $C_{IN}$  is calculated using [公式 15](#).

Based on [公式 15](#), the value of the input capacitor is calculated to be approximately  $1.68 \text{ } \mu\text{F}$  at  $D = 0.5$ . Taking into account the decrease in capacitance over an applied voltage, two standard value ceramic capacitors of  $2.2 \text{ } \mu\text{F}$  are selected for C4 and C6. The input capacitors should be rated for the maximum input voltage under all operating and transient conditions. A 100-V, X7R dielectric was selected for this design.

A third input capacitor C5 is needed in this design as a bypass path for the high frequency component of the input switching current. The value of C5 is  $0.1 \text{ } \mu\text{F}$  and this bypass capacitor must be placed directly across VIN and PGND (pin 3 and 2) near the IC. The  $C_{IN}$  values and location are critical to reducing switching noise and transients.

### 8.2.1.2.9 Soft-Start Capacitor Selection

The capacitor at the SS pin determines the soft-start time, that is the time for the output voltage to reach its final steady state value. The capacitor value is determined from 公式 16:

$$C_{SS} = \frac{I_{SS} \times T_{Startup}}{V_{SS}} \quad (16)$$

With C9 (C<sub>SS</sub>) set at 22 nF and the V<sub>SS</sub> = 2 V, I<sub>SS</sub> = 10 μA, the T<sub>Startup</sub> should measure approximately 4 ms.

### 8.2.1.2.10 EN/UVLO Resistor Selection

The UVLO resistors R3 (R<sub>UV2</sub>) and R9 (R<sub>UV1</sub>) set the input undervoltage lockout threshold and hysteresis according to 公式 17 and 公式 18:

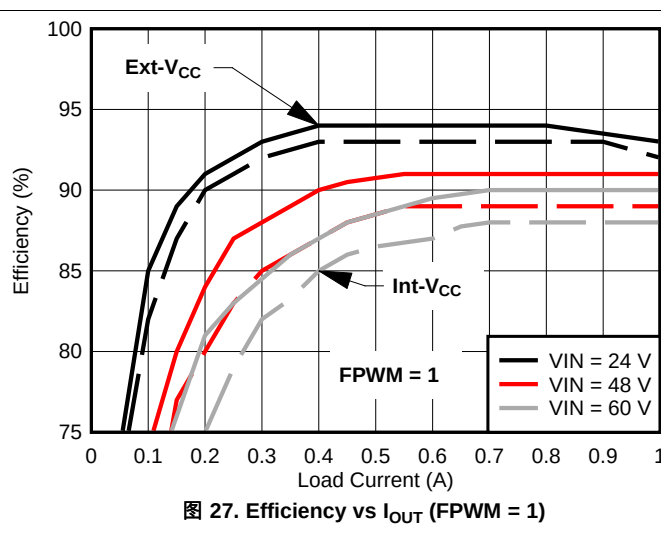
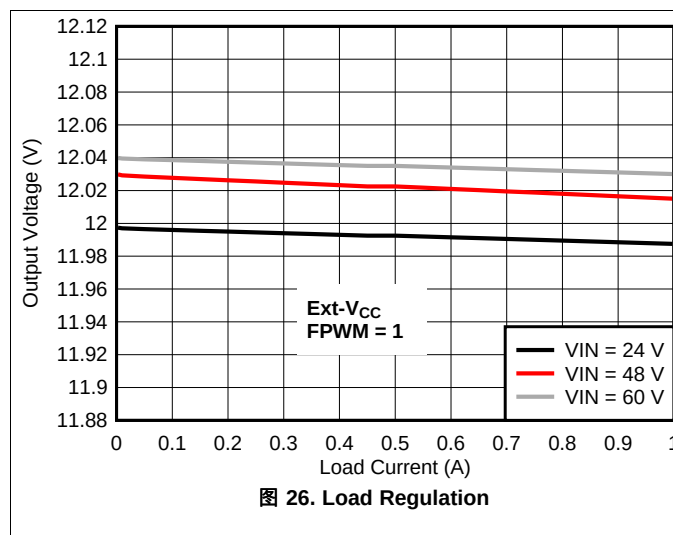
$$V_{IN(HYS)} = I_{UVLO(HYS)} \times R_{UV2} \quad (17)$$

and,

$$V_{IN, UVLO(rising)} = V_{UVLO(TH)} \left( 1 + \frac{R_{UV2}}{R_{UV1}} \right) \quad (18)$$

From the [Electrical Characteristics](#), I<sub>UVLO(HYS)</sub> = 20 μA (typical). To design for V<sub>IN</sub> rising threshold (V<sub>IN, UVLO(rising)</sub>) at 15 V and EN/UVLO hysteresis of 1.5 V, 公式 17 and 公式 18 yield R<sub>UV1</sub> = 6.81 kΩ and R<sub>UV2</sub> = 75 kΩ. Selecting 1% standard value of R9 (R<sub>UV1</sub>) = 6.81 kΩ and R3 (R<sub>UV2</sub>) = 75 kΩ results in UVLO threshold (rising) and hysteresis of 14.9 V and 1.5 V respectively.

### 8.2.1.3 Application Curves



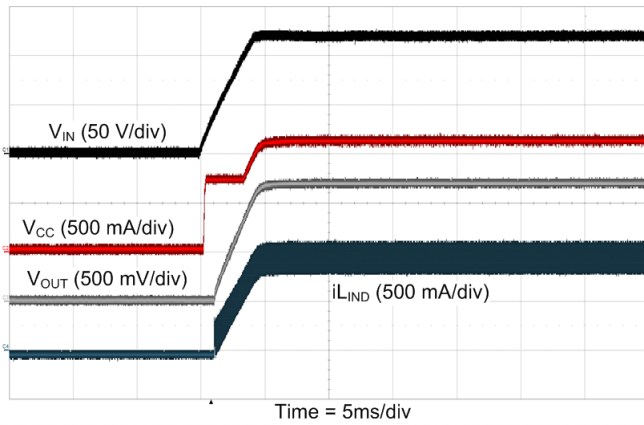


图 28. EN/UVLO Start-up at  $V_{IN} = 48\text{ V}$  and  $I_{OUT} = 1\text{ A}$

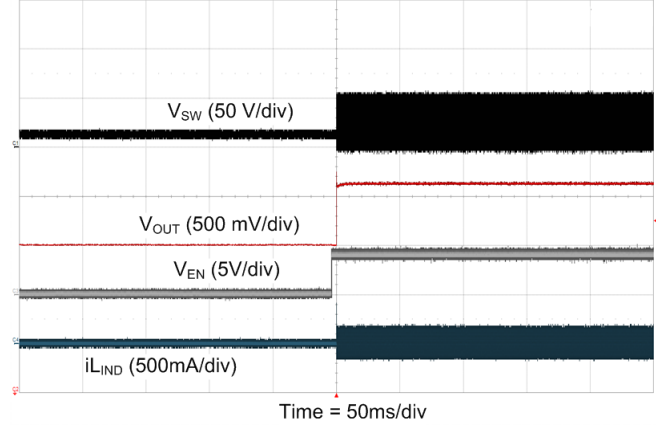


图 29. Pre-Bias (11.5 V) Start-up at  $V_{IN} = 48\text{ V}$  at No Load &  $FPWM = 1$

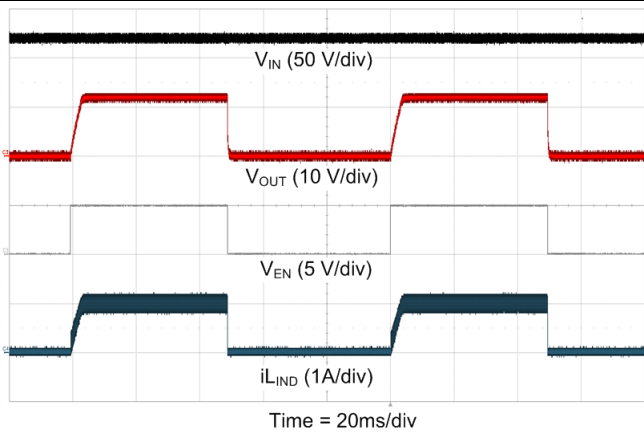


图 30. EN/UVLO Start-up at  $V_{IN} = 48\text{ V}$  and  $R_{LOAD} = 12\ \Omega$  at  $FPWM = 1$

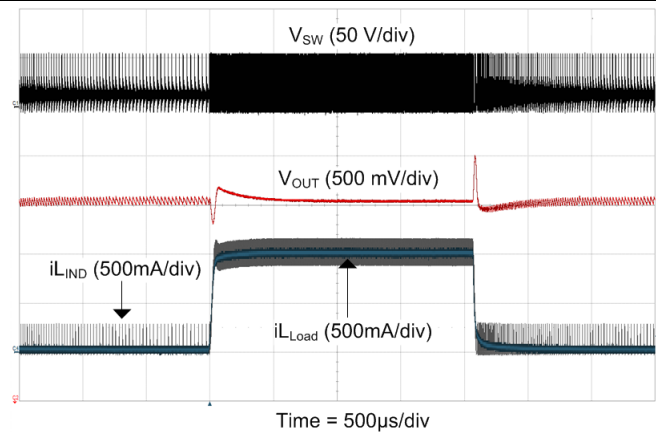


图 31. Load Transient (0 A - 1 A) at  $V_{IN} = 48\text{ V}$  at  $FPWM = 0$

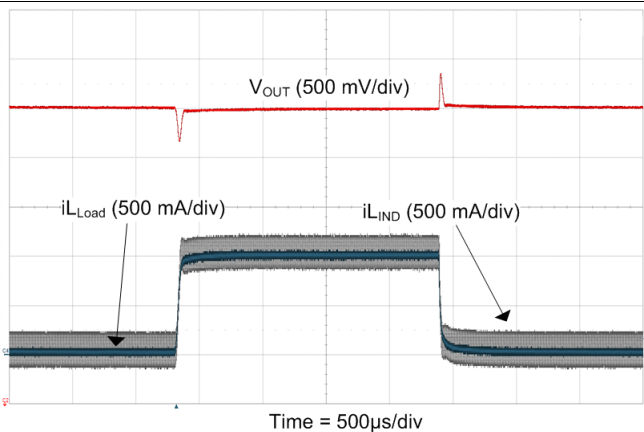


图 32. Load Transient (0 A - 1 A) at  $V_{IN} = 48\text{ V}$  at  $FPWM = 1$

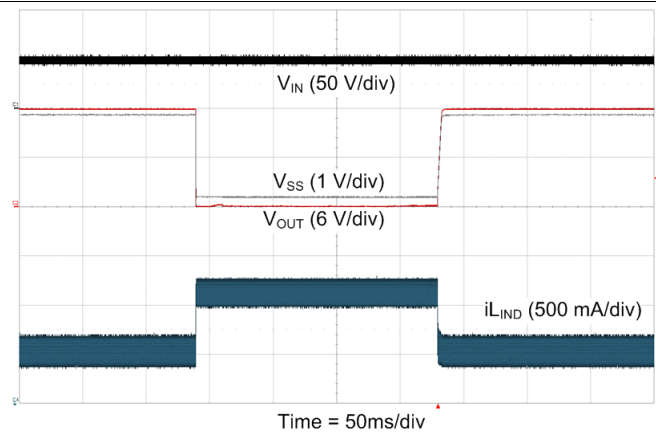


图 33. Output Short-Circuit at  $V_{IN} = 48\text{ V}$  (Full Load to Short)

## 8.2.2 LM5161 Isolated Fly-Buck (36-V to 72-V Input, 12-V, 12-W Isolated Output)

A typical application example for an isolated Fly-Buck converter operates over an input voltage range of 36 V to 72 V. It provides a stable 12 V isolated output voltage with output power capability of 10 W. The complete schematic of the Fly-Buck application circuit is shown in 图 34.

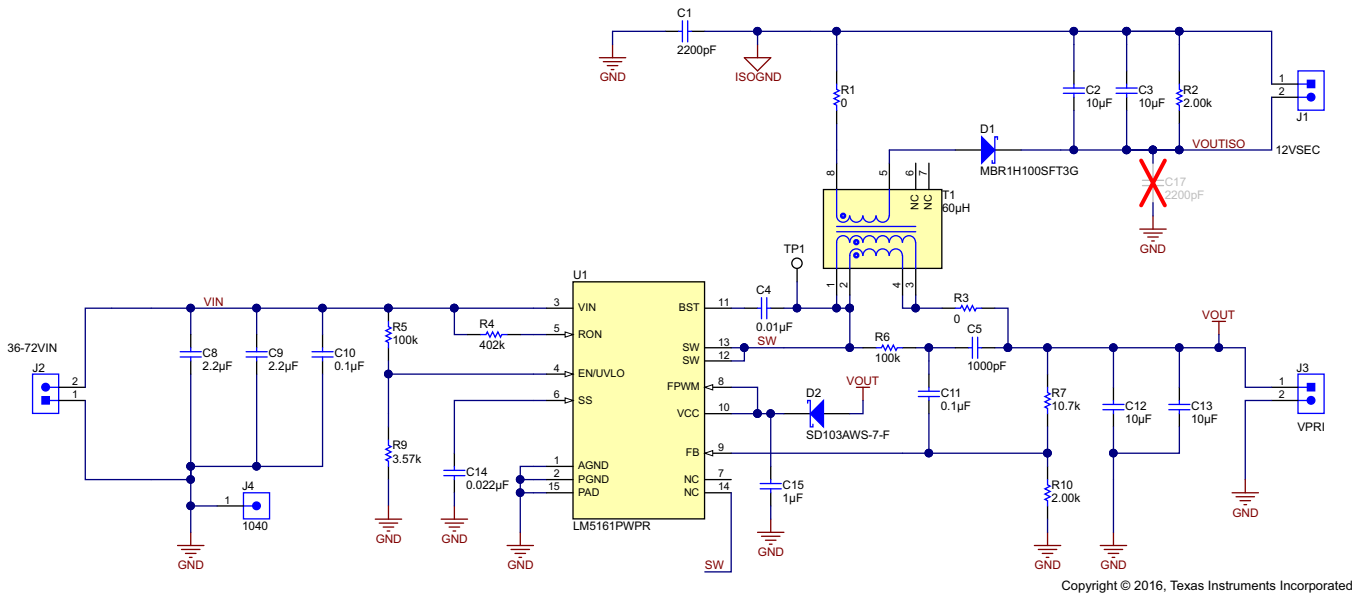


图 34. 12-V, 10-W Fly-Buck Schematic

### 8.2.2.1 LM5161 Fly-Buck Design Requirements

The LM5161 Fly-Buck application example is designed to operate from a nominal 48-V DC supply with line variations from 36-V to 72-V. This example provides a space-optimized and efficient 12-V isolated output solution with secondary load current capability from 0-A to 800 mA. The primary side remains unloaded in this application. The switching frequency is set at 300 kHz (nominal). This design achieves greater than 88% peak efficiency.

表 4. Design Parameters

| DESIGN PARAMETER                          | EXAMPLE VALUE  |
|-------------------------------------------|----------------|
| Input voltage range                       | 36 V - 72 V    |
| Isolated output                           | 12 V (+/- 10%) |
| Isolated load current range ( $I_{ISO}$ ) | 0-A to 0.8-A   |
| Nominal switching frequency               | 300 KHz        |
| Peak efficiency                           | ~87%           |
| Operation mode                            | FPWM = 1       |

### 8.2.2.2 Detailed Design Procedure

The Fly-Buck converter design procedure closely follows the buck converter design outlined in [LM5161 Synchronous Buck \(15-V to 95-V Input, 12-V Output, 1-A Load\)](#). The selection of primary output voltage, transformer turns ratio, rectifier diode, and output capacitors are covered here.

#### 8.2.2.2.1 Selection of $V_{OUT}$ and Turns Ratio

The primary output voltage in a Fly-Buck converter should be no more than one half of the minimum input voltage. Therefore, at the minimum  $V_{IN}$  of 36 V, the primary output voltage ( $V_{OUT}$ ) should be no higher than 18 V. The isolated output voltage of  $V_{OUTISO}$  in 图 34 is set at 12 V by selecting a transformer with a turns ratio ( $N_1:N_2 :: N_{PRI}:N_{SEC}$ ) of 1:1. Using this turns ratio, the required primary output voltage  $V_{OUT}$  is calculated in 公式 19:

$$V_{OUT} = \frac{V_{OUTISO} + V_{FD1}}{\frac{N_2}{N_1}} = \frac{V_{OUTISO} + 0.7V}{1} = 12.7V \quad (19)$$

The 0.7 V ( $V_{FD1}$ ) added to  $V_{OUTISO}$  in 公式 19 represents the forward voltage drop of the secondary rectifier diode. By setting the primary output voltage  $V_{OUT}$  to 12.7-V by selecting the correct feedback resistors, the secondary voltage is regulated at 12-V nominally. Adjustment of the primary side  $V_{OUT}$  may be required to compensate for voltage errors due to the leakage inductance of the transformer, the resistance of the transformer windings, the diode drop in the power path on the secondary side and the low-side FET of the LM5161.

#### 8.2.2.2.2 Secondary Rectifier Diode

The secondary side rectifier diode must block the maximum input voltage reflected at secondary side switch node. The minimum diode reverse voltage  $V_{(RD1)}$  rating is given in 公式 20:

$$V_{RD1} = V_{IN(max)} \times \frac{N_2}{N_1} + V_{OUTISO} = 72V \times 1 + 12V = 84V \quad (20)$$

A diode of 100-V or higher reverse voltage rating must be selected in this application. If the input voltage ( $V_{IN}$ ) has transients above the normal operating maximum input voltage of 72 V, then the worst-case transient input voltage must be used in the 公式 20 while selecting the secondary side rectifier diode.

#### 8.2.2.2.3 External Ripple Circuit

The FPWM pin in the LM5161 should never be grounded or left open when used in a Fly-Buck application. Type 3 ripple circuit is required for Fly-Buck applications. Follow the design procedure used in the buck converter for selecting the Type 3 ripple injection components. See [Ripple Configuration](#) for ripple design information.

#### 8.2.2.2.4 Output Capacitor ( $C_{VISO}$ )

The Fly-Buck output capacitor conducts higher ripple current than a buck converter output capacitor. The ripple voltage across the isolated output capacitor is calculated based on the time the rectifier diode is off. During this time the entire output current is supplied by the output capacitor. The required capacitance for the worst-case ripple voltage can be calculated using 公式 21 where,  $\Delta V_{ISO}$  is the expected ripple voltage at the secondary output.

$$C_{VISO} = \frac{I_{ISO}}{\Delta V_{ISO}} \left( \frac{V_{PRI}}{V_{IN(MIN)}} \right) \times \frac{1}{f_{sw}} \quad (21)$$

公式 21 is an approximation and ignores the ripple components associated with ESR and ESL of the output capacitor. For a  $\Delta V_{ISO} = 100$  mV, 公式 21 requires  $C_{VISO} = 11.12$   $\mu$ F. When selecting the  $C_{VISO}$  output capacitors (C2 and C3 in the 图 34), the DC bias must be considered in order to ensure sufficient capacitance over the output voltage.

### 8.2.2.3 Application Curves

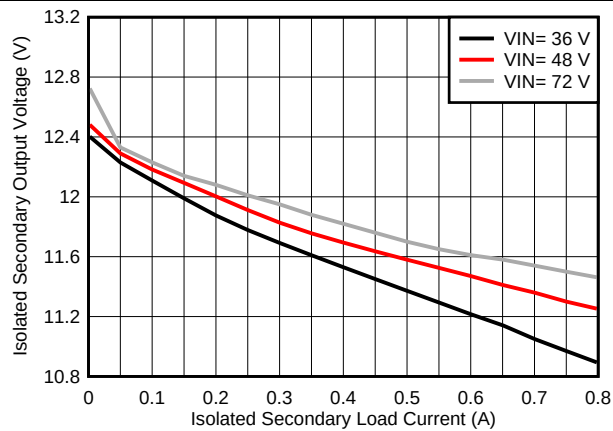


图 35. Load Regulation

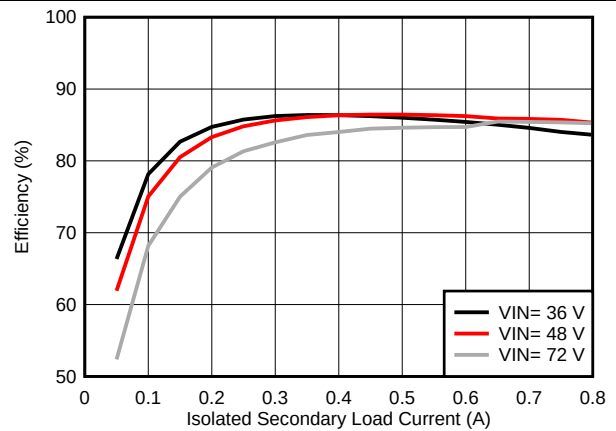


图 36. Efficiency vs I<sub>ISO</sub>

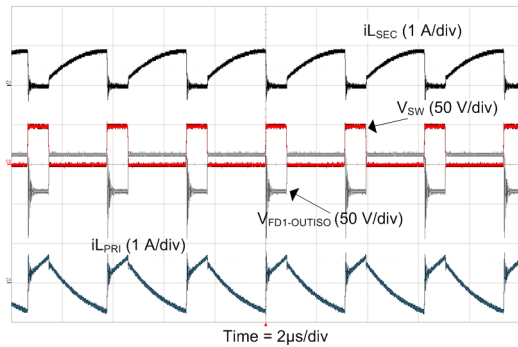


图 37. Steady State at V<sub>IN</sub> = 48 V and I<sub>OUT2</sub> = 500 mA

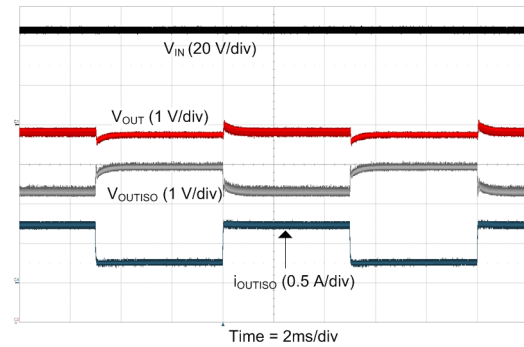


图 38. Secondary Load Transient at I<sub>ISO</sub> = 250 mA - 750 mA

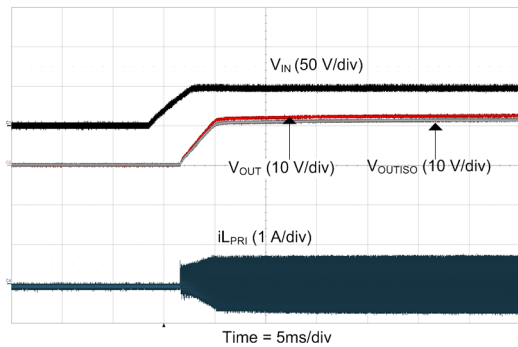


图 39. VIN Start-up at I<sub>ISO</sub> = 500 mA

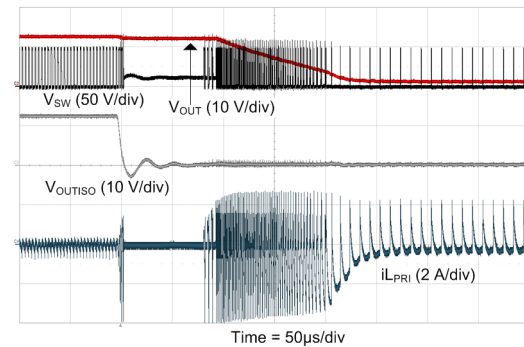


图 40. Secondary-Side Short at I<sub>OUT2</sub> = 0 A and I<sub>PRI</sub> = 0 A

### 8.2.3 Ripple Configuration

LM5161 uses a Constant-On-Time (COT) control scheme, in which the ON-time is terminated by a one-shot, and the OFF-time is terminated by the feedback voltage ( $V_{FB}$ ) falling below the reference voltage. Therefore, for stable operation, the feedback voltage must decrease monotonically and in phase with the inductor current during the OFF-time. Furthermore, this change in feedback voltage ( $V_{FB}$ ) during OFF-time must be large enough to dominate any noise present at the feedback node.

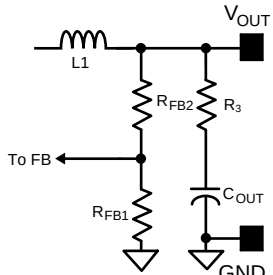
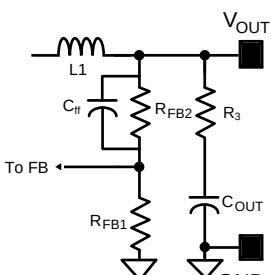
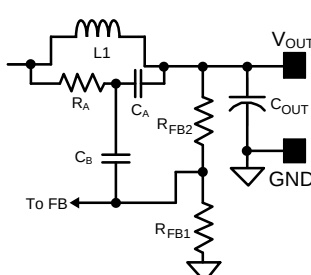
表 5 presents three different methods for generating appropriate voltage ripple at the feedback node. Type 1 and Type 2 ripple circuits couple the ripple from the output of the converter to the feedback node (FB). The output voltage ripple has two components:

1. Capacitive ripple caused by the inductor current ripple charging or discharging the output capacitor.
2. Resistive ripple caused by the inductor current ripple flowing through the ESR of the output capacitor and  $R_3$ .

The capacitive ripple is out-of-phase with the inductor current. As a result, the capacitive ripple does not decrease monotonically during the OFF-time. The resistive ripple is in phase with the inductor current and decreases monotonically during the OFF-time. The resistive ripple must exceed the capacitive ripple at output ( $V_{OUT}$ ) for stable operation. If this condition is not satisfied unstable switching behavior is observed in COT converters, with multiple ON-time bursts in close succession followed by a long OFF-time.

Type 3 ripple method uses a ripple injection circuit with  $R_A$ ,  $C_A$  and the switch node (SW) voltage to generate a triangular ramp. This triangular ramp is then AC-coupled into the feedback node (FB) using the capacitor  $C_B$ . Because this circuit does not use the output voltage ripple, it is suited for applications where low output voltage ripple is imperative. See application note [Controlling Output Ripple and Achieving ESR Independence in Constant On-Time \(COT\) Regulator Designs](#) for more details for each ripple generation method.

**表 5. Ripple Configuration**

| TYPE 1                                                                                                                                      | TYPE 2                                                                                                                                       | TYPE 3                                                                                                                                        |
|---------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| Lowest Cost                                                                                                                                 | Reduced Ripple                                                                                                                               | Minimum Ripple                                                                                                                                |
|  <p>Copyright © 2016, Texas Instruments Incorporated</p> |  <p>Copyright © 2016, Texas Instruments Incorporated</p> |  <p>Copyright © 2016, Texas Instruments Incorporated</p> |
| $R_3 \geq \frac{25 \text{ mV} \times V_O}{V_{REF} \times \Delta I_{L1, \min}} \quad (22)$                                                   | $C_{ff} \geq \frac{5}{F_{SW} \times (R_{FB2} \parallel R_{FB1})}$ $R_3 \geq \frac{25 \text{ mV}}{\Delta I_{L1, \min}} \quad (23)$            | $R_A C_A \leq \frac{(V_{IN, \min} - V_O) \times T_{ON}(@ V_{IN, \min})}{25 \text{ mV}} \quad (24)$                                            |

### 8.3 Do's and Don'ts

As mentioned earlier in [Soft-Start](#), the SS capacitor  $C_{SS}$ , must be more than 1 nF in both Buck and Fly-Buck applications. Apart from determining the start-up time, this capacitor serves for the external compensation of the internal  $G_M$  error amplifier. A minimum value of 1 nF is necessary to maintain stability. The SS pin must not be left floating.

When the FPWM pin is shorted to ground or left unconnected, no external ripple injection is necessary in a Buck application. Should an external feedback ripple circuit be configured when FPWM = 0, it will produce higher ripple at the output.

## Do's and Don'ts (接下页)

Add a resistor ( $>3\Omega$ ) in series with the BST capacitor when using the part in  $FPWM = 0$ , as described in detail in [Forced Pulse Width Modulation \(FPWM\) Mode](#).

When configured as a Fly-Buck, the  $FPWM$  pin must always be connected to  $VCC$ . A Fly-Buck application must operate in the continuous conduction mode all the time in order to maintain adequate voltage regulation on the secondary side.  $FPWM = 0$  is not a valid mode in the Fly-Buck application.

## 9 Power Supply Recommendations

The LM5161 is designed to operate with an input power supply capable of supplying a voltage range between 4.5 V and 100 V. The power supply should be well regulated and capable of supplying sufficient current to the regulator during the sync buck mode or the isolated Fly-Buck mode of operation. As in all DC/DC applications, the power supply source impedance must be small compared to the converter input impedance in order to maintain the stability of the converter.

If the LM5161 is used in a buck topology with low input supply voltage (4.5 V) and large load current (1 A), it is prudent to add a large electrolytic capacitor, in parallel the  $C_{IN}$  capacitors. The electrolytic capacitor stabilizes the input voltage to the IC and prevent droop or oscillation, over the entire load range. Also, it is necessary to add the electrolytic capacitor or a ceramic capacitor in series with appropriate ESR, parallel to the input capacitors  $C_{IN}$ , in order to dampen the input voltage spikes, as detected by the LM5161 when connected to a power supply with long power leads. These input voltage spikes can easily be twice the input voltage step amplitude and a damping capacitor is necessary to contain the input voltage to less than 100V in order to protect the LM5161.

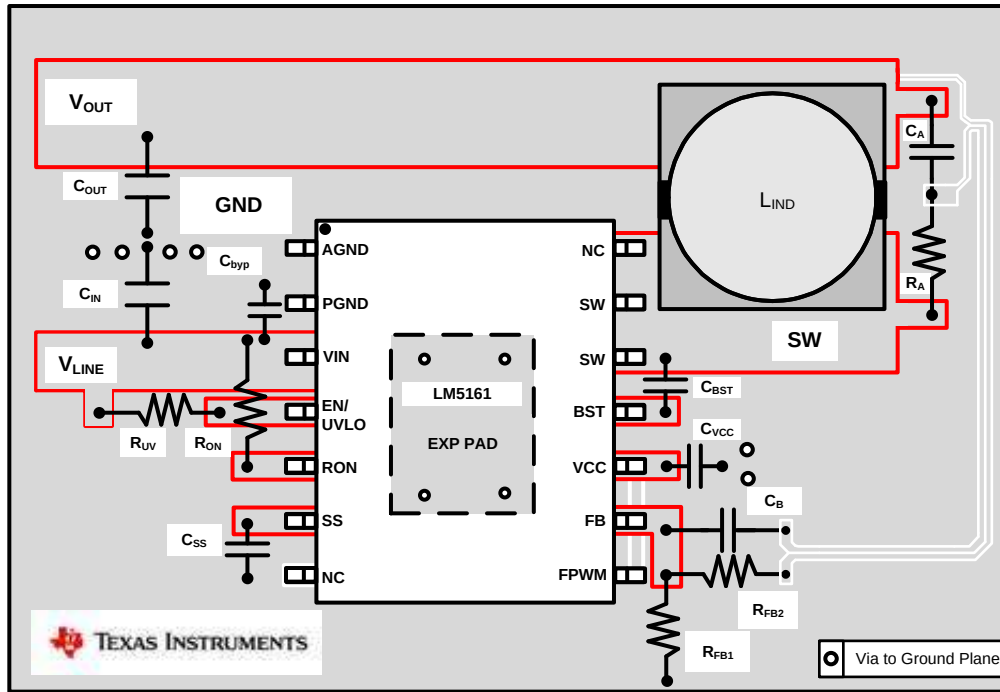
## 10 Layout

### 10.1 Layout Guidelines

A proper layout is essential for optimum performance of the circuit. In particular, observe the following layout guidelines:

- $C_{IN}$ : The loop consisting of input capacitor ( $C_{IN}$ ), VIN pin, and PGND pin carries the switching current. Therefore, in the LM5161, the input capacitor must be placed close to the IC, directly across VIN and PGND pins, and the connections to these two pins should be direct to minimize the loop area. In general it is not possible to place all of input capacitances near the IC. However, a good layout practice includes placing the bulk capacitor as close as possible to the VIN pin (see [图 41](#)). When using the LM5161 HTSSOP-14 package, a bypass capacitor ( $C_{byp}$ ) measuring  $\sim 0.1 \mu F$  must be placed directly across VIN and PGND (pin 3 and 2), as close as possible to the IC while complying with all layout design rules.
- The  $R_{ON}$  resistor between the VIN and the RON pin and the SS capacitor should be placed as close as possible to their respective pins.
- $C_{VCC}$  and  $C_{BST}$ : The VCC and bootstrap (BST) bypass capacitors supply switching currents to the high-side and low-side gate drivers. These two capacitors should also be placed as close to the IC as possible, and the connecting trace lengths and the loop area must be kept at minimum (see [图 41](#)).
- The feedback trace carries the output voltage information and a small ripple component that is necessary for proper operation of the LM5161. Therefore, care must be taken while routing the feedback trace to avoid coupling any noise into this pin. In particular, the feedback trace must be short and not run close to magnetic components, or parallel to any other switching trace.
- In  $FPWM=1$  mode, if a ripple injection circuit is being used for ripple generation at the FB pin, it is considered a good layout practice to lay out the feedback ripple injection DC trace and the  $V_{OUT}$  trace differentially. This scheme helps in reducing the scope for any noise injection at the FB pin.
- SW trace: The SW node switches rapidly between VIN and GND every cycle and is therefore a source of noise. The SW node area must be kept at minimum. In particular, the SW node should not be inadvertently connected to a copper plane or pour.

## 10.2 Layout Example



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图 41. Typical Buck Layout Example with the LM5161

## 11 器件和文档支持

### 11.1 使用 WEBENCH® 工具创建定制设计

单击[此处](#)，使用 LM5161 器件并借助 WEBENCH® 电源设计器创建定制设计方案。

1. 首先键入输入电压 ( $V_{IN}$ )、输出电压 ( $V_{OUT}$ ) 和输出电流 ( $I_{OUT}$ ) 要求。
2. 使用优化器拨盘优化关键参数设计，如效率、封装和成本。
3. 将生成的设计与德州仪器 (TI) 的其他解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案导出至常用 CAD 格式
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 [www.ti.com/WEBENCH](http://www.ti.com/WEBENCH)。

### 11.2 相关文档

- [AN-2292 设计隔离式降压 \(Fly-Buck\) 转换器](#)
- [AN-1481 《在恒定导通时间稳压器设计中控制输出纹波并获得 ESR 非相关性》](#)
- [AN-1481 《在恒定导通时间稳压器设计中控制输出纹波并获得 ESR 非相关性》](#)

[AN-1481 《在恒定导通时间稳压器设计中控制输出纹波并获得 ESR 非相关性》](#) 应用报告，

### 11.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。请单击右上角的提醒我 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 11.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

**TI E2E™ 在线社区** TI 的工程师对工程师 (E2E) 社区。此社区的创建目的在于促进工程师之间的协作。在 [e2e.ti.com](http://e2e.ti.com) 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

**设计支持** TI 参考设计支持 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

### 11.5 商标

E2E is a trademark of Texas Instruments.

WEBENCH is a registered trademark of Texas Instruments.

### 11.6 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 11.7 Glossary

**SLYZ022** — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

## 12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

## PACKAGING INFORMATION

| Orderable part number      | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|----------------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">LM5161PWPR</a> | Active        | Production           | HTSSOP (PWP)   14 | 2500   LARGE T&R      | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 125   | LM5161<br>PWP       |
| LM5161PWPR.A               | Active        | Production           | HTSSOP (PWP)   14 | 2500   LARGE T&R      | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 125   | LM5161<br>PWP       |
| <a href="#">LM5161PWPT</a> | Active        | Production           | HTSSOP (PWP)   14 | 250   SMALL T&R       | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 125   | LM5161<br>PWP       |
| LM5161PWPT.A               | Active        | Production           | HTSSOP (PWP)   14 | 250   SMALL T&R       | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 125   | LM5161<br>PWP       |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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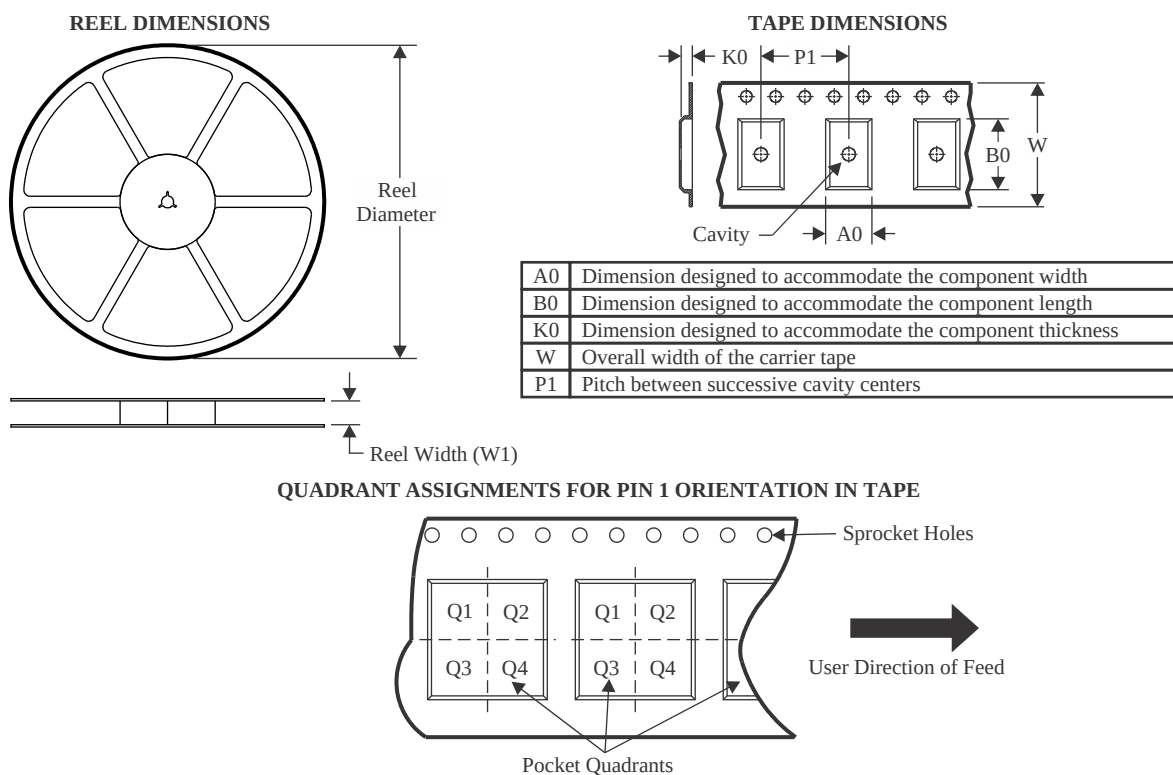
**OTHER QUALIFIED VERSIONS OF LM5161 :**

- Automotive : [LM5161-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

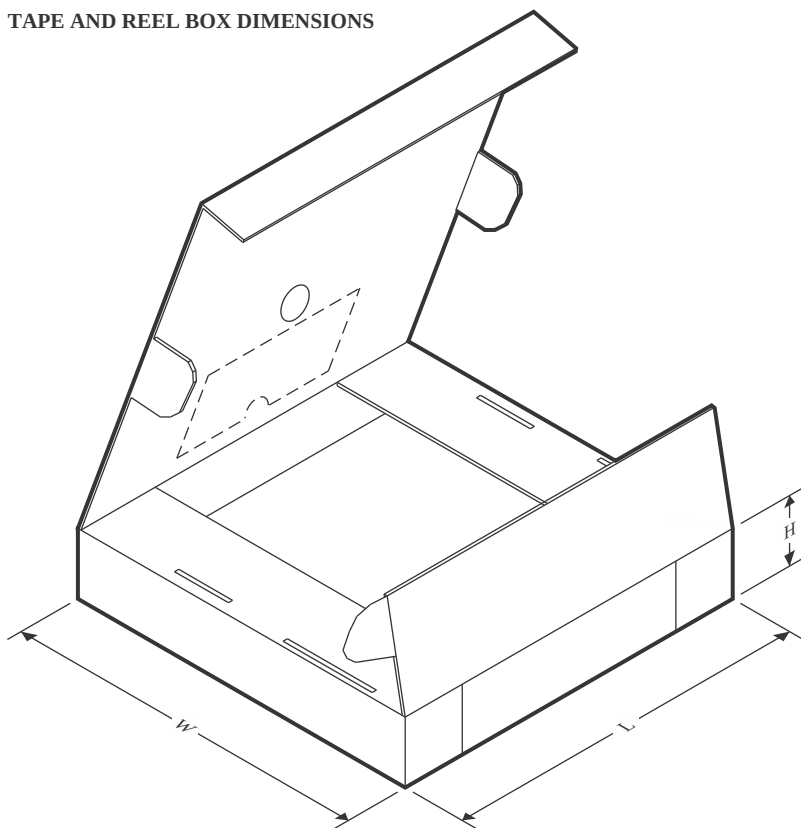
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LM5161PWPR | HTSSOP       | PWP             | 14   | 2500 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| LM5161PWPT | HTSSOP       | PWP             | 14   | 250  | 177.8              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LM5161PWPR | HTSSOP       | PWP             | 14   | 2500 | 356.0       | 356.0      | 36.0        |
| LM5161PWPT | HTSSOP       | PWP             | 14   | 250  | 208.0       | 191.0      | 35.0        |



## PowerPAD™ TSSOP - 1.2 mm max height

Technical drawing of a 14-pin D-subminiature connector. The drawing includes a top view, a side view, and a detail view of the pin and shell interface.

**Top View Dimensions:**

- Overall width: 6.6 (typical), 6.2
- Overall height: 5.1, 4.9 (NOTE 3)
- Pin 1 ID Area: Indicated by a dashed rectangle.
- Pin 14 position: 12X 0.65, 2X 3.9, 14X 0.30, 0.19
- Pin 8 position: 14X 0.30, 0.19
- Pin 1 position: 4.5, 4.3

**Side View Dimensions:**

- Seating Plane: Indicated by a dashed line.
- Pin 14 position: 12X 0.65, 2X 3.9, 14X 0.30, 0.19
- Pin 8 position: 14X 0.30, 0.19
- Pin 1 position: 4.5, 4.3

**Detail A Dimensions:**

- Pin 14 position: 12X 0.65, 2X 3.9, 14X 0.30, 0.19
- Pin 8 position: 14X 0.30, 0.19
- Pin 1 position: 4.5, 4.3
- Pin 14 position: 12X 0.65, 2X 3.9, 14X 0.30, 0.19
- Pin 8 position: 14X 0.30, 0.19
- Pin 1 position: 4.5, 4.3
- Pin 14 position: 12X 0.65, 2X 3.9, 14X 0.30, 0.19
- Pin 8 position: 14X 0.30, 0.19
- Pin 1 position: 4.5, 4.3

PowerPAD is a trademark of Texas Instruments.

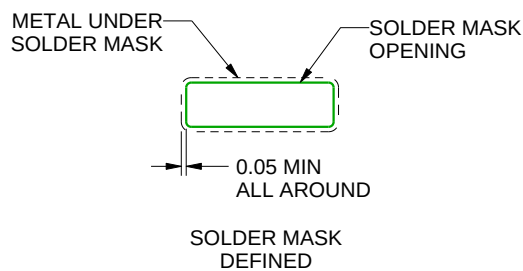
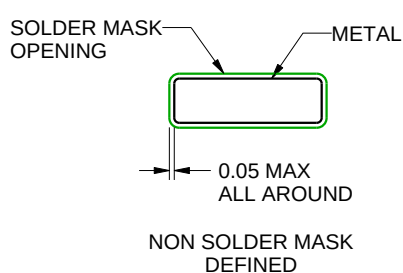
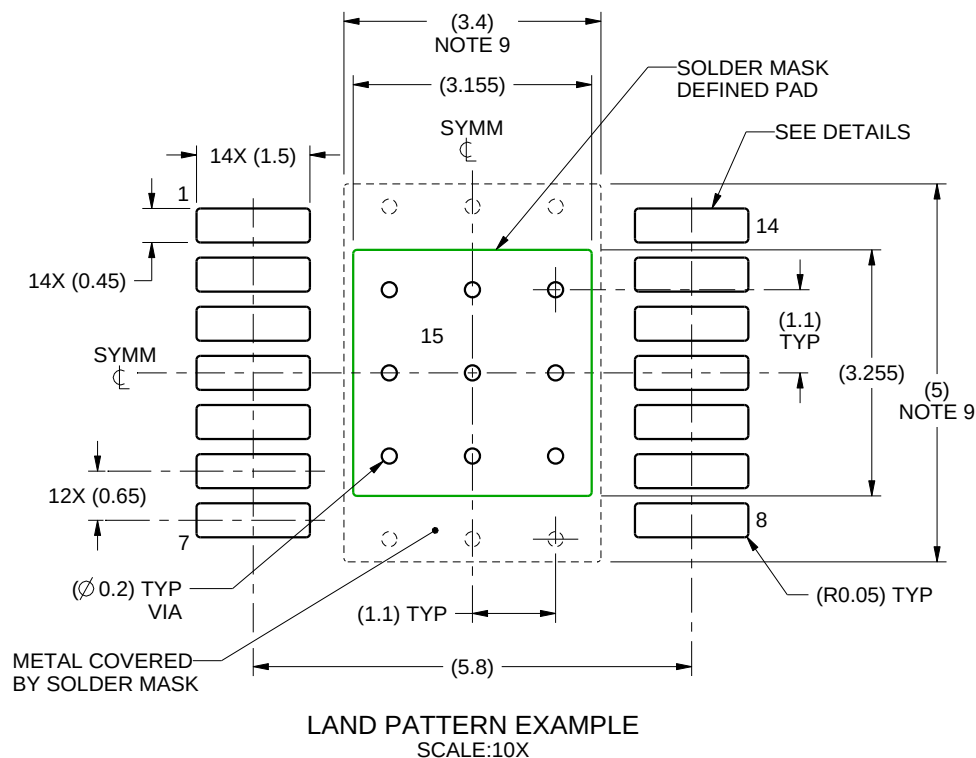
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.

# EXAMPLE BOARD LAYOUT

PWP0014A

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



SOLDER MASK DETAILS  
PADS 1-14

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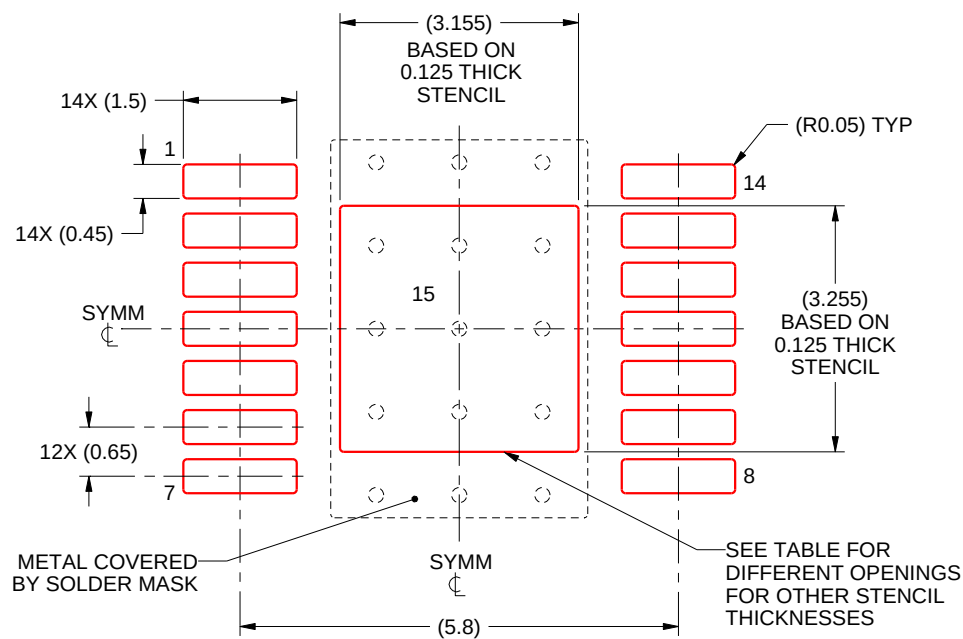
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.

**PWP0014A**

## PowerPAD™ TSSOP - 1.2 mm max height

## PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
EXPOSED PAD  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE:10X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
| 0.1               | 3.53 X 3.64            |
| 0.125             | 3.155 X 3.255 (SHOWN)  |
| 0.15              | 2.88 X 2.97            |
| 0.175             | 2.67 X 2.75            |

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

## 重要通知和免责声明

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