具有输入极性保护功能的 LM66100 5.5V、1.5A、79mΩ、低 IQ 理想二极管

1 特性

- 宽工作电压范围：1.5V 至 5.5V
- 输入电压反向关断电压：
  绝对最大电压为 –6V
- 最大持续电流 (I_{MAX})：1.5A
- 导通电阻 (R_{ON})：
  - 5V V_{IN} = 79mΩ（典型值）
  - 3.6V V_{IN} = 91mΩ（典型值）
  - 1.8V V_{IN} = 141mΩ（典型值）
- 启用比较器芯片 ($\overline{CE}$)
- 通道状态指示 (ST)
- 低电流消耗：
  - 3.6V V_{IN} 关断电流 ($I_{SD,VIN}$)：120nA（典型值）
  - 3.6V V_{IN} 静态电流 ($I_{Q,\ VIN}$)：150nA（典型值）

2 应用

- 智能仪表
- 楼宇自动化
- GPS 和跟踪
- 原电池和备用电池

3 说明

LM66100 是单输入单输出 (SISO) 集成式理想二极管，非常适用于各种 解决方案。该器件包含一个可在 1.5V 至 5.5V 输入电压范围内运行的 P 沟道 MOSFET，并且支持 1.5A 的最大持续电流。

该芯片通过比较 $\overline{CE}$ 引脚电压和输入电压来提供支持。当 $\overline{CE}$ 引脚电压高于输入电压时，该器件被禁用并且 MOSFET 关闭。当 $\overline{CE}$ 引脚电压比较低时，MOSFET 开启。LM66100 还具有反极性保护 (RPP) 功能，该功能可以保护器件不受误接线输入的影响，例如电池装反。

可在 ORing 配置中使用两个 LM66100 器件，其实施方法与双二极管 ORing 相似。在此配置中，该器件将最高输出电压传递到输出端，同时阻断反向电流流入输入电源。这些器件可以比较输入和输出电压，以确保内部电压比较器成功阻止反向电流。

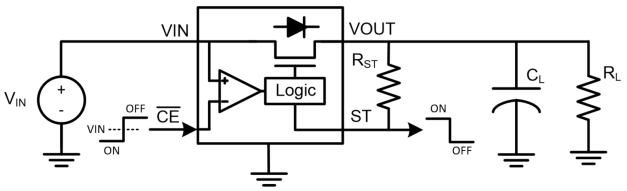
LM66100 采用标准 SC-70 封装，工作结温范围为 –40°C 至 125°C。

器件信息(1)

器件编号	封装	封装尺寸（标称值）
LM66100	SC-70 (6)	2.1mm x 2.0mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用



目录

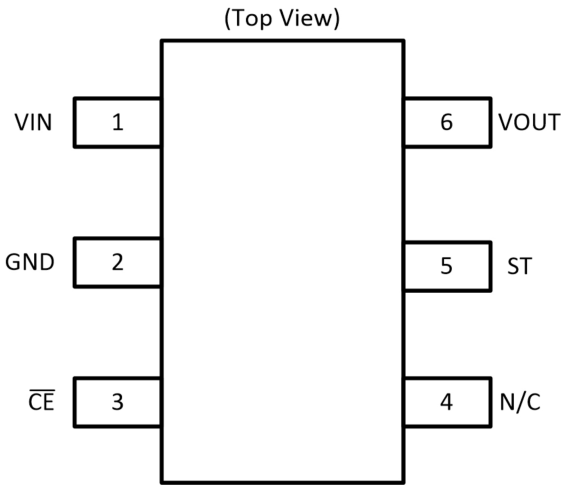
4 修订历史记录

Changes from Original (March 2019) to Revision A **Page**

- 已更改 将“高级信息”更改为“生产数据” 1

5 Pin Configuration and Functions

DCK Package
6-Pin SC-70
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VIN	I	Device input
2	GND	-	Device ground
3	$\overline{CE}$	I	Active-low chip enable. Can be connected to VOUT for reverse current protection. Do not leave floating.
4	N/C	-	Not internally connected, can be tied to GND or left floating.
5	ST	O	Active-low open-drain output, pulled low when the chip is disabled. Hi-Z when the chip is enabled. Connect to GND if not required.
6	VOUT	O	Device output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{IN}	Maximum Input Voltage Range	–6	6	V
V_{OUT}	Maximum Output Voltage Range	–0.3	6	V
$V_{\overline{CE}}$	Maximum $\overline{CE}$ Pin Voltage	–0.3	6	V
V_{ST}	Maximum ST Pin Voltage	–0.3	6	V
$I_{SW, MAX}$	Maximum Continuous Switch Current		1.5	A
$I_{SW, PLS}$	Maximum Pulsed Switch Current (≤120 ms, 2% Duty Cycle)		2.5	A
$I_{D, PLS}$	Maximum Pulsed Body Diode Current (≤0.1 ms, 0.2% Duty Cycle)		2.5	A
$I_{\overline{CE}}$	Maximum $\overline{CE}$ Pin Current	–1		mA
I_{ST}	Maximum ST Pin Current	–1		mA
T_J	Junction temperature	–40	125	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Maximum Lead Temperature (10 s soldering time)		300	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, allpins (1)	±2000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less is possible with the necessary precautions. Pins listed may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range	1.5		5.5	V
V_{OUT}	Output Voltage Range	1		5.5	V
$V_{\overline{CE}}$	$\overline{CE}$ Pin Voltage Range	0		5.5	V
V_{ST}	ST Pin Voltage Range	0		5.5	V

6.4 Thermal Information

THERMAL METRIC (1)		LM66100 DCK (SC-70) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	192	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	124	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	34	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	52	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Typical values are at 25°C with an input voltage of 3.6V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Input Supply (VIN)								
$I_{SD,VIN}$	VIN Shutdown Current	VOUT = VIN $V\overline{CE}$ > VIN + 80mV I_{OUT} = 0 A (VOUT = open)		25°C		0.12	0.3	µA
				-40°C to 105°C			0.3	µA
$I_{Q,VIN}$	VIN Quiescent Current	VOUT = VIN $V\overline{CE}$ < VIN - 250mV I_{OUT} = 0 A (VOUT = open)		25°C		0.15	0.3	µA
				-40°C to 105°C			0.3	µA
$I_{OUT, OFF}$	OUT to IN Leakage Current (Current out of VIN)	VOUT - VIN ≤ 5.5 V $V\overline{CE}$ > VIN + 80mV		25°C		0.2	0.5	µA
				-40°C to 85°C			2.7	µA
				-40°C to 105°C			8	µA
		VOUT - VIN ≤ 4.5 V $V\overline{CE}$ > VIN + 80mV		-40°C to 85°C			1.7	µA
				-40°C to 105°C			5.1	µA
		VOUT - VIN ≤ 1.0 V $V\overline{CE}$ > VIN + 80mV		-40°C to 85°C			0.7	µA
				-40°C to 105°C			2.1	µA
ON-Resistance (RON)								
R_{ON}	ON-State Resistance	IOUT = -200 mA	VIN = 5 V	25°C		79	95	mΩ
				-40°C to 85°C			110	
				-40°C to 125°C			120	
R_{ON}	ON-State Resistance	IOUT = -200 mA	VIN = 3.6 V	25°C		91	110	mΩ
				-40°C to 85°C			125	
				-40°C to 125°C			140	
R_{ON}	ON-State Resistance	IOUT = -200 mA	VIN = 1.8 V	25°C		141	180	mΩ
				-40°C to 85°C			210	
				-40°C to 125°C			230	
Comparator Chip Enable (CE)								
V_{ON}	Turn ON Threshold	$V\overline{CE}$ - VIN		-40°C to 125°C	–250	–150	–80	mV
V_{OFF}	Turn OFF Threshold	$V\overline{CE}$ - VIN		-40°C to 125°C	0	35	80	mV
$I_{\overline{CE}}$	$\overline{CE}$ Pin Leakage Current	VCE < VIN - 250mV		-40°C to 125°C	0	160	300	nA
$I_{\overline{CE}}$	$\overline{CE}$ Pin Leakage Current	$V\overline{CE}$ > VIN + 80mV		-40°C to 125°C	0	400	610	nA
Reverse Current Blocking (RCB) and Body Diode Characteristics								
I_{RCB}	Reverse Activation Current	$V\overline{CE}$ = VOUT		-40°C to 125°C		0.5	1	A
V_{FWD}	Body Diode Forward Voltage	I_{OUT} = 10 mA $V\overline{CE}$ > VIN + 80mV		-40°C to 125°C	0.1	0.5	1.1	V
Status Indication (ST)								
$V_{OL, ST}$	Output Low Voltage	IST = 1 mA		-40°C to 125°C			0.1	V
t_{ST}	Status Delay Time	$V\overline{CE}$ transitions from low to high		-40°C to 125°C		1		µs
I_{ST}	ST Pin Leakage Current	$V\overline{CE}$ < VIN - 250mV		-40°C to 125°C	–20		20	nA

6.6 Switching Characteristics

Unless otherwise noted, the typical characteristics in the following table applies over the entire recommended operating voltage at an ambient temperature of 25°C and a load of C_L = 100 nF and R_L = 1kΩ

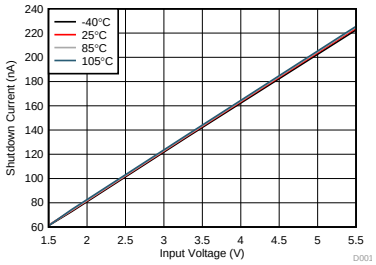
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Turn ON Time	VIN = 1.8 V		90		µs
		VIN = 3.6 V		40		µs
		VIN = 5 V		27		µs
t_{OFF}	Turn OFF Time	VIN = 1.8 V		2		µs
		VIN = 3.6 V		2		µs
		VIN = 5 V		2		µs

Switching Characteristics (continued)

Unless otherwise noted, the typical characteristics in the following table applies over the entire recommended operating voltage at an ambient temperature of 25°C and a load of C_L = 100 nF and R_L = 1kΩ

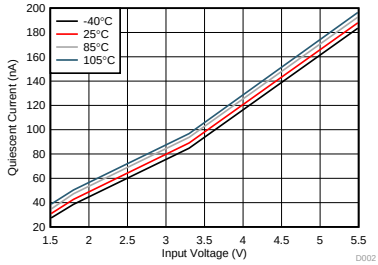
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{FALL}	Output Fall Time	VIN = 1.8 V		20		µs
		VIN = 3.6 V		10		µs
		VIN = 5 V		7.5		µs

6.7 Typical Characteristics



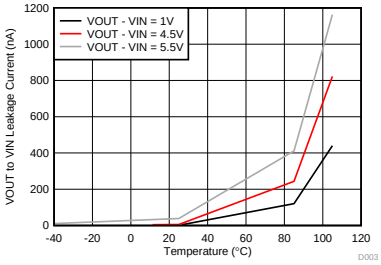
$V_{\overline{CE}} > V_{IN}$

图 1. Shutdown Current vs Input Voltage



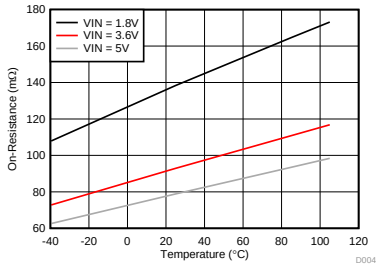
$V_{\overline{CE}} < V_{IN}$

图 2. Quiescent Current vs Input Voltage



$V_{\overline{CE}} > V_{IN}$

图 3. Reverse Leakage Current vs Junction Temperature



$V_{\overline{CE}} < V_{IN}$ I_{OUT} = 200mA

图 4. On-Resistance vs Junction Temperature

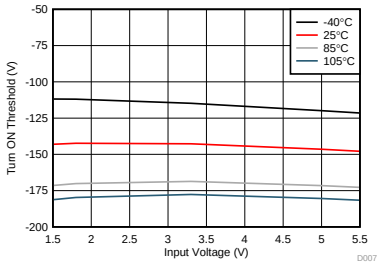


图 5. Turn ON Threshold vs Input Voltage

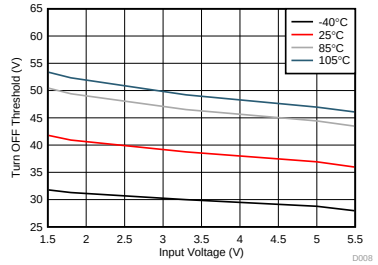
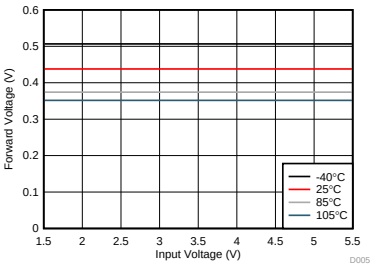


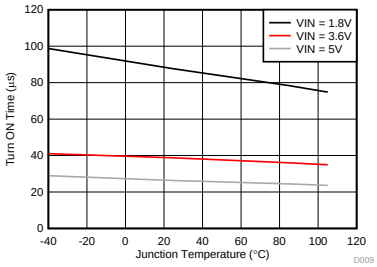
图 6. Turn OFF Threshold vs Input Voltage

Typical Characteristics (接下页)



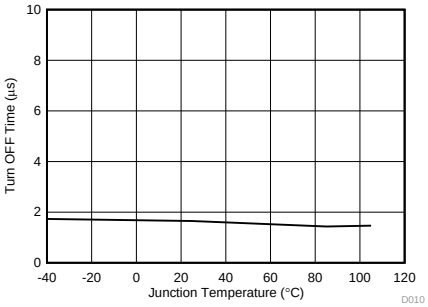
$V_{\overline{CE}} > V_{IN}$ I_{OUT} = 10mA

图 7. Body Diode Forward Voltage vs Input Voltage



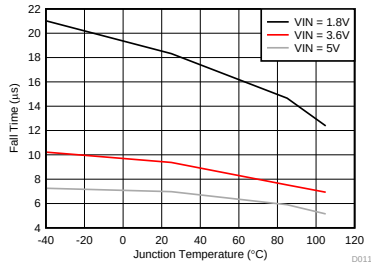
C_L = 100nF R_L = 1kΩ

图 8. Turn ON Time vs Junction Temperature



C_L = 100nF R_L = 1kΩ V_{IN} = 1.8V to 5V

图 9. Turn OFF Time vs Junction Temperature



C_L = 100nF R_L = 1kΩ

图 10. Fall Time vs Junction Temperature

7 Parameter Measurement Information

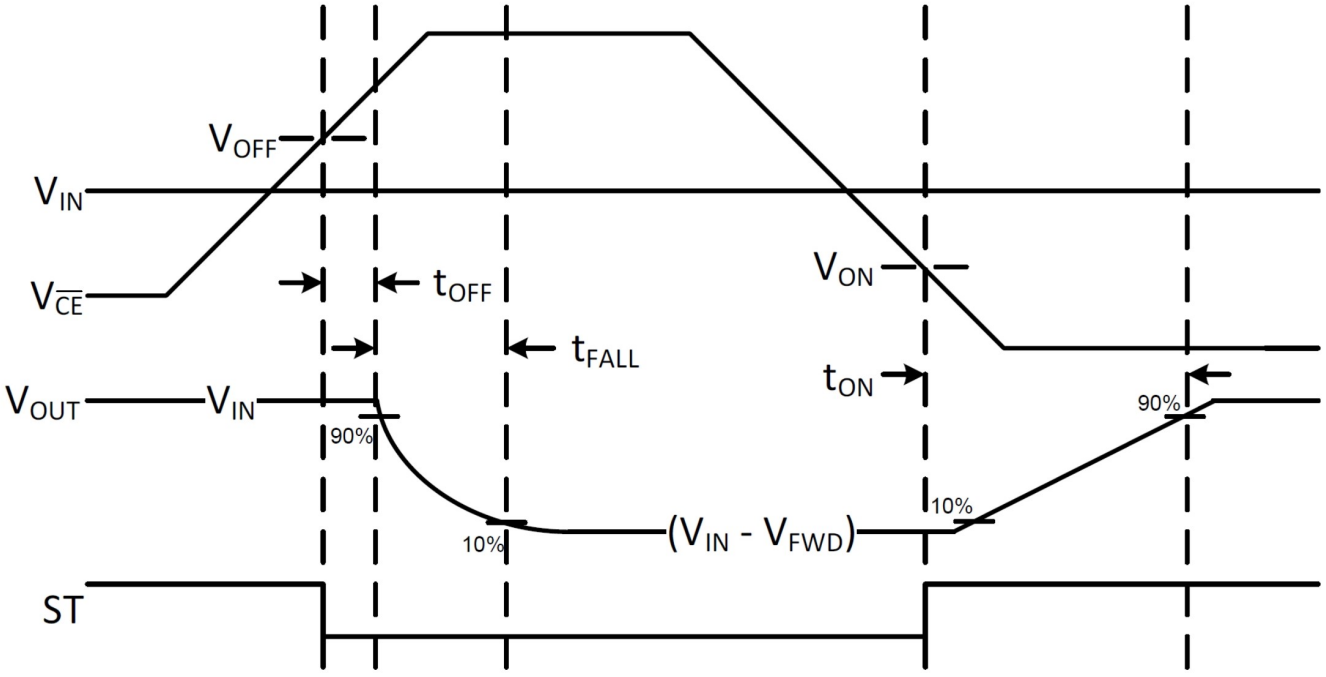


图 11. Timing Diagram

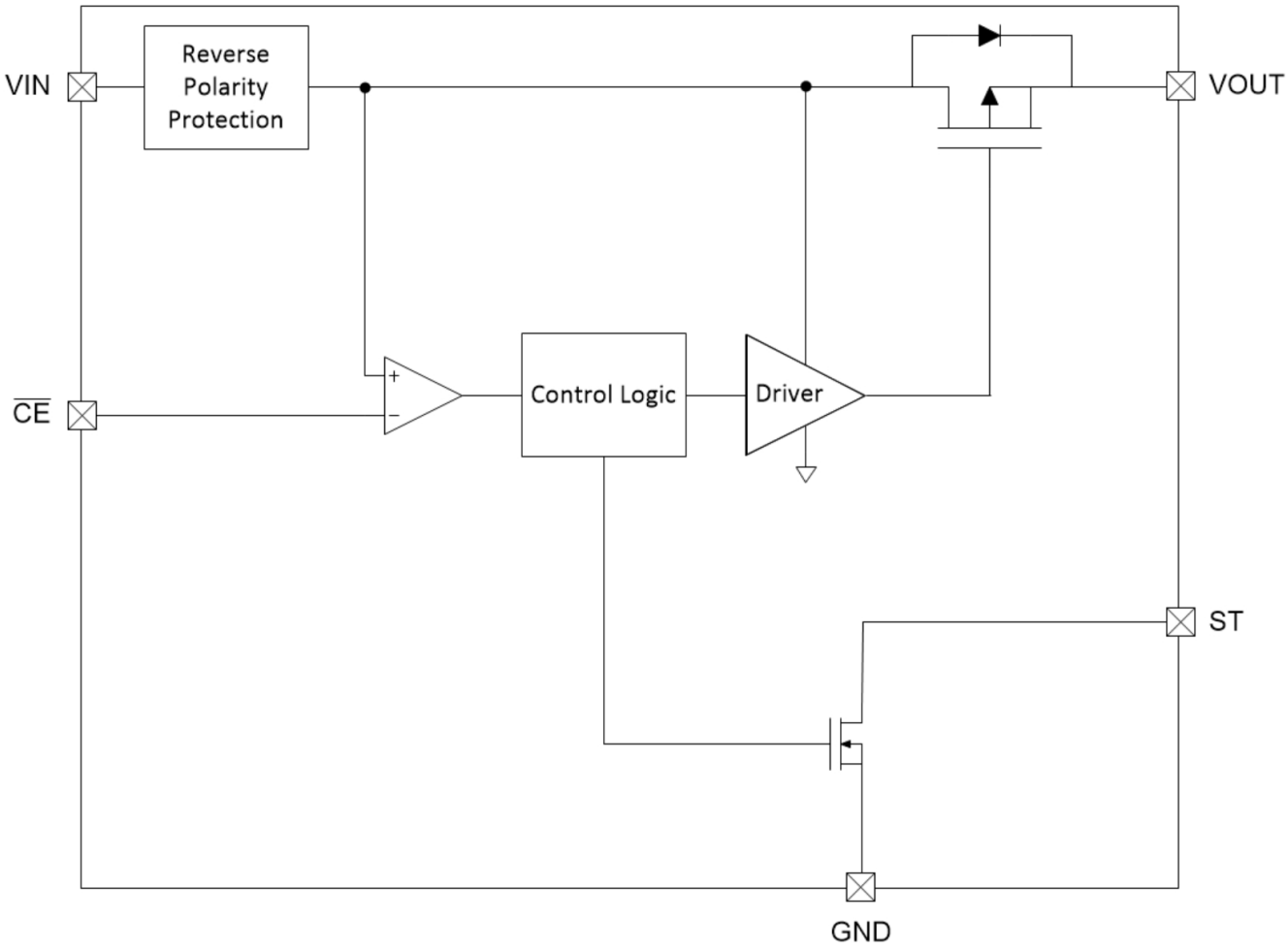
8 Detailed Description

8.1 Overview

The LM66100 is a Single-Input, Single-Output (SISO) integrated ideal diode that is well suited for a variety of applications. The device contains a P-channel MOSFET that can operate over an input voltage range of 1.5 V to 5.5 V and can support a maximum continuous current of 1.5 A.

The chip enable works by comparing the $\overline{CE}$ pin voltage to the input voltage. When the $\overline{CE}$ pin voltage is higher than VIN by 80 mV, the device is disabled and the MOSFET is off. When the $\overline{CE}$ pin voltage is lower than V_{IN} by 250 mV, the MOSFET is on. The LM66100 also comes with reverse polarity protection (RPP) that can protect the device from a miswired input, such as a reversed battery.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Reverse Polarity Protection (RPP)

In the event a negative input voltage is applied, the ideal diode will stay off and prevent current flow to protect the system load. For a stand-alone, always on application, $\overline{CE}$ can be tied to GND so it will not go negative with respect to GND see 图 12.

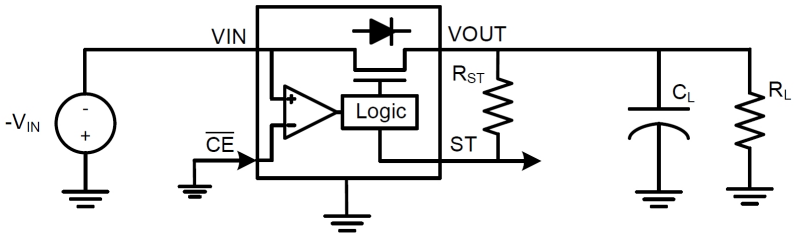


图 12. RPP Protection Circuit

8.3.2 Always-ON Reverse Current Blocking (RCB)

By connecting the $\overline{CE}$ pin to VOUT, this allows the comparator to detect reverse current flow through the switch. If the output is forced above the selected input by V_{OFF}, the channel will switch off to stop the reverse current I_{RCB} within t_{OFF}. Once the output falls to below V_{IN} by V_{ON}, the device will turn back on.

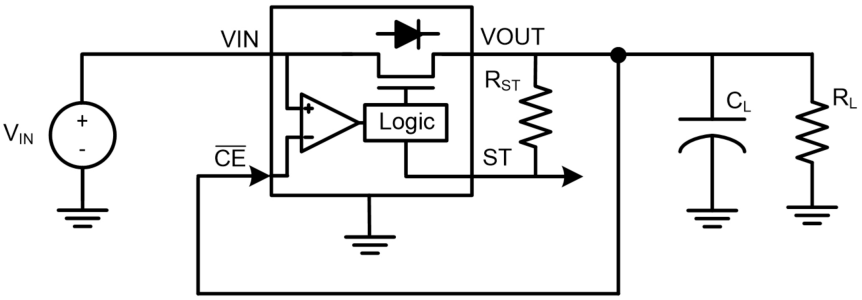


图 13. RCB Circuit

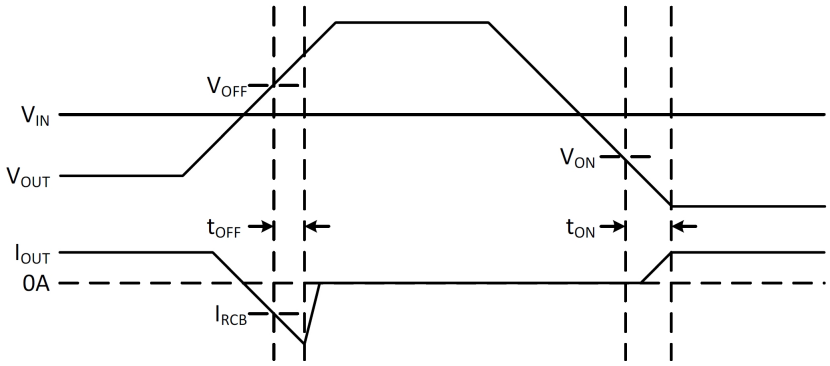


图 14. RCB Waveforms

8.4 Device Functional Modes

表 1 summarizes the Device Functional Modes:

表 1. Device Functional Modes

State	IN-to-OUT	Power Dissipation	ST State
OFF	Diode	I_{OUT} x V_{FWD}	L
ON	Switch	I_{OUT}^2 x R_{ON}	H

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LM66100 Ideal Diode can be used in a variety of stand-alone and multi-channel applications.

9.2 Typical Applications

9.2.1 Dual Ideal Diode ORing

Two LM66100 Ideal Diodes can be used together for ORing between two power supplies.

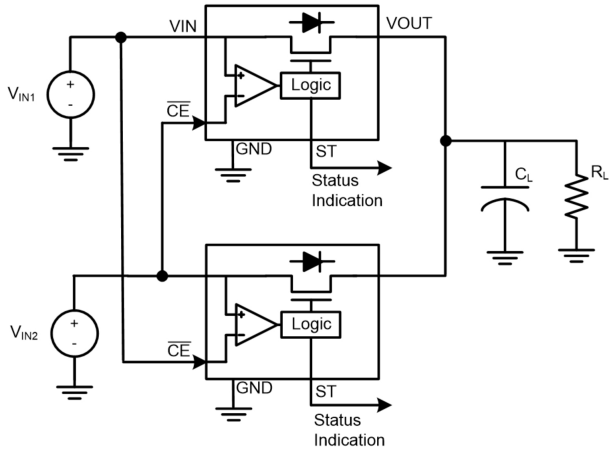


图 15. Dual Ideal Diode ORing

9.2.1.1 Design Requirements

Design a circuit that allows the highest input voltage to power a downstream system while providing reverse current protection.

9.2.1.2 Detailed Design Procedure

This circuit ties the $\overline{CE}$ of each device to the opposite power source. In this configuration, the highest supply will always be selected using a make-before-break logic. This prevents any reverse current flow between the supplies and avoids the need of a dedicated reverse current blocking comparator. For ORing applications that need RPP, it is recommended to use a series resistor ($R_{\overline{CE}}$) to limit the current into the $\overline{CE}$ pin during a negative voltage event.

Typical Applications (接下页)

9.2.1.3 Application Curves

The below scope shot shows the output voltage (VOUT) being initially powered by VIN1. When VIN2 is applied, it powers VOUT because it is a higher voltage. When VIN2 is removed, VOUT is once again powered by VIN1.

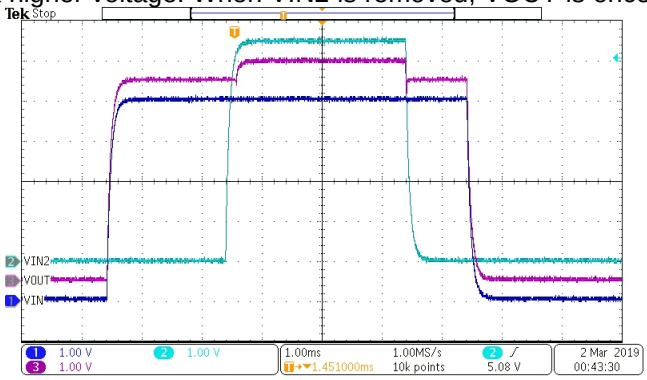


图 16. Dual Ideal Diode ORing Behavior

9.2.2 Dual Ideal Diode ORing for Continuous Output Power

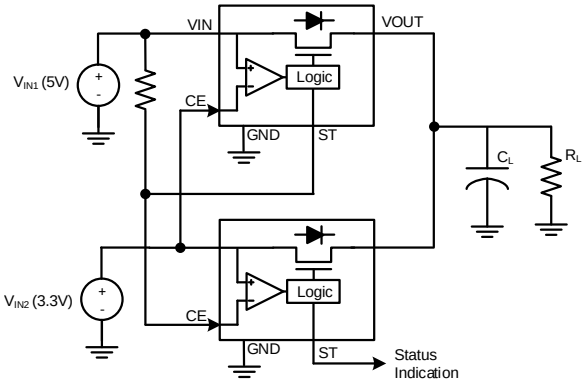


图 17. Dual Ideal Diode ORing for Continuous Output Power

9.2.2.1 Design Requirements

The shortcoming of the previous implementation happens when both input voltages are the same for a long period of time, then both devices will completely turn off, powering down the output load. To avoid this case, the status output from the priority supply and a pull up resistor can be used causing both devices to switchover at the same time. For ORing applications that need RPP, it is recommended to use a series resistor ($R_{\overline{CE}}$) to limit the current into the $\overline{CE}$ pin during a negative voltage event.

Typical Applications (接下页)

9.2.2.2 Application Curves

The figures below show the switchover performance between VIN1 and VIN2.

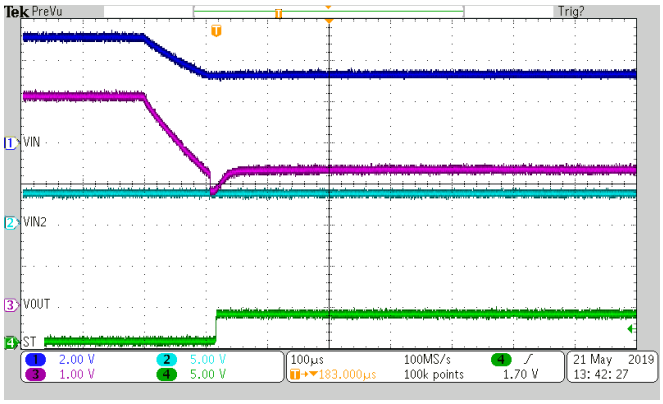


图 18. Switchover from VIN1 (5 V) to VIN2 (3.3 V)

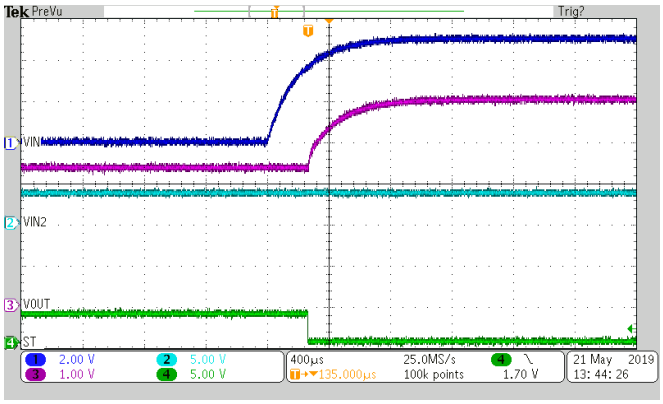


图 19. Switchover from VIN2 (3.3V) to VIN1 (5V)

9.2.3 ORing with Discrete MOSFET

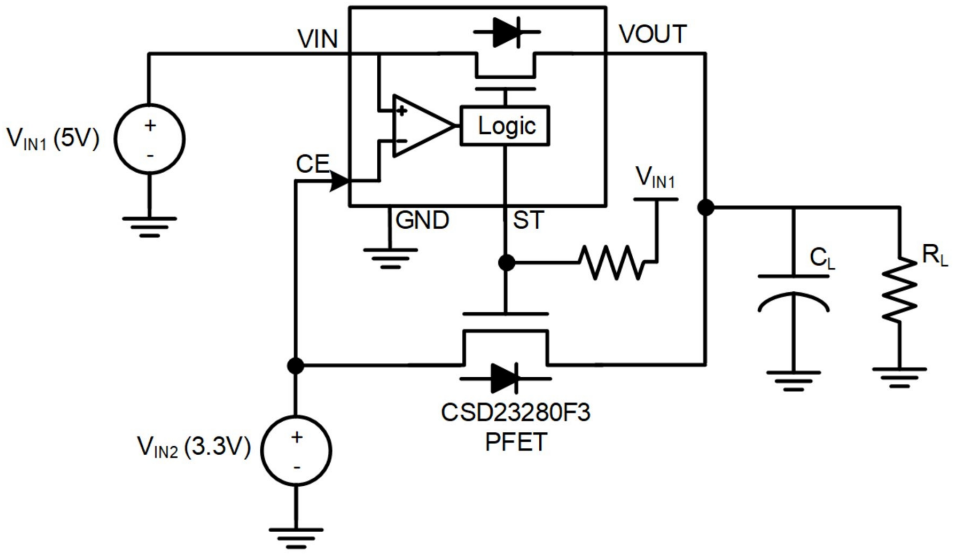


图 20. ORing with a Discrete MOSFET

9.2.3.1 Design Requirements

Similar to the Dual Ideal Diode circuit, the Status Output can also be used to control a discrete P-Channel MOSFET. This can be useful in applications that want to minimize the leakage current on the secondary supply, such as battery backup systems. This configuration can also be used on systems that require a lower RON on the secondary rail, useful for higher current applications.

When the Ideal Diode path is enabled, the status will be Hi-Z and pull up the gate of the external PFET to keep it off. When the main supply (VIN1) drops such that backup supply (VIN2) is higher than VIN1, the ideal diode will be disabled and pull the ST pin and the PFET gate low to turn on the discrete MOSFET path.

Typical Applications (接下页)

9.2.3.2 Application Curves

The figures below show the switchover performance between VIN1 and VIN2.

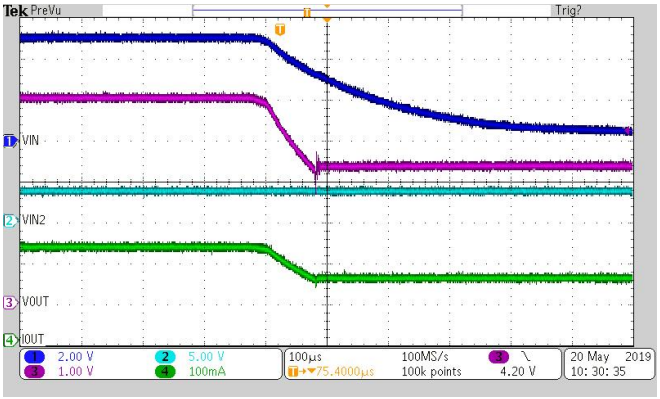


图 21. Switchover from VIN1 5 V to VIN2 3.3 V

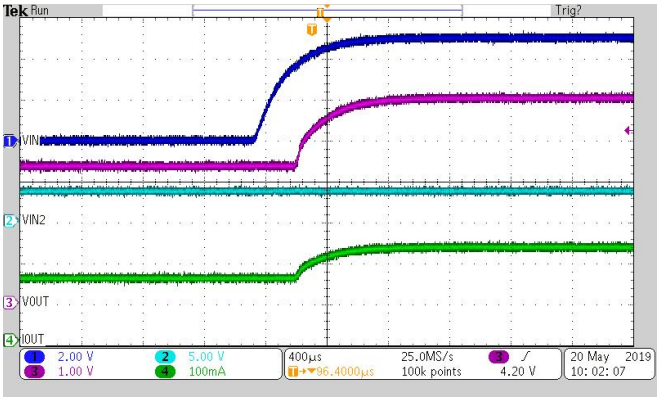


图 22. Switchover from VIN2 3.3 V to VIN1 5 V

10 Power Supply Recommendations

The device is designed to operate with a VIN range of 1.5 V to 5.5 V. The VIN power supply must be well regulated and placed as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance (CIN) of 1 µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

11 Layout

11.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT and GND helps minimize the parasitic electrical effects.

11.2 Layout Example

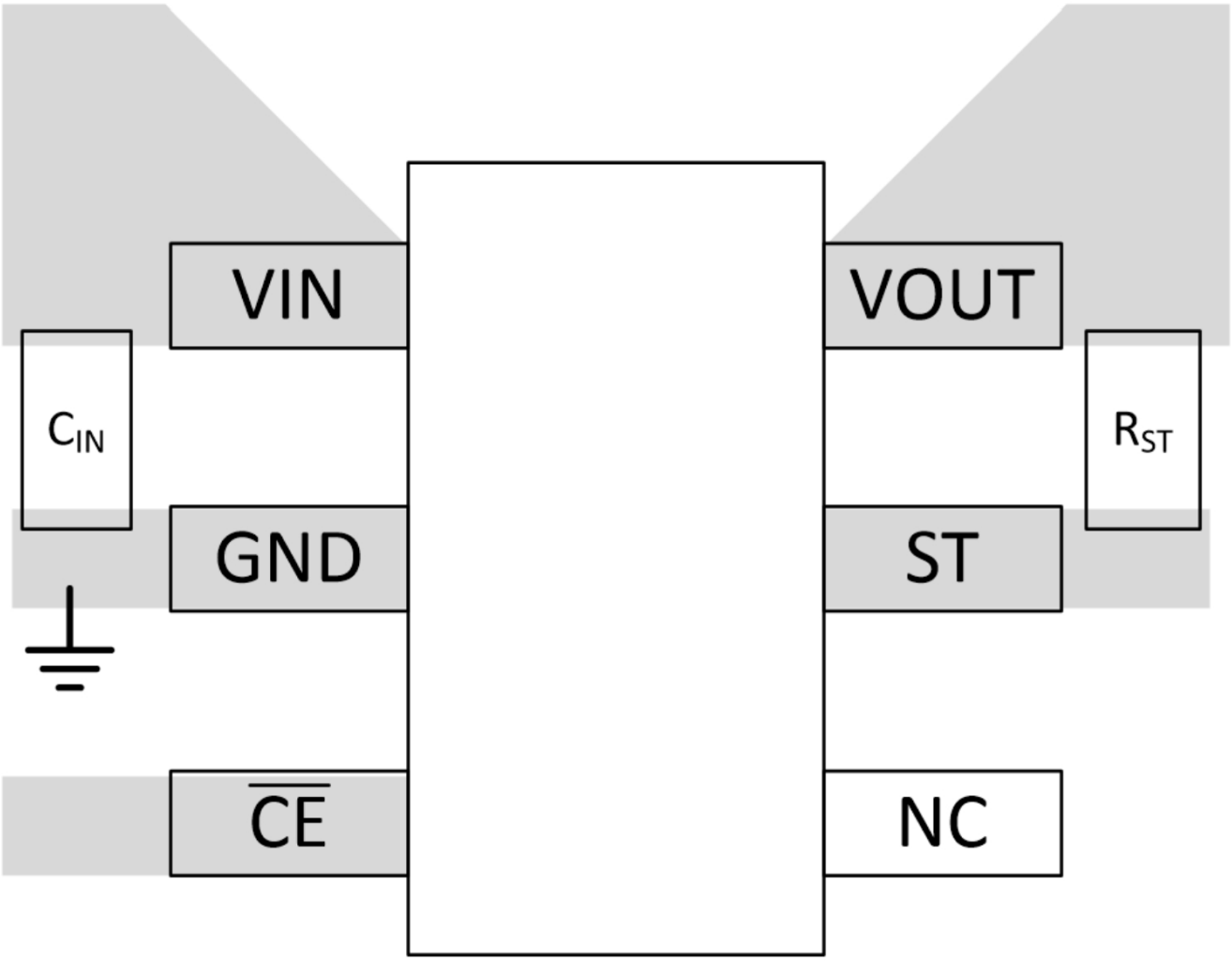


图 23. LM66100 Layout Example

12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 商标

E2E is a trademark of Texas Instruments.

12.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM66100DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1CU	Samples
LM66100DCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 105	1CU	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

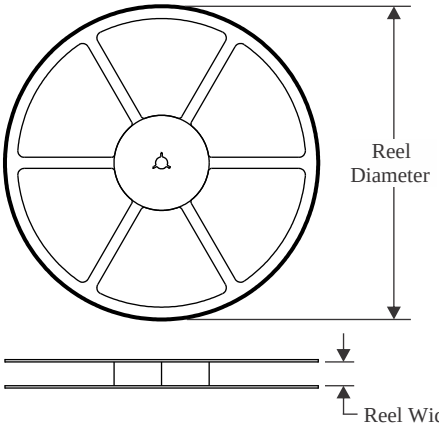
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

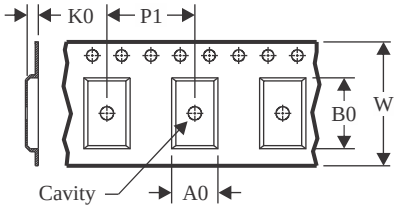
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

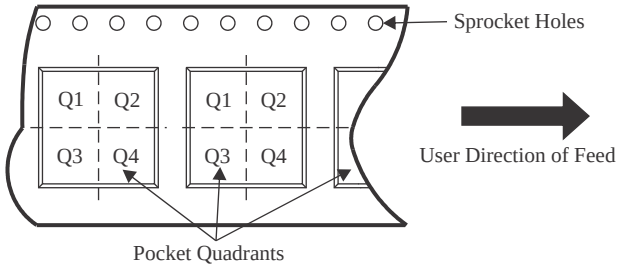


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

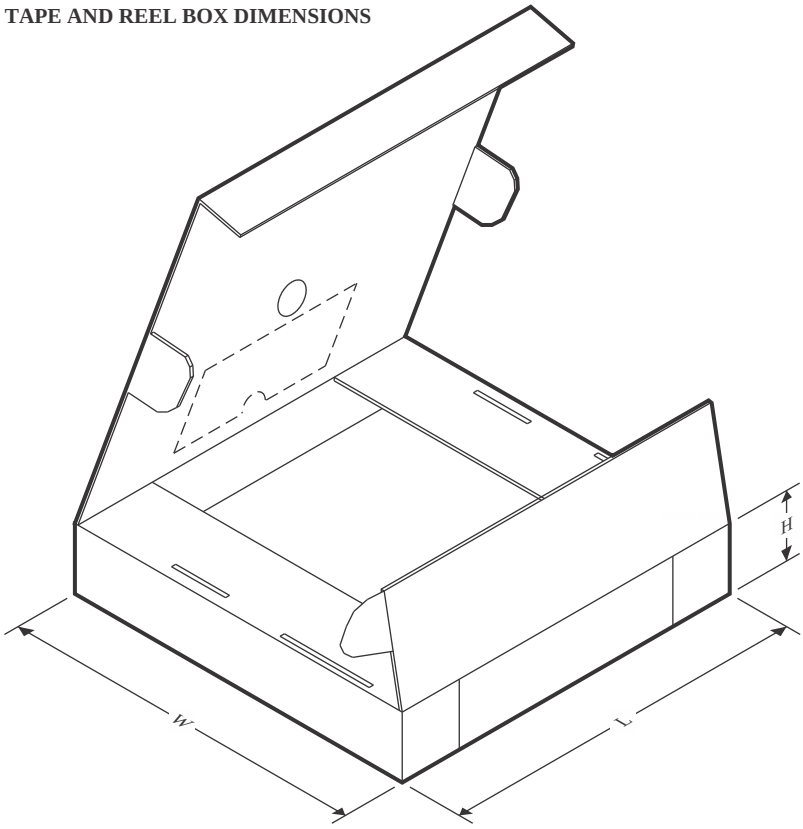
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM66100DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
LM66100DCKT	SC70	DCK	6	250	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3

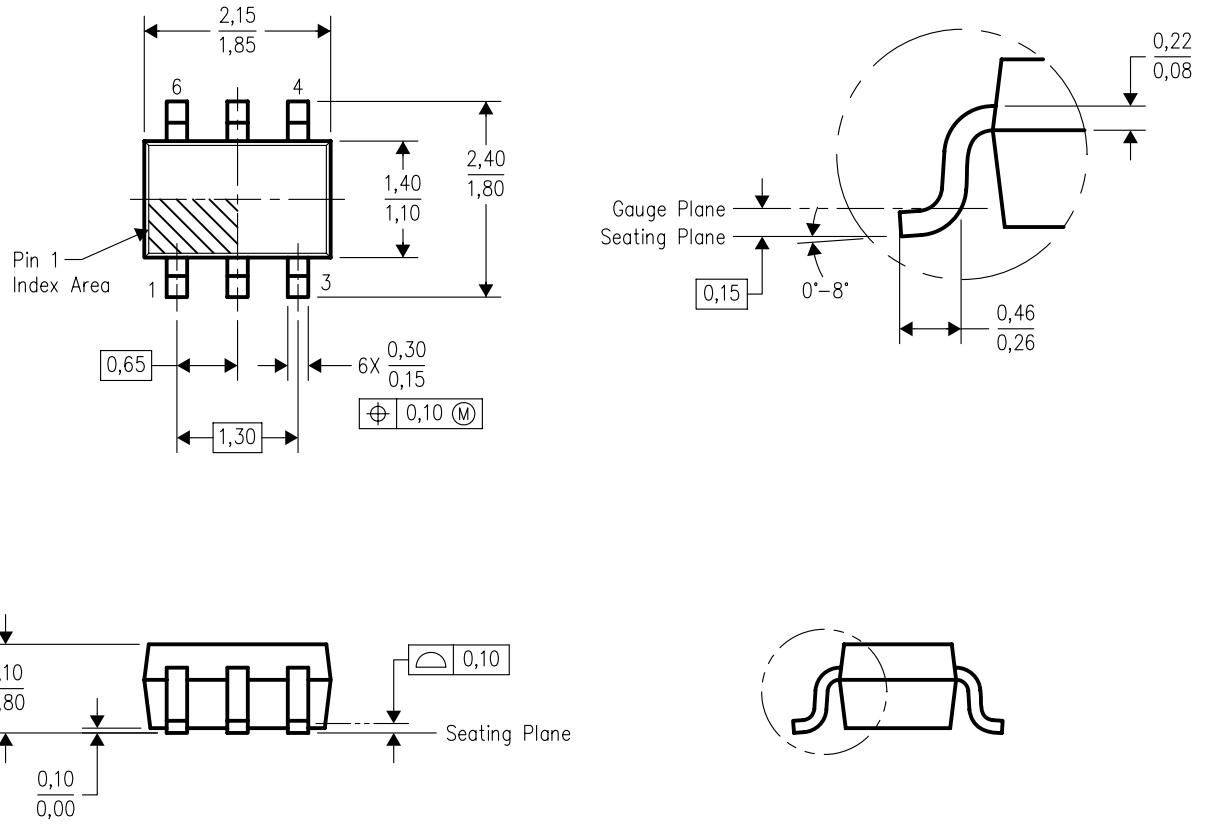
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM66100DCKR	SC70	DCK	6	3000	210.0	185.0	35.0
LM66100DCKT	SC70	DCK	6	250	210.0	185.0	35.0

DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



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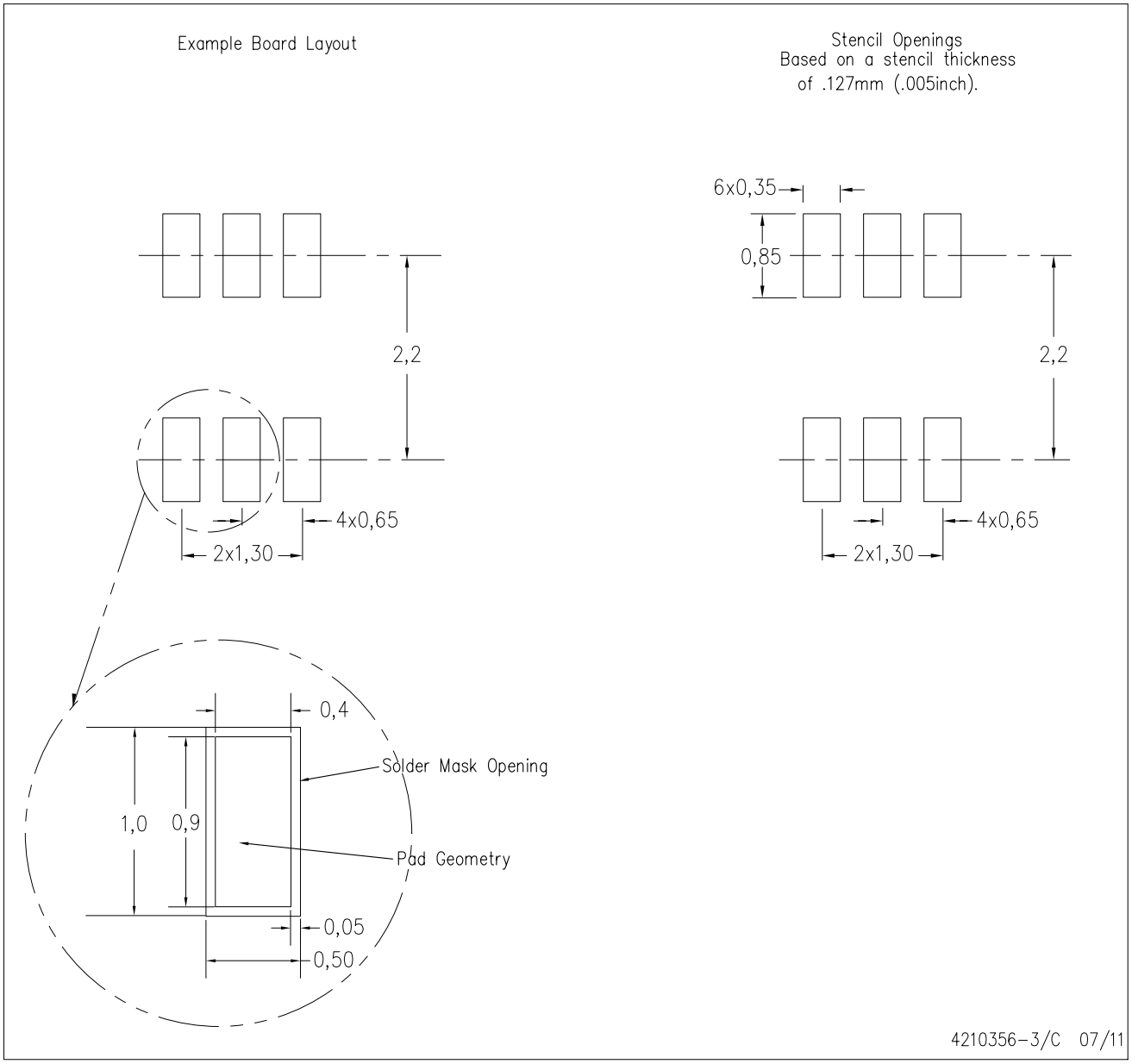
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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