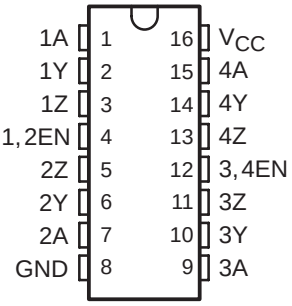
SLLS098C − MAY 1980 − REVISED FEBRUARY 2004

- **Meets or Exceeds Requirements of ANSI TIA/EIA-422-B and ITU Recommendation V.11**
- **3-State, TTL-Compatible Outputs**
- **Fast Transition Times**
- **High-Impedance Inputs**
- **Single 5-V Supply**
- **Power-Up and Power-Down Protection**

D, N, OR NS PACKAGE
(TOP VIEW)



description/ordering information

The MC3487 offers four independent differential line drivers designed to meet the specifications of ANSI TIA/EIA-422-B and ITU Recommendation V.11. Each driver has a TTL-compatible input buffered to reduce current and minimize loading.

The driver outputs utilize 3-state circuitry to provide high-impedance states at any pair of differential outputs when the appropriate output enable is at a low logic level. Internal circuitry is provided to ensure the high-impedance state at the differential outputs during power-up and power-down transition times, provided the output enable is low.

The MC3487 is designed for optimum performance when used with the MC3486 quadruple line receiver. It is supplied in a 16-pin dual-in-line package and operates from a single 5-V supply.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP − N	Tube	MC3487N	MC3487N
	SOIC − D	Tube	MC3487D	MC3487
		Tape and reel	MC3487DR	
	SOP − NS	Tape and reel	MC3487NSR	MC3487

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each driver)

INPUT	OUTPUT ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = TTL high level, L = TTL low level,
X = irrelevant, Z = High impedance

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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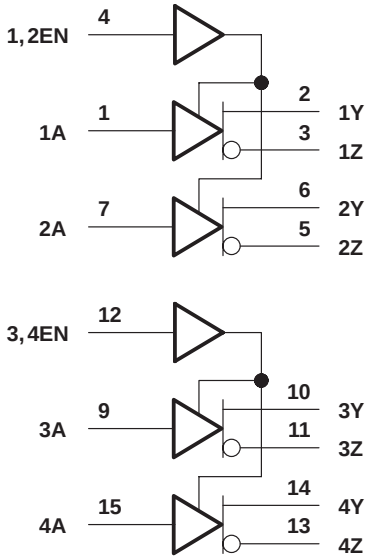
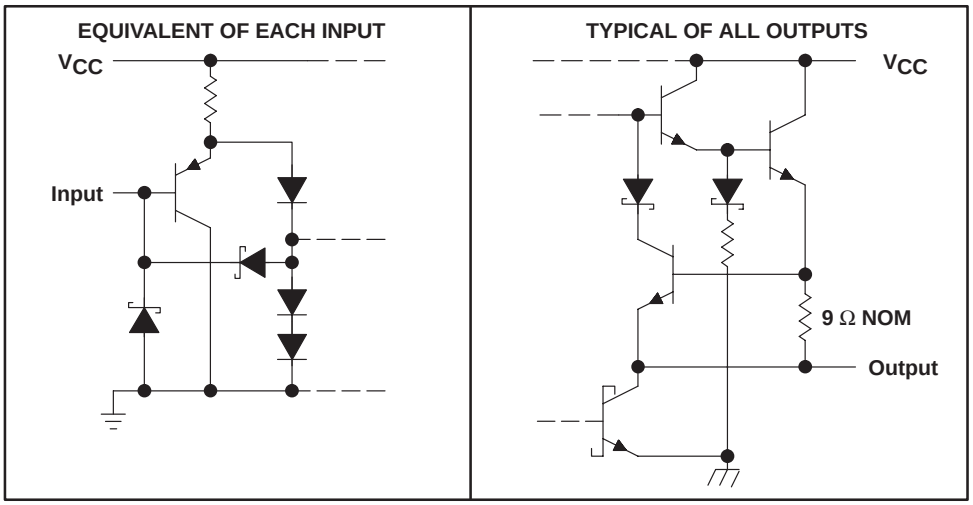
logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 8 V
Input voltage, V_I . . . . . 5.5 V
Output voltage, V_O . . . . . 7 V
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package . . . . . 73°C/W
N package . . . . . 67°C/W
NS package . . . . . 64°C/W
Operating virtual junction temperature, T_J . . . . . 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential output voltage, V_{OD}, are with respect to the network ground terminal.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IL} = 0.8 V,	V_{IH} = 2 V,	I_{OH} = −20 mA	2.5		V
V_{OL}	Low-level output voltage	V_{IL} = 0.8 V,	V_{IH} = 2 V,	I_{OL} = 48 mA		0.5	V
$\|V_{OD}\|$	Differential output voltage	R_L = 100 Ω,	See Figure 1		2		
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage†	R_L = 100 Ω,	See Figure 1			±0.4	V
V_{OC}	Common-mode output voltage‡	R_L = 100 Ω,	See Figure 1			3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage†	R_L = 100 Ω,	See Figure 1			±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V			100	µA
			V_O = −0.25 V			−100	
I_{OZ}	High-impedance-state output current	Output enables at 0.8 V	V_O = 2.7 V			100	µA
			V_O = 0.5 V			−100	
I_I	Input current at maximum input voltage	V_I = 5.5 V				100	µA
I_{IH}	High-level input current	V_I = 2.7 V				50	µA
I_{IL}	Low-level input current	V_I = 0.5 V				−400	µA
I_{OS}	Short-circuit output current§	V_I = 2 V			−40	−140	mA
I_{CC}	Supply current (all drivers)	Outputs disabled				105	mA
		Outputs enabled,	No load			85	

† $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

‡ In ANSI Standard TIA/EIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

§ Only one output at a time should be shorted, and duration of the short circuit should not exceed one second.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 15 pF,	See Figure 2		20	ns
t_{PHL}	Propagation delay time, high- to low-level output				20	
t_{sk}	Skew time	C_L = 15 pF,	See Figure 2		6	ns
$t_{t(OD)}$	Differential-output transition time	C_L = 15 pF,	See Figure 3		20	ns
t_{PZH}	Output enable time to high level	C_L = 50 pF,	See Figure 4		30	ns
t_{PZL}	Output enable time to low level				30	
t_{PHZ}	Output disable time from high level	C_L = 50 pF,	See Figure 4		25	ns
t_{PLZ}	Output disable time from low level				30	

PARAMETER MEASUREMENT INFORMATION

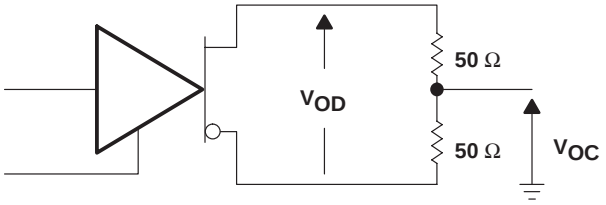
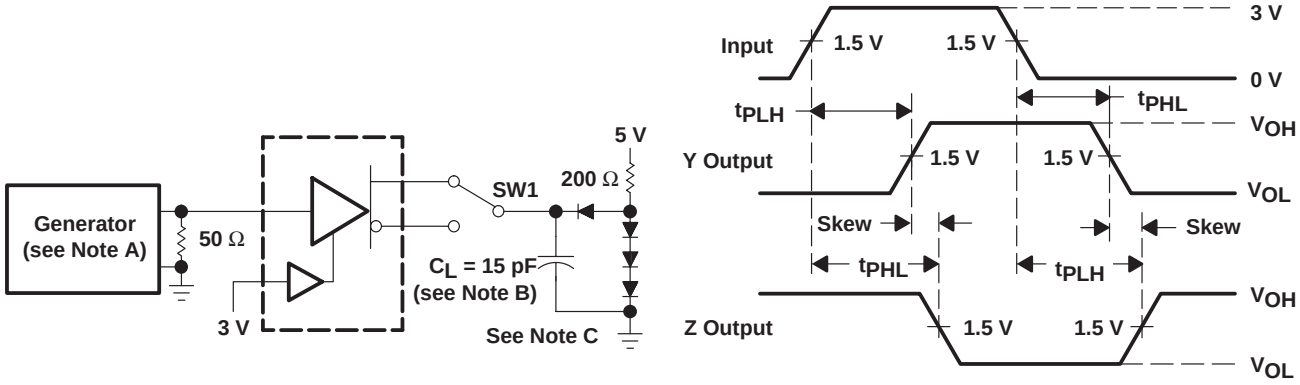
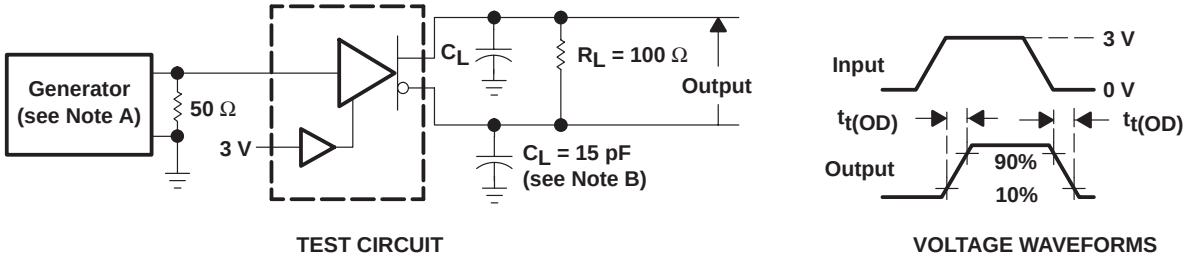


Figure 1. Differential and Common-Mode Output Voltages



NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or 1N3064.

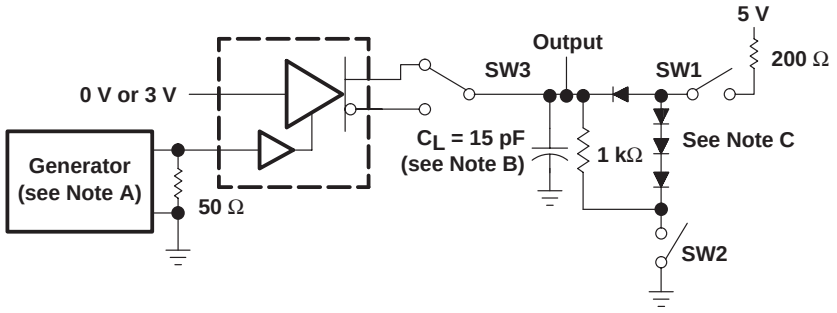
Figure 2. Test Circuit and Voltage Waveforms



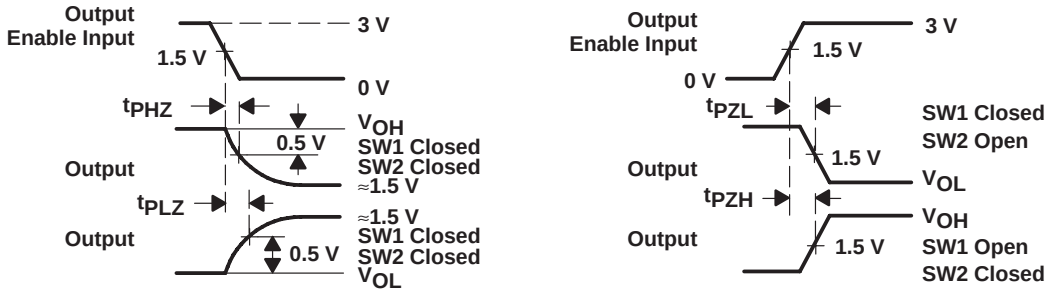
NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.
B. C_L includes probe and stray capacitance.

Figure 3. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or 1N3064.

Figure 4. Driver Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MC3487D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MC3487	Samples
MC3487DE4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MC3487	Samples
MC3487DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MC3487	Samples
MC3487DRE4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MC3487	Samples
MC3487N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	MC3487N	Samples
MC3487NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	MC3487N	Samples
MC3487NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MC3487	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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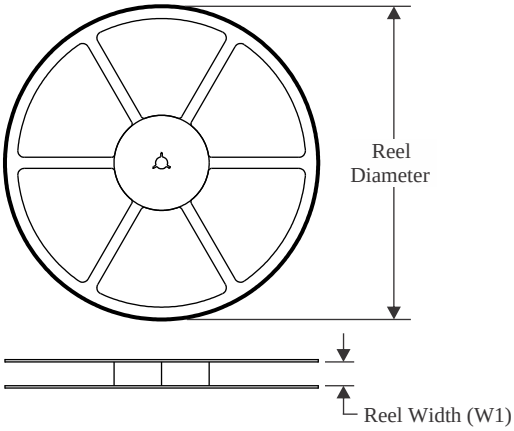
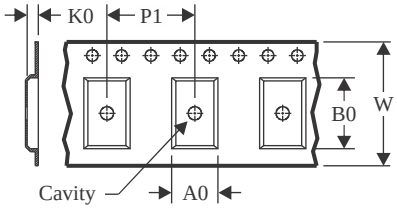
TAPE AND REEL INFORMATION

REEL DIMENSIONS

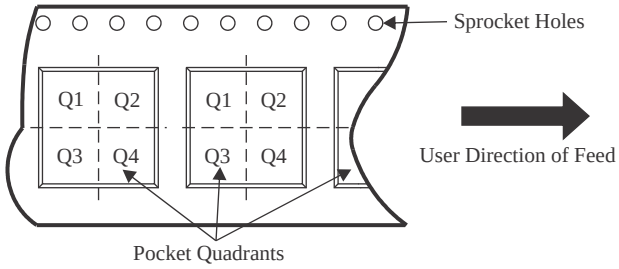


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

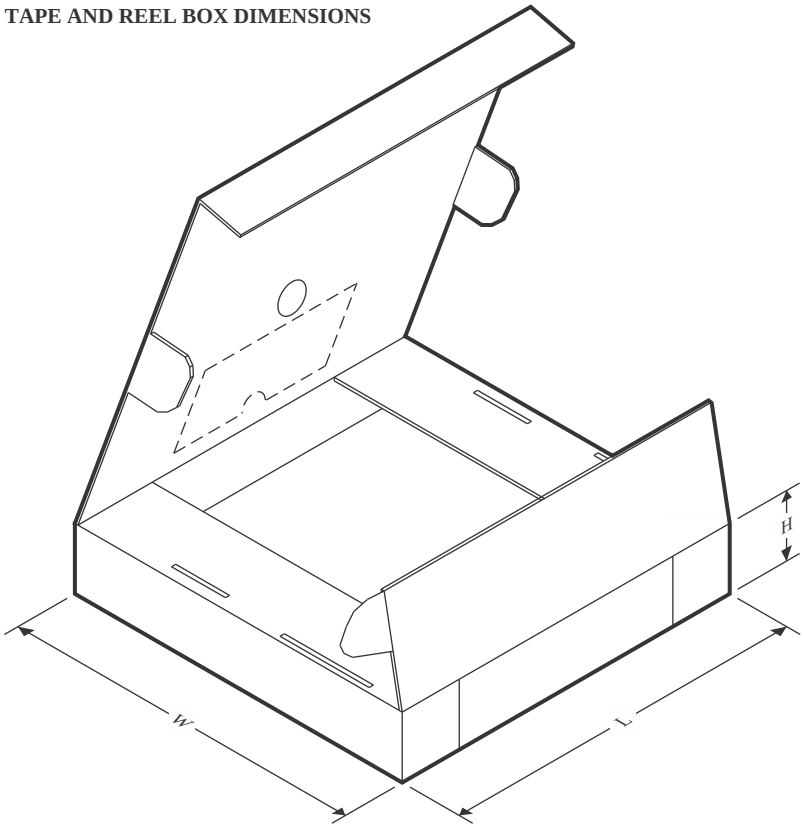
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MC3487DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MC3487DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
MC3487NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

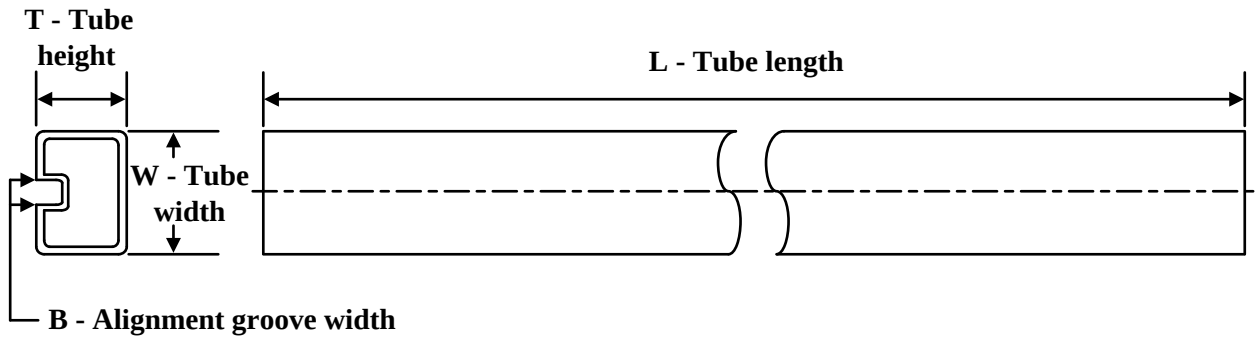
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

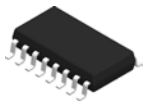
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MC3487DR	SOIC	D	16	2500	356.0	356.0	35.0
MC3487DR	SOIC	D	16	2500	340.5	336.1	32.0
MC3487NSR	SO	NS	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MC3487D	D	SOIC	16	40	506.6	8	3940	4.32
MC3487D	D	SOIC	16	40	507	8	3940	4.32
MC3487DE4	D	SOIC	16	40	506.6	8	3940	4.32
MC3487DE4	D	SOIC	16	40	507	8	3940	4.32
MC3487N	N	PDIP	16	25	506	13.97	11230	4.32
MC3487N	N	PDIP	16	25	506	13.97	11230	4.32
MC3487NE4	N	PDIP	16	25	506	13.97	11230	4.32
MC3487NE4	N	PDIP	16	25	506	13.97	11230	4.32

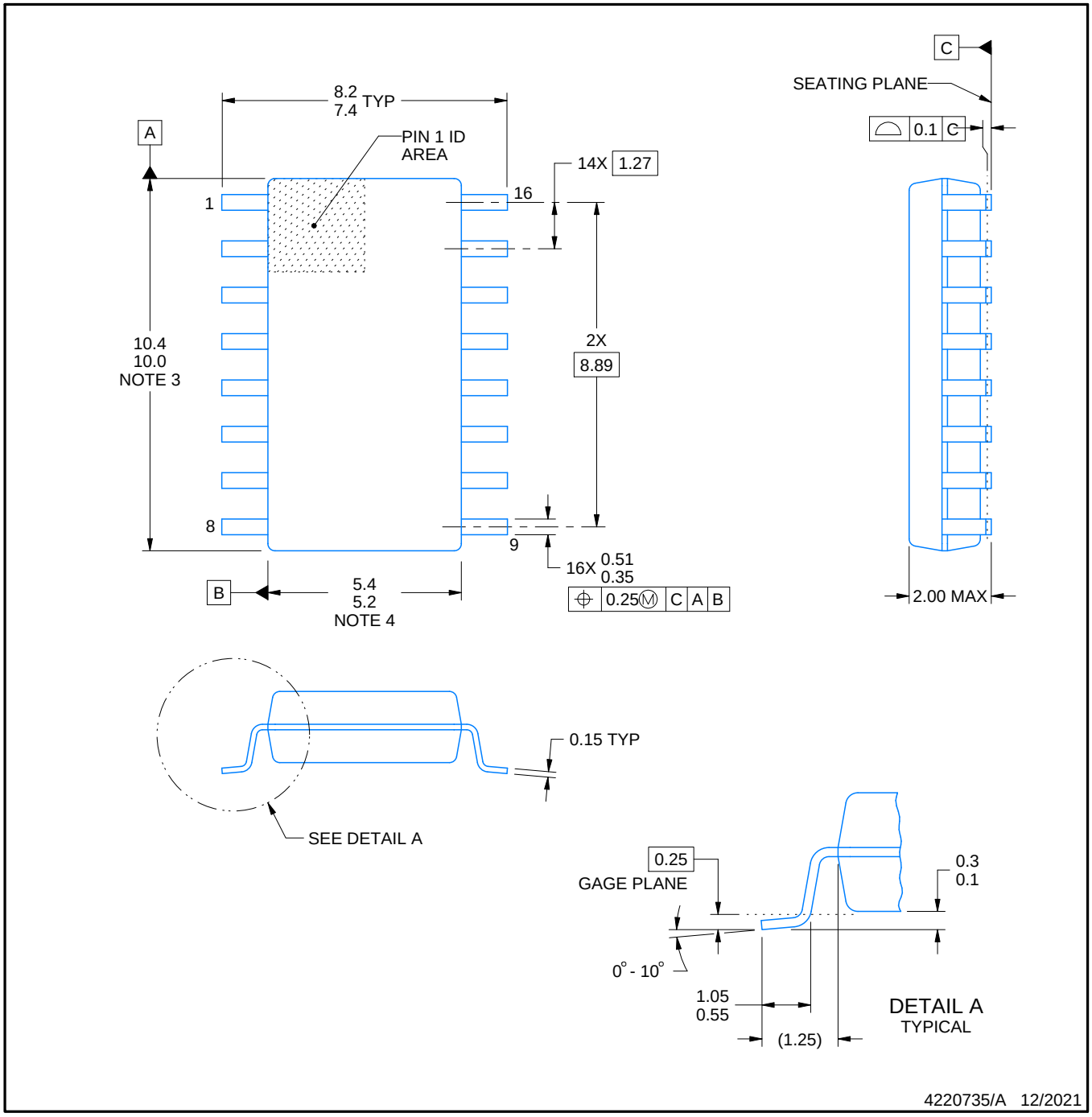


PACKAGE OUTLINE

NS0016A

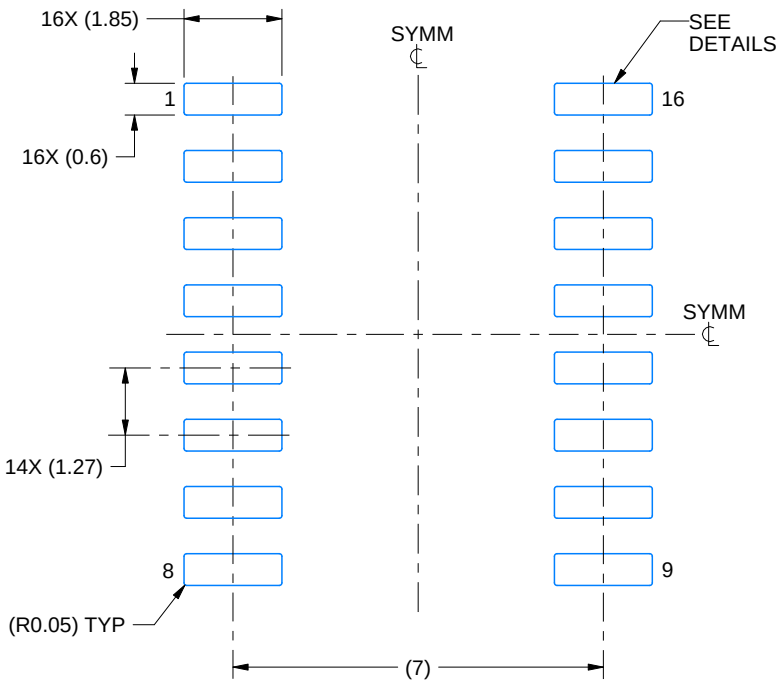
SOP - 2.00 mm max height

SOP

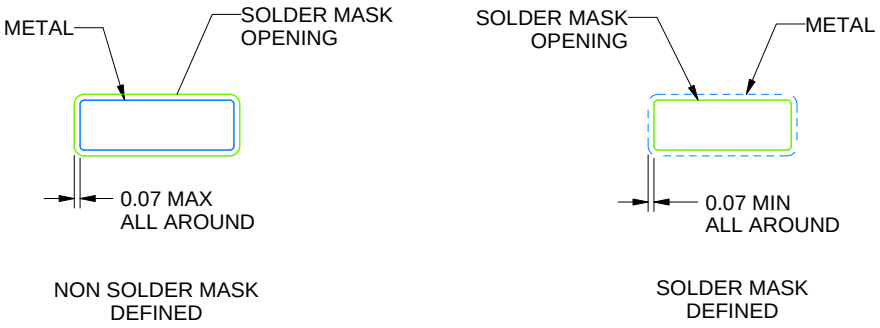


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

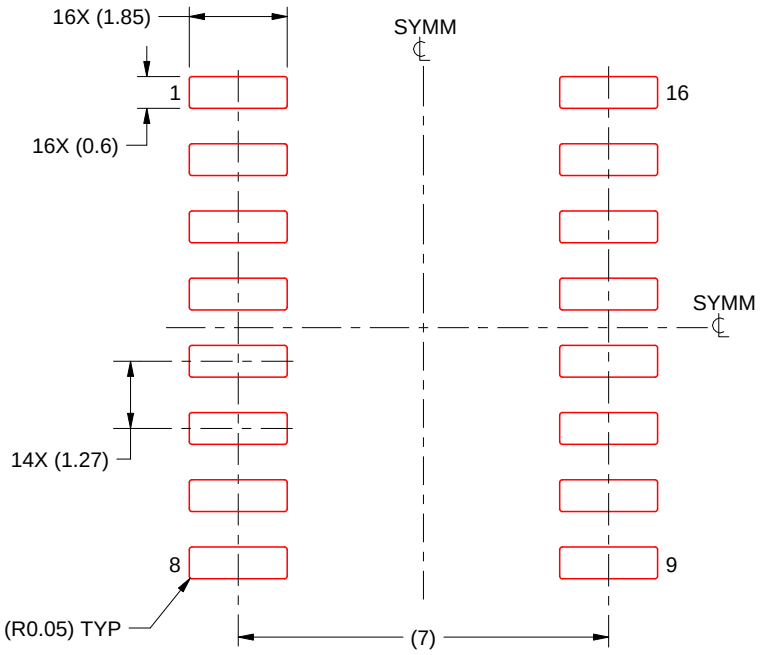
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



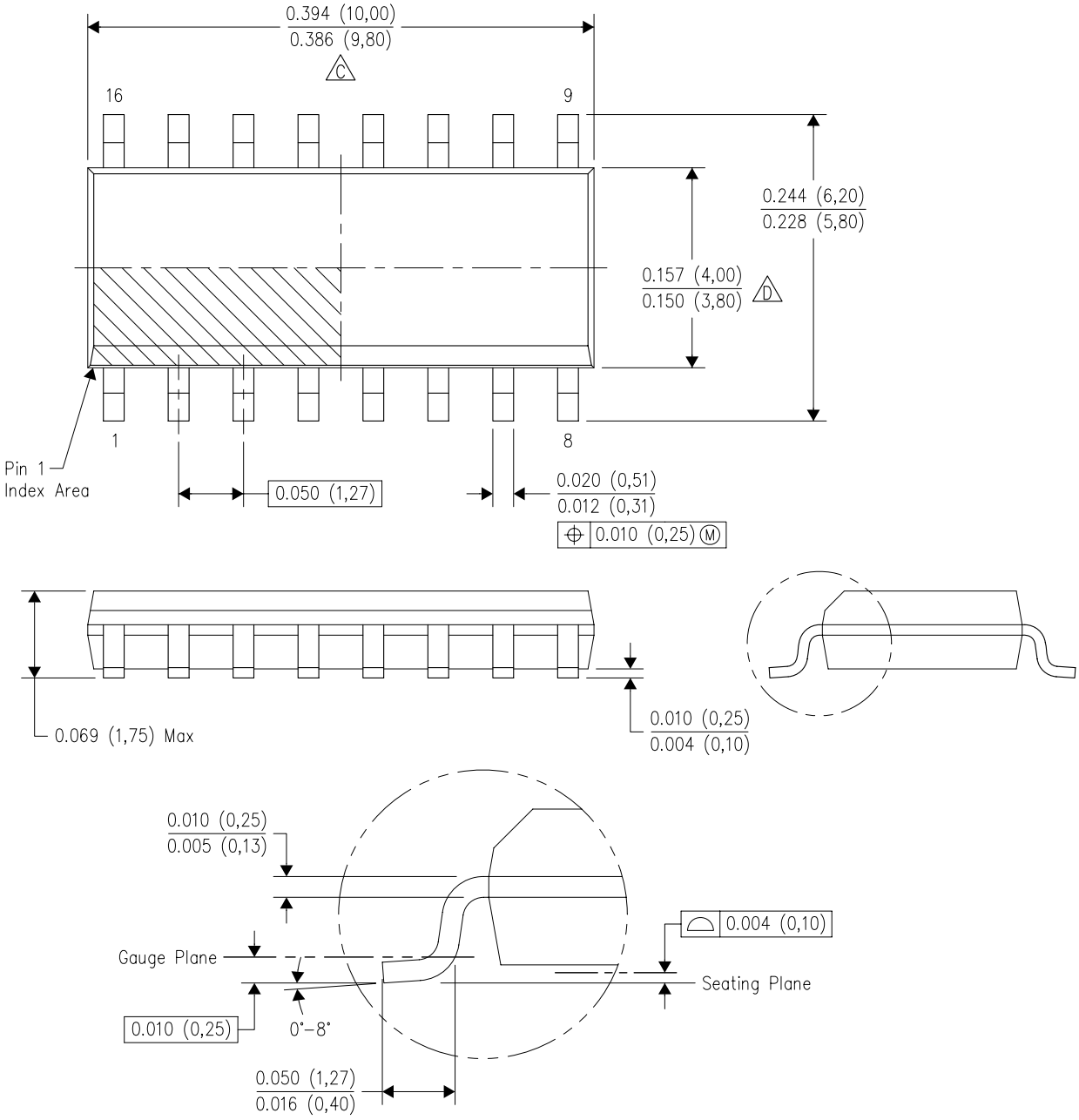
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

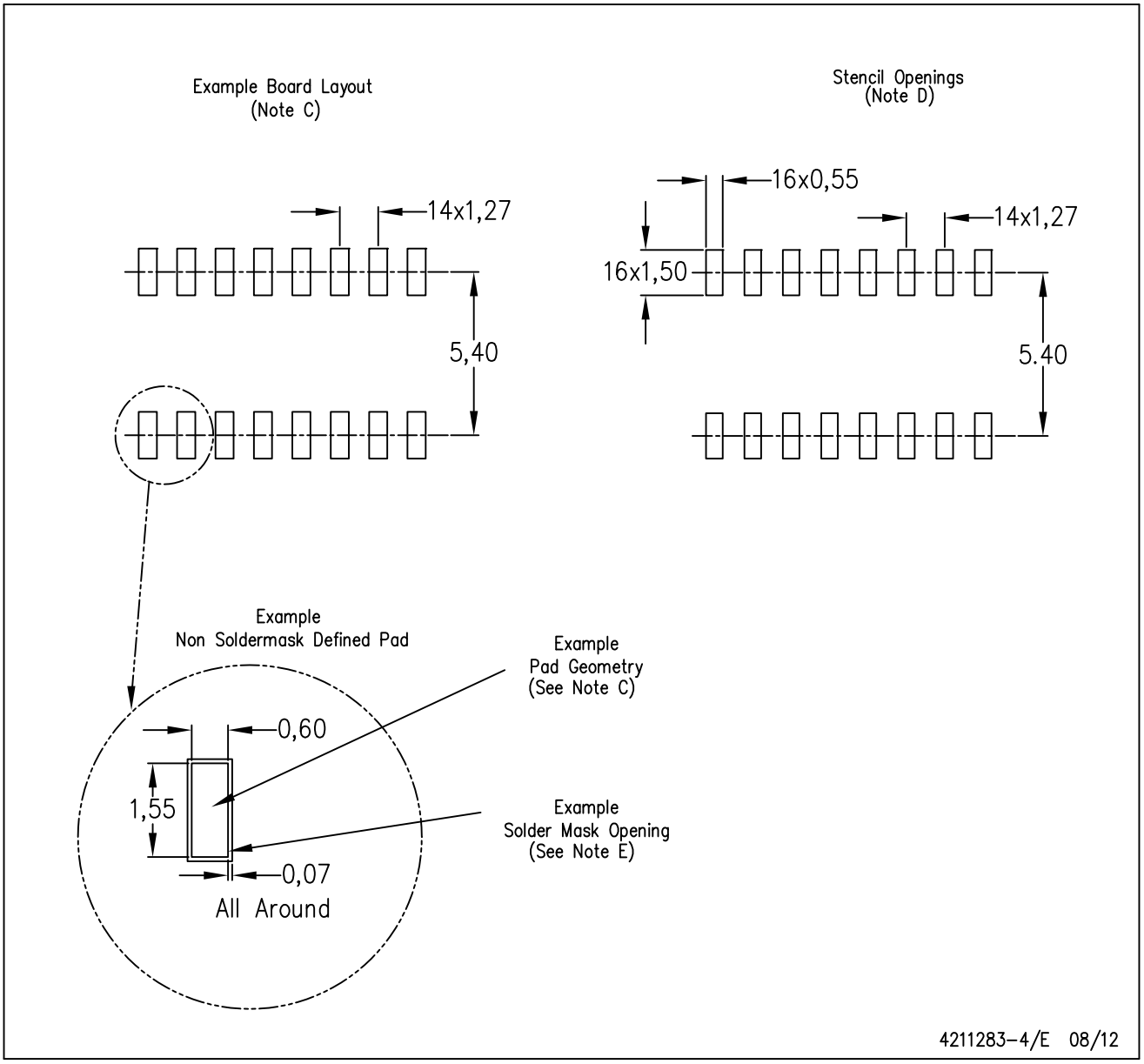
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

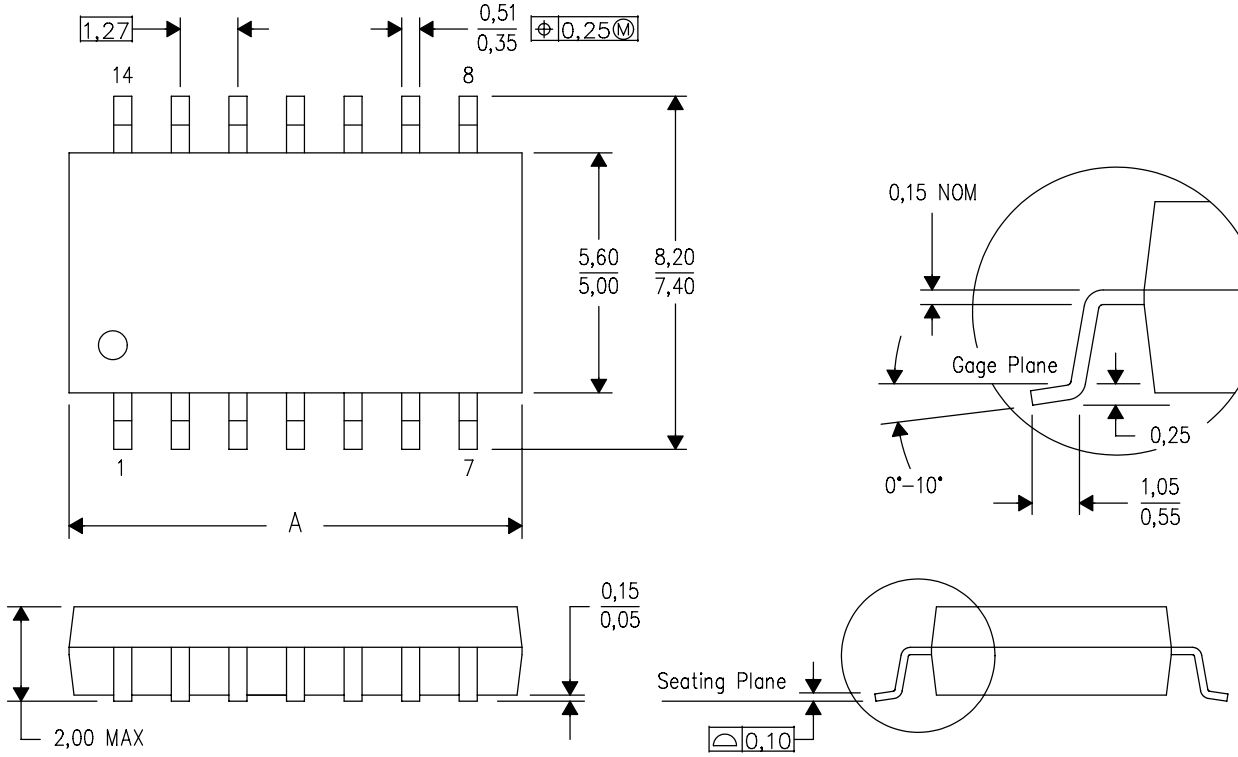


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

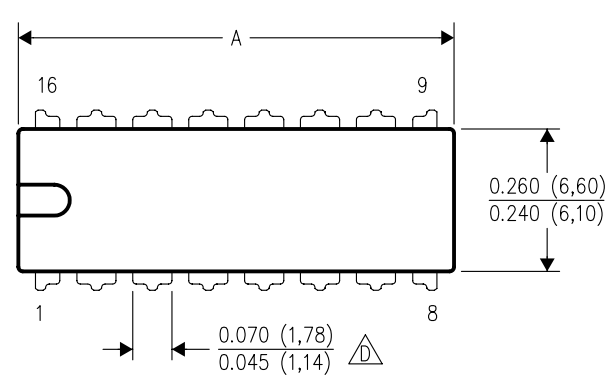
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

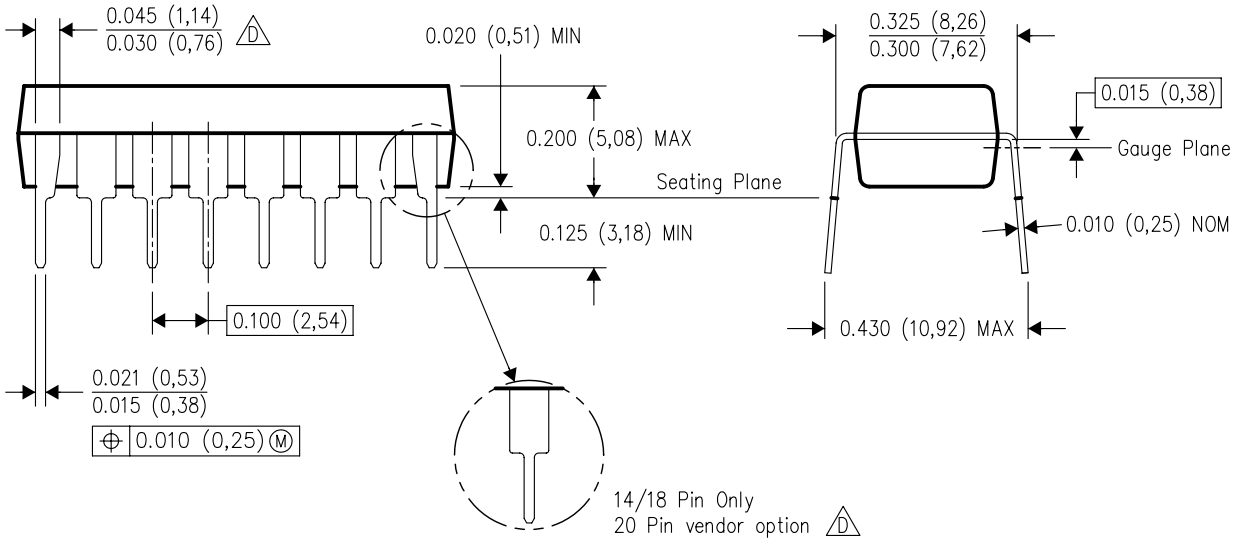
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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