SN74LV573A 具有三态输出的八路透明 D 类锁存器

1 特性

- V_{CC} 工作范围为 2V 至 5.5V
- 电压为 5V 时，t_{pd} 最大值为 8ns
- V_{CC} = 3.3V、T_A = 25°C 时，V_{OLP}（输出接地反弹）典型值小于 0.8V，闩锁性能超过 250mA
- V_{CC} = 3.3V、T_A = 25°C 时，V_{OHV}（输出 V_{OH} 下冲）典型值大于 2.3V
- 所有端口上均支持混合模式电压运行
- I_{off} 支持局部断电模式运行
- 闩锁性能超过 250mA，符合 JESD 17 规范

2 应用

- 缓冲寄存器
- 双向总线驱动器
- 工作寄存器

连接至其他七个通道

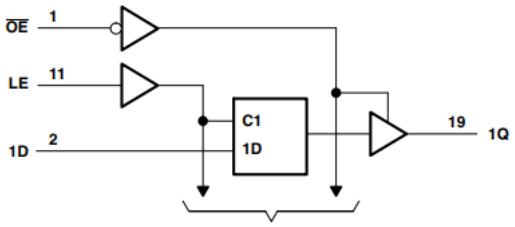
3 说明

'LV573A 器件为八路透明 D 类锁存器，可在 2V 至 5.5V V_{CC} 下运行。

封装信息(1)

器件型号	封装	封装尺寸（标称值）
SN74LV573A	NS（SO，20）	12.6 mm × 5.3 mm
	DW（SOIC，20）	12.8mm × 7.5mm
	DB（SSOP，20）	7.2 mm × 5.3 mm
	PW（TSSOP，20）	6.5mm × 4.4mm
	DGV（TVSOP，20）	5mm × 4.4mm
	RGY（VQFN，20）	4.5mm × 3.5mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



逻辑图（正逻辑）

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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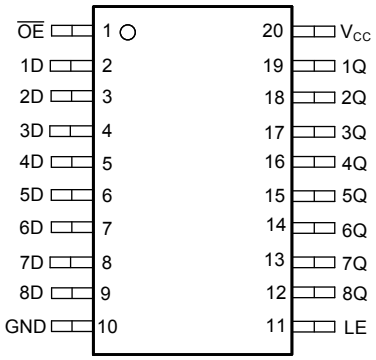
4 Revision History

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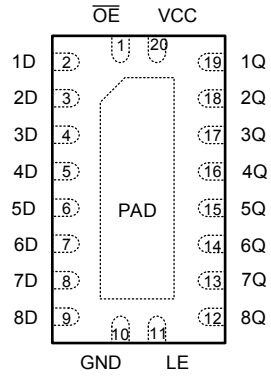
Changes from Revision I (April 2005) to Revision J (March 2023)	Page
• 添加了*应用*、*封装信息* 表、*引脚功能* 表、*ESD 等级* 表、*热性能信息* 表、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分	1
• Updated thermal values for PW package from R θ JA = 131.8 to 128.2, all values in °C/W	5

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5 Pin Configuration and Functions



DB, DGV, DW, NS, or PW Packages Top View



RGY Package Top View

表 5-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NO.	NAME		
1	$\overline{OE}$	I	Output enable
2	1D	I	1D input
3	2D	I	2D input
4	3D	I	3D input
5	4D	I	4D input
6	5D	I	5D input
7	6D	I	6D input
8	7D	I	7D input
9	8D	I	8D input
10	GND	—	Ground
11	LE	I	Latch enable input
12	8Q	O	8Q output
13	7Q	O	7Q output
14	6Q	O	6Q output
15	5Q	O	5Q output
16	4Q	O	4Q output
17	3Q	O	3Q output
18	2Q	O	2Q output
19	1Q	O	1Q output
20	V_{CC}	—	Power pin

1. I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		– 0.5	7	V
V_I	Input voltage(1)		– 0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(1)		– 0.5	7	V
V_O	Output voltage range applied in the high or low state(1) (2)		– 0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current(2)	V_I < 0		±20	mA
I_{OK}	Output clamp current(2)	V_O < 0		−50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_{stg}	Storage temperature		– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (A114-A)(1)	±2000	V
		Charged-Device Model (C101)(2)	±1000	
		Machine Model (A115-A)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 2 V		− 50	ns
		V_{CC} = 2.3 V to 2.7 V		− 2	
		V_{CC} = 3 V to 3.6 V		− 8	
		V_{CC} = 4.5 V to 5.5 V		− 16	

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over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
I_{OL}	Low-level output current	V_{CC} = 2 V		50	ns
		V_{CC} = 2.3 V to 2.7 V		2	
		V_{CC} = 3 V to 3.6 V		8	
		V_{CC} = 4.5 V to 5.5 V		16	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200	ns
		V_{CC} = 3 V to 3.6 V		100	
		V_{CC} = 4.5 V to 5.5 V		20	
T_A	Operating free-air temperature		−40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the *Implications of Slow or Floating CMOS Inputs* application report (SCBA004).

6.4 Thermal Information

THERMAL METRIC		SN74LV573A						UNIT
		DGV (TVSOP)	DW (SOIC)	DB (SSOP)	NS (SO)	PW (TSSOP)	RGY (VQFN)	
		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	92	109.1	122.7	84.6	128.2	37	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = −50 μA	2 V to 5.5 V	V_{CC} −0.1			V
	I_{OH} = −2 mA	2.3 V	2			
	I_{OH} = −8 mA	3 V	2.48			
	I_{OH} = −16 mA	4.5 V	3.8			
V_{OL}	I_{OL} = 50 μA	2 V to 5.5 V			0.1	V
	I_{OL} = 2 mA	2.3 V			0.4	
	I_{OL} = 8 mA	3 V			0.44	
	I_{OL} = 16 mA	4.5 V			0.55	
I_I	V_I = 5.5 V or GND	0 to 5.5 V			± 1	μA
I_{OZ}	V_O = V_{CC}or GND	5.5 V			±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			20	μA
I_{off}	V_I or V_O = 0 to 5.5 V	0			5	μA
C_i	V_I = V_{CC} or GND	3.3 V		1.8		pF

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6.6 Timing Requirements, V_{CC} = 2.5 V ± 0.2 V

over operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration	LE high	5		5		ns
t_{su}	Setup time	Data before LE ↓	3.5		3.5		ns
t_h	Hold time	Data after LE ↓	1.5		1.5		ns

6.7 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

over operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration	LE high	5		5		ns
t_{su}	Setup time	Data before LE ↓	3.5		3.5		ns
t_h	Hold time	Data after LE ↓	1.5		1.5		ns

6.8 Timing Requirements, V_{CC} =5 V ± 0.5 V

over operating free-air temperature range, V_{CC} = 5 V ± 0.5 V(unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration	LE high	5		5		ns
t_{su}	Setup time	Data before LE ↓	3.5		3.5		ns
t_h	Hold time	Data after LE ↓	1.5		1.5		ns

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6.9 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted; see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN74LV573A		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	D	Q	C_L = 15 pF		8.9[1]	15.8[1]	1	18	ns
t_{pd}	LE	Q			9.6[1]	16.2[1]	1	19	
t_{en}	$\overline{OE}$	Q			9.3[1]	16.2[1]	1	19	
t_{dis}	$\overline{OE}$	Q			6.7[1]	12.6[1]	1	15	
t_{pd}	D	Q	C_L = 50 pF		10.9	18.7	1	21	ns
t_{pd}	LE	Q			11.6	19.1	1	23	
t_{en}	$\overline{OE}$	Q			11.4	19	1	22	
t_{dis}	$\overline{OE}$	Q			8.6	17.3	1	19	
$t_{sk(o)}$						2		2	

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.10 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted; see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN74LV573A		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	D	Q	C_L = 15 pF		6.2[1]	11[1]	1	13	ns
t_{pd}	LE	Q			6.8[1]	11.9[1]	1	14	
t_{en}	$\overline{OE}$	Q			6.6[1]	11.5[1]	1	13.5	
t_{dis}	$\overline{OE}$	Q			4.9[1]	11[1]	1	13	
t_{pd}	D	Q	C_L = 50 pF		7.7	14.5	1	16.5	ns
t_{pd}	LE	Q			8.2	15.4	1	17.5	
t_{en}	$\overline{OE}$	Q			8	15	1	17	
t_{dis}	$\overline{OE}$	Q			6.2	14.5	1	16.5	
$t_{sk(o)}$						1.5		1.5	

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

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6.11 Switching Characteristics, 5 V ± 0.5 V

over operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted; see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN74LV573A		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	D	Q	C_L = 15 pF		4.3[1]	6.8[1]	1	8	ns
t_{pd}	LE	Q			4.7[1]	7.7[1]	1	9	
t_{en}	$\overline{OE}$	Q			4.7[1]	7.7[1]	1	9	
t_{dis}	$\overline{OE}$	Q			3.5[1]	7.7[1]	1	9	
t_{pd}	D	Q	C_L = 50 pF		5.3	8.8	1	10	ns
t_{pd}	LE	Q			5.7	9.7	1	11	
t_{en}	$\overline{OE}$	Q			5.7	9.7	1	11	
t_{dis}	$\overline{OE}$	Q			4.2	9.7	1	11	
$t_{sk(o)}$						1		1	

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.12 Noise Characteristics

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C

PARAMETER		SN74LV573A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.6	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.5	−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

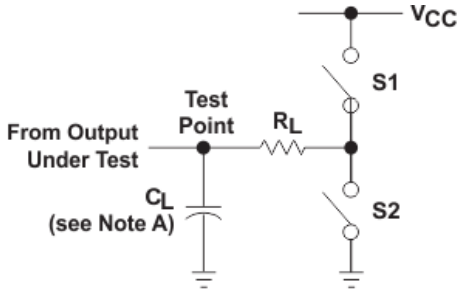
6.13 Operating Characteristics

T_A = 25°C

PARAMETER				TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	D to Q	C_L = 50 pF, f = 10 MHz	3.3 V	16	pF
					5 V	18	
					3.3 V	18.2	
			LE to Q		5 V	21.3	

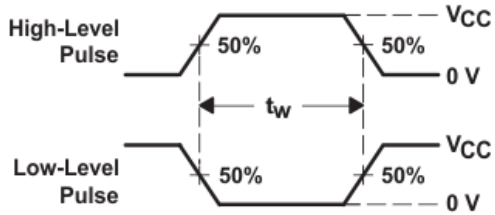
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7 Parameter Measurement Information

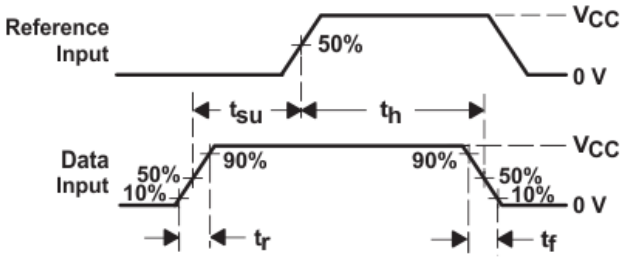


LOAD CIRCUIT

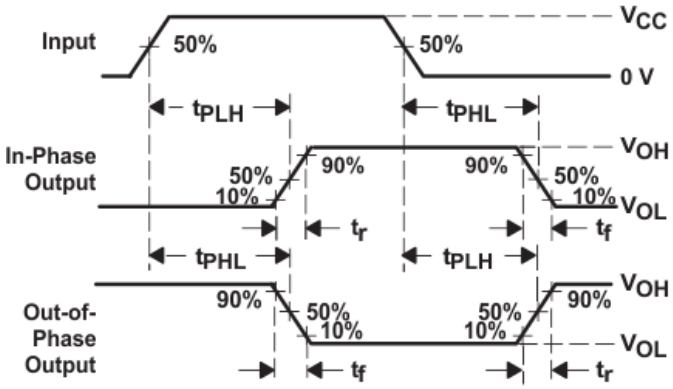
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		--	50 pF or 150 pF	Open	Open



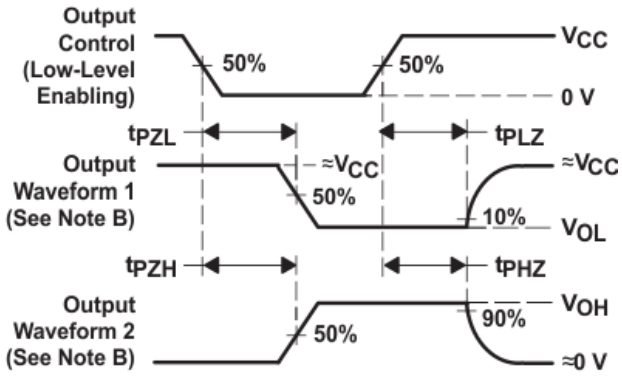
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

图 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The 'LV573A devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

8.2 Functional Block Diagram

To seven other channels

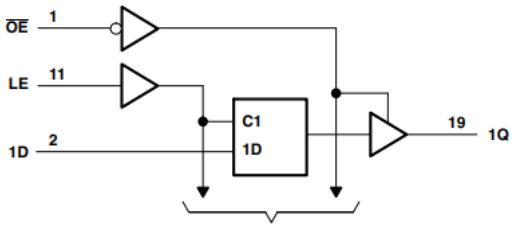


图 8-1. Logic Diagram (Positive Logic)

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8.3 Device Functional Modes

表 8-1 lists the functional modes of the SN74LV573A.

表 8-1. Function Table (Each Latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

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9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the 节 6.3 table. The total current through Ground or V_{CC} must not exceed ±70 mA as per 节 6.1 table.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1-µF capacitor; if there are multiple V_{CC} pins, then TI recommends 0.01-µF or 0.022-µF capacitor for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1-µF and 1-µF capacitor are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

9.2 Layout

9.2.1 Layout Guidelines

When using multiple-bit logic devices, inputs must never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input and the gate are used, or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Layout Diagram specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, they are tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted. This does not disable the input section of the I/Os, so they cannot float when disabled.

9.2.1.1 Layout Example

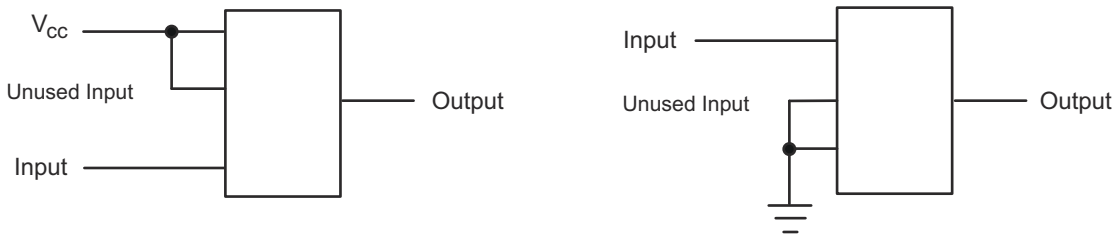


图 9-1. Layout Diagram

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10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 10-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV573A	Click here	Click here	Click here	Click here	Click here

10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

Trademarks

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10.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV573ADBR	NRND	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A
SN74LV573ADBR.A	NRND	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A
SN74LV573ADBRG4	NRND	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A
SN74LV573ADGVR	NRND	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A
SN74LV573ADGVR.A	NRND	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A
SN74LV573ADW	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	-40 to 85	LV573A
SN74LV573ADWR	Last Time Buy	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A
SN74LV573ADWR.A	Last Time Buy	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A
SN74LV573ANSR	NRND	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV573A
SN74LV573ANSR.A	NRND	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV573A
SN74LV573APW	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	-40 to 85	LV573A
SN74LV573APWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A
SN74LV573APWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A
SN74LV573APWRG4	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV573A
SN74LV573ARGYR	NRND	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LV573A
SN74LV573ARGYR.A	NRND	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LV573A
SN74LV573ARGYRG4	NRND	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LV573A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

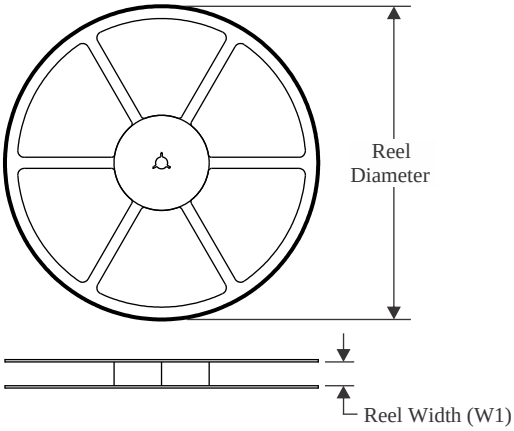
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

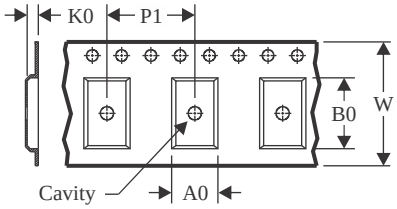
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

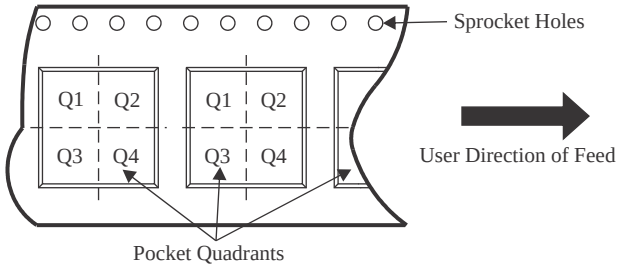


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

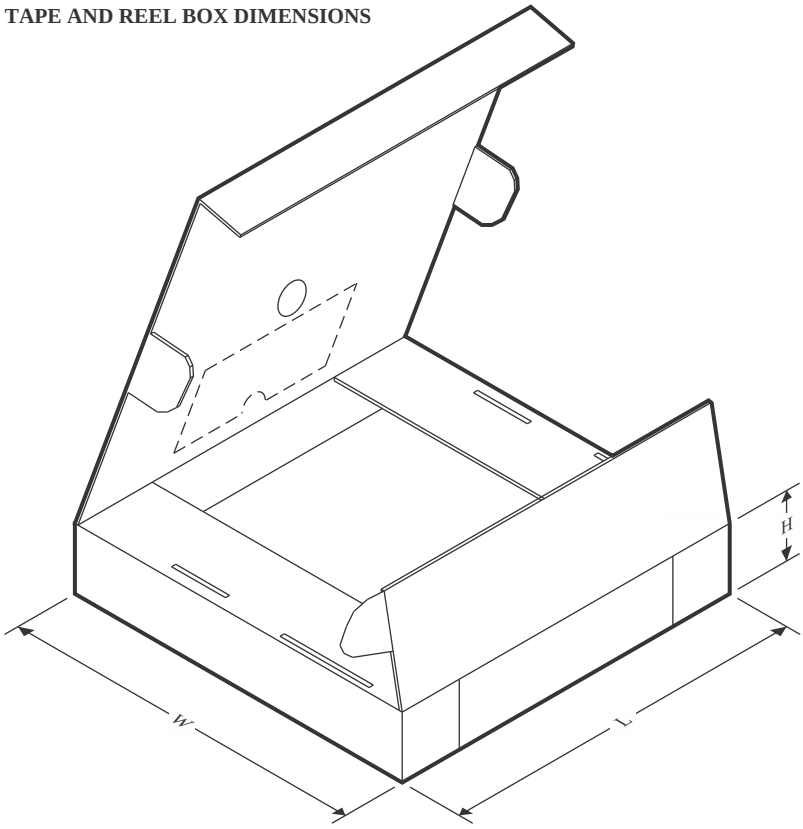
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV573ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LV573ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV573ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LV573ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LV573APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV573ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

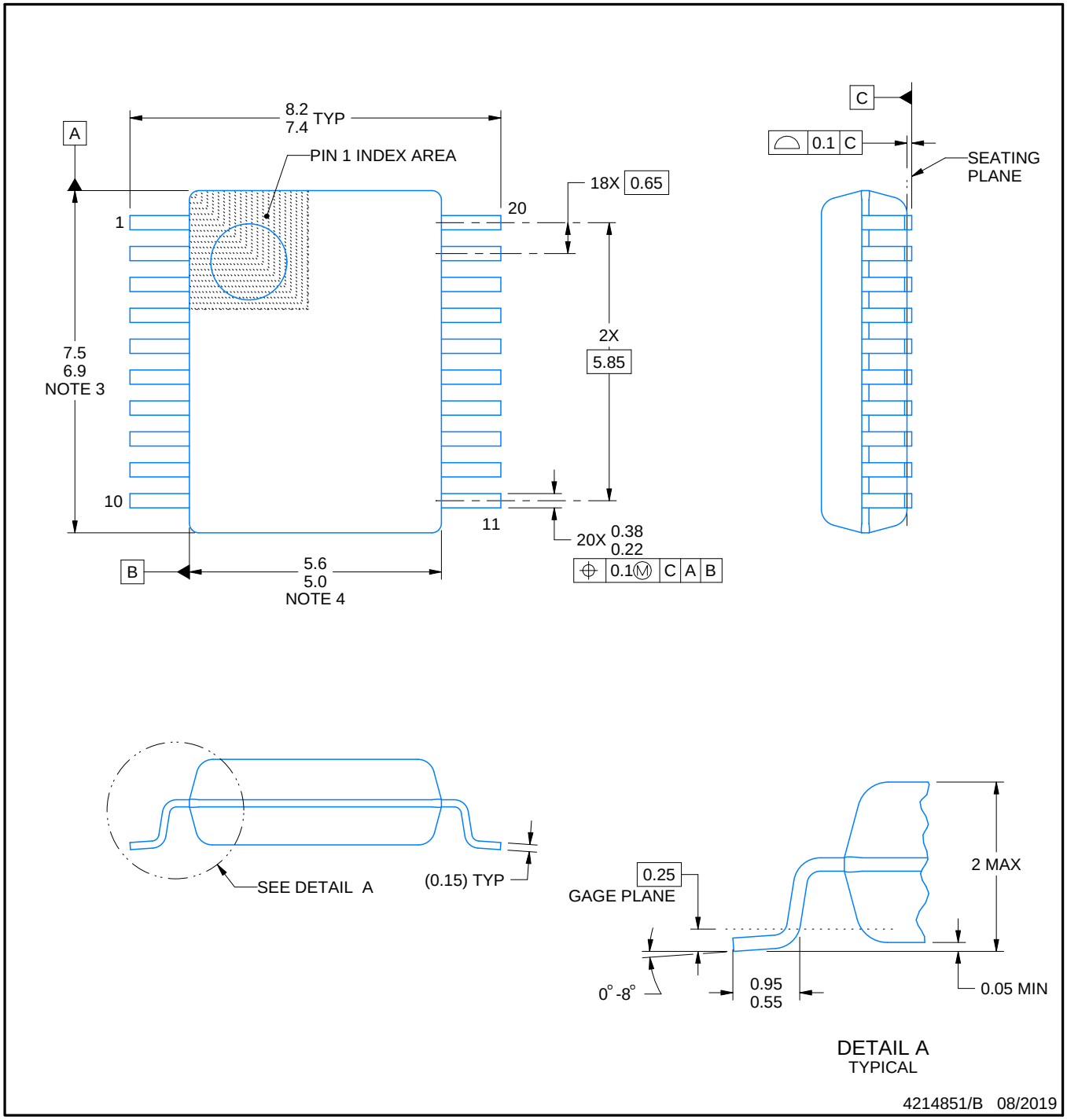
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV573ADBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74LV573ADGVR	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74LV573ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LV573ANSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74LV573APWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LV573ARGYR	VQFN	RGY	20	3000	353.0	353.0	32.0

PACKAGE OUTLINE

DB0020A

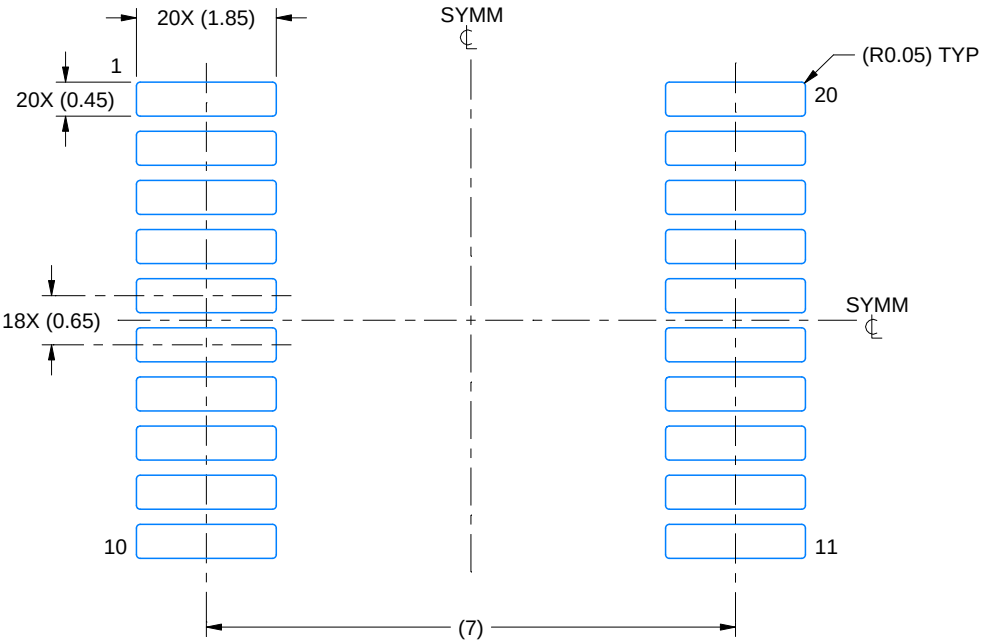
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

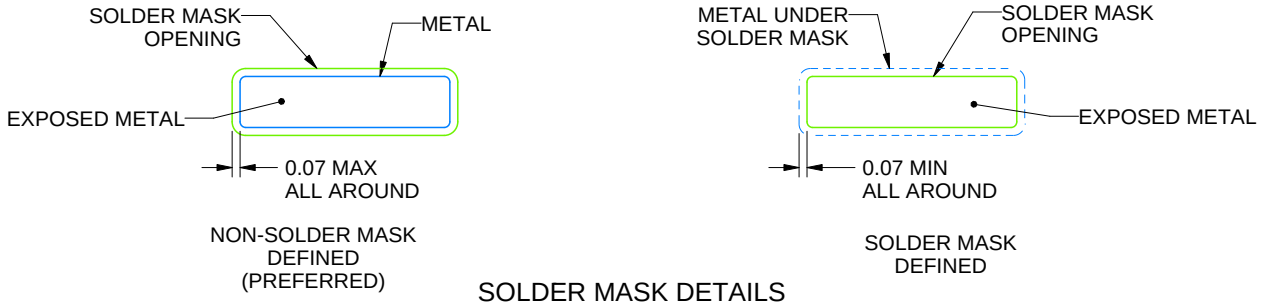


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

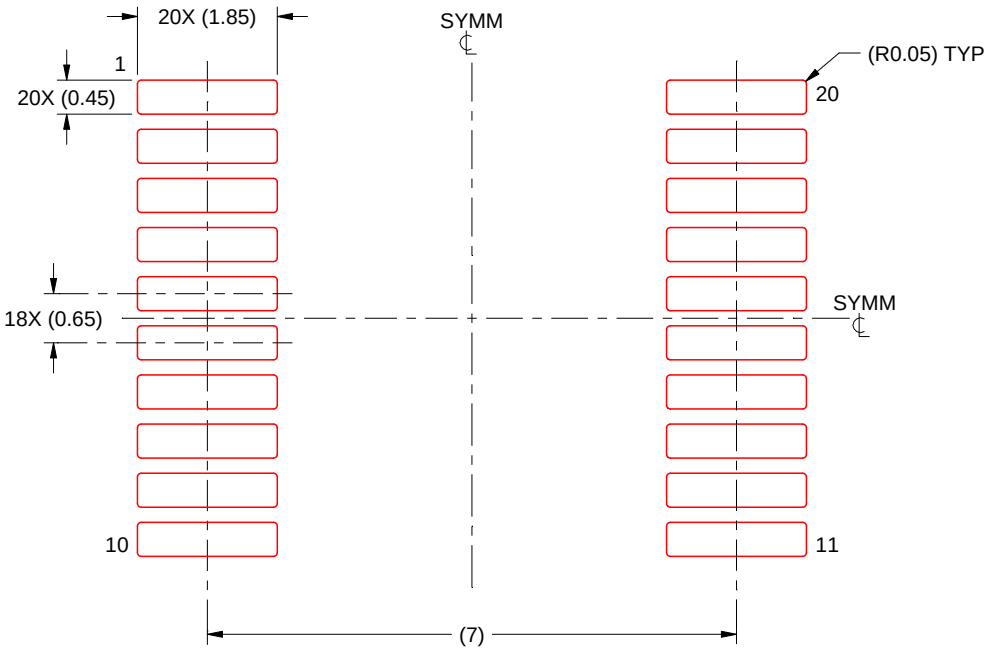
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

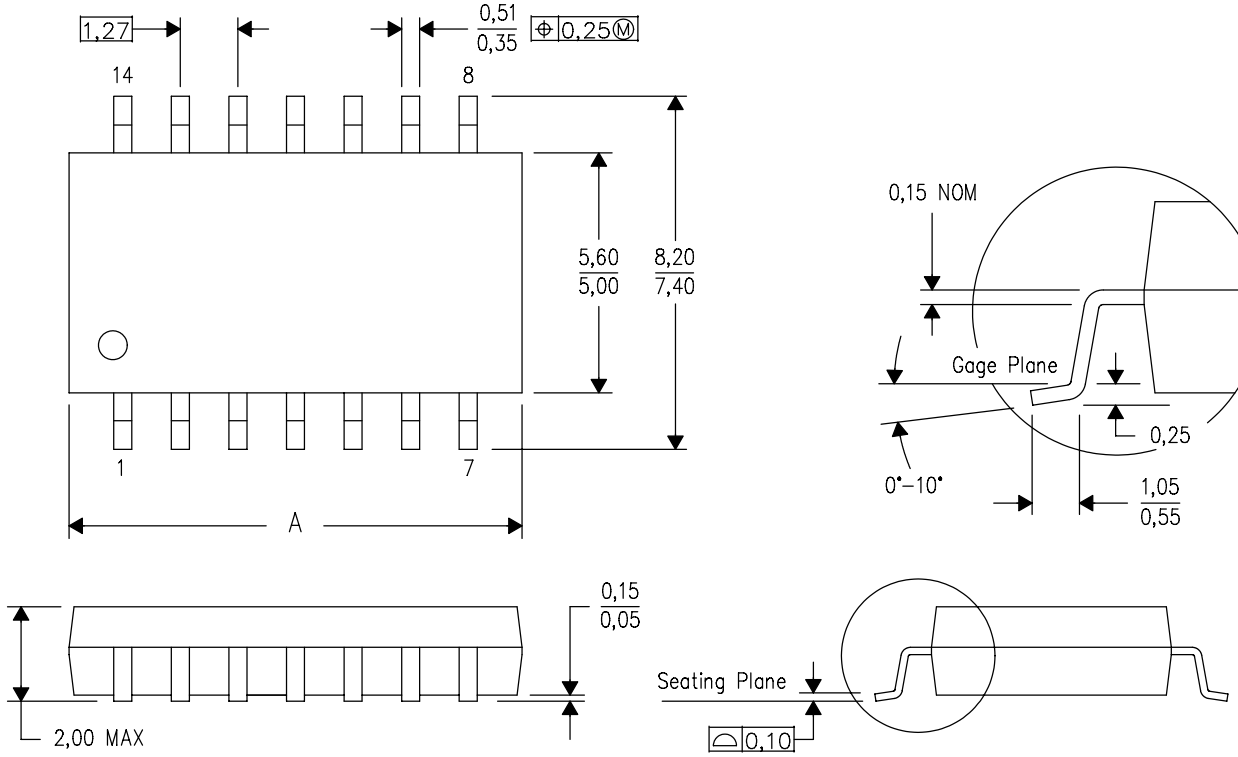
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



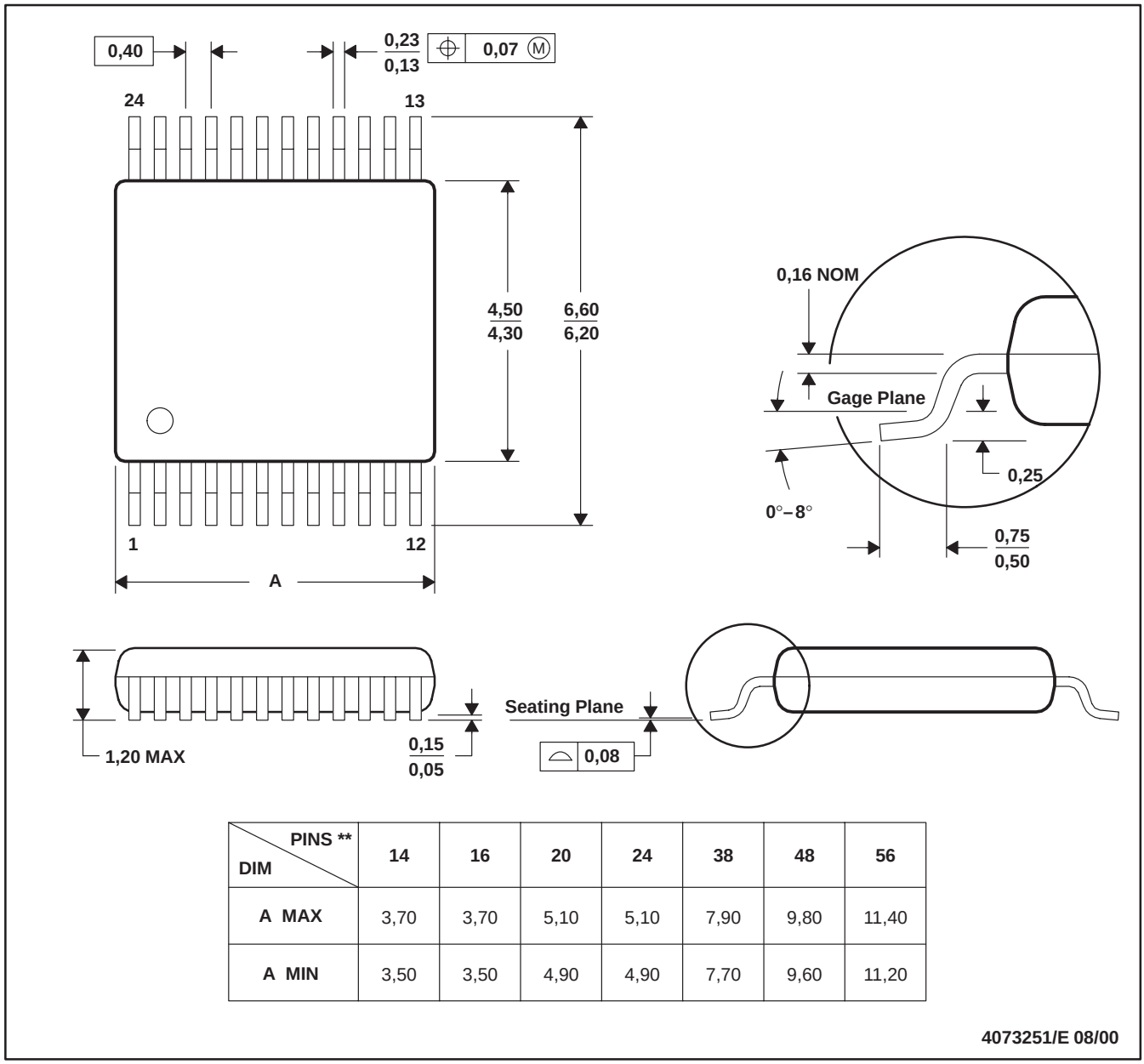
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

GENERIC PACKAGE VIEW

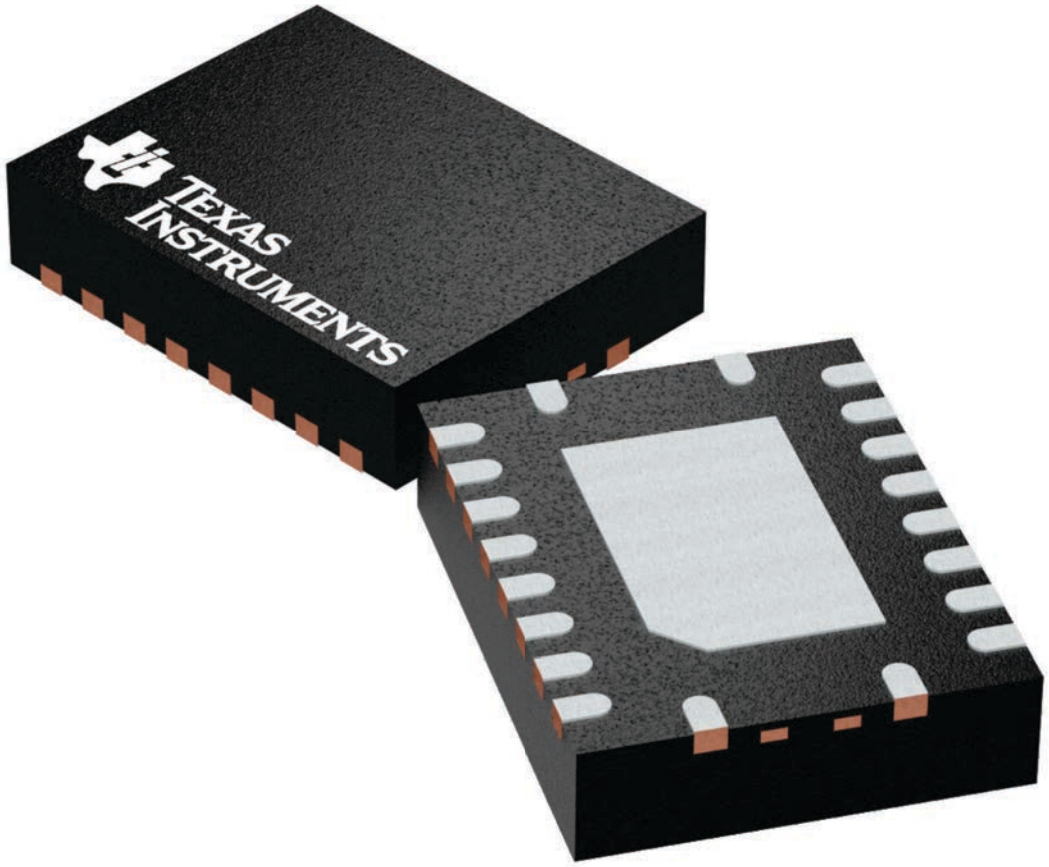
RGY 20

VQFN - 1 mm max height

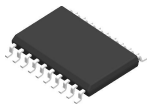
3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225264/A

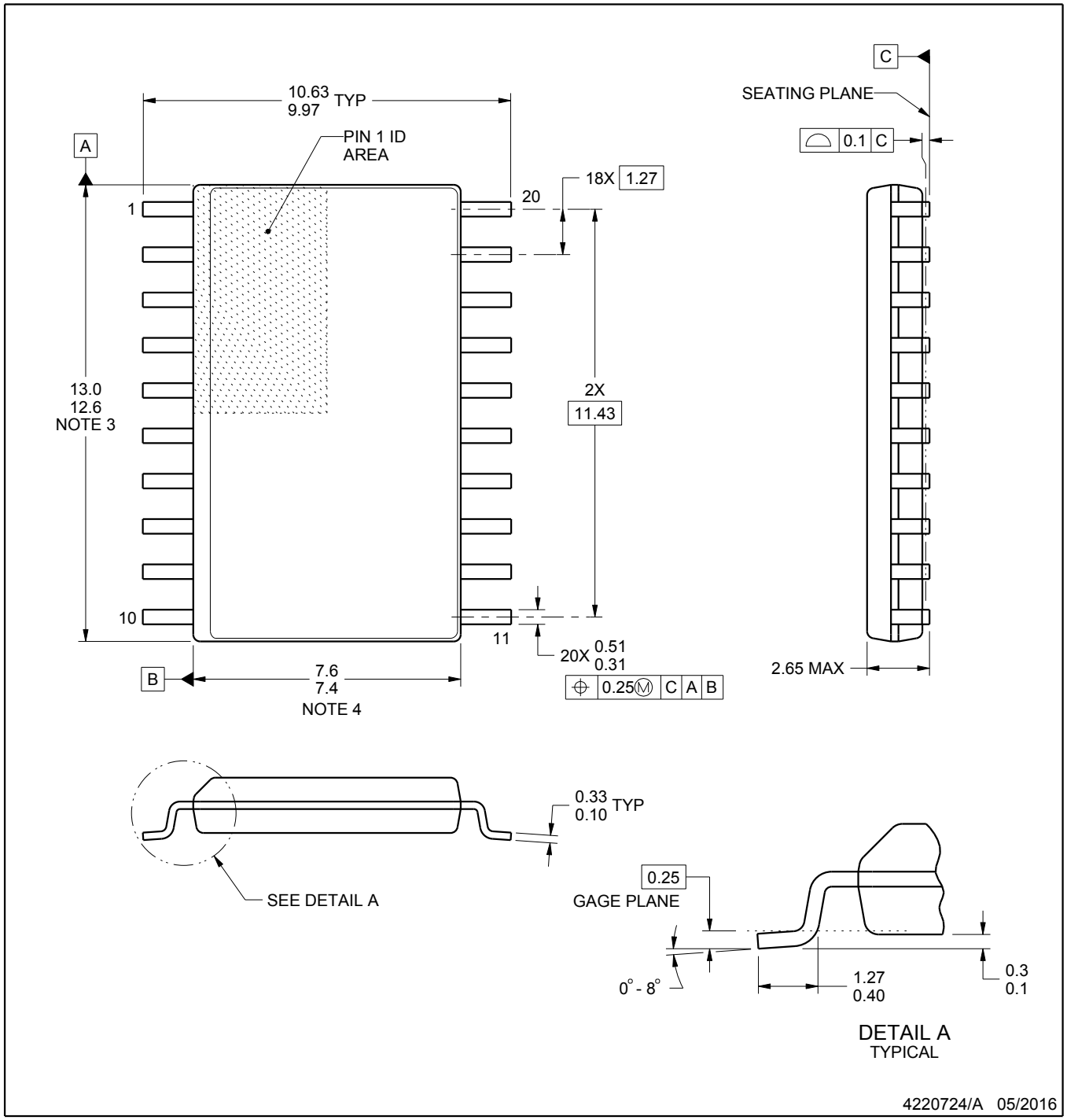


PACKAGE OUTLINE

DW0020A

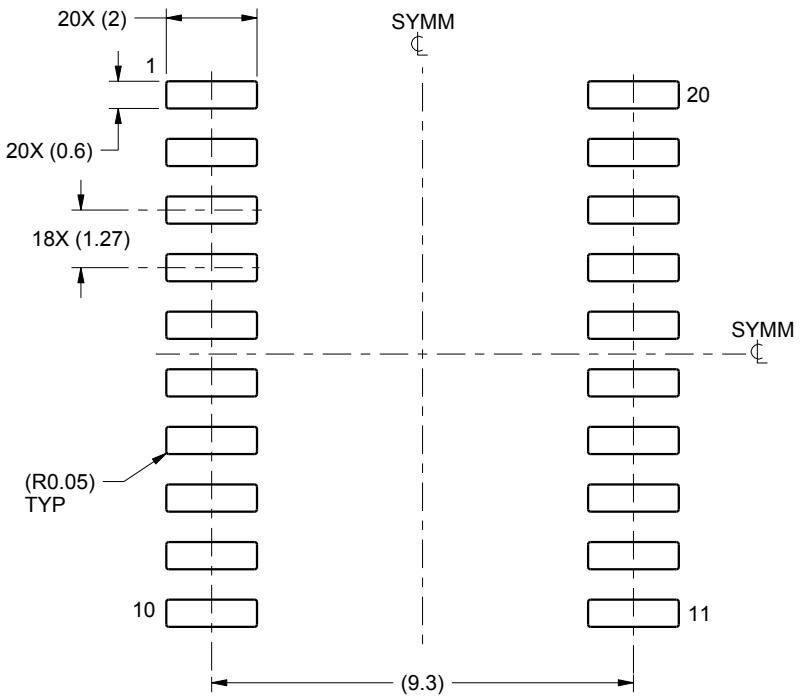
SOIC - 2.65 mm max height

SOIC

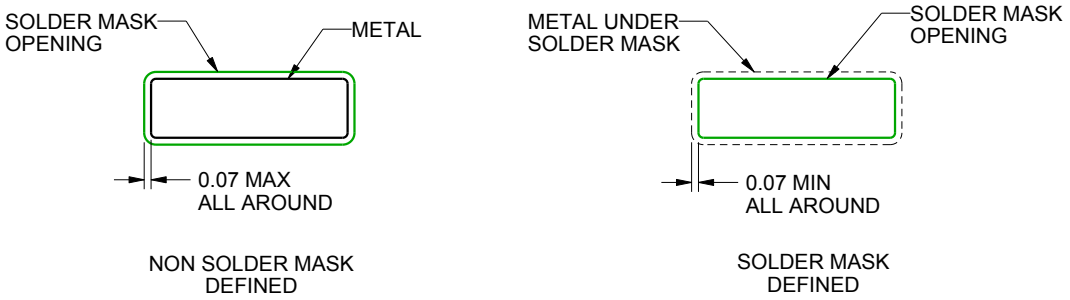


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

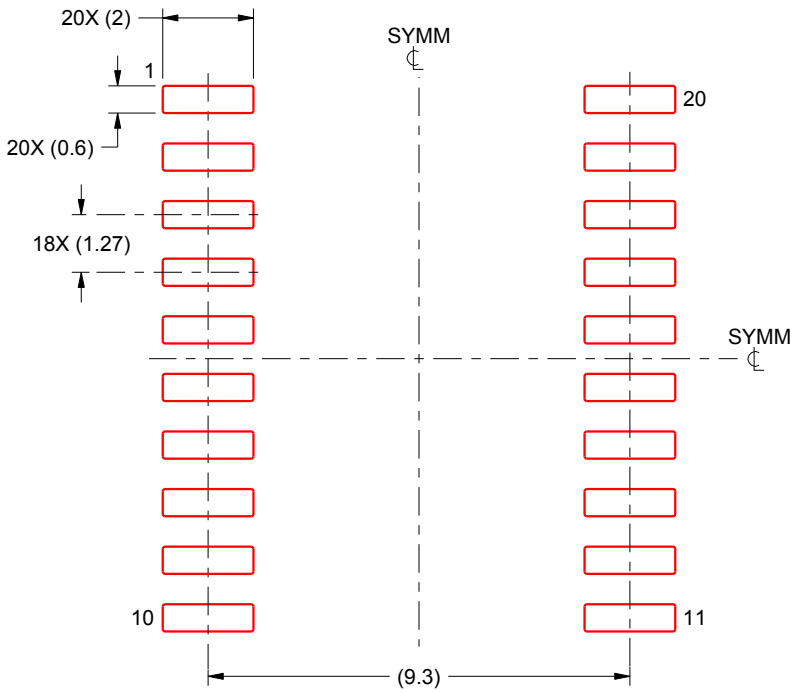


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

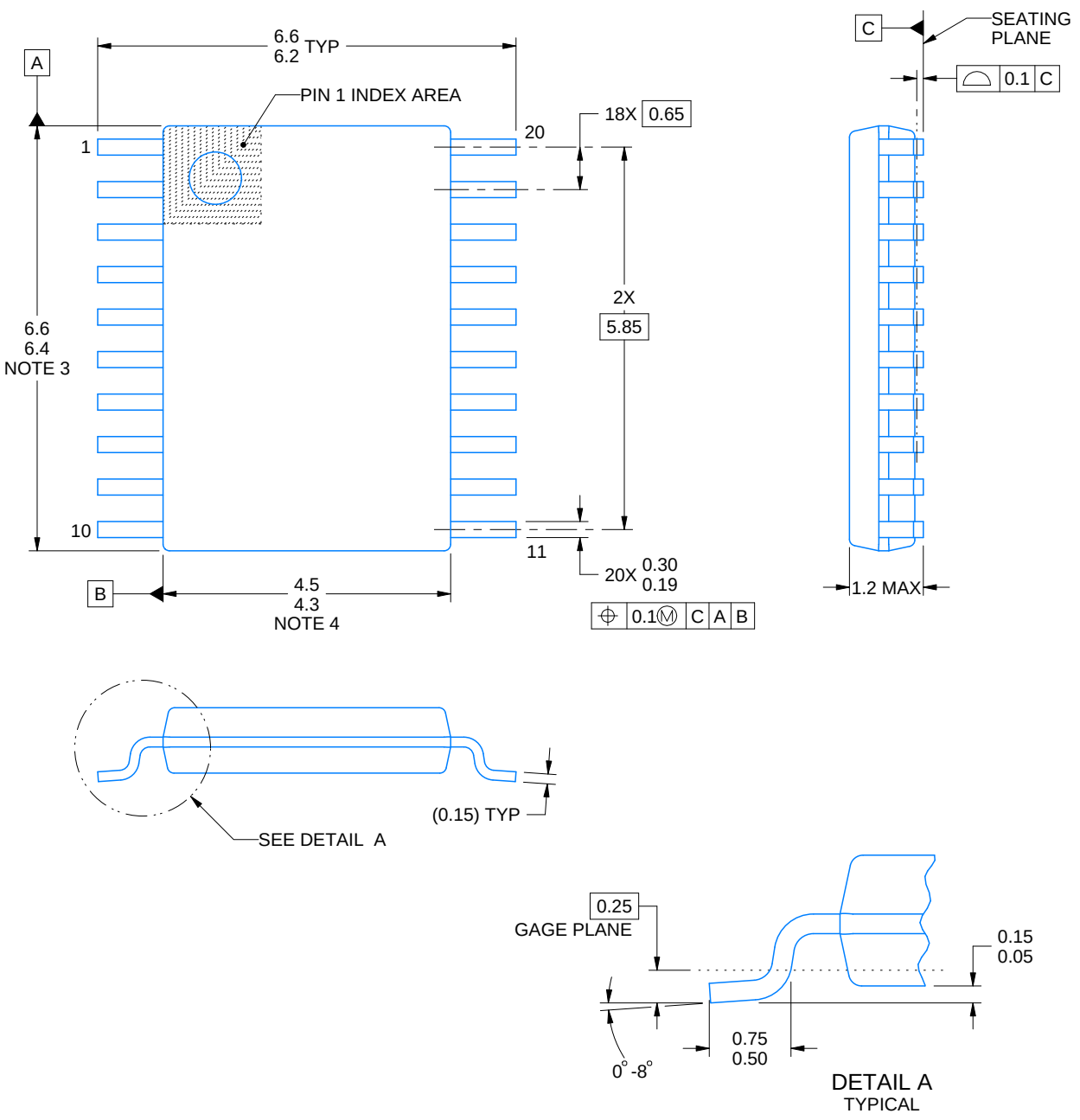
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0020A

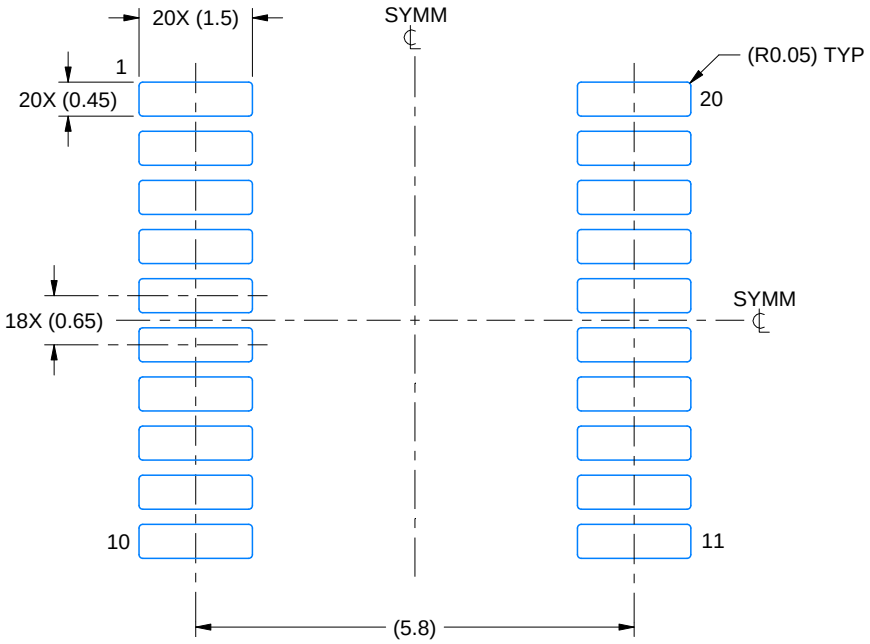
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

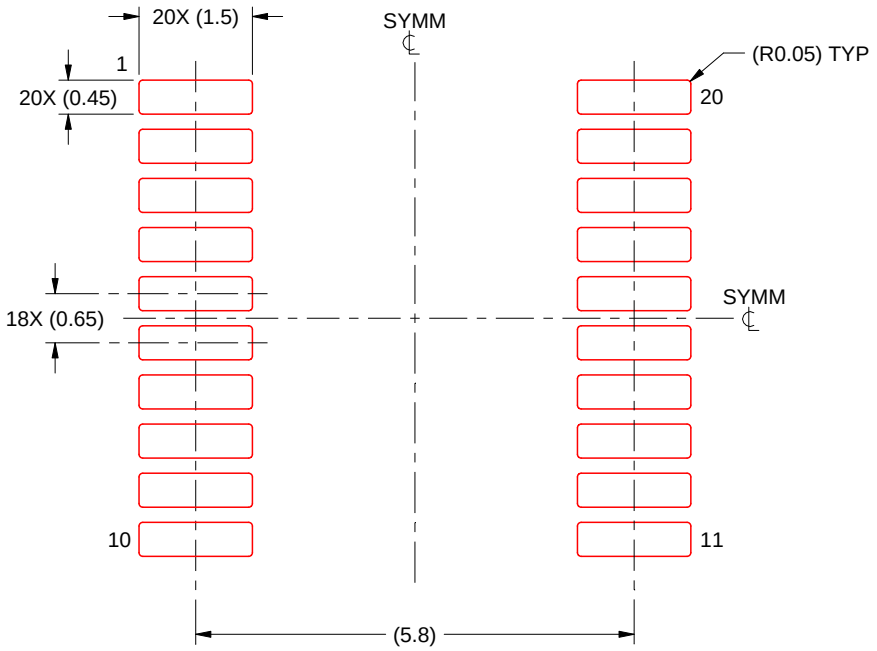


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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