TCA9517 电平转换 I²C 总线中继器

1 特性

- 双通道双向缓冲器
- 与 I²C 总线和系统管理总线 (SMBus) 兼容
- 在 A 侧上，运行电源电压范围为 0.9V 至 5.5V
- 在 B 侧上，运行电源电压范围为 2.7V 至 5.5V
- 从 0.9V-5.5V 到 2.7V-5.5V 的电压电平转换
- 针对 PCA9515B 的封装和功能替代产品
- 高电平有效中继器启用输入
- 漏极开路 I²C I/O
- 5.5V 耐压 I²C 和使能输入支持混合模式信号操作
- 适用于标准模式和快速模式 I²C 器件和多重主器件
- 器件断电时 I²C 引脚呈高阻态
- 锁断性能超过 100mA，符合 JESD 78 II 类规范的要求
- 静电放电 (ESD) 保护性能超过 JESD 22 规范的要求
  - 5500V 人体放电模式 (A114-A)
  - 200V 机器放电模式 (A115-A)
  - 1000V 组件充电模式 (C101)

2 应用

- 服务器
- 路由器（电信交换设备）
- 工业设备
- 具有多个 I²C 从器件和/或印刷电路板 (PCB) 走线较长的产品

3 说明

TCA9517 是一款具有电平转换功能的双向缓冲器，适用于 I²C 和 SMBus 系统。此器件可在混合模式应用中提供低电压（低至 0.9V）和较高电压（2.7V 至 5.5V）间的双向电压电平转换（上行转换/下行转换）。 应用中的杂音问题。。该器件能够扩展 I²C 和 SMBus 系统，甚至在电平转换期间也不会影响系统性能。

TCA9517 可缓冲 I²C 总线上的串行数据 (SDA) 和串行时钟 (SCL) 信号，因此允许 I²C 应用中的两条总线连接高达 400pF 的总线电容。

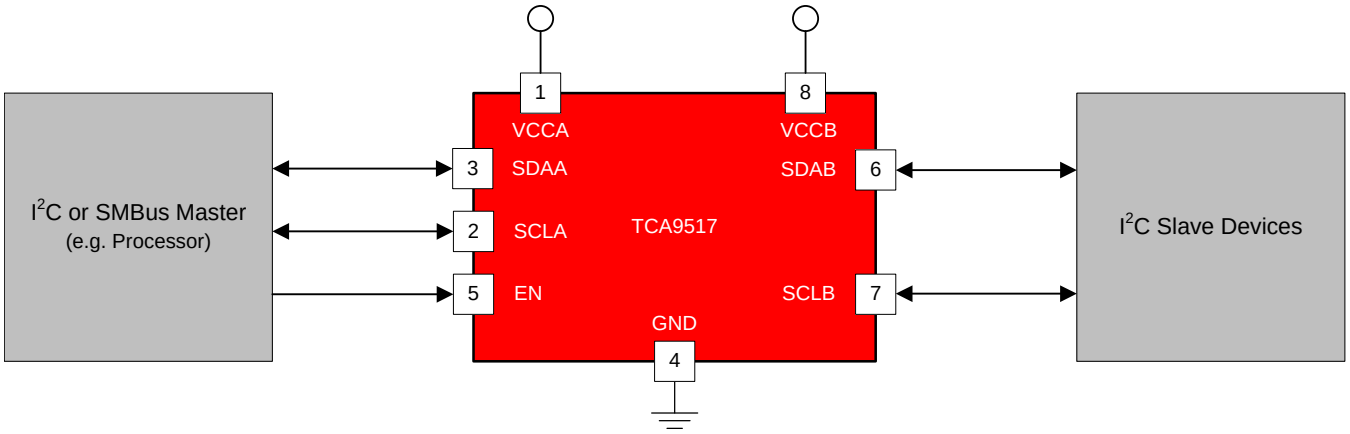
TCA9517 具有两类驱动器：A 侧驱动器和 B 侧驱动器。所有输入和 I/O 均可耐受 5.5V 过压，甚至在器件断电时（V_{CCB} 和/或 V_{CCA} = 0V）也如此。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TCA9517	VSSOP (8)	3.00mm × 3.00mm
	SOIC (8)	4.90mm x 3.91mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化的原理图



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (June 2015) to Revision D **Page**

- Deleted $V_{CCA} < V_{CCB}$ from the *Design Requirements* list ... 12

Changes from Revision B (May 2013) to Revision C **Page**

- 已添加 *引脚配置和功能*部分、*ESD 额定值*表、*特性 说明* 部分、*器件功能模式*、*应用和实施*部分、*电源相关建议*部分、*布局*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1
- 删除了订购信息表。 ... 3

Changes from Revision A (April 2013) to Revision B **Page**

- 更新了订购信息表的顶部标记列。 ... 1

Changes from Original (December 2012) to Revision A **Page**

- 在文档中增加了 D 封装。 ... 1
- 更新了订购信息表的顶部标记列。 ... 1

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5 说明（续）

B 侧上的缓冲器设计类型使其无法与使用静态电压偏移的器件串联使用。这是因为这类器件并不将经缓冲的低电平信号识别为有效低电平，并且不再将其作为经缓冲的低电平进行传送。

B 侧驱动器运行电压介于 2.7V 至 5.5V 之间。针对这个内部缓冲器的输出低电平大约为 0.5V，但是当输出在内部被驱动为低电平时，输入电压必须比输出低电平低 70mV 或者更多。更高的电压低信号被称为经缓冲的低电平。当 B 侧 I/O 被内部驱动为低电平时，输入并不将此低电平识别为低电平。当输入低电平状态被释放时，这一特性防止了锁定情况的发生。

A 侧驱动器运行电压介于 0.9V 至 5.5V 之间并且能够驱动更大电流。它们不需要经缓冲的低电平特性（或者静态偏移电压）。这意味着，B 侧上的低电平信号将转换为 A 侧上接近 0V 的低电平，以适应低压逻辑的较小电压摆幅。A 侧上的输出下拉电阻会驱动一个“硬”低电平，输入电平会设置在 $0.3 \times V_{CCA}$ 以满足低压侧电源电压低至 0.9V 的系统对于较低低电平的需求。

可将 A 侧作为公共总线，将两个或两个以上的 TCA9517 的 A 侧连接在一起，从而实现多个拓扑结构（请参阅 图 8 和 图 9）。此外，还可以将 A 侧直接连接至任意具有静态或动态偏移电压的其他缓冲器。可以将多个 TCA9517 串联在一起（相邻器件间通过 A 侧和 B 侧相连），偏移电压不会增大，只是需要考虑飞行时间延迟。由于 B 侧缓冲低电压的原因，TCA9517 不能通过 B 侧相连。B 侧不能连接配有上升时间加速器的器件。

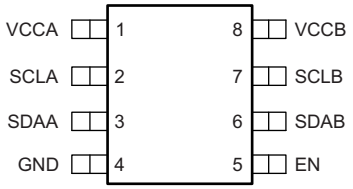
VCCA 只能用于为 A 侧输入比较器提供 $0.3 \times V_{CCA}$ 参考电压，或者用于电源正常状态检测电路。TCA9517 逻辑和所有 I/O 均由 VCCB 引脚供电。

当与标准 I^2C 系统一同工作时，需要用上拉电阻在经缓冲的总线上提供逻辑高电平。TCA9517 具有 I^2C 总线的标准漏极开路配置。这些上拉电阻器的尺寸由系统决定，然而，中继器的每一侧都必须有一个上拉电阻器。此器件专为与标准模式及快速模式 I^2C 器件（而不单是 SMBus 器件）一起工作而设计。在可以接受标准模式器件和多个主控器的通用型 IC 系统中，标准模式 I^2C 器件的额定值只为 3mA。在特定条件下，可以采用更高的终止电流。

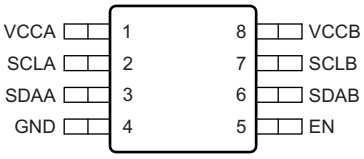
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6 Pin Configuration and Functions

D Packages
8-Pin SOIC
Top View



DGK Package
8-Pin VSSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VCCA	Supply	A-side supply voltage (0.9 V to 5.5 V)
2	SCLA	Input/Output	Serial clock bus, A-side. Connect to V_{CCA} through a pull-up resistor. If unused, connect directly to ground.
3	SDAA	Input/Output	Serial data bus, A-side. Connect to V_{CCA} through a pull-up resistor. If unused, connect directly to ground.
4	GND	Ground	Ground
5	EN	Input	Active-high repeater enable input
6	SDAB	Input/Output	Serial data bus, B-side. Connect to V_{CCB} through a pull-up resistor. If unused, connect directly to ground.
7	SCLB	Input/Output	Serial clock bus, B-side. Connect to V_{CCB} through a pull-up resistor. If unused, connect directly to ground.
8	VCCB	Supply	B-side and device supply voltage (2.7 V to 5.5 V)

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCB}	Supply voltage range		–0.5	7	V
V_{CCA}	Supply voltage range		–0.5	7	V
V_I	Enable input voltage range(2)		–0.5	7	V
$V_{I/O}$	I^2C bus voltage range(2)		–0.5	7	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

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7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±5500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	
		Machine model (A115-A)	±200	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CCA}	Supply voltage, A-side bus		0.9 (1)	5.5	V
V_{CCB}	Supply voltage, B-side bus		2.7	5.5	V
V_{IH}	High-level input voltage	SDAA, SCLA	0.7 × V_{CCA}	5.5	V
		SDAB, SCLB	0.7 × V_{CCB}	5.5	
		EN	0.7 × V_{CCB}	5.5	
V_{IL}	Low-level input voltage	SDAA, SCLA		0.3 × V_{CCA}	V
		SDAB, SCLB (2)		0.3 × V_{CCB}	
		EN		0.3 × V_{CCB}	
I_{OL}	Low-level output current			6	mA
T_A	Operating free-air temperature		–40	85	°C

(1) Low-level supply voltage
(2) V_{IL} specification is for the first low level seen by the SDAB and SCLB lines. V_{ILc} is for the second and subsequent low levels seen by the SDAB and SCLB lines. See *V_{ILC} and Pullup Resistor Sizing* for V_{ILC} application information

7.4 Thermal Information

THERMAL METRIC (1)		TCA9517		UNIT
		DGK (VSSOP)	D (SOIC)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.6	133.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.3	87.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	108.6	74.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.4	36.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	106.9	73.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

V_{CCB} = 2.7 V to 5.5 V, GND = 0 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CCB}	MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = –18 mA	2.7 V to 5.5 V			–1.2	V
V_{OL}	Low-level output voltage	SDAB, SCLB	I_{OL} = 100 μA or 6 mA, V_{ILA} = V_{ILB} = 0 V	2.7 V to 5.5 V	0.45	0.52	0.6	V
		SDAA, SCLA	I_{OL} = 6 mA			0.1	0.2	
V_{OL} – V_{ILc}	Low-level input voltage below low-level output voltage	SDAB, SCLB	ensured by design	2.7 V to 5.5 V		70		mV
V_{ILC}	SDA and SCL low-level input voltage contention	SDAB, SCLB		2.7 V to 5.5 V		0.4		V
I_{CC}	Quiescent supply current for V_{CCA}		Both channels low, SDAA = SCLA = GND and SDAB = SCLB = open, or SDAA = SCLA = open and SDAB = SCLB = GND				1	mA
I_{CC}	Quiescent supply current		Both channels high, SDAA = SCLA = V_{CCA} and SDAB = SCLB = V_{CCB} and EN = V_{CCB}	5.5 V		1.5	5	mA
			Both channels low, SDAA = SCLA = GND and SDAB = SCLB = open			1.5	5	
			In contention, SDAA = SCLA = GND and SDAB = SCLB = GND			3	5	
I_I	Input leakage current	SDAB, SCLB	V_I = V_{CCB}	2.7 V to 5.5 V			±1	μA
			V_I = 0.2 V				10	
		SDAA, SCLA	V_I = V_{CCB}				±1	
			V_I = 0.2 V				10	
		EN	V_I = V_{CCB}				±1	
			V_I = 0.2 V			–10	–30	
I_{OH}	High-level output leakage current	SDAB, SCLB	V_O = 3.6 V	2.7 V to 5.5 V			10	μA
		SDAA, SCLA					10	
C_I	Input capacitance	EN	V_I = 3 V or 0 V	3.3 V		6	10	pF
		SCLA, SCLB	V_I = 3 V or 0 V	3.3 V		8	13	
				0 V		7	11	
C_{IO}	Input/output capacitance	SDAA, SDAB	V_I = 3 V or 0 V	3.3 V		8	13	pF
				0 V		7	11	

7.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
t_{su}	Setup time, EN high before Start condition(1)	100		ns
t_h	Hold time, EN high after Stop condition(1)	100		ns

(1) EN should change state only when the global bus and the repeater port are in an idle state.

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7.7 I²C Interface Switching Characteristics

V_{CCB} = 2.7 V to 5.5 V, GND = 0 V, T_A = –40°C to 85°C (unless otherwise noted)(1) (2)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP(3)	MAX	UNIT
t_{PLZ}	Propagation delay		SDAB, SCLB(4) (see Figure 6)	SDAA, SCLA(4) (see Figure 6)		80	141	250	ns
			SDAA, SCLA(5) (see Figure 5)	SDAB, SCLB(5) (see Figure 5)		25	74	110	
t_{PZL}	Propagation delay		SDAB, SCLB	SDAA, SCLA	V_{CCA} ≤ 2.7 V (see Figure 4)	30	76(6)	110	ns
					V_{CCA} ≥ 3 V (see Figure 4)	10	86	230	
			SDAA, SCLA(5) (see Figure 5)	SDAB, SCLB(5) (see Figure 5)		60	107	230	
t_{TLH}	Transition time	B-side to A side	80%	20%	V_{CCA} ≤ 2.7 V (see Figure 5)	10	12	15	ns
					V_{CCA} ≥ 3 V (see Figure 5)	40	42	45	
		A side to B-side (see Figure 4)				110	125	140	
t_{THL}	Transition time	B-side to A side	80%	20%	V_{CCA} ≤ 2.7 V (see Figure 5)	1	52(6)	105	ns
					V_{CCA} ≥ 3 V (see Figure 5)	20	67	175	
		A side to B-side (see Figure 4)				30	48	90	

(1) Times are specified with loads of 1.35-kΩ pull-up resistance and 50-pF load capacitance on the B-side and 167-Ω pull-up and 57-pF load capacitance on the A side. Different load resistance and capacitance alter the RC time constant, thereby changing the propagation delay and transition times.
(2) pull-up voltages are V_{CCA} on the A side and V_{CCB} on the B-side.
(3) Typical values were measured with V_{CCA} = V_{CCB} = 3.3 V at T_A = 25°C, unless otherwise noted.
(4) The t_{PLH} delay data from B to A side is measured at 0.4 V on the B-side to 0.5 V_{CCA} on the A side when V_{CCA} is less than 2 V, and 1.5 V on the A side if V_{CCA} is greater than 2 V.
(5) The proportional delay data from A to B-side is measured at 0.3 V_{CCA} on the A side to 1.5 V on the B-side.
(6) Typical value measured with V_{CCA} = 2.7 V at T_A = 25°C

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7.8 Typical Characteristics

V_{CCA} = 0.9 V, V_{CCB} = 2.7 V

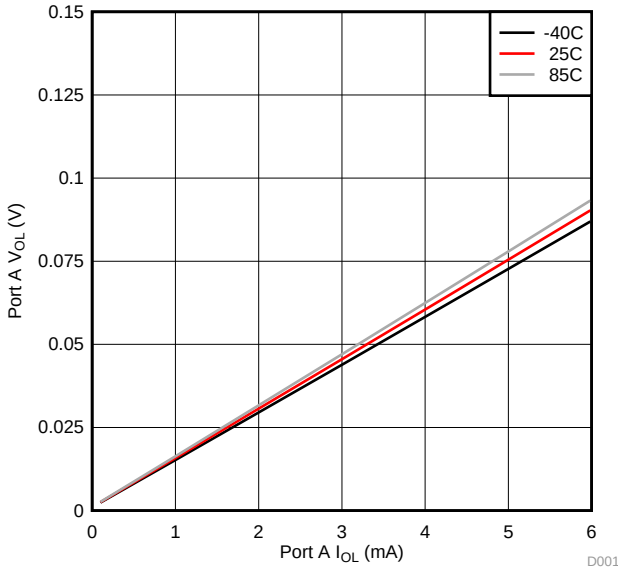


Figure 1. Port A V_{OL} vs I_{OL}

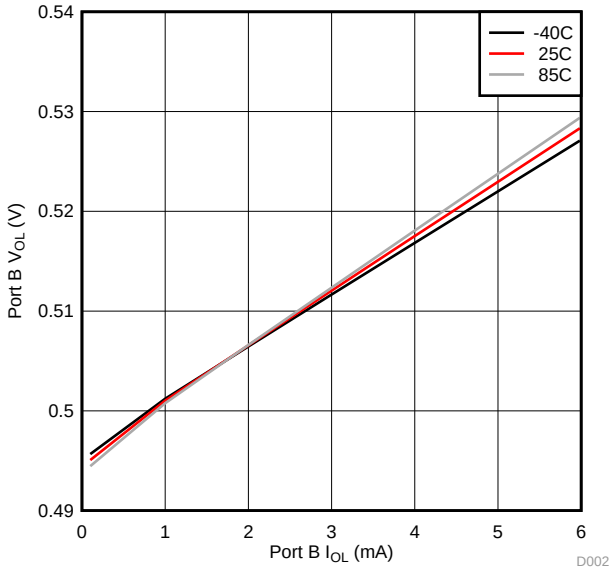
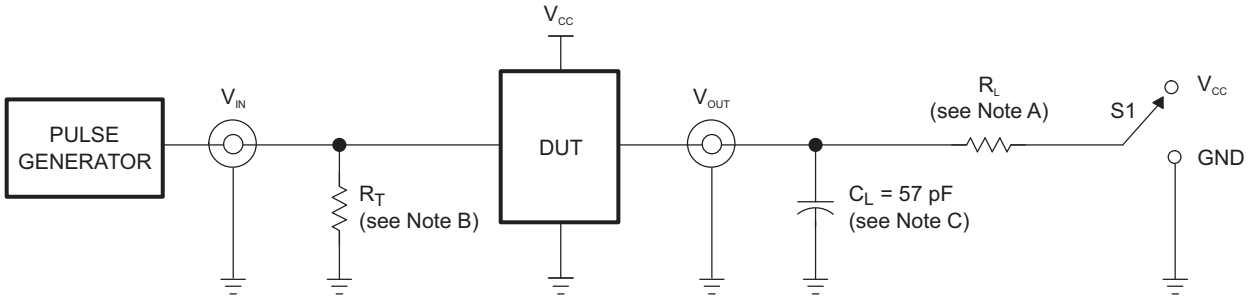


Figure 2. Port B V_{OL} vs I_{OL}

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8 Parameter Measurement Information



TEST	S1
t_{PLZ}/t_{PZL}	V_{CC}

TEST CIRCUIT FOR OPEN-DRAIN OUTPUT

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A. R_L = 167 Ω (0.9 V to 2.7 V) and R_L = 450 Ω (3.0 V to 5.5 V) on the A side and 1.35 kΩ on the B-side
B. R_T termination resistance should be equal to Z_{OUT} of pulse generators.
C. C_L includes probe and jig capacitance.
D. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.
E. The outputs are measured one at a time, with one transition per measurement.
F. t_{PLH} and t_{PHL} are the same as t_{pd}.
G. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
H. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 3. Test Circuit

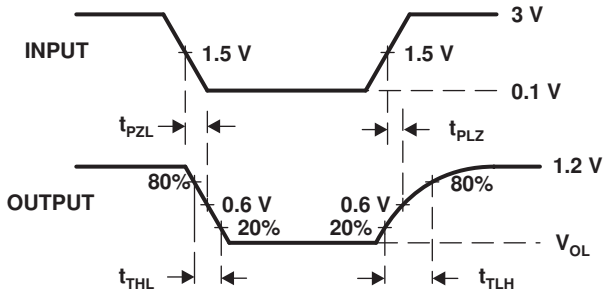


Figure 4. Waveform 1 – Propagation Delay and Transition Times for B-side to A-side

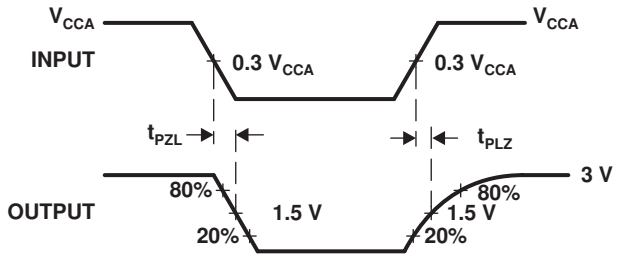


Figure 5. Waveform 2 – Propagation Delay and Transition Times for A-side to B-side

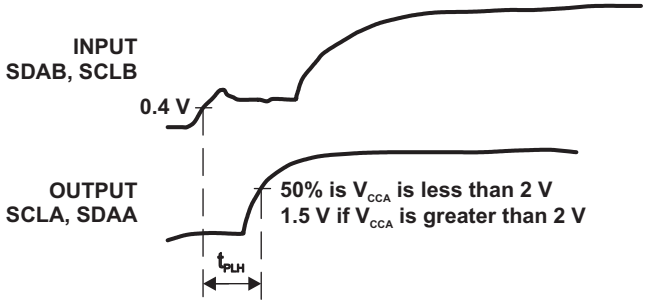


Figure 6. Waveform 3 – Propagation Delay for B-side to A-side

9 Detailed Description

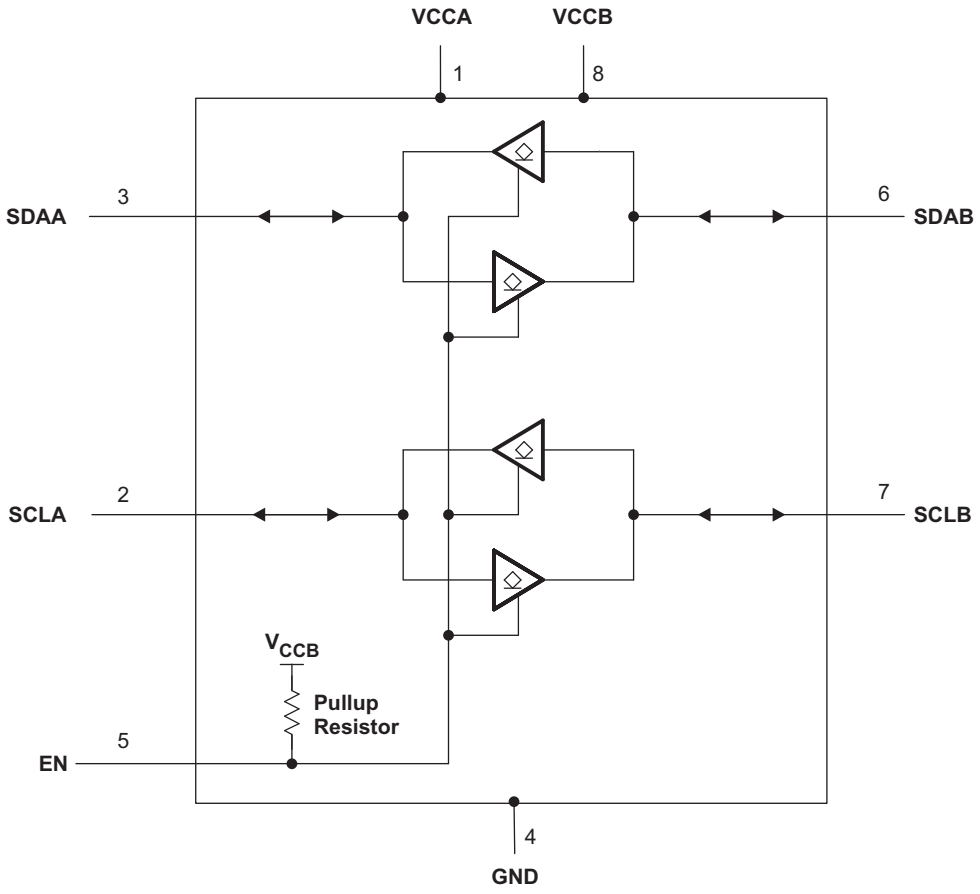
9.1 Overview

The TCA9517 is a bidirectional buffer with level shifting capabilities for I^2C and SMBus systems. It provides bidirectional voltage-level translation (up-translation/down-translation) between low voltages (down to 0.9 V) and higher voltages (2.7 V to 5.5 V) in mixed-mode applications. This device enables I^2C and SMBus systems to be extended without degradation of performance, even during level shifting.

The TCA9517 buffers both the serial data (SDA) and the serial clock (SCL) signals on the I^2C bus, thus allowing two buses of up to 400-pF bus capacitance to be connected in an I^2C application.

The TCA9517 has two types of drivers: A-side drivers and B-side drivers. All inputs and I/Os are over-voltage tolerant to 5.5 V, even when the device is unpowered (V_{CCB} and/or V_{CCA} = 0 V).

9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 Two-Channel Bidirectional Buffer

The TCA9517 is a two-channel bidirectional buffer with level-shifting capabilities

9.3.2 Active-High Repeater-Enable Input

The TCA9517 has an active-high enable (EN) input with an internal pull-up to V_{CCB}, which allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up reset. The EN input should change state only when the global bus and repeater port are in an idle state, to prevent system failures.

9.3.3 V_{OL} B-Side Offset Voltage

The B-side drivers operate from 2.7 V to 5.5 V. The output low level for this internal buffer is approximately 0.5 V, but the input voltage must be 70 mV or more below the output low level when the output internally is driven low. The higher-voltage low signal is called a buffered low. When the B-side I/O is driven low internally, the low is not recognized as a low by the input. This feature prevents a lockup condition from occurring when the input low condition is released. This type of design prevents 2 B-side ports from being connected to each other.

9.3.4 Standard Mode and Fast Mode Support

The TCA9517 supports standard mode as well as fast mode I^2C. The maximum system operating frequency will depend on system design and the delays added by the repeater.

9.3.5 Clock Stretching Support

The TCA9517 can support clock stretching, but care needs to be taken to minimize the overshoot voltage presented during the hand-off between the slave and master. This is best done by increasing the pull-up resistor value.

9.4 Device Functional Modes

Table 1. Function Table

INPUT EN	FUNCTION
L	Outputs disabled
H	SDAA = SDAB SCLA = SCLB

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

A typical application is shown in Figure 7. In this example, the system master is running on a 3.3 V I^2C bus, and the slave is connected to a 1.2 V I^2C bus. Both buses run at 400 kHz. Master devices can be placed on either bus.

The TCA9517 is 5-V tolerant, so it does not require any additional circuitry to translate between 0.9 V to 5.5 V bus voltages and 2.7 V to 5.5 V bus voltages.

When the A side of the TCA9517 is pulled low by a driver on the I^2C bus, a comparator detects the falling edge when it goes below 0.3 × V_{CCA} and causes the internal driver on the B-side to turn on, causing the B-side to pull down to about 0.5 V. When the B-side of the TCA9517 falls, first a CMOS hysteresis-type input detects the falling edge and causes the internal driver on the A side to turn on and pull the A-side pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 9 and Figure 10. If the bus master in Figure 7 were to write to the slave through the TCA9517 , waveforms shown in Figure 9 would be observed on the A bus. This looks like a normal I^2C transmission, except that the high level may be as low as 0.9 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

On the B-side bus of the TCA9517 , the clock and data lines would have a positive offset from ground equal to the V_{OL} of the TCA9517 . After the eighth clock pulse, the data line is pulled to the V_{OL} of the slave device, which is very close to ground in this example. At the end of the acknowledge, the level rises only to the low level set by the driver in the TCA9517 for a short delay, while the A-bus side rises above 0.3 × V_{CCA} and then continues high.

10.2 Typical Application

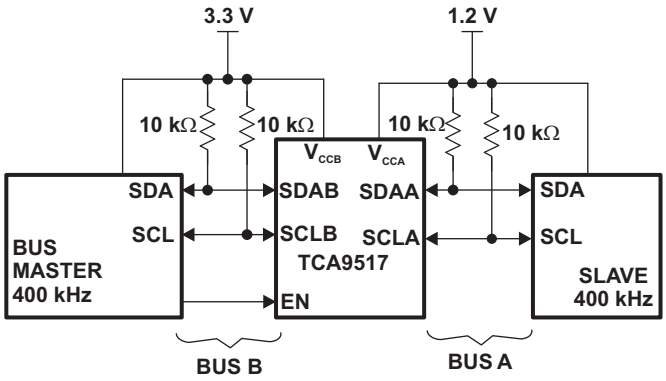


Figure 7. Typical Application Schematic

10.2.1 Design Requirements

For the level translating application, the following should be true:

- V_{CCA} = 0.9 V to 5.5 V
- V_{CCB} = 2.7 to 5.5 V
- B-side ports must not be connected together

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Typical Application (continued)

10.2.2 Detailed Design Procedure

10.2.2.1 Clock Stretching Support

The TCA9517 can support clock stretching, but care needs to be taken to minimize the overshoot voltage presented during the hand-off between the slave and master. This is best done by increasing the pull-up resistor value.

10.2.2.2 V_{ILC} and Pullup Resistor Sizing

For the TCA9517 to function correctly, all devices on the B-side must be able to pull the B-side below the voltage input low contention level (V_{ILC}). This means that the V_{OL} of any device on the B-side must be below 0.4 V.

V_{OL} of a device can be adjusted by changing the I_{OL} through the device which is set by the pull-up resistance value. The pull-up resistance on the B-side must be carefully selected to ensure that logic levels will be transferred correctly to the A-side.

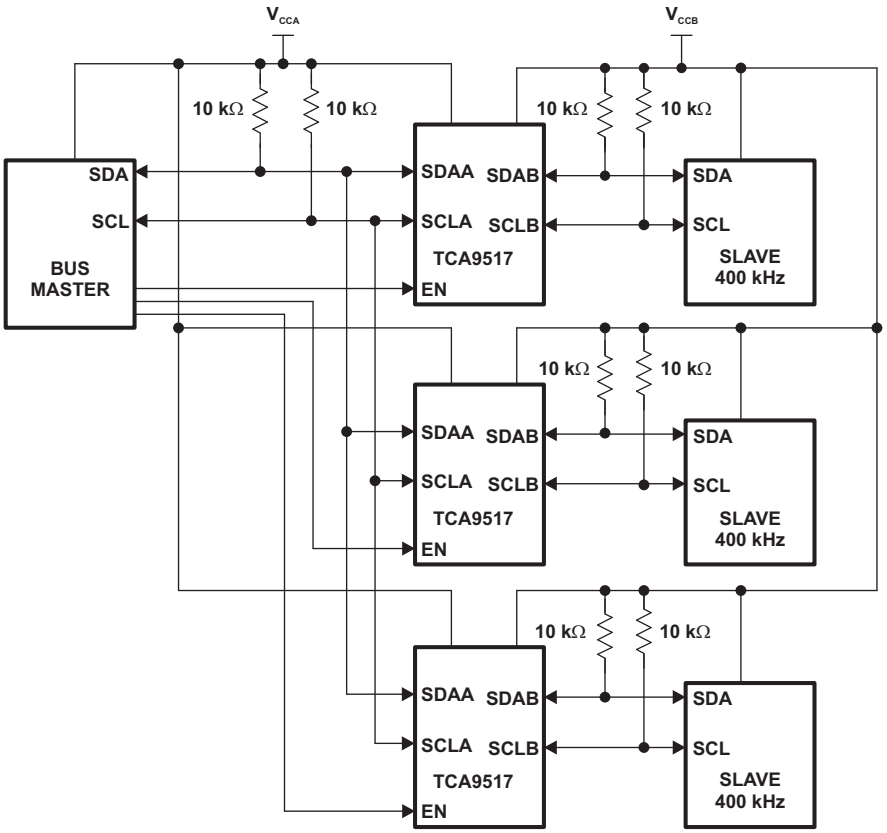


Figure 8. Typical Star Application

Multiple A sides of TCA9517 s can be connected in a star configuration, allowing all nodes to communicate with each other.

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Typical Application (continued)

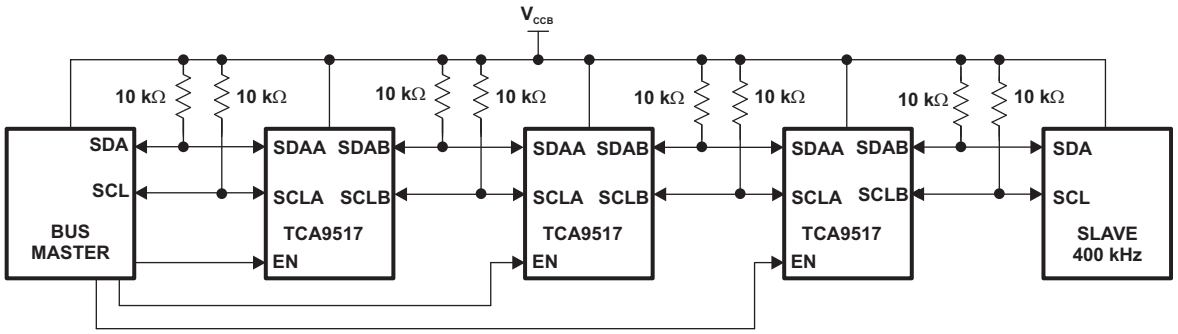


Figure 9. Typical Series Application

To further extend the I^2C bus for long traces/cables, multiple TCA9517 s can be connected in series as long as the A-side is connected to the B-side. I^2C bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

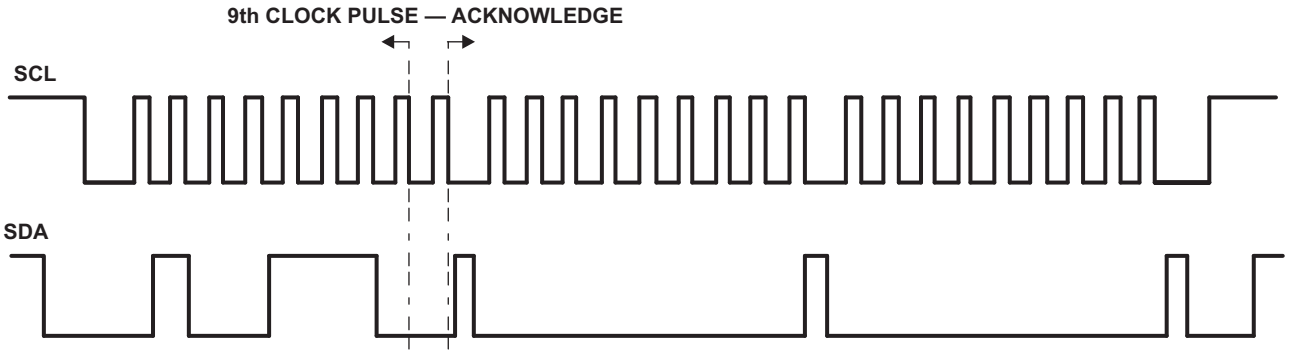


Figure 10. Bus A (0.9 V to 5.5 V Bus) Waveform

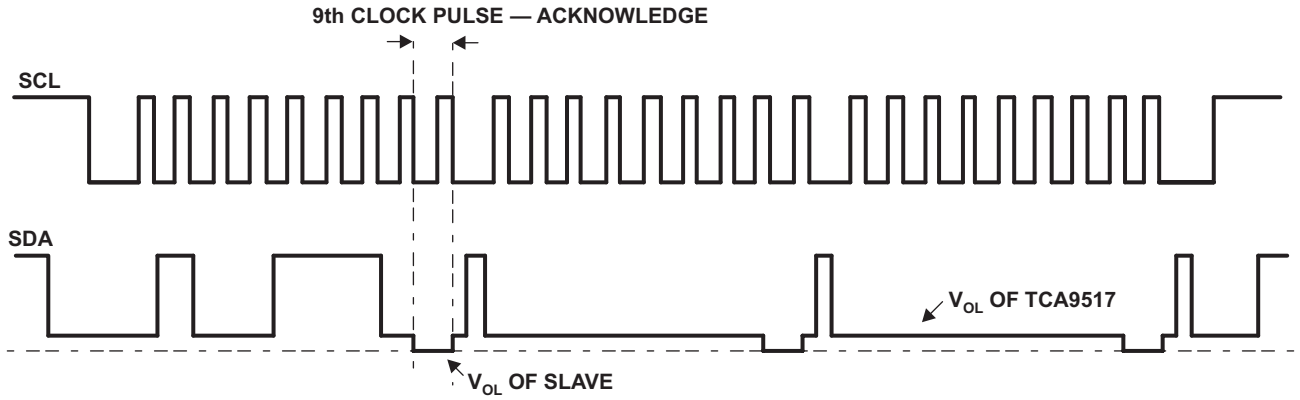


Figure 11. Bus B (2.7 V to 5.5 V Bus) Waveform

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Typical Application (continued)

10.2.3 Application Curve

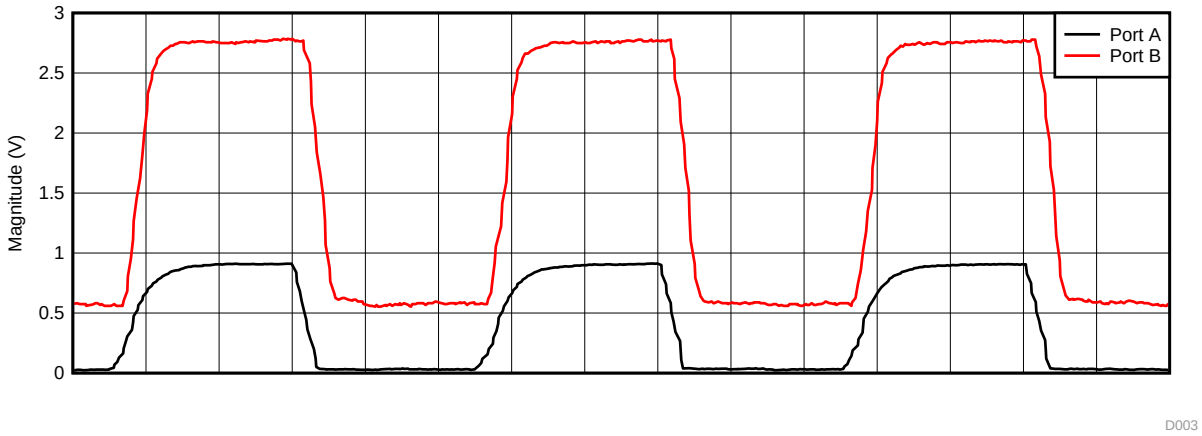


Figure 12. Voltage Translation at 400 kHz, V_{CCA} = 0.9 V, V_{CCB} = 2.7 V

11 Power Supply Recommendations

V_{CCB} and V_{CCA} can be applied in any sequence at power up. The TCA9517 includes a power-up circuit that keeps the output drivers turned off until V_{CCB} is above 2.5 V and the V_{CCA} is above 0.8 V. After power up and with the EN high, a low level on the A-side (below 0.3 × V_{CCA}) turns the corresponding B-side driver (either SDA or SCL) on and drives the B-side down to approximately 0.5 V. When the A-side rises above 0.3 × V_{CCA}, the B-side pull-down driver is turned off and the external pull-up resistor pulls the pin high. When the B-side falls first and goes below 0.3 × V_{CCB}, the A-side driver is turned on and the A-side pulls down to 0 V. The B-side pull-down is not enabled unless the B-side voltage goes below 0.4 V. If the B-side low voltage does not go below 0.5 V, the A-side driver turns off when the B-side voltage is above 0.7 × V_{CCB}. If the B-side low voltage goes below 0.4 V, the B-side pull-down driver is enabled, and the B-side is able to rise to only 0.5 V until the A-side rises above 0.3 × V_{CCA}.

TI recommends using a decoupling capacitor and placing it close to the VCCA and VCCB pins of a value of about 100 nF.

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12 Layout

12.1 Layout Guidelines

There are no special layout procedures required for the TCA9517 .

It is recommended that the decoupling capacitors be placed as close to the VCC pins as possible.

12.2 Layout Example

Figure 13 shows an example layout of the DGK package.

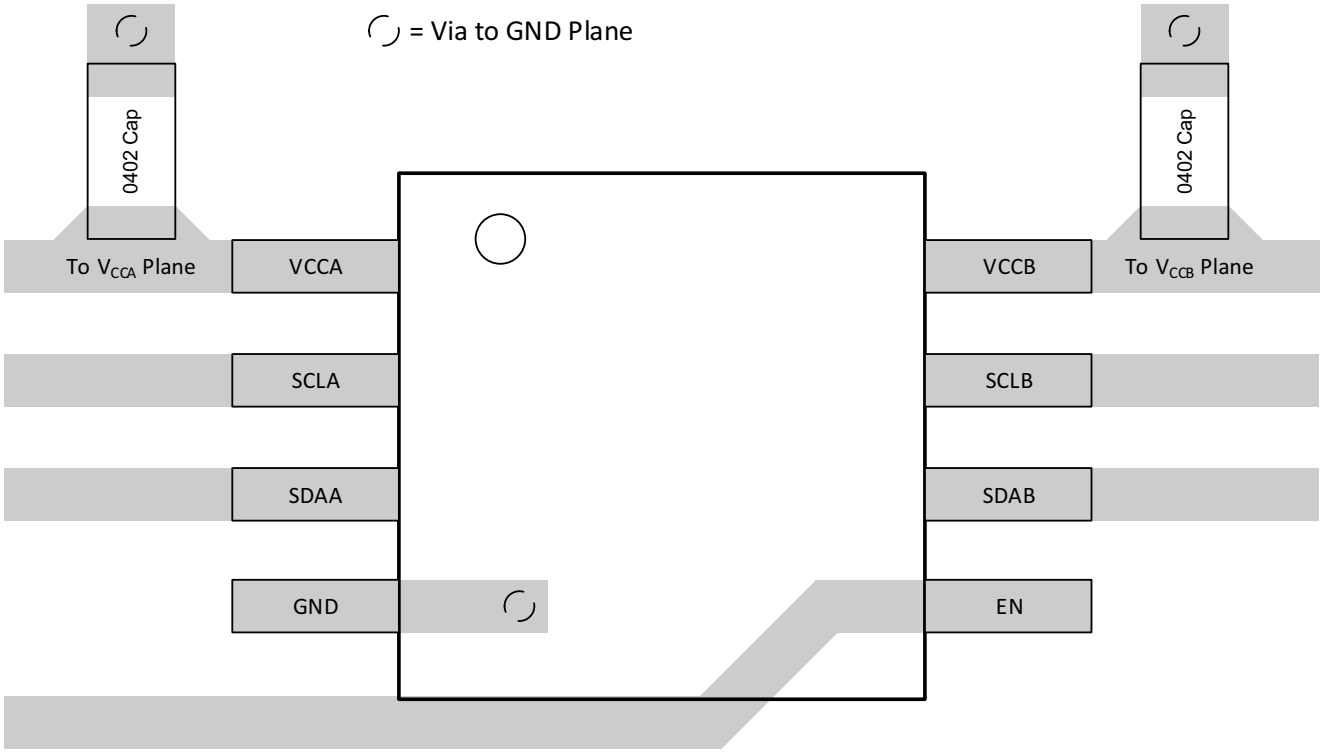


Figure 13. TCA9517A Layout Example

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13 器件和文档支持

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13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCA9517DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AYK
TCA9517DGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AYK
TCA9517DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW517
TCA9517DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW517
TCA9517DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW517
TCA9517DRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW517

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TCA9517 :

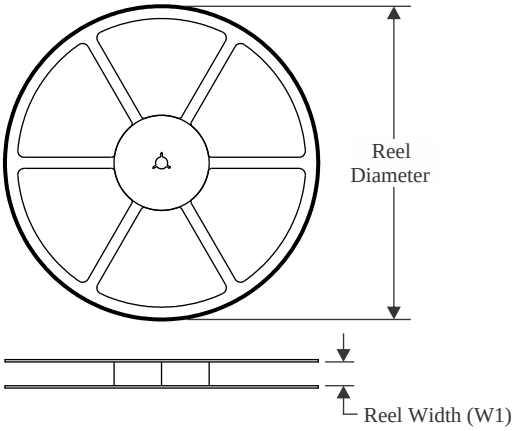
- Automotive : TCA9517-Q1

NOTE: Qualified Version Definitions:

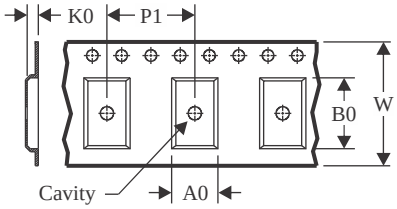
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

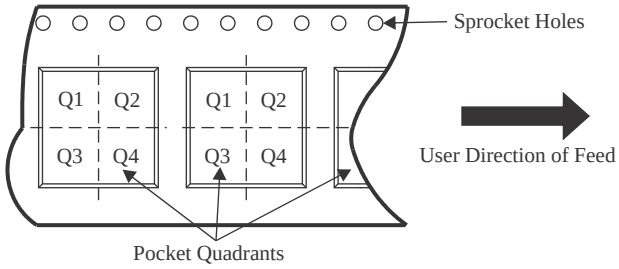


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

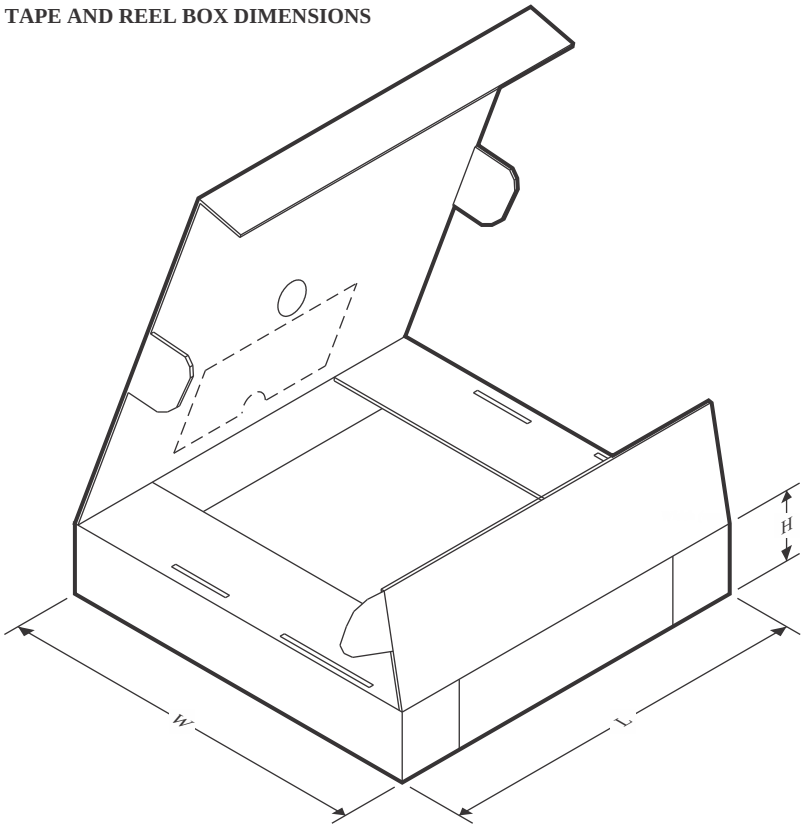
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

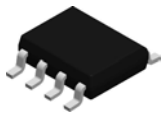
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9517DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TCA9517DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TCA9517DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9517DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TCA9517DR	SOIC	D	8	2500	340.5	336.1	25.0
TCA9517DRG4	SOIC	D	8	2500	340.5	336.1	25.0

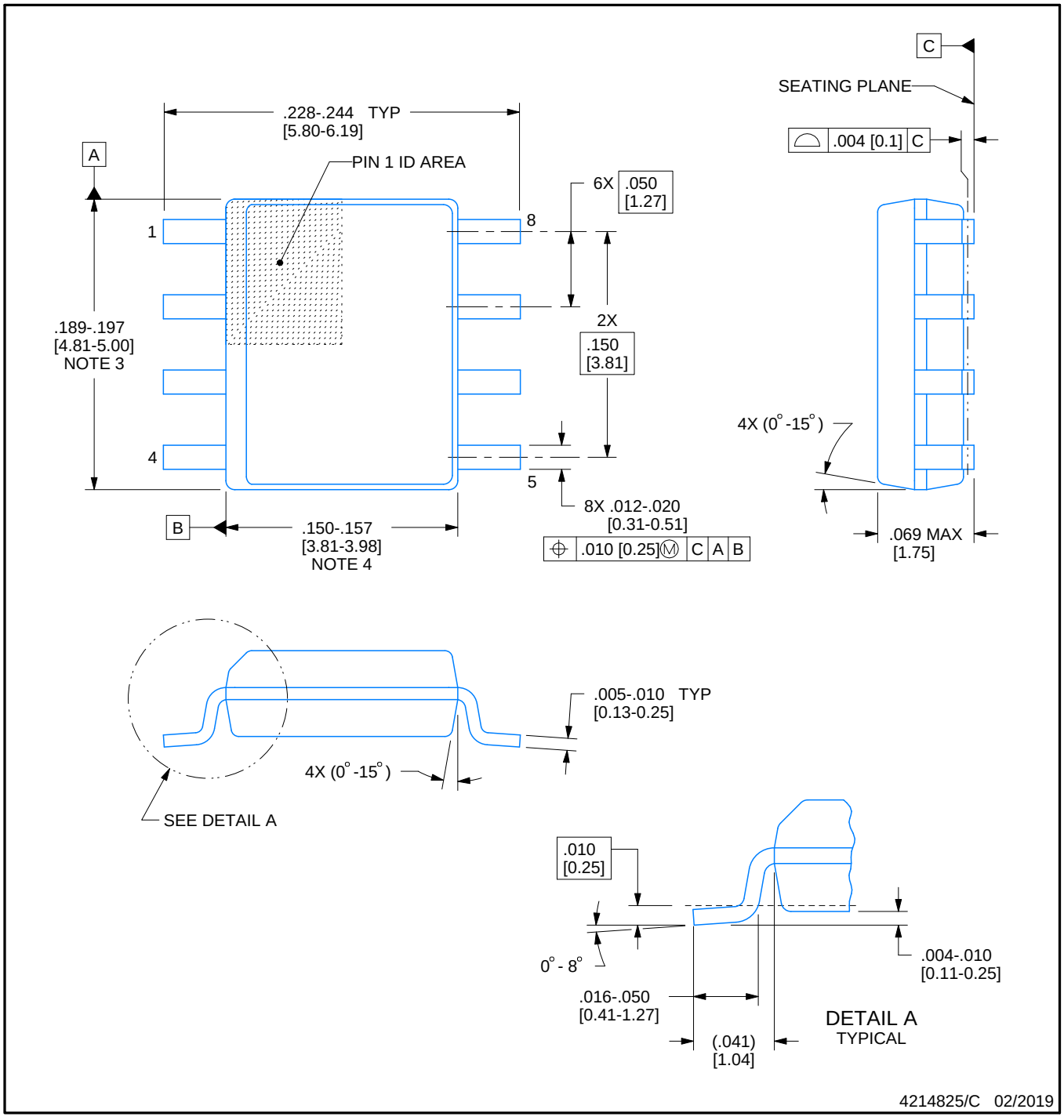


PACKAGE OUTLINE

D0008A

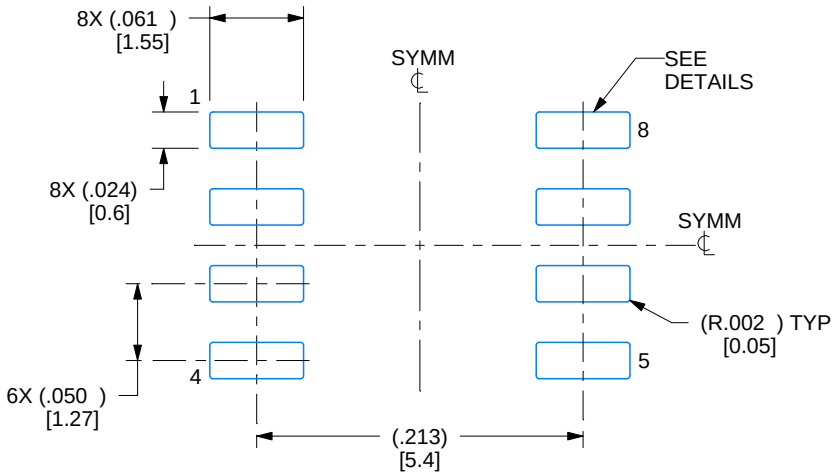
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

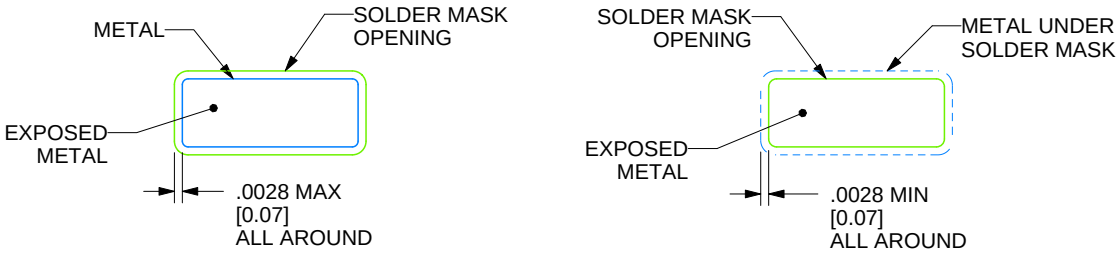


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

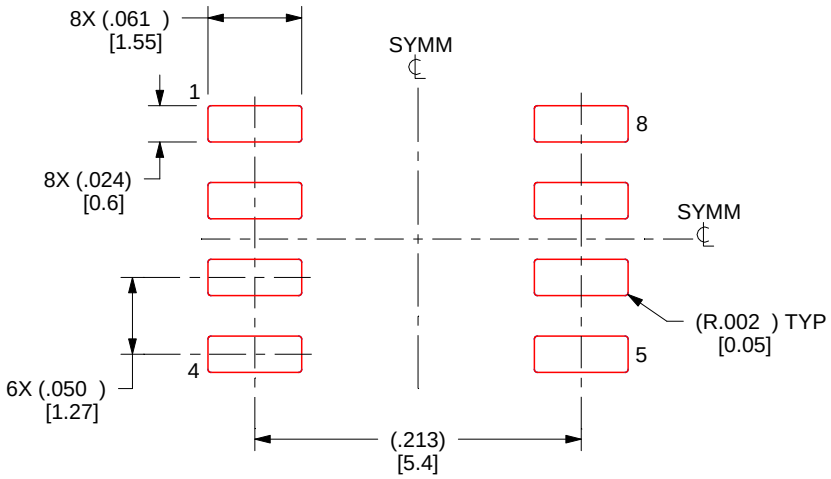
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

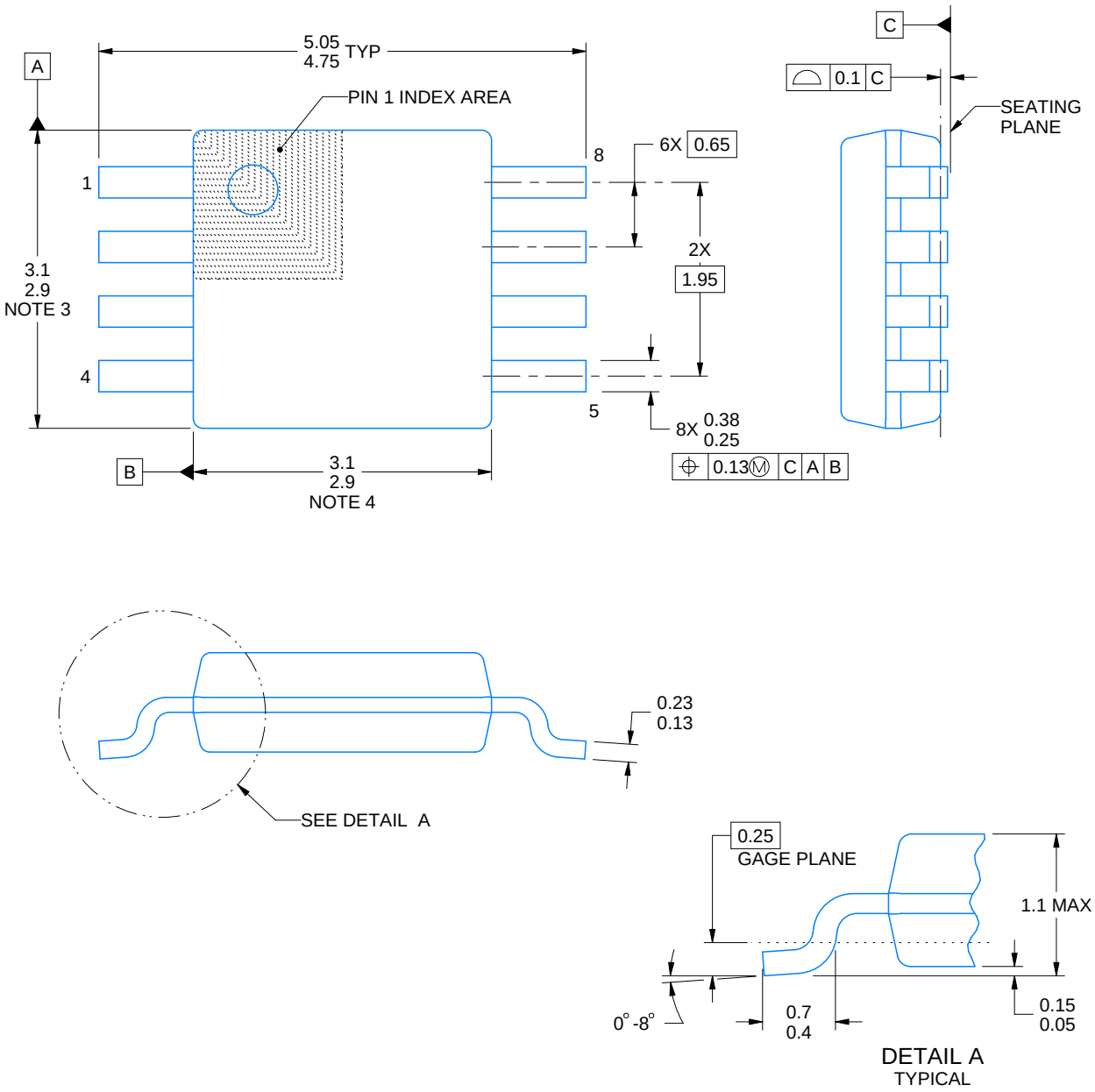
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

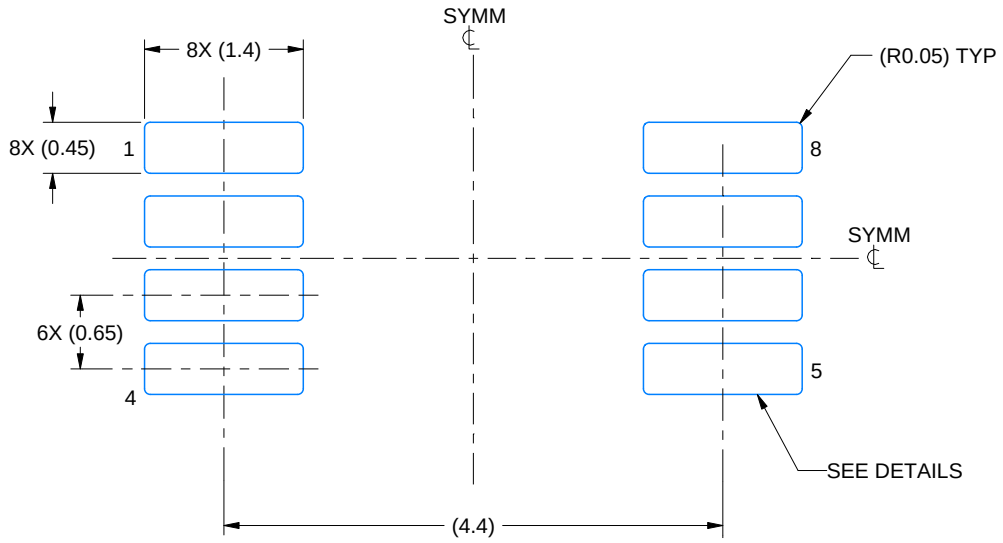
SMALL OUTLINE PACKAGE



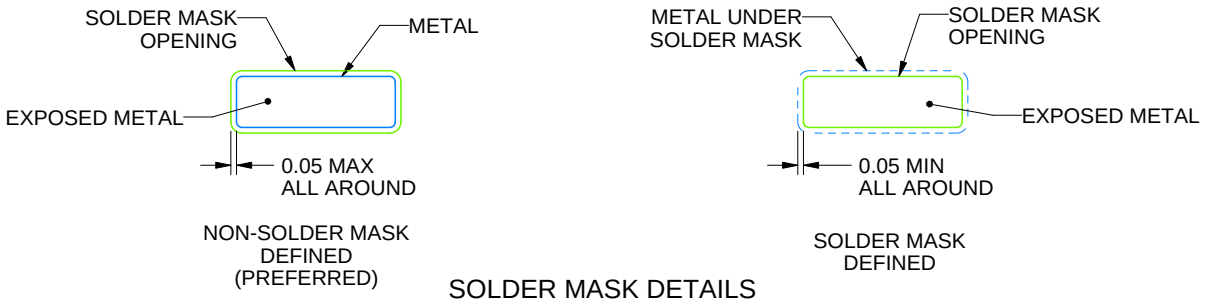
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

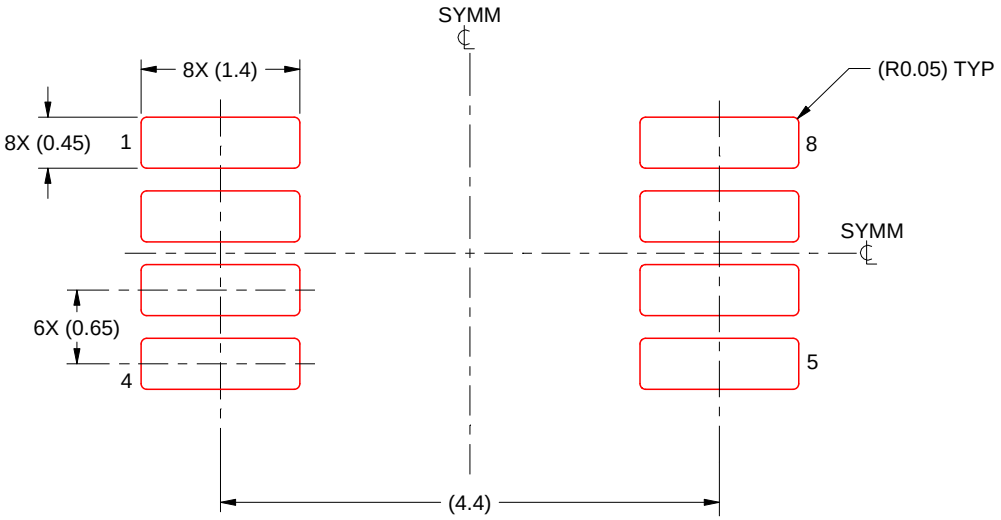


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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