具有闩锁效应抑制和 1.8V 逻辑电平的 TMUX821x 100V、扁平 Ron、1:1 (SPST)、四通道开关

1 特性

- 支持高电源电压：
  - 双电源：±10V 至 ±50V
  - 单电源：10V 至 100V
  - 非对称双电源运行
- 在整个电源电压范围内提供一致的参数性能
- 闩锁效应抑制
- 高持续电流：200mA
- 低串扰：-110dB
- 低输入泄漏电流：10pA
- 低导通电阻平坦度：0.05Ω
- 低导通电阻：5Ω
- 低电容：12pF
- 无需额外逻辑轨 (V_L)
- 支持 1.8V 逻辑电平
- 失效防护逻辑：高达 48V（与电源无关）
- 逻辑引脚上带有集成下拉电阻器
- 双向信号路径
- 宽工作温度 T_A：–40°C 至 125°C
- 业界通用的 TSSOP 封装和较小的 WQFN 封装

2 应用

- 高电压双向切换
- 模拟和数字信号开关
- 半导体测试设备
- LCD 测试设备
- 电池测试设备
- 数据采集系统 (DAQ)
- 数字万用表 (DMM)
- 工厂自动化和控制
- 可编程逻辑控制器 (PLC)
- 模拟输入模块

3 说明

TMUX8211、TMUX8212 和 TMUX8213 是具有闩锁效应抑制并支持高电压的现代模拟开关。每个器件均具有四个独立可控的 1:1 单极单投 (SPST) 开关通道。此器件可在双电源、单电源或非对称电源供电时正常运行，最大电源电压为 100V。TMUX821x 器件可在整个电源电压范围内提供一致的模拟参数性能。TMUX821x 系列可在源极 (Sx) 和漏极 (Dx) 引脚上支持双向模拟和数字信号。

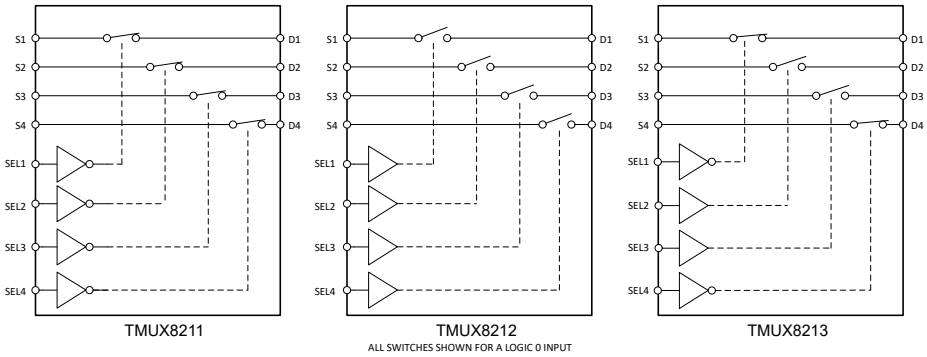
所有逻辑输入均支持 1.8V、3.3V 和 5V 的逻辑电平，并可在电压高达 48V 时进行连接，从而通过控制信号电压实现系统灵活性。失效防护逻辑电路允许在施加电源引脚上的电压之前，先施加逻辑引脚上的电压，从而保护器件免受潜在的损害。

此器件系列具有闩锁效应抑制功能，可防止器件内寄生结构之间的大电流不良事件。闩锁状态通常会一直持续到电源轨关闭为止，并可能导致器件故障。凭借闩锁效应抑制功能，此系列多路复用器能够在恶劣的环境中使用。

封装信息(1) (2)

器件型号	封装	封装尺寸（标称值）
TMUX8211 TMUX8212 TMUX8213	PW（TSSOP，16）	5.00mm × 4.40mm
	RUM（WQFN，16）	4.00mm × 4.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 请参阅*器件比较表*。



功能方框图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (December 2021) to Revision B (March 2023)	Page
• 将 RUM 封装状态从 *预发布* 更改为 *正在供货*	1

Changes from Revision * (October 2021) to Revision A (December 2021)	Page
• 将数据表的状态从 *预告信息* 更改为 *量产数据*	1

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5 Device Comparison Table

PRODUCT	DESCRIPTION
TMUX8211	High Voltage, 4-channel, 1:1 (SPST) switches, (Logic Low)
TMUX8212	High Voltage, 4-channel, 1:1 (SPST) switches, (Logic High)
TMUX8213	High Voltage, 4-channel, 1:1 (SPST) switches, (Logic Low + Logic High)

6 Pin Configuration and Functions

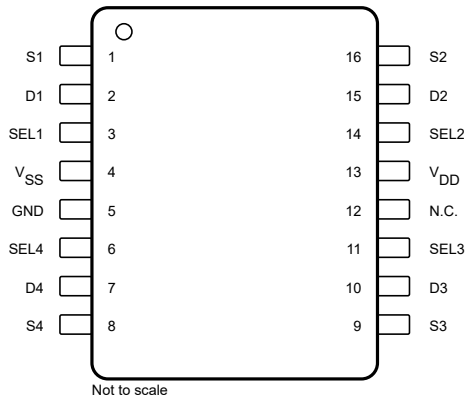

图 6-1. PW Package, 16-Pin TSSOP (Top View)

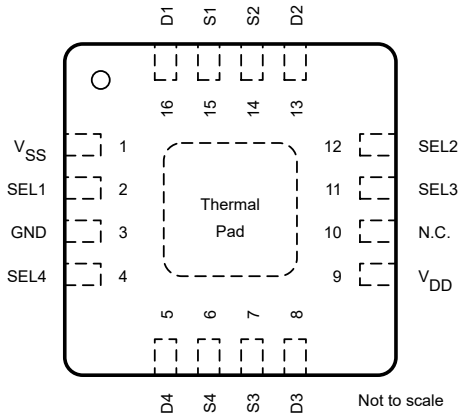

图 6-2. RUM Package, 16-Pin WQFN (Top View)

表 6-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	TSSOP	WQFN		
D1	2	16	I/O	Drain pin 1. Can be an input or output.
D2	15	13	I/O	Drain pin 2. Can be an input or output.
D3	10	8	I/O	Drain pin 3. Can be an input or output.
D4	7	5	I/O	Drain pin 4. Can be an input or output.
GND	5	3	P	Ground (0 V) reference
S1	1	15	I/O	Source pin 1. Can be an input or output.
S2	16	14	I/O	Source pin 2. Can be an input or output.
S3	9	7	I/O	Source pin 3. Can be an input or output.
S3	9	7	I/O	Source pin 3. Can be an input or output.
S4	8	6	I/O	Source pin 4. Can be an input or output.
SEL1	3	2	I	Logic control input 1.
SEL2	14	12	I	Logic control input 2.
SEL3	11	11	I	Logic control input 3.
SEL4	6	4	I	Logic control input 4.
N.C.	12	10	—	No internal connection.
V_{DD}	13	9	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 1 µF to 10 µF between V_{DD} and GND.
V_{SS}	4	1	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 1 µF to 10 µF between V_{SS} and GND.
Thermal Pad			—	The thermal pad is not connected internally. It is recommended that the pad be tied to GND or V_{SS} for best performance.

(1) I = input, O = output, I/O = input and output, P = power

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7 Specifications

7.1 Absolute Maximum Ratings: TMUX821x Devices

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD} – V_{SS}	Supply voltage		110	V
V_{DD}		– 0.5	110	V
V_{SS}		– 110	0.5	V
V_{SELx}	Logic control input pin voltage (SELx)	– 0.5	50	V
I_{SELx}	Logic control input pin current (SELx)	– 30	30	mA
V_S or V_D	Source or drain voltage (Sx, Dx)	V_{SS} – 2	V_{DD}+2	V
I_{DC}	Source or drain continuous current (Sx, Dx)	– 200	200	mA
I_{IK} (2)	Diode clamp current at 85°C	– 100	100	mA
	Diode clamp current at 125°C	– 15	15	mA
T_{stg}	Storage temperature	– 65	150	°C
T_A	Ambient temperature	– 55	150	°C
T_J	Junction temperature		150	°C
P_{tot} (3)	Total power dissipation (QFN)		1680	mW
P_{tot} (4)	Total power dissipation (TSSOP)		720	mW

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Signal path pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(3) For QFN package: P_{tot} derates linearly above T_A = 70°C by 24.0 mW/°C
(4) For TSSOP package: P_{tot} derates linearly above T_A = 70°C by 10.5 mW/°C

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions: TMUX821x Devices

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD} – V_{SS} (1)	Power supply voltage differential	10		100	V
V_{DD}	Positive power supply voltage	10		100	V
V_S or V_D (2)	Signal path input/output voltage (source or drain pin)	V_{SS}		V_{DD}	V
V_{SEL}	Logic input pin voltage	0		48	V
T_A	Ambient temperature	– 40		125	°C
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)			I_{DC} (3)	mA

(1) V_{DD} and V_{SS} can be any value as long as 10 V ≤ (V_{DD} – V_{SS}) ≤ 100 V, and the minimum V_{DD} is met.
(2) V_S or V_D is the voltage on any Source or Drain pins.
(3) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.

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7.4 漏极持续电流源

在自然通风条件下的工作温度范围内测得（除非另有说明）

	封装			最小值	标称值	最大值	单位
I_{DC} 1 通道 (1)	PW (TSSOP) RUM (WQFN)	流经 1 通道的开关的连续电流	T_A = 25°C			200	mA
			T_A = 85°C			200	
			T_A = 125°C			200	
I_{DC} 全通道 (2)	PW (TSSOP)	同时流经所有通道上的开关的连续电流	T_A = 25°C			185	mA
			T_A = 85°C			125	
			T_A = 125°C			65	
I_{DC} 全通道 (2)	RUM (WQFN)	同时流经所有通道上的开关的连续电流	T_A = 25°C			200	mA
			T_A = 85°C			190	
			T_A = 125°C			100	

(1) 每次显示单个通道的最大连续电流。
(2) 每次显示所有通道的最大连续电流。请参阅最大功耗 (P_{tot}) 以确保不违反封装限制。

7.5 漏极脉冲电流源

在自然通风条件下的工作温度范围内测得（除非另有说明）

	封装			最小值	标称值	最大值	单位
I_{DC} 1 通道 (1)	PW (TSSOP)	(3)流经 1 通道上开关的脉冲电流	T_A = 25°C			370	mA
			T_A = 85°C			310	
			T_A = 125°C			240	
I_{DC} 全通道 (2)	PW (TSSOP)	(3)同时流经所有通道上的开关的脉冲电流	T_A = 25°C			185	mA
			T_A = 85°C			155	
			T_A = 125°C			120	
I_{DC} 1 通道 (1)	RUM (WQFN)	(3)流经 1 通道上开关的脉冲电流	T_A = 25°C			560	mA
			T_A = 85°C			470	
			T_A = 125°C			365	
I_{DC} 全通道 (2)	RUM (WQFN)	(3)同时流经所有通道上的开关的脉冲电流	T_A = 25°C			280	mA
			T_A = 85°C			235	
			T_A = 125°C			180	

(1) 每次显示单个通道的最大连续电流。
(2) 每次显示所有通道的最大连续电流。请参阅最大功耗 (P_{tot}) 以确保不违反封装限制。
(3) 在 1ms、10% 占空比时发出脉冲

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7.6 Thermal Information

THERMAL METRIC(1)		TMUX821x PW (TSSOP) 16 PINS	TMUX821x RUM (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	96.0	41.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.8	25.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.7	16.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.2	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	42.0	16.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	3.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.7 Electrical Characteristics (Global): TMUX821x Devices

over operating free-air temperature range (unless otherwise noted)
typical at V_{DD} = +36 V, V_{SS} = – 36 V, GND = 0 V and T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
LOGIC INPUTS							
V_{IH}	Logic voltage high		– 40°C to +125°C	1.3		48	V
V_{IL}	Logic voltage low		– 40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current	Logic inputs = 0 V, 5 V, or 48 V	– 40°C to +125°C		0.4	3.8	µA
I_{IL}	Input leakage current	Logic inputs = 0 V, 5 V, or 48 V	– 40°C to +125°C	– 0.2	– 0.005		µA
C_{IN}	Logic input capacitance		– 40°C to +125°C		3		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V, 5 V, or 48 V	25°C		350	800	µA
			– 40°C to +85°C			800	µA
			– 40°C to +125°C			900	µA
I_{SS}	V_{SS} supply current	Logic inputs = 0 V, 5 V, or 48 V	25°C		350	800	µA
			– 40°C to +85°C			800	µA
			– 40°C to +125°C			900	µA

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7.8 Electrical Characteristics (±15-V Dual Supply)

V_{DD} = +15 V ± 10%, V_{SS} = – 15 V ± 10%, GND = 0 V (unless otherwise noted)
Typical at T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = – 10 V to +10 V I_D = – 10 mA	25°C		5	7	Ω
			– 40°C to +85°C			8	
			– 40°C to +125°C			10	
ΔR_{ON}	On-resistance mismatch between channels	V_S = – 10 V to +10 V I_D = – 10 mA	25°C		0.2	0.3	Ω
			– 40°C to +85°C			0.4	
			– 40°C to +125°C			0.5	
$R_{ON\ FLAT}$	On-resistance flatness	V_S = – 10 V to +10 V I_D = – 10 mA	25°C		0.07		Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = – 10 mA	– 40°C to +125°C		0.03		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 16.5 V, V_{SS} = – 16.5 V Switch state is off V_S = +10 V / – 10 V V_D = – 10 V / +10 V	25°C		0.01		nA
			– 40°C to +85°C	– 4		4	
			– 40°C to +125°C	– 40		40	
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 16.5 V, V_{SS} = – 16.5 V Switch state is off V_S = +10 V / – 10 V V_D = – 10 V / +10 V	25°C		0.01		nA
			– 40°C to +85°C	– 4		4	
			– 40°C to +125°C	– 40		40	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 16.5 V, V_{SS} = – 16.5 V Switch state is on V_S = V_D = ±10 V	25°C		0.01		nA
			– 40°C to +85°C	– 1		1	
			– 40°C to +125°C	– 2		2	
$\Delta I_{S(ON)}$ $\Delta I_{D(ON)}$	Leakage current mismatch between channels(2)	V_{DD} = 16.5 V, V_{SS} = – 16.5 V Switch state is on V_S = V_D = ±10 V	25°C		5		pA
			85°C		35		
			125°C		120		

(1) When V_S is positive,V_D is negative. And when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating. And when V_D is at a voltage potential, V_S is floating.

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7.9 Electrical Characteristics (±36-V Dual Supply)

V_{DD} = +36 V ± 10%, V_{SS} = – 36 V ± 10%, GND = 0 V (unless otherwise noted)
Typical at T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = – 25 V to +25 V I_D = – 10 mA	25°C		5	7	Ω
			– 40°C to +85°C			8	
			– 40°C to +125°C			10	
ΔR_{ON}	On-resistance mismatch between channels	V_S = – 25 V to +25 V I_D = – 10 mA	25°C		0.1	0.3	Ω
			– 40°C to +85°C			0.4	
			– 40°C to +125°C			0.5	
$R_{ON\ FLAT}$	On-resistance flatness	V_S = – 25 V to +25 V I_D = – 10 mA	25°C		0.12		Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = – 10 mA	– 40°C to +125°C		0.03		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 39.6 V, V_{SS} = – 39.6 V Switch state is off V_S = +25 V / – 25 V V_D = – 25 V / +25 V	25°C		0.01		nA
			– 40°C to +85°C	– 4		4	
			– 40°C to +125°C	– 40		40	
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 39.6 V, V_{SS} = – 39.6 V Switch state is off V_S = +25 V / – 25 V V_D = – 25 V / +25 V	25°C		0.01		nA
			– 40°C to +85°C	– 4		4	
			– 40°C to +125°C	– 40		40	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 39.6 V, V_{SS} = – 39.6 V Switch state is on V_S = V_D = ±25 V	25°C		0.01		nA
			– 40°C to +85°C	– 1		1	
			– 40°C to +125°C	– 2		2	
$\Delta I_{S(ON)}$ $\Delta I_{D(ON)}$	Leakage current mismatch between channels(2)	V_{DD} = 39.6 V, V_{SS} = – 39.6 V Switch state is on V_S = V_D = ±25 V	25°C		5		pA
			85°C		35		
			125°C		120		

(1) When V_S is positive,V_D is negative. And when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating. And when V_D is at a voltage potential, V_S is floating.

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7.10 Electrical Characteristics (±50-V Dual Supply)

V_{DD} = +50 V, V_{SS} = – 50 V, GND = 0 V (unless otherwise noted)
Typical at T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = – 45 V to 45 V I_D = – 10 mA	25°C		5	7	Ω
			– 40°C to +85°C			8	
			– 40°C to +125°C			10	
ΔR_{ON}	On-resistance mismatch between channels	V_S = – 45 V to 45 V I_D = – 10 mA	25°C		0.2	0.3	Ω
			– 40°C to +85°C			0.4	
			– 40°C to +125°C			0.5	
$R_{ON\ FLAT}$	On-resistance flatness	V_S = – 45 V to 45 V I_D = – 10 mA	25°C		0.13		Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = – 10 mA	– 40°C to +125°C		0.03		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 50 V, V_{SS} = – 50 V Switch state is off V_S = +45 V / – 45 V V_D = – 45 V / +45 V	25°C		0.01		nA
			– 40°C to +85°C	– 4		4	
			– 40°C to +125°C	– 40		40	
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 50 V, V_{SS} = – 50 V Switch state is off V_S = +45 V / – 45 V V_D = – 45 V / +45 V	25°C		0.01		nA
			– 40°C to +85°C	– 4		4	
			– 40°C to +125°C	– 40		40	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 50 V, V_{SS} = – 50 V Switch state is on V_S = V_D = ±45 V	25°C		0.01		nA
			– 40°C to +85°C	– 2		2	
			– 40°C to +125°C	– 5		5	
$\Delta I_{S(ON)}$ $\Delta I_{D(ON)}$	Leakage current mismatch between channels(2)	V_{DD} = 50 V, V_{SS} = – 50 V Switch state is on V_S = V_D = ±45 V	25°C		10		pA
			85°C		50		
			125°C		220		

(1) When V_S is positive,V_D is negative. And when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating. And when V_D is at a voltage potential, V_S is floating.

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7.11 Electrical Characteristics (72-V Single Supply)

V_{DD} = +72 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 60 V I_D = –10 mA	25°C		5	7	Ω
			–40°C to +85°C			8	
			–40°C to +125°C			10	
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 60 V I_D = –10 mA	25°C		0.2	0.3	Ω
			–40°C to +85°C			0.4	
			–40°C to +125°C			0.5	
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to 60 V I_D = –10 mA	25°C		0.05		Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA	–40°C to +125°C		0.03		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	Switch state is off V_S = +60 V / 1 V V_D = 1 V / +60 V	25°C		0.01		nA
			–40°C to +85°C	–4		4	
			–40°C to +125°C	–40		40	
$I_{D(OFF)}$	Drain off leakage current(1)	Switch state is off V_S = +60 V / 1 V V_D = 1 V / +60 V	25°C		0.01		nA
			–40°C to +85°C	–4		4	
			–40°C to +125°C	–40		40	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	Switch state is on V_S = V_D = 1 V / +60 V	25°C		0.01		nA
			–40°C to +85°C	–2		2	
			–40°C to +125°C	–5		5	
$\Delta I_{S(ON)}$ $\Delta I_{D(ON)}$	Leakage current mismatch between channels(2)	Switch state is on V_S = V_D = 1 V / +60 V	25°C		15		pA
			85°C		75		
			125°C		300		

(1) When V_S is 60 V, V_D is 1 V. Or when V_S is 1 V, V_D is 60 V.
(2) When V_S is at a voltage potential, V_D is floating. Or when V_D is at a voltage potential, V_S is floating.

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7.12 Electrical Characteristics (100-V Single Supply)

V_{DD} = +100 V, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to +95 V I_D = –10 mA	25°C		5	7	Ω
			–40°C to +85°C			8	
			–40°C to +125°C			10	
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to +95 V I_D = –10 mA	25°C		0.2	0.3	Ω
			–40°C to +85°C			0.4	
			–40°C to +125°C			0.5	
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to +95 V I_D = –10 mA	25°C		0.07		Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 50 V, I_S = –10 mA	–40°C to +125°C		0.03		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	Switch state is off V_S = +95 V / 1 V V_D = 1 V / +95 V	25°C		0.01		nA
			–40°C to +85°C	–4		4	
			–40°C to +125°C	–40		40	
$I_{D(OFF)}$	Drain off leakage current(1)	Switch state is off V_S = +95 V / 1 V V_D = 1 V / +95 V	25°C		0.01		nA
			–40°C to +85°C	–4		4	
			–40°C to +125°C	–40		40	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	Switch state is on V_S = V_D = 1 V / +95 V	25°C		0.01		nA
			–40°C to +85°C	–4		4	
			–40°C to +125°C	–10		10	
$\Delta I_{S(ON)}$ $\Delta I_{D(ON)}$	Leakage current mismatch between channels(2)	Switch state is on V_S = V_D = 1 V / +95 V	25°C		15		pA
			85°C		100		
			125°C		450		

(1) When V_S is 95 V, V_D is 1 V. Or when V_S is 1 V, V_D is 95 V.
(2) When V_S is at a voltage potential, V_D is floating. Or when V_D is at a voltage potential, V_S is floating.

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7.13 Switching Characteristics: TMUX821x Devices

over operating free-air temperature range (unless otherwise noted)
typical at V_{DD} = +36 V, V_{SS} = – 36 V, GND = 0 V and T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 10 V R_L = 10 kΩ, C_L = 15 pF	25°C		4		µs
			– 40°C to +85°C			10	
			– 40°C to +125°C			12	
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 10 V R_L = 10 kΩ, C_L = 15 pF	25°C		100		ns
			– 40°C to +85°C			600	
			– 40°C to +125°C			700	
$t_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} ramp rate = 1 V/µs, V_S = 10 V R_L = 10 kΩ, C_L = 15pF	25°C		60		µs
t_{PD}	Propagation delay	R_L = 50 Ω, C_L = 5 pF	25°C		190		ps
Q_{INJ}	Charge injection	V_S = (V_{DD} + V_{SS}) / 2, C_L = 1 nF	25°C		– 1.3		nC
O_{ISO}	Off isolation	R_L = 50 Ω, C_L = 5 pF V_S = (V_{DD} + V_{SS}) / 2, f = 100 kHz	25°C		– 110		dB
X_{TALK}	Inter-channel crosstalk	R_L = 50 Ω, C_L = 5 pF V_S = (V_{DD} + V_{SS}) / 2, f = 100 kHz	25°C		– 110		dB
BW	– 3 dB bandwidth	R_L = 50 Ω, C_L = 5 pF V_S = (V_{DD} + V_{SS}) / 2	25°C		420		MHz
I_L	Insertion loss	R_L = 50 Ω, C_L = 5 pF V_S = (V_{DD} + V_{SS}) / 2, f = 1 MHz	25°C		– 0.4		dB
THD+N	Total harmonic distortion + Noise	Dual supply voltage V_{PP} = 5 V, V_{BIAS} = (V_{DD} + V_{SS}) / 2 R_L = 1 kΩ, C_L = 5 pF, f = 20 Hz to 20 kHz	25°C		0.0008		%
$C_{S(OFF)}$	Source off capacitance	V_S = (V_{DD} + V_{SS}) / 2 V, f = 1 MHz	25°C		12		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = (V_{DD} + V_{SS}) / 2 V, f = 1 MHz	25°C		12		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = (V_{DD} + V_{SS}) / 2 V, f = 1 MHz	25°C		14		pF

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7.14 Typical Characteristics

at T_A = 25°C, V_{DD} = +36 V, and V_{SS} = – 36 V (unless otherwise noted)

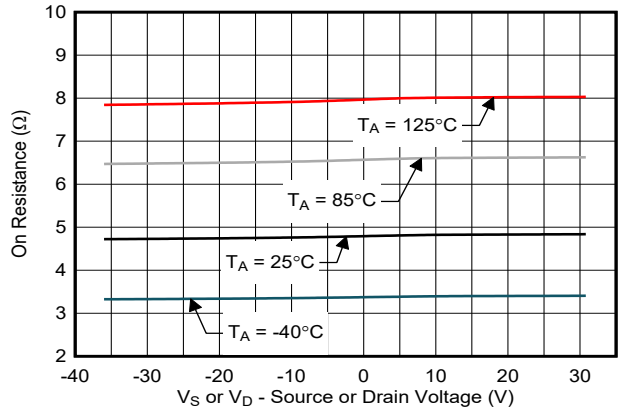

图 7-1. On-Resistance vs Source or Drain Voltage

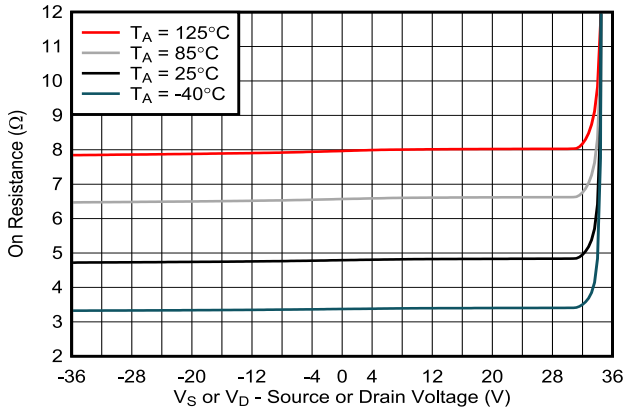

图 7-2. On-Resistance vs Source or Drain Voltage

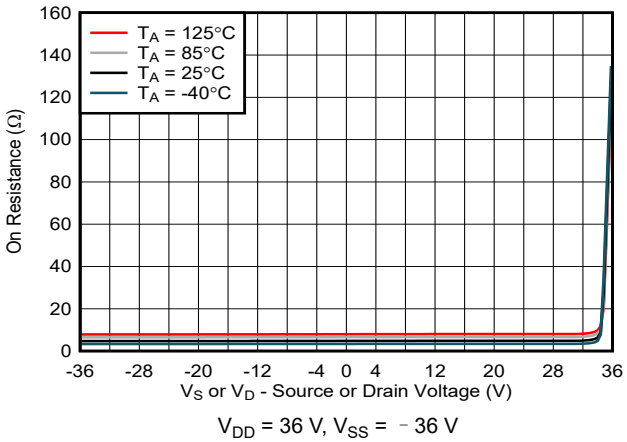

图 7-3. On-Resistance vs Source or Drain Voltage

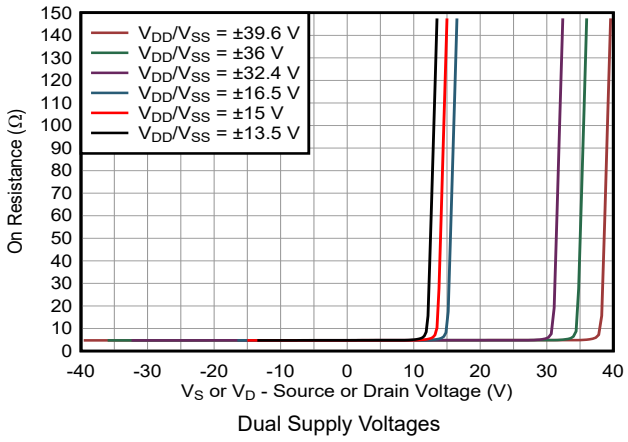

图 7-4. On-Resistance vs Source or Drain Voltage

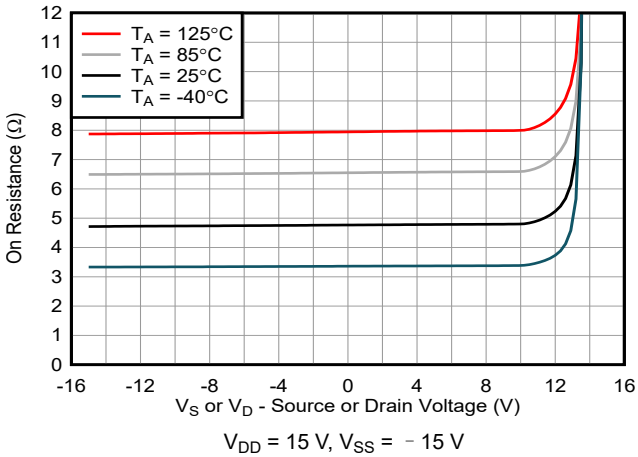

图 7-5. On-Resistance vs Source or Drain Voltage

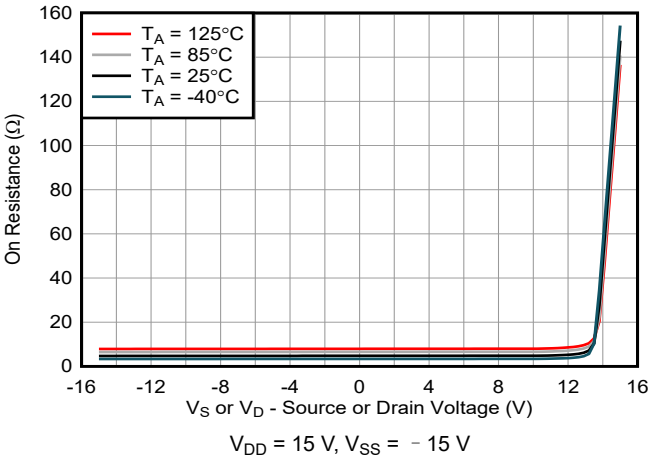

图 7-6. On-Resistance vs Source or Drain Voltage

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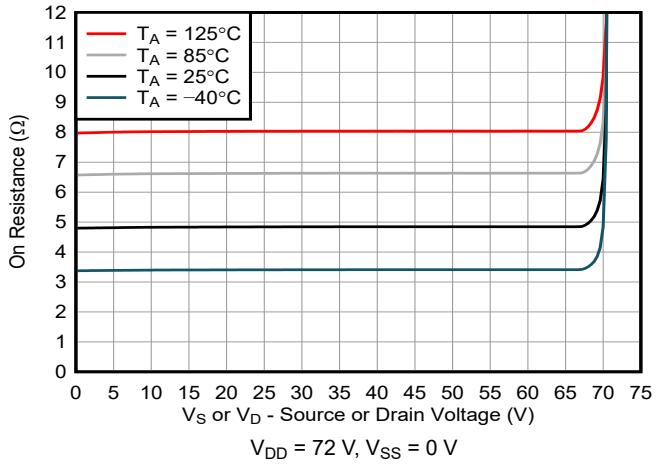
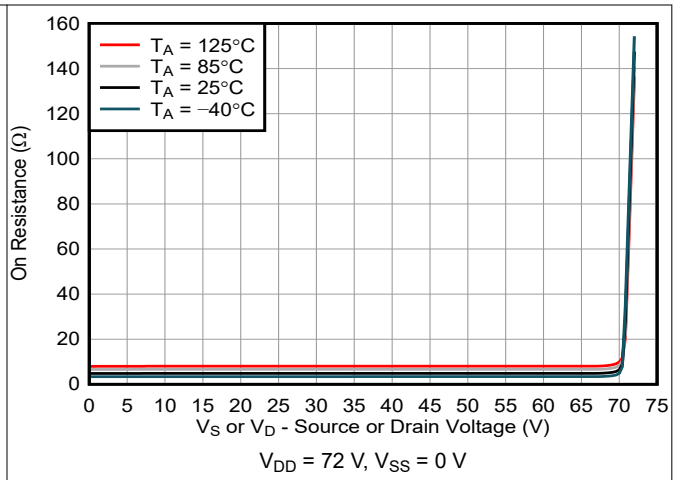
7.14 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = +36 V, and V_{SS} = – 36 V (unless otherwise noted)



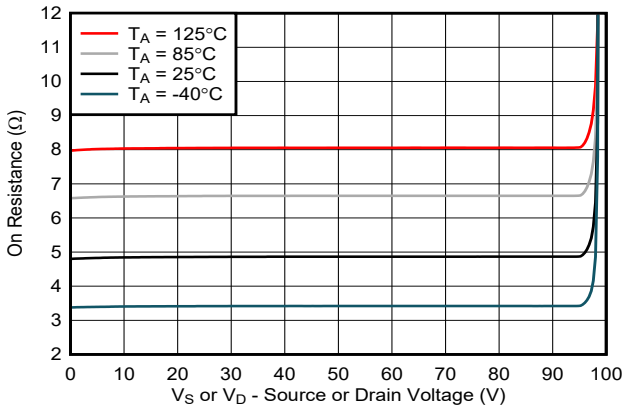
V_{DD} = 72 V, V_{SS} = 0 V

图 7-7. On-Resistance vs Source or Drain Voltage



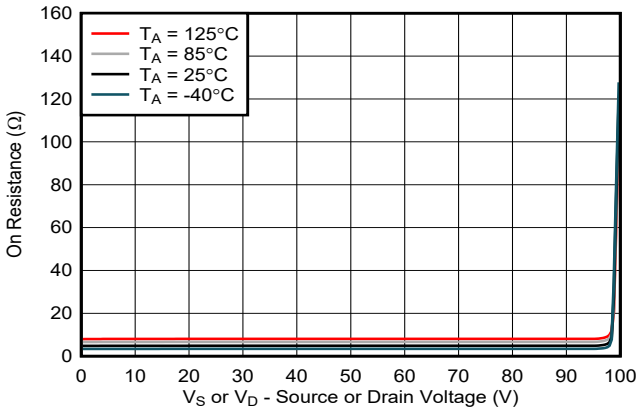
V_{DD} = 72 V, V_{SS} = 0 V

图 7-8. On-Resistance vs Source or Drain Voltage



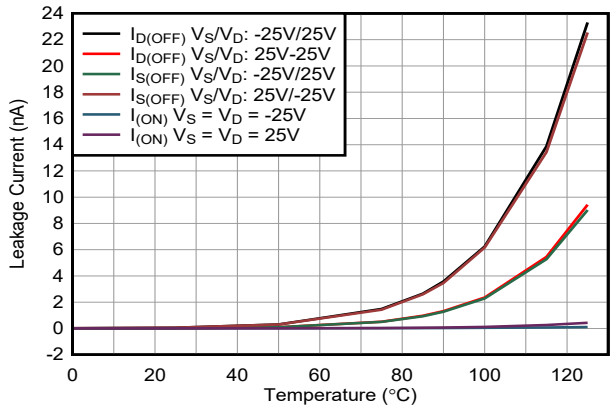
V_{DD} = 100 V, V_{SS} = 0 V

图 7-9. On-Resistance vs Source or Drain Voltage



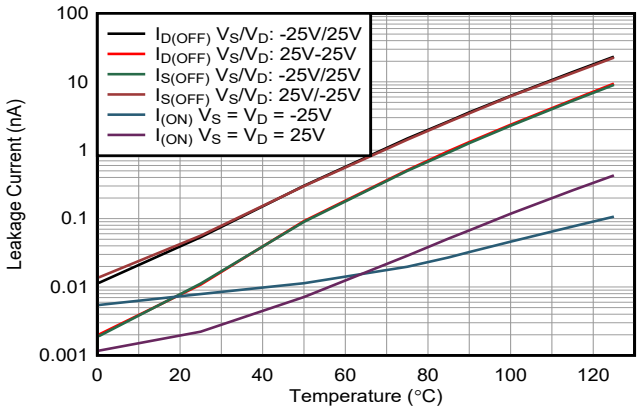
V_{DD} = 100 V, V_{SS} = 0 V

图 7-10. On-Resistance vs Source or Drain Voltage



V_{DD} = 36 V, V_{SS} = – 36 V

图 7-11. Leakage Current vs Temperature



V_{DD} = 36 V, V_{SS} = – 36 V

图 7-12. Leakage Current vs Temperature

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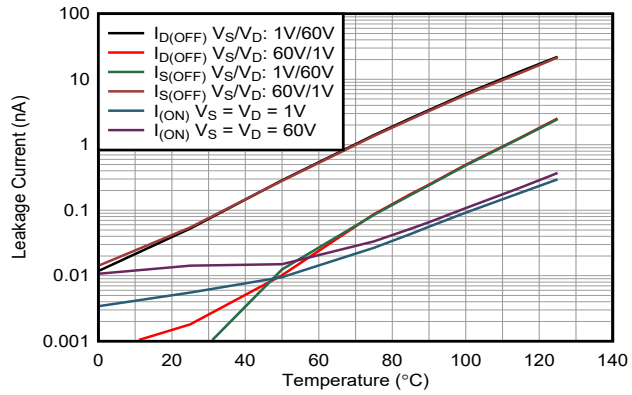
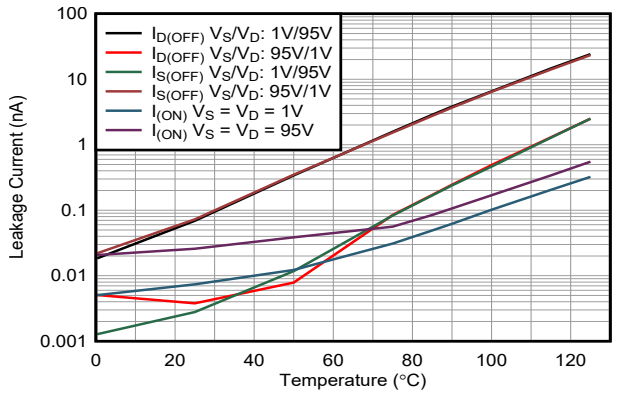
7.14 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = +36 V, and V_{SS} = – 36 V (unless otherwise noted)



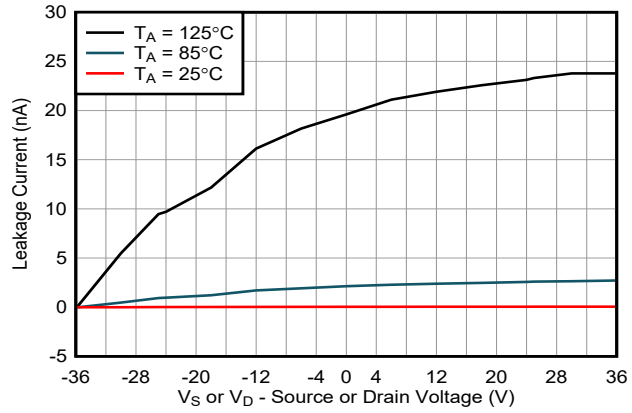
V_{DD} = 72 V, V_{SS} = 0 V

图 7-13. Leakage Current vs Temperature



V_{DD} = 100 V, V_{SS} = 0 V

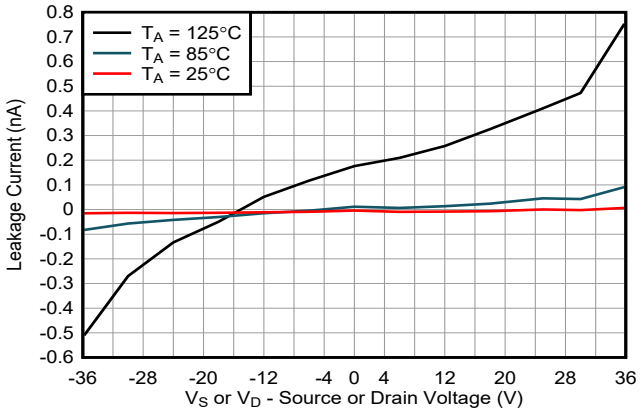
图 7-14. Leakage Current vs Temperature



V_{DD} = 36 V, V_{SS} = – 36 V

$I_{S(OFF)}$ and $I_{D(OFF)}$

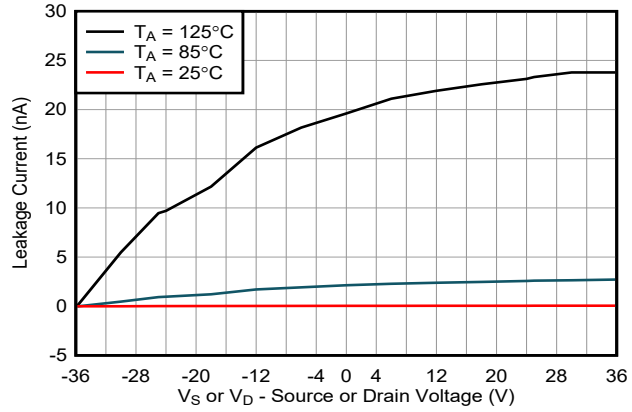
图 7-15. Off-Leakage Current vs Source or Drain Voltage



V_{DD} = 36 V, V_{SS} = – 36 V

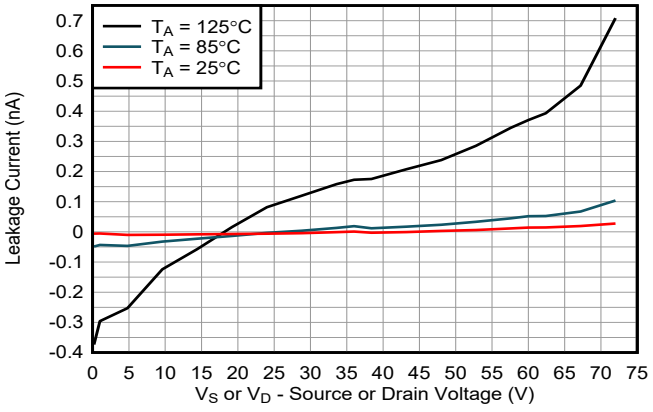
I_{ON}

图 7-16. On-Leakage Current vs Source or Drain Voltage



V_{DD} = 72 V, V_{SS} = 0 V

图 7-17. Off-Leakage Current vs Source or Drain Voltage



V_{DD} = 72 V, V_{SS} = 0 V

图 7-18. On-Leakage Current vs Source or Drain Voltage

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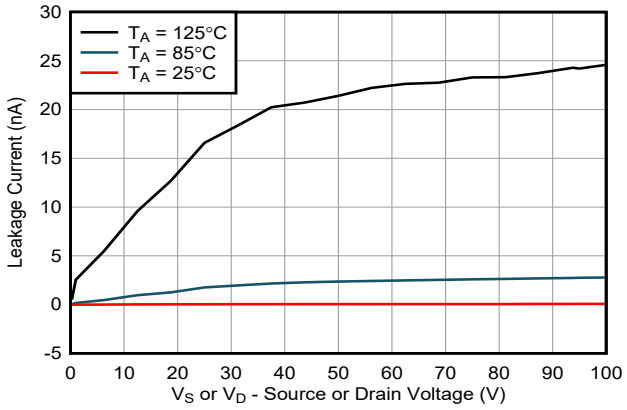
7.14 Typical Characteristics (continued)

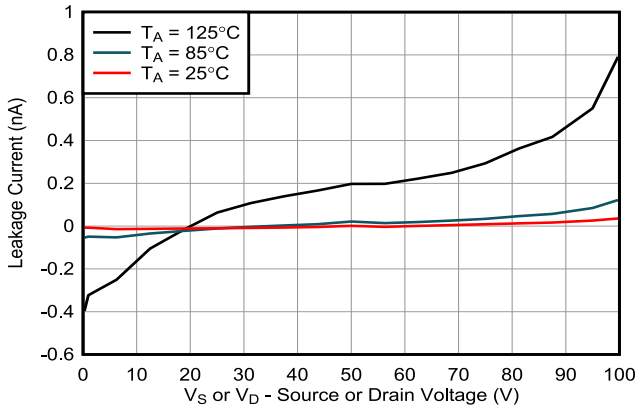
at T_A = 25°C, V_{DD} = +36 V, and V_{SS} = – 36 V (unless otherwise noted)



V_{DD} = 100 V, V_{SS} = 0 V

$I_{S(OFF)}$ and $I_{D(OFF)}$

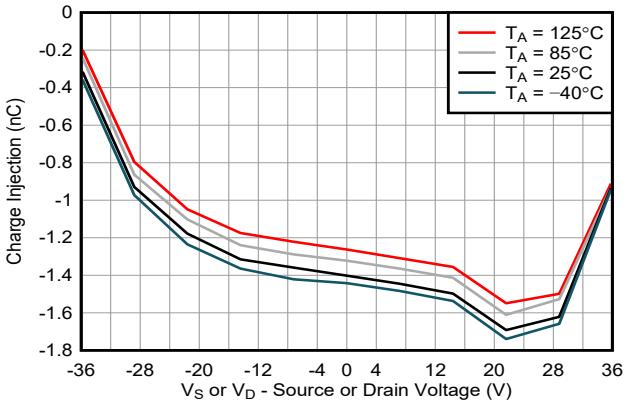
图 7-19. Off-Leakage Current vs Source or Drain Voltage



V_{DD} = 100 V, V_{SS} = 0 V

I_{ON}

图 7-20. On-Leakage Current vs Source or Drain Voltage



V_{DD} = 36 V, V_{SS} = – 36 V

图 7-21. Charge Injection vs Source Voltage

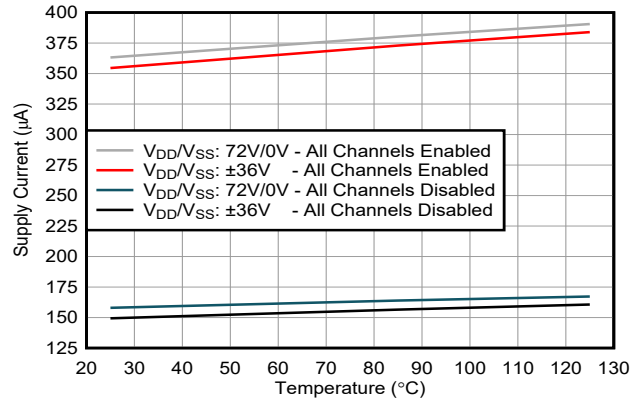
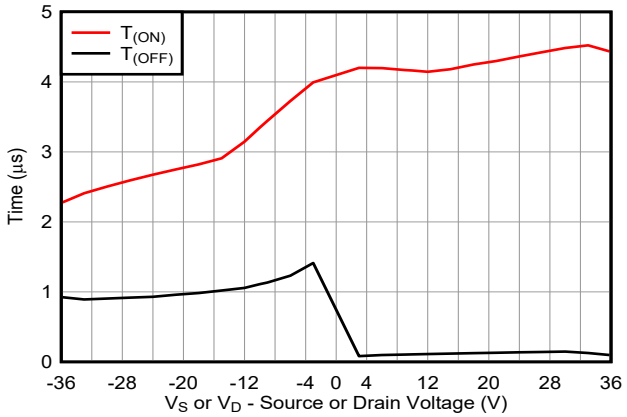
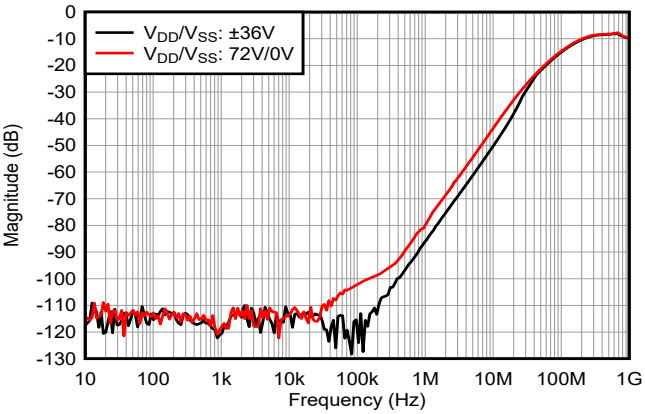


图 7-22. Supply Current vs Temperature



V_{DD} = 36 V, V_{SS} = – 36 V

图 7-23. Turn-On and Turn-Off Times vs Source Voltage



T_A = 25°C

图 7-24. Off Isolation vs Frequency

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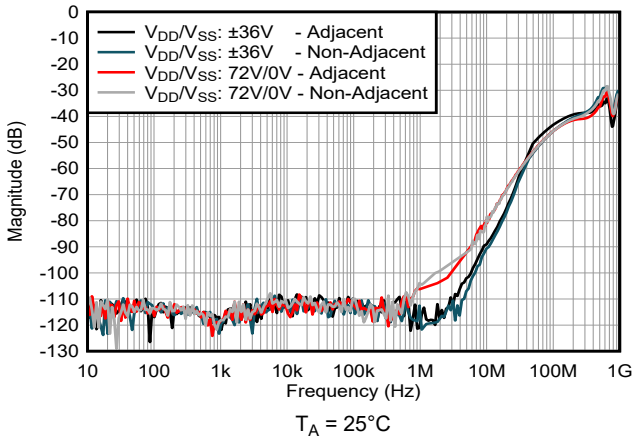
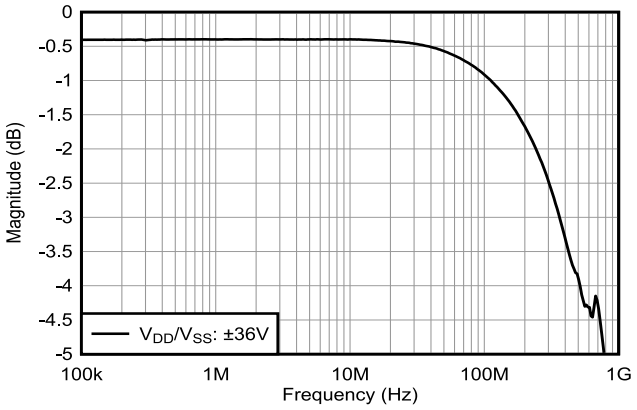
7.14 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = +36 V, and V_{SS} = – 36 V (unless otherwise noted)



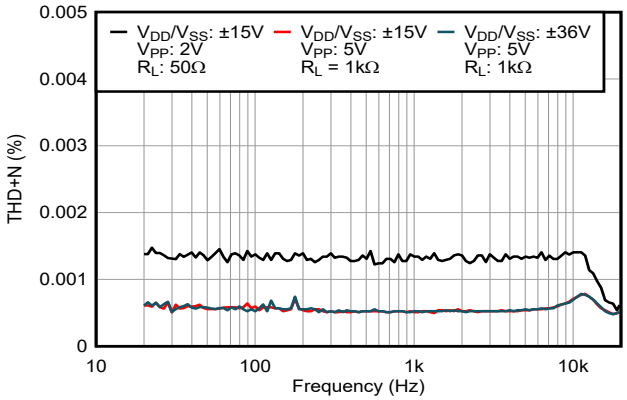
T_A = 25°C

图 7-25. Crosstalk vs Frequency



Bandwidth

图 7-26. Insertion Loss vs Frequency



T_A = 25°C

图 7-27. THD+N vs Frequency

8 Parameter Measurement Information

8.1 On-Resistance

The On-Resistance of the TMUX821x is the ohmic resistance across the source (Sx) and drain (Dx) pins of the device. The On-Resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote On-Resistance. 图 8-1 shows the measurement setup used to measure R_{ON}. ΔR_{ON} represents the difference between the R_{ON} of any two channels, while R_{ON_FLAT} denotes the flatness that is defined as the difference between the maximum and minimum value of On-Resistance measured over the specified analog signal range.

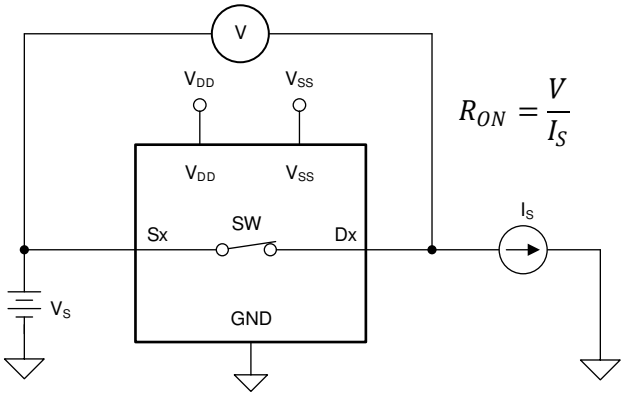


图 8-1. On-Resistance Measurement Setup

8.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source Off-Leakage current $I_{S(OFF)}$: the leakage current flowing into or out of the source pin when the switch is off.
2. Drain Off-Leakage current $I_{D(OFF)}$: the leakage current flowing into or out of the drain pin when the switch is off.

图 8-2 shows the setup used to measure both Off-Leakage currents.

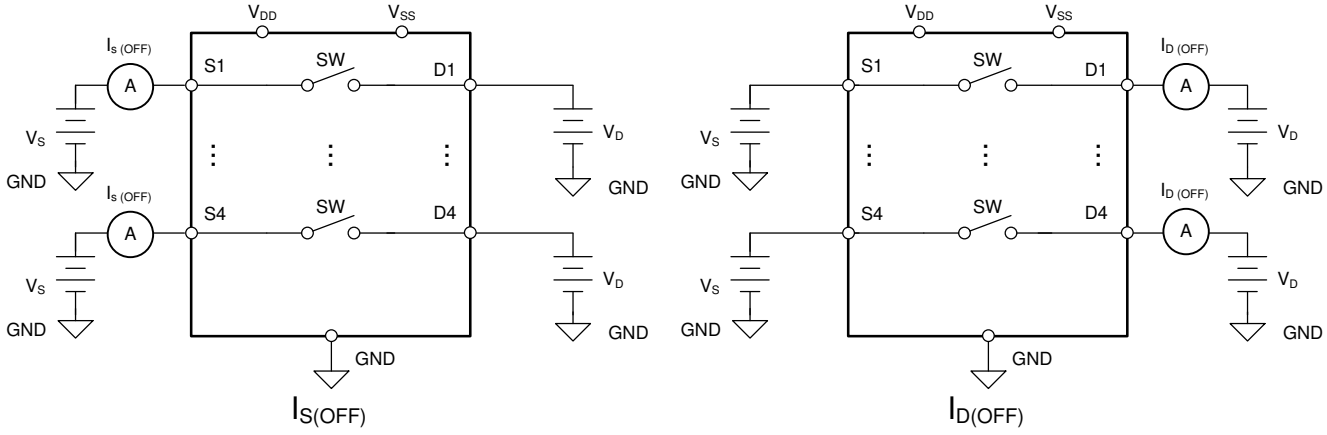


图 8-2. Off-Leakage Measurement Setup

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8.3 On-Leakage Current

Source On-Leakage current ($I_{S(ON)}$) and drain On-Leakage current ($I_{D(ON)}$) denote the channel leakage currents when the switch is in the on state. $I_{S(ON)}$ is measured with the drain floating, while $I_{D(ON)}$ is measured with the source floating. 图 8-3 shows the circuit used for measuring the On-Leakage currents.

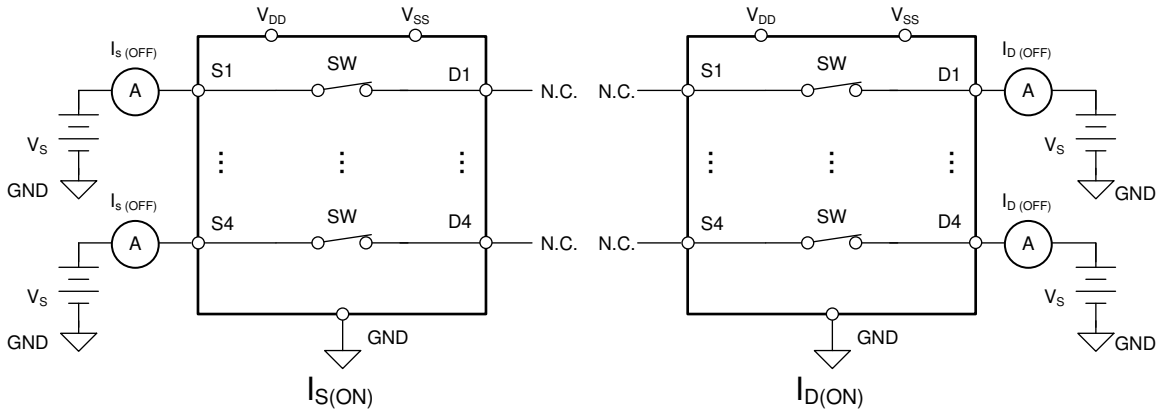

图 8-3. On-Leakage Measurement Setup

8.4 Device Turn-On and Turn-Off Time

Turn-On time (t_{ON}) is defined as the time taken by the output of the TMUX8211, TMUX8212, and TMUX8213 to rise to a 90% final value after the SELx signal has risen (for NC switches) or fallen (for NO switches) to a 50% final value. Turn-Off time (t_{OFF}) is defined as the time taken by the output of the TMUX8211, TMUX8212, and TMUX8213 to fall to a 10% initial value after the SELx signal has fallen (for NC switches) or risen (for NO switches) to a 50% initial value. 图 8-4 shows the setup used to measure t_{ON} and t_{OFF}.

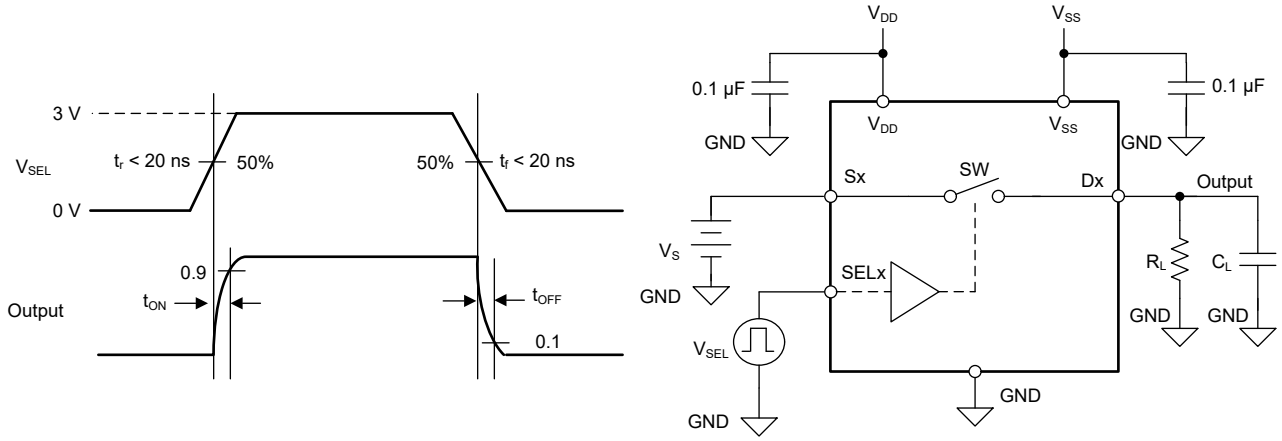

图 8-4. Enable Delay Measurement Setup

8.5 Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching, and is denoted by the symbol Q_{INJ}. 图 8-5 shows the setup used to measure charge injection from the source to drain.

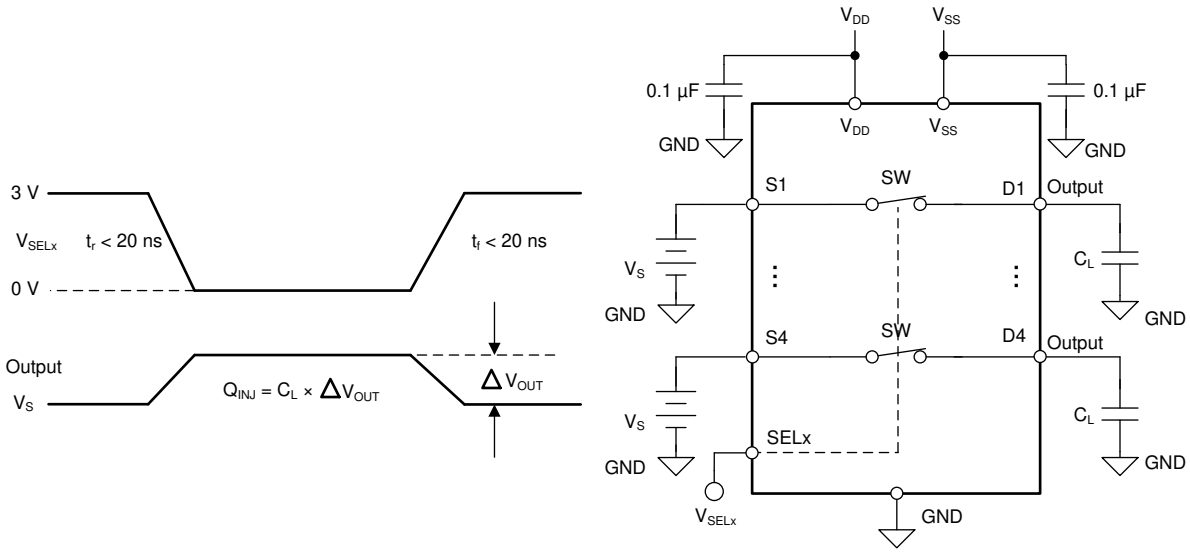

图 8-5. Charge-Injection Measurement Setup

8.6 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. The characteristic impedance, Z_O, for the measurement is 50 Ω. 图 8-6 and 方程式 1 shows the setup used to measure off isolation.

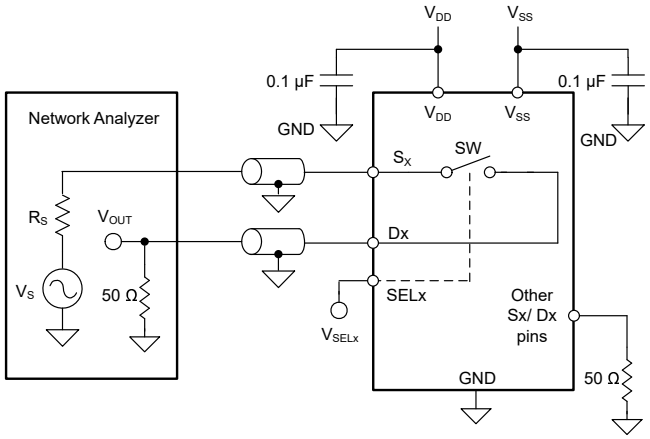

图 8-6. Off Isolation Measurement Setup

$$Off\ Isolation = 20 \times Log \frac{V_{OUT}}{V_S} \quad (1)$$

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8.7 Crosstalk

Crosstalk (X_{TALK}) is defined as the ratio of the signal at the drain pin (Dx) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. The characteristic impedance, Z_O, for the measurement is 50 Ω, as shown in 图 8-7 and 方程式 2.

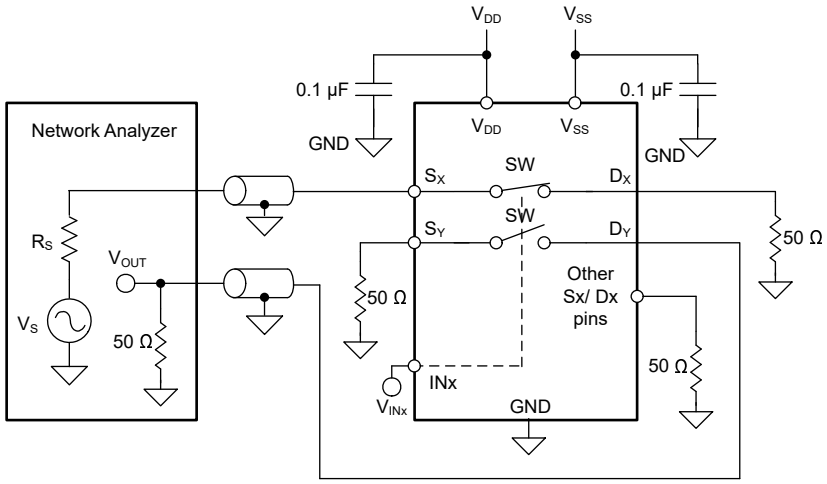

图 8-7. Inter-channel Crosstalk Measurement Setup

$$Inter-channel\ Crosstalk\ =\ 20\ \times\ Log\ \frac{V_{OUT}}{V_S} \tag{2}$$

8.8 Bandwidth

Bandwidth (BW) is defined as the range of frequencies that are attenuated by < 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (Dx). 图 8-8 and 方程式 3 shows the setup used to measure bandwidth of the switch.

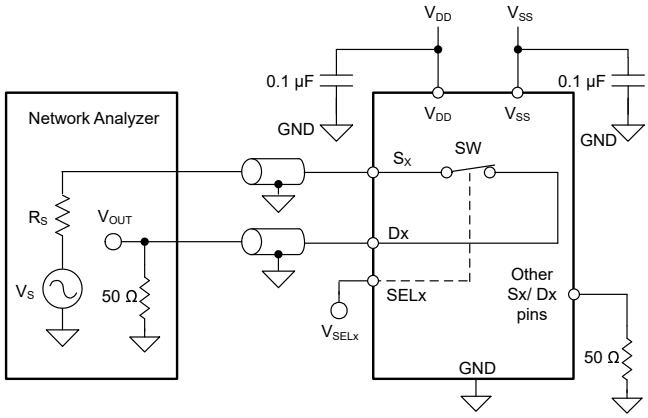

图 8-8. Bandwidth Measurement Setup

$$Bandwidth\ =\ 20\ \times\ Log\ \frac{V_{OUT}}{V_S} \tag{3}$$

8.9 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the multiplexer output. The On-Resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N. 图 8-9 shows the setup used to measure THD+N of the devices.

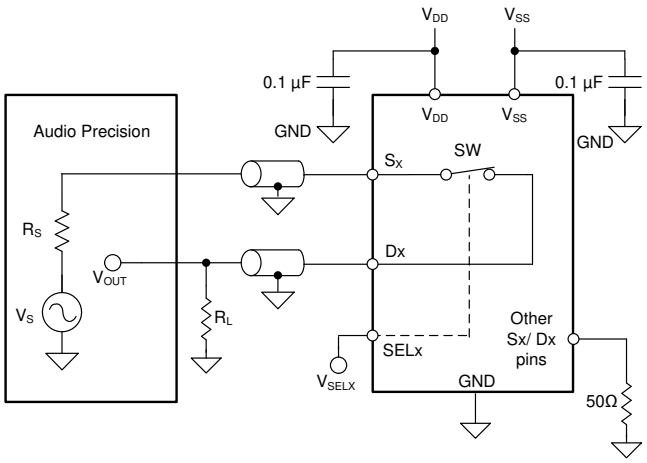

图 8-9. THD+N Measurement Setup

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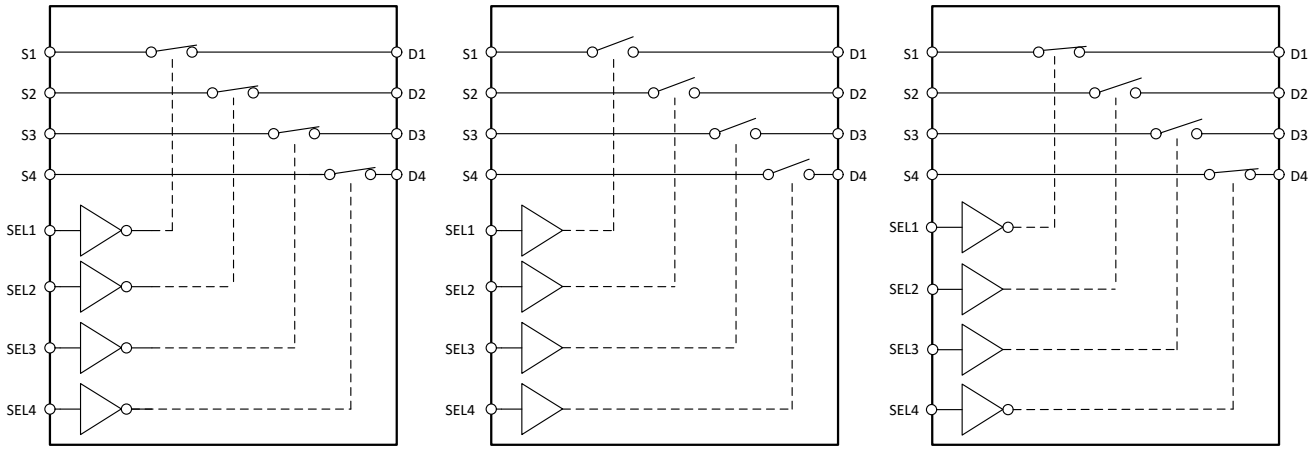
9 Detailed Description

9.1 Overview

The TMUX8211, TMUX8212 and TMUX8213 are a modern complementary metal-oxide semiconductor (CMOS) analog switches in quad single-pole single-throw configuration. The devices work well with dual supplies, a single supply, or asymmetric supplies.

9.2 Functional Block Diagram



TMUX8211 TMUX8212 TMUX8213

ALL SWITCHES SHOWN FOR A LOGIC 0 INPUT

9.3 Feature Description

9.3.1 Bidirectional Operation

The devices conduct equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each signal path has similar characteristics in both directions.

9.3.2 Flat On-Resistance

The TMUX821x devices are designed with a special switch architecture to produce ultra-flat On-Resistance (R_{ON}) across most of the switch input operating region. The flat R_{ON} response allows the device to be used in precision sensor applications since the R_{ON} is controlled regardless of the signals sampled. The architecture is implemented without a charge pump so no unwanted noise is produced from the device to affect sampling accuracy.

The flattest On-Resistance region extends from V_{SS} to roughly 5 V below V_{DD}. Once the signal is within 5 V of V_{DD} the On-Resistance will exponentially increase and may impact desired signal transmission.

9.3.3 Protection Features

These devices offer a number of protection features to enable robust system implementations.

9.3.3.1 Fail-Safe Logic

Fail-safe logic circuitry allows voltages on the logic control pins to be applied before the supply pins, protecting the device from potential damage. Additionally the fail safe logic feature allows the logic inputs of the mux to be interfaced with high voltages, allowing for simplified interfacing if only high voltage control signals are present. The logic inputs are protected against positive faults of up to +48 V in powered-off condition, but do not offer protection against negative over-voltage condition.

Fail-safe logic also allows the devices to interface with a voltage greater than V_{DD} on the control pins during normal operation to add maximum flexibility in system design. For example, with a V_{DD} = 15 V, the logic control pins could be connected to +24 V for a logic high signal which allows different types of signals, such as analog feedback voltages, to be used when controlling the logic inputs. Regardless of the supply voltage, the logic inputs can be interfaced as high as 48 V.

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9.3.3.2 ESD Protection

All pins support HBM ESD protection level up to ±2 kV, which helps protect the devices from ESD events during the manufacturing process.

9.3.3.3 Latch-Up Immunity

Latch-Up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or over-voltage), but once activated the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The Latch-Up condition typically requires a power cycle to eliminate the low impedance path.

In the TMUX821x devices, an insulating oxide layer is placed on top of the silicon substrate to prevent any parasitic junctions from forming. As a result, the devices are Latch-Up immune under all circumstances by device construction.

The TMUX821x devices are constructed on silicon on insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to over-voltage or current injections. The Latch-Up immunity feature allows the TMUX821x to be used in harsh environments. For more information on Latch-Up immunity, refer to *Using Latch Up Immune Multiplexers to Help Improve System Reliability*.

9.3.4 1.8 V Logic Compatible Inputs

The TMUX821x devices have 1.8 V logic compatible control for all logic control inputs. 1.8 V logic level inputs allows the TMUX821x to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations, refer to *Simplifying Design with 1.8 V logic Muxes and Switches*.

9.3.5 Integrated Pull-Down Resistor on Logic Pins

The TMUX821x have internal weak Pull-Down resistors to GND to ensure the logic pins are not left floating. The value of this Pull-Down resistor is approximately 4 MΩ, but is clamped to 1 µA at higher voltages. This feature integrates up to four external components and reduces system size and cost.

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9.4 Device Functional Modes

9.4.1 Normal Mode

In Normal Mode operation, signals of up to V_{DD} and V_{SS} can be passed through the switch from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). The select (SELx) pins determine which switch path to turn on, according to the Truth Table. The following conditions must be satisfied for the switch to stay in the ON condition:

- The difference between the primary supplies (V_{DD} – V_{SS}) must be greater than or equal to 10 V. With a minimum V_{DD} of 10 V.
- The input signals on the source (Sx) or the drain (Dx) must be between V_{DD} and V_{SS}.
- The logic control (SELx) must have selected the switch.

9.4.2 Truth Tables

表 9-1, 表 9-2, and 表 9-3 show the truth tables for the TMUX8211, TMUX8212, and TMUX8213, respectively.

表 9-1. TMUX8211 Truth Table

SEL #(1)	CHANNEL #
0	Channel # ON
1	Channel # OFF

(1) "#"designates the channel number controlled by SEL pin: "1, 2, 3, or 4"

表 9-2. TMUX8212 Truth Table

SEL #(1)	CHANNEL #
0	Channel # OFF
1	Channel # ON

(1) "#"designates the channel number controlled by SEL pin: "1, 2, 3, or 4"

表 9-3. TMUX8213 Truth Table

SEL1	SEL2	SEL3	SEL4	ON / OFF CHANNELS
0	X(1)	X	X	CHANNEL 1 ON
1	X	X	X	CHANNEL 1 OFF
X	0	X	X	CHANNEL 2 OFF
X	1	X	X	CHANNEL 2 ON
X	X	0	X	CHANNEL 3 OFF
X	X	1	X	CHANNEL 3 ON
X	X	X	0	CHANNEL 4 ON
X	X	X	1	CHANNEL 4 OFF

(1) "X" means "do not care."

If unused, then the SELx pins must be tied to GND or Logic High so that the devices do not consume additional current as highlighted in *Implications of Slow or Floating CMOS Inputs*. Unused signal path inputs (Sx or Dx) should be connected to GND for best performance.

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10 Application and Implementation

备注

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10.1 Application Information

The TMUX821x are high voltage switches capable of supporting analog and digital signals. The high voltage capability of these multiplexers allow them to be used in systems with high voltage signal swings, or in systems with high common mode voltages.

Additionally, the TMUX821x devices provide consistent analog parametric performance across the entire supply voltage range allowing the devices to be powered by the most convenient supply rails in the system while still providing excellent performance.

10.2 Typical Application

A common feature of many PMUs (precision measurement units) is the ability to change current ranges. This allows for a system defined current clamp when testing devices and reduces possible damage to the PMU and DUT (device under test). In high voltage PMUs, large relays are often used to enable this switching, but this comes with the trade-off of size. To reduce system size, a multi-channel high voltage switch can be added to facilitate this switching with minimal impact to system size and performance. The TMUX821x allows for switching between multiple current ranges, and has the added flexibility to use multiple channels in parallel for high current applications.

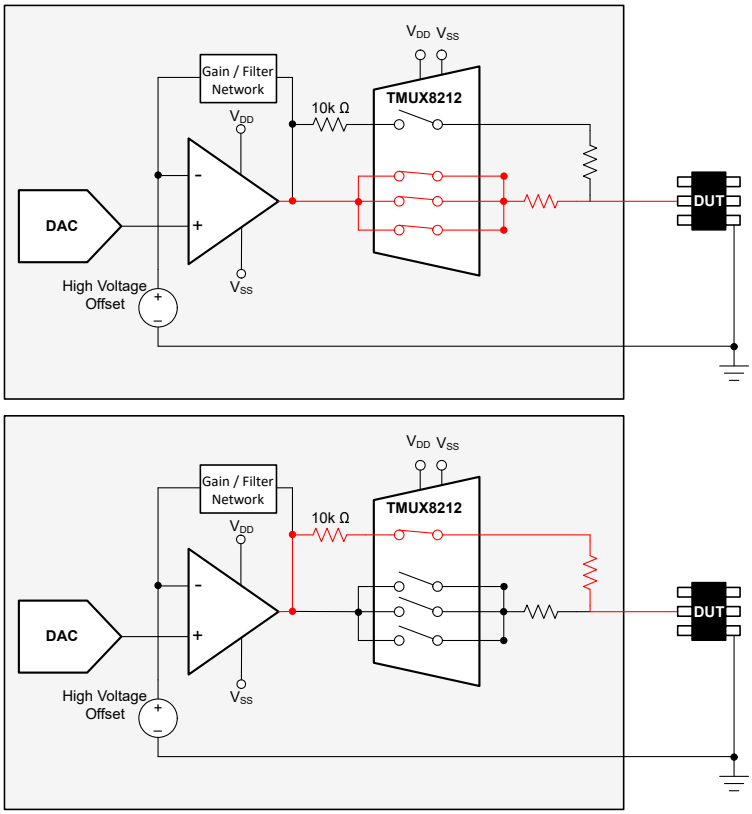

图 10-1. TMUX8212 Application Schematic

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10.2.1 Design Requirements

表 10-1. Design Parameters

PARAMETERS	VALUES
Positive supply (V_{DD}) mux and Op Amps	36 V
Positive supply (V_{SS}) mux and Op Amps	-36 V
Maximum input or output signals with common mode shift	-36 V to 36 V
Control logic thresholds	1.8 V compatible, up to 48 V
Temperature range	-40°C to +125°C

10.2.2 Detailed Design Procedure

Multiplexing PMU systems enables a small, flexible solution that can be used over a wide range of current ranges. TI’ s high voltage multiplexers offer a size advantage over typical relay solutions while still achieving an extremely low level of distortion, noise, and leakage. This high voltage multiplexer can be use in tandem with high voltage operational amplifiers and DACs to create an accurate PMU with excellent signal-to-noise ratio.

In this example application, the TMUX8212 is paired with a high voltage amplifier and a DAC. The DAC generates an arbitrary voltage signal that feeds into the amplifier. An additional high voltage offset is also fed into the amplifier to add any needed common mode shift. This arbitrary signal is then passed through a current limiting resistor before reaching the DUT. To change the current range of the system, different current limiting resistors are added in series with each channel of the multiplexer. In this example, the first channel of the multiplexer uses a 10 kΩ resistor for the low current clamp. The maximum output current of the PMU in this range is 5 mA because of this design. During the system operation, the PMU is set to this lower current range in the beginning of the test routine. After the DUT is initially checked in this range and is operating normally with no unexpected shorts, the current range can be switched to high current. This way the PMU and DUT will not be unnecessarily damaged from excess current due to a short. In this example, the remaining three channels of the TMUX8212 are connected in parallel, increasing the maximum current through the device and reducing the low On-Resistance. Because of the flexibility of the TMUX8212, this could easily be modified to fit any system need. For example, if less maximum current is needed, then two channels could be connected in parallel instead of three, and the additional single channel could be used to add a third current range option. The additional input channels make this multiplexed application increasingly valuable by greatly reducing solution size.

The TMUX821x switches have exceptionally flat On-Resistance and low leakage currents across the signal voltage range. The ultra-flat On-Resistance keeps the current clamp constant across the signal voltage range, and the low leakage current reduces the potential noise/offset when measuring on the lowest current range. Additionally, excellent crosstalk and off-isolation performance allows the TMUX821x devices to perform well in multi-channel switching applications without having an unselected channel impact the measurement on selected channels.

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10.2.3 Application Curves

The example application utilizes the excellent leakage and On-Resistance flatness performance of the TMUX821x devices. 图 10-2 shows the leakage current for a channel that is ON across a varying source voltage. 图 10-3 shows the extremely flat On-Resistance across source voltage while operating within the flattest R_{ON} range of the TMUX821x devices. These features make the devices an ideal solution for applications that require excellent linearity and low distortion.

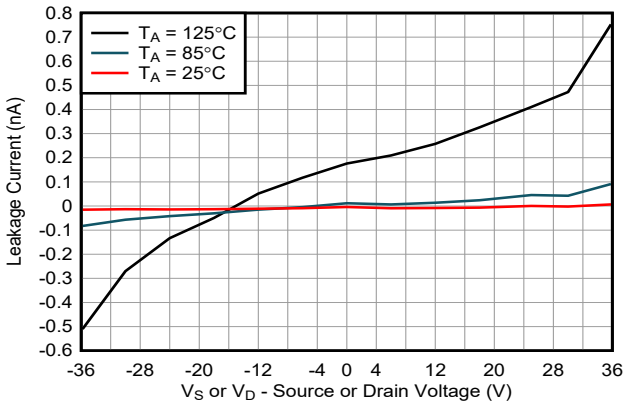

图 10-2. On-Leakage

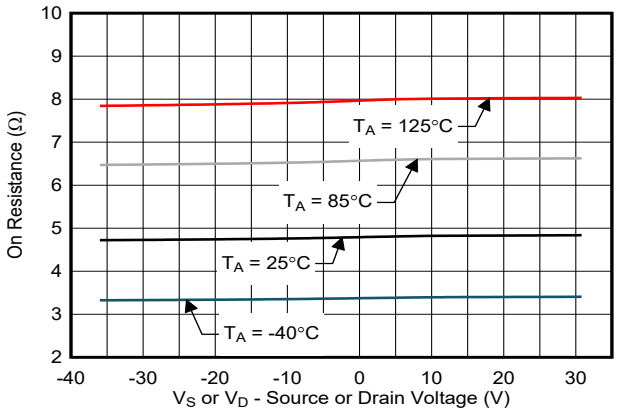

图 10-3. R_{ON} Flatness

11 Power Supply Recommendations

The TMUX821x devices operate across a wide supply range of ±10 V to ±50 V (10 V to 100 V in single-supply mode). They also perform well with asymmetrical supplies such as V_{DD} = 50 V and V_{SS}= – 10 V. For improved supply noise immunity, use a supply decoupling capacitor ranging from 1 µF to 10 µF at both the V_{DD} and V_{SS} pins to ground. An additional 0.1 µF capacitor placed closest to the supply pins will provide the best supply decoupling solution. Always ensure the ground (GND) connection is established before supplies are ramped.

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12 Layout

12.1 Layout Guidelines

The image below illustrates an example of a PCB layout with the TMUX821x device. Some key considerations are:

- For reliable operation, connect at least one decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and V_{SS} to GND. We recommend a 0.1 µF and 1 µF capacitor, placing the lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

12.2 Layout Example

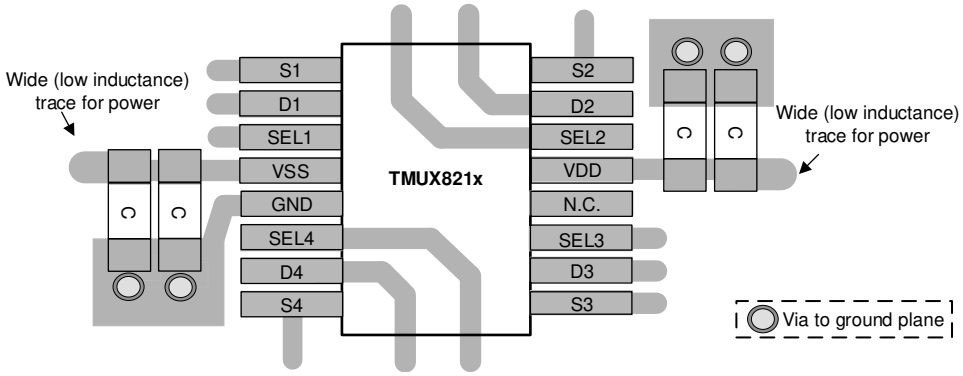

图 12-1. TMUX821x TSSOP Layout Example

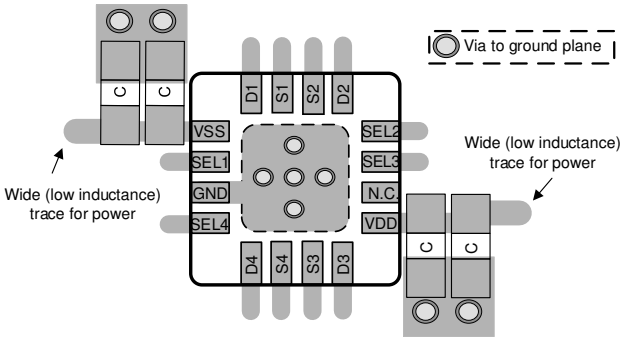

图 12-2. TMUX821x QFN Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note
- Texas Instruments, *Multiplexers and Signal Switches Glossary* application report
- Texas Instruments, *Using Latch-Up Immune Multiplexers to Help Improve System Reliability* application report

13.2 接收文档更新通知

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX8211PWR	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM8211
TMUX8211PWR.B	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM8211
TMUX8211RUMR	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TMUX 8211
TMUX8211RUMR.B	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TMUX 8211
TMUX8212PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM8212
TMUX8212PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM8212
TMUX8212PWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM8212
TMUX8212PWRG4.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM8212
TMUX8212RUMR	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TMUX 8212
TMUX8212RUMR.B	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TMUX 8212
TMUX8213PWR	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM8213
TMUX8213PWR.B	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM8213
TMUX8213RUMR	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TMUX 8213
TMUX8213RUMR.B	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TMUX 8213

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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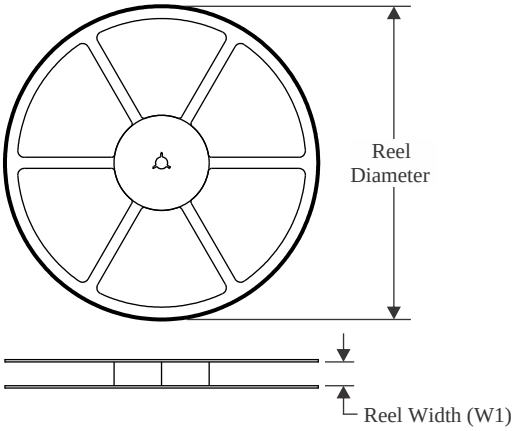
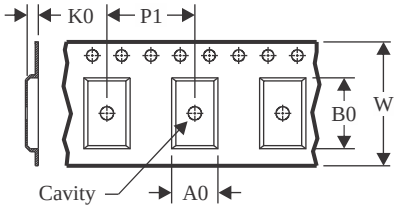
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

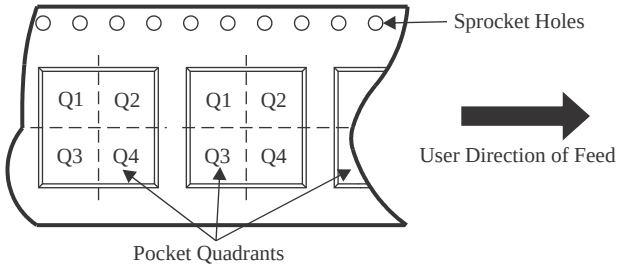


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

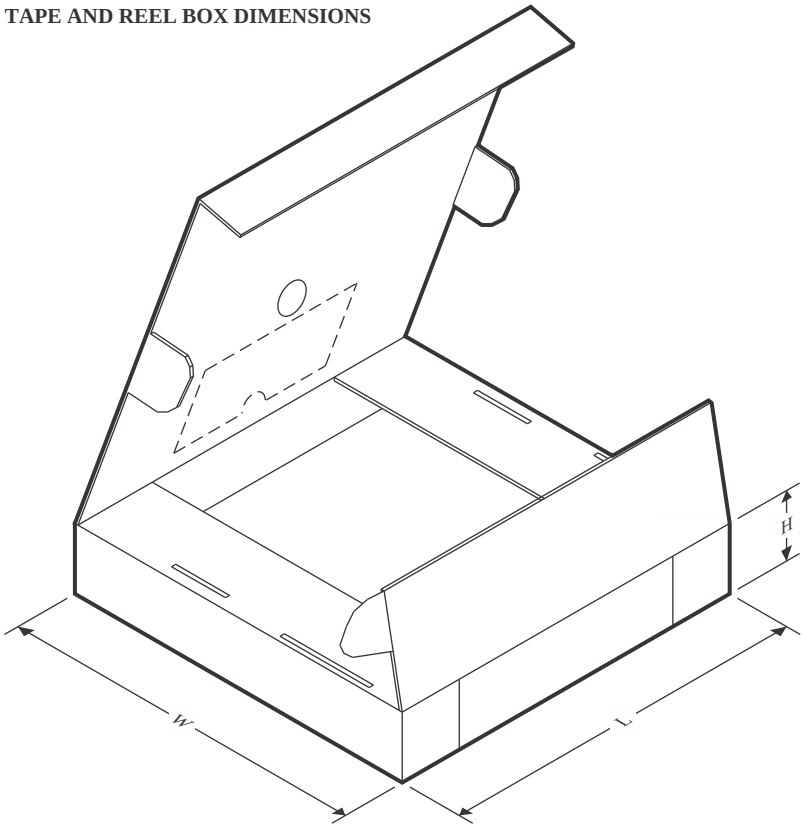
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX8211PWR	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX8211RUMR	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TMUX8212PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX8212PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX8212RUMR	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TMUX8213PWR	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX8213RUMR	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX8211PWR	TSSOP	PW	16	3000	353.0	353.0	32.0
TMUX8211RUMR	WQFN	RUM	16	3000	360.0	360.0	36.0
TMUX8212PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
TMUX8212PWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
TMUX8212RUMR	WQFN	RUM	16	3000	360.0	360.0	36.0
TMUX8213PWR	TSSOP	PW	16	3000	353.0	353.0	32.0
TMUX8213RUMR	WQFN	RUM	16	3000	360.0	360.0	36.0

GENERIC PACKAGE VIEW

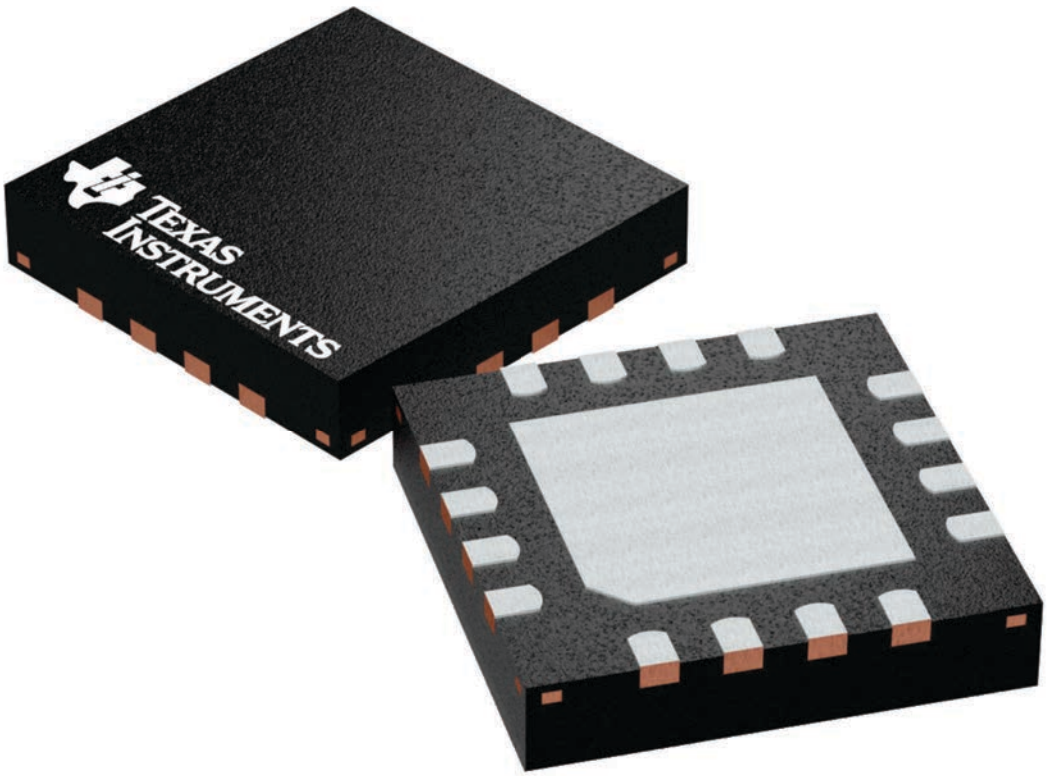
RUM 16

WQFN - 0.8 mm max height

4 x 4, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



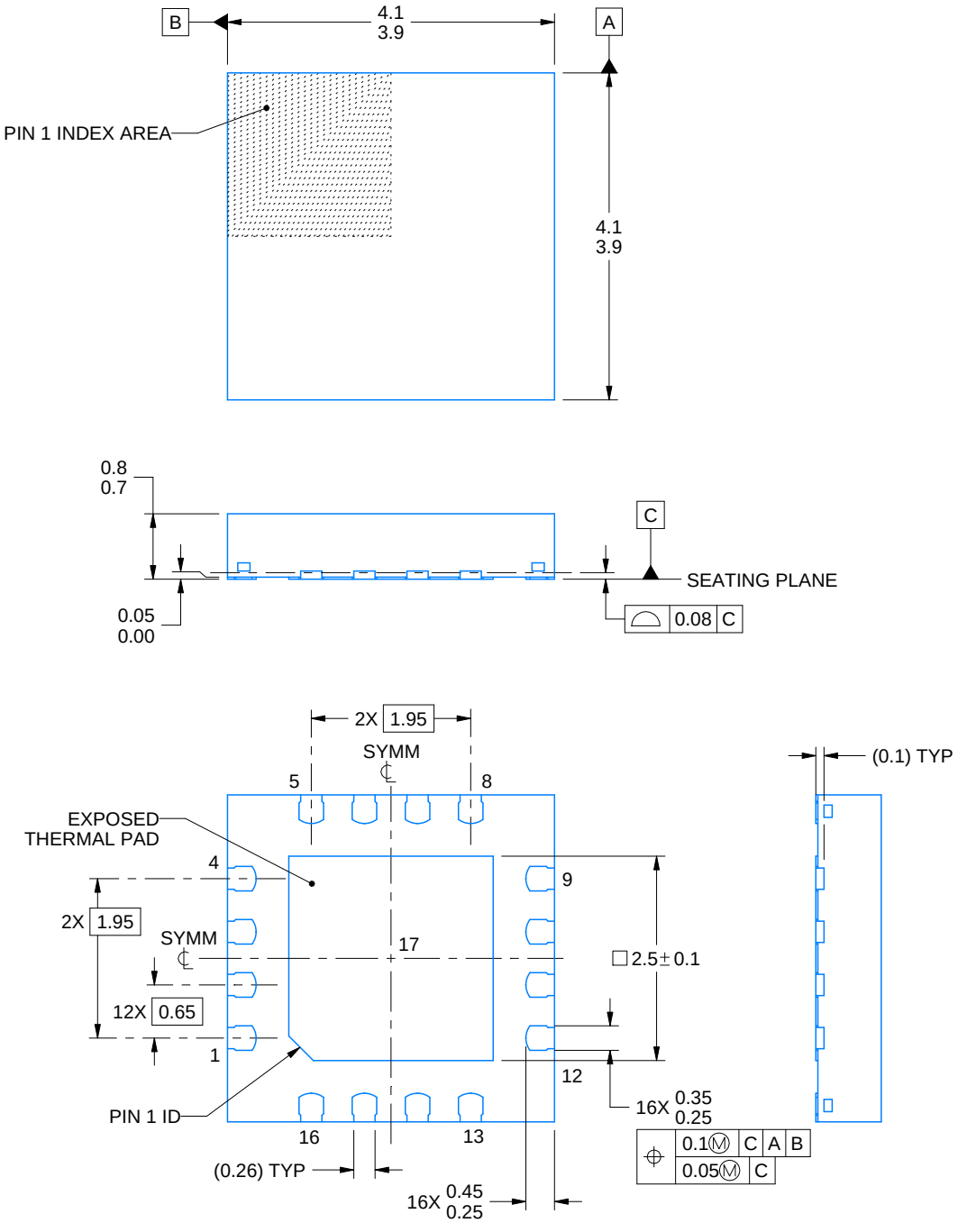
4224843/A

RUM0016E

PACKAGE OUTLINE

WQFN - 0.8 mm max height

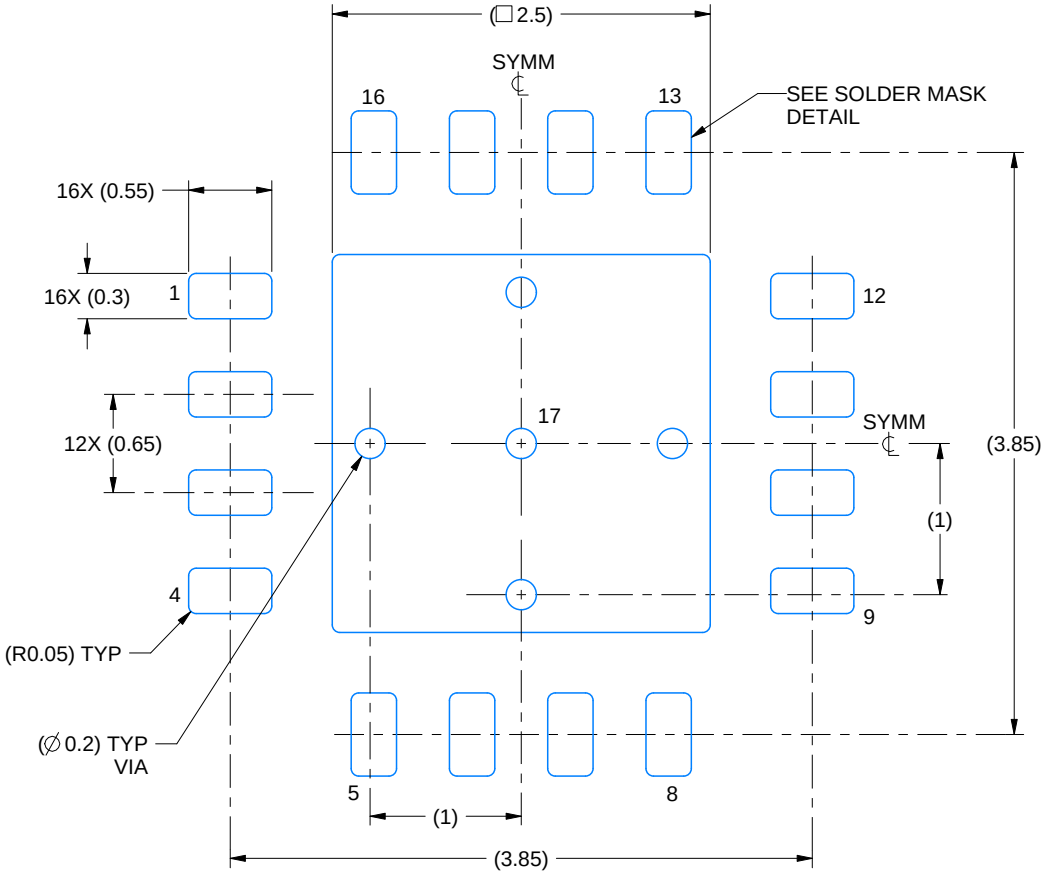
PLASTIC QUAD FLATPACK - NO LEAD



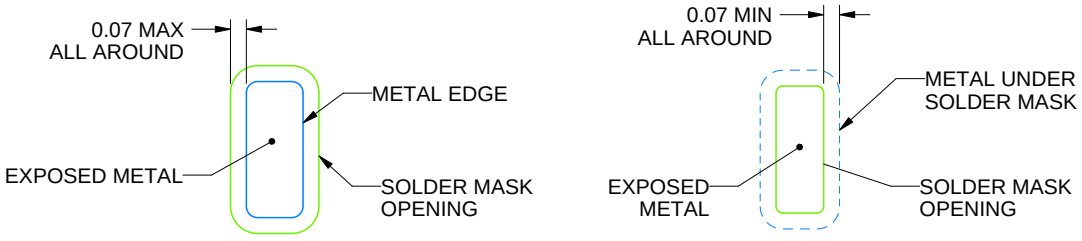
4224815/B 03/2026

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

4224815/B 03/2026

NOTES: (continued)

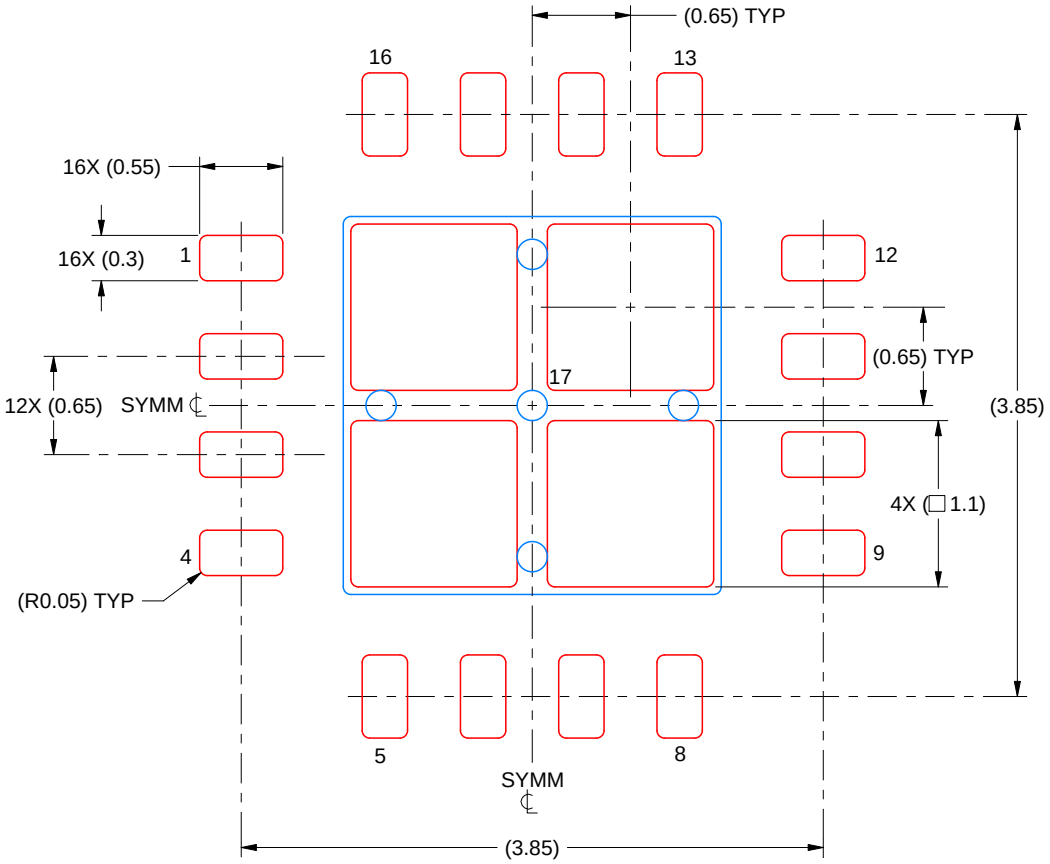
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUM0016E

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224815/B 03/2026

NOTES: (continued)

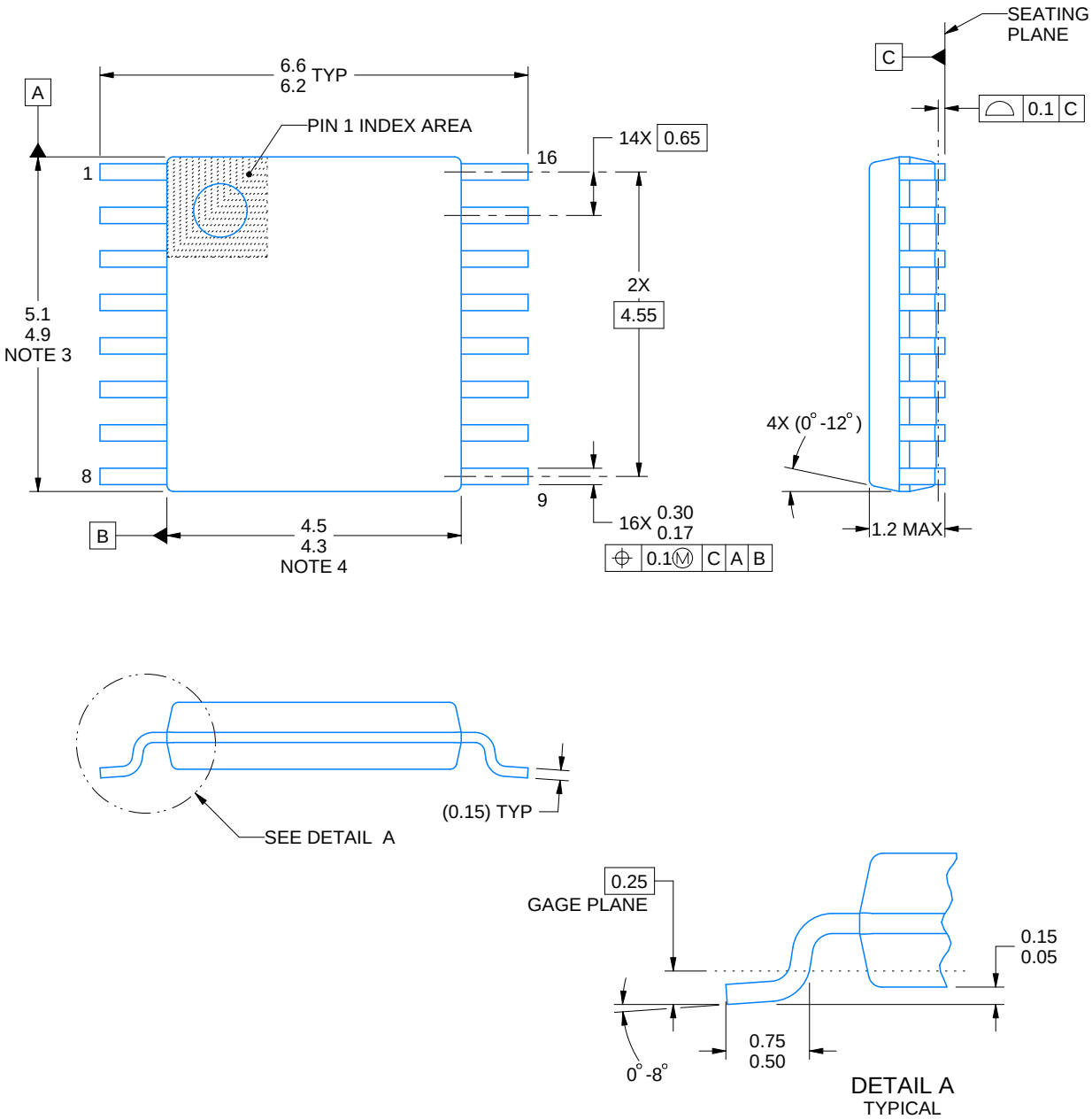
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0016A

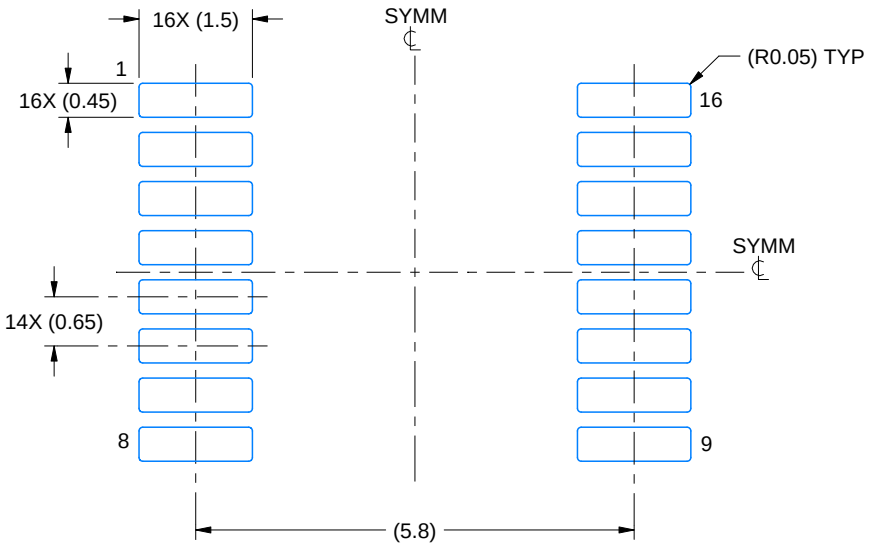
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

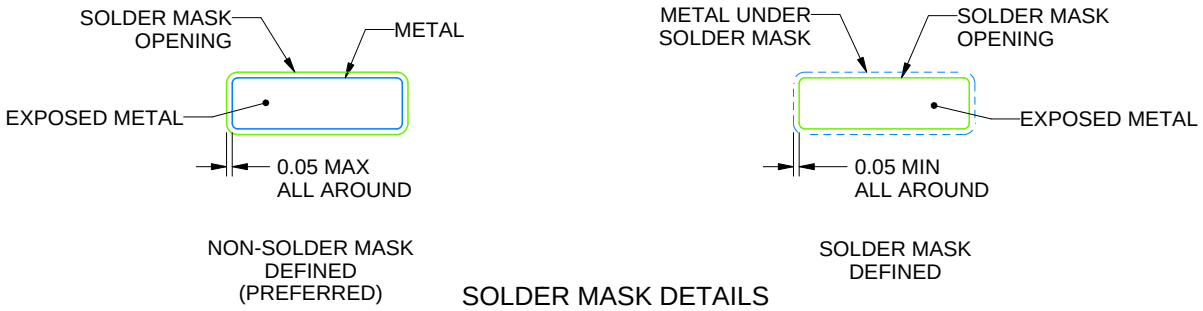


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

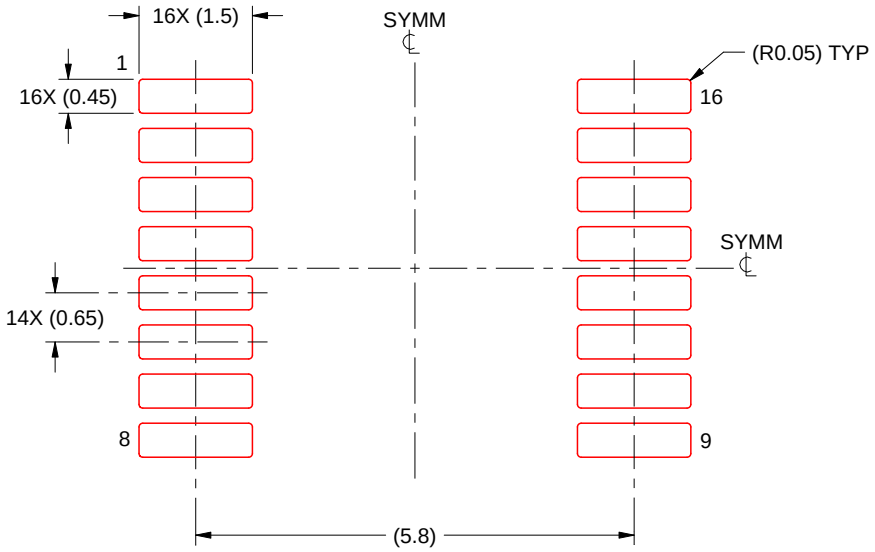


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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