TPD1E1B04 具有低 R_{DYN} 和低钳位电压的单通道 ESD 保护二极管

1 特性

- IEC 61000-4-2 4 级静电放电 (ESD) 保护
  - ±30kV 接触放电
  - ±30kV 气隙放电
- IEC 61000-4-4 瞬态放电 (EFT) 保护
  - 80A (5/50ns)
- IEC 61000-4-5 浪涌保护
  - 6.3A (8/20μs)
- IO 电容值：1pF（典型值）
- 直流击穿电压：6.4V（典型值）
- 低泄漏电流：100nA（最大值）
- 极低 ESD 钳位电压
  - 8.5V（±16A TLP 时）
  - R_{DYN}：0.15Ω
- 工业温度范围：-40°C 至 +125°C
- 行业标准的 0402 封装

2 应用

- 终端设备
  - 可穿戴产品
  - 便携式计算机和台式机
  - 手机和平板电脑
  - 机顶盒
  - 数字视频录像机 (DVR) 和网络视频录像机 (NVR)
  - 电视和监视器
  - EPOS（电子销售终端）
- 接口
  - USB 2.0/1.1
  - 通用输入/输出 (GPIO)
  - 按钮
  - 音频

3 说明

TPD1E1B04 是一款双向 TVS ESD 保护二极管，特有低 R_{DYN} 和低钳位电压。TPD1E1B04 的额定 ESD 冲击消散值等于 IEC 61000-4-2（4 级）国际标准中规定的最高水平。

超低动态电阻 (0.15Ω) 和极低钳位电压（16A TLP 时为 8.5V）可针对瞬变事件提供系统级保护。该器件 特有 一个 1pF IO 电容，非常适合用于保护 USB 2.0 等接口。

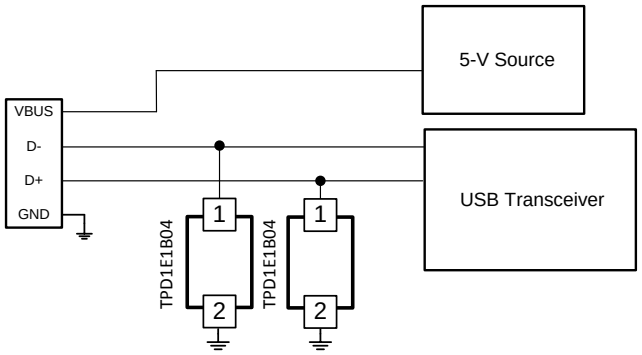
TPD1E1B04 采用符合行业标准的 0402 (DPY) 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPD1E1B04	X1SON (2)	0.60mm x 1.00mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

典型的 **USB 2.0** 应用原理图



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目录

1 特性 ... 1
2 应用 ... 1
3 说明 ... 1
4 修订历史记录 ... 2
5 **Pin Configuration and Functions** ... 3
6 **Specifications** ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 ESD Ratings—IEC Specification ... 4
6.4 Recommended Operating Conditions ... 4
6.5 Thermal Information ... 4
6.6 Electrical Characteristics ... 5
6.7 Typical Characteristics ... 6
7 **Detailed Description** ... 8
7.1 Overview ... 8
7.2 Functional Block Diagram ... 8
7.3 Feature Description ... 8
7.4 Device Functional Modes ... 9
8 **Application and Implementation** ... 10
8.1 Application Information ... 10
8.2 Typical Application ... 10
9 **Power Supply Recommendations** ... 12
10 **Layout** ... 12
10.1 Layout Guidelines ... 12
10.2 Layout Example ... 12
11 器件和文档支持 ... 13
11.1 文档支持 ... 13
11.2 接收文档更新通知 ... 13
11.3 社区资源 ... 13
11.4 商标 ... 13
11.5 静电放电警告 ... 13
11.6 Glossary ... 13
12 机械、封装和可订购信息 ... 13

4 修订历史记录

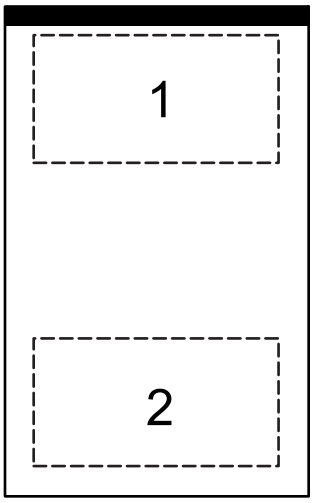
注：之前版本的页码可能与当前版本有所不同。

Changes from Original (May 2016) to Revision A	**Page**
• 已将器件状态从*产品预览*更改为*量产数据*	1

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5 Pin Configuration and Functions

DPY Package
2-Pin X1SON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IO	I/O	ESD Protected Channel. If used as ESD IO, connect pin 2 to ground
2	IO	I/O	ESD Protected Channel. If used as ESD IO, connect pin 1 to ground

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Electrical fast transient	IEC 61000-4-4 (5/50 ns)		80	A
Peak pulse	IEC 61000-4-5 Power (t_p - 8/20 µs)		50	W
	IEC 61000-4-5 Current (t_p - 8/20 µs)		6.3	A
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±30000	V
		IEC 61000-4-2 air-gap discharge	±30000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	–3.6	3.6	V
T_A	Operating free-air temperature	–40	125	°C

6.5 Thermal Information

THERMAL METRIC(1)		TPD1E1B04 DPY (X1SON) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	420	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	169.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	276.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	122.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	157.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 100 nA	–3.6		3.6	V
V_{BRF}	Breakdown voltage, any IO pin to GND	Measured as the maximum voltage before device snaps back into V_{HOLD} voltage		6.4		V
V_{BRR}	Breakdown voltage, GND to any IO pin	Measured as the maximum voltage before device snaps back into V_{HOLD} voltage		–6.4		V
V_{HOLD}	Holding voltage	I_{IO} = 1 mA, T_A = 25°C	5	6	6.6	V
V_{CLAMP}	Clamping voltage	I_{PP} = 1 A, TLP, from IO to GND		6.3		V
		I_{PP} = 5 A, TLP, from IO to GND		6.8		
		I_{PP} = 16 A, TLP, from IO to GND		8.5		
		I_{PP} = 1 A, TLP, from GND to IO		6.3		
		I_{PP} = 5 A, TLP, from GND to IO		6.8		
		I_{PP} = 16 A, TLP, from GND to IO		8.5		
I_{LEAK}	Leakage current, IO to GND	V_{IO} = ±2.5 V		0.2	100	nA
R_{DYN}	Dynamic resistance	IO to GND		0.15		Ω
		GND to IO		0.15		
C_L	Line capacitance	V_{IO} = 0 V, f = 1 MHz, IO to GND, T_A = 25°C		1	1.3	pF

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6.7 Typical Characteristics

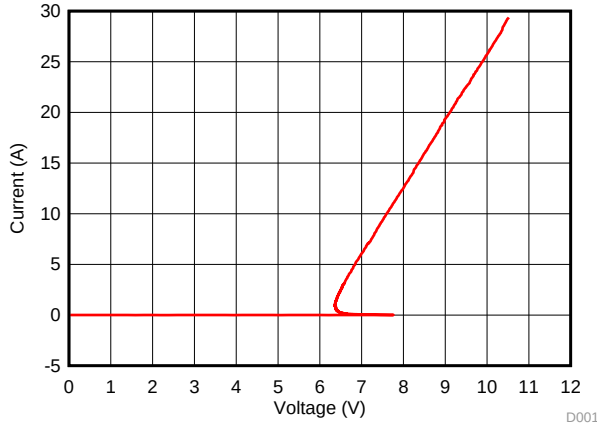


Figure 1. Positive TLP Curve

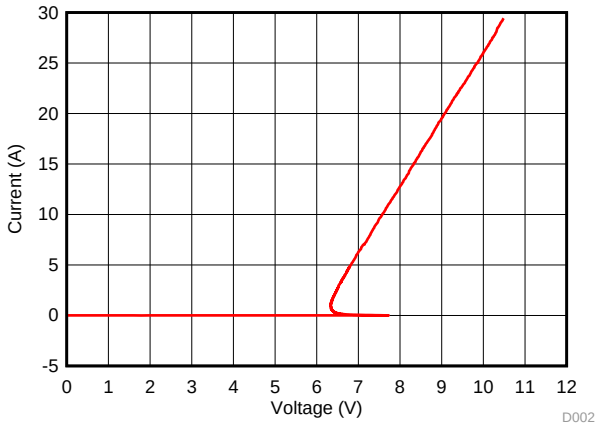


Figure 2. Negative TLP Curve

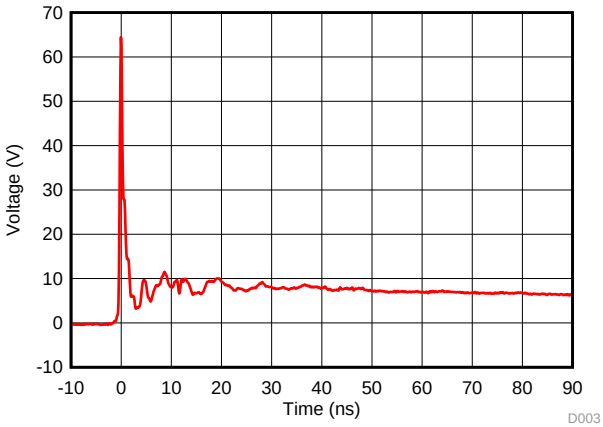


Figure 3. 8-kV IEC Waveform

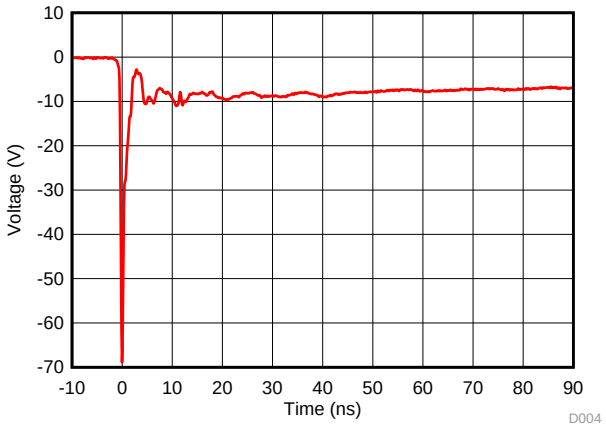


Figure 4. –8-kV IEC Waveform

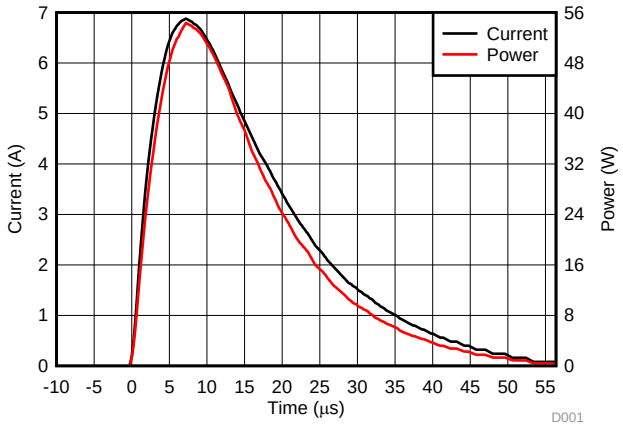


Figure 5. Surge Curve (t_p = 8/20 µs), Any IO Pin to GND

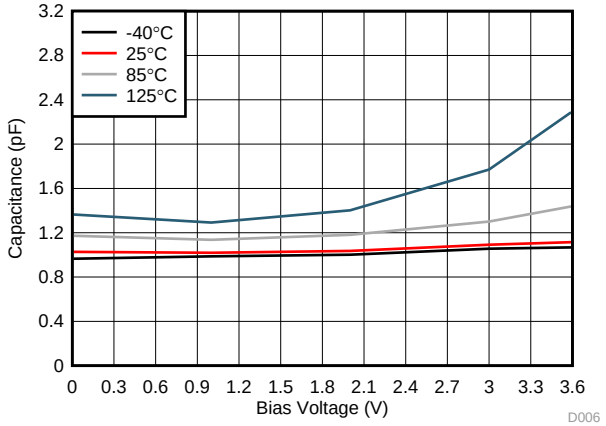


Figure 6. Capacitance vs. Bias Voltage

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Typical Characteristics (continued)

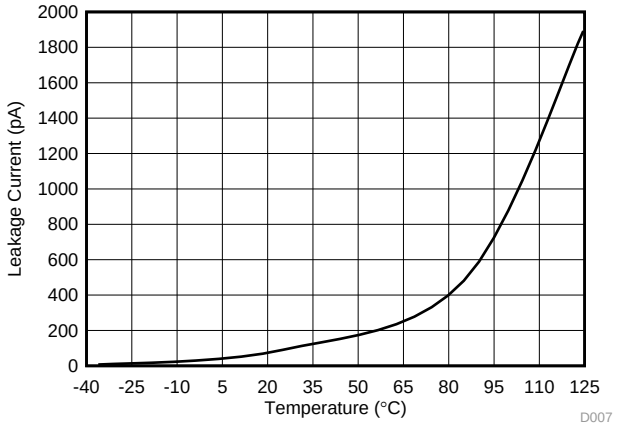


Figure 7. Leakage Current vs. Temperature

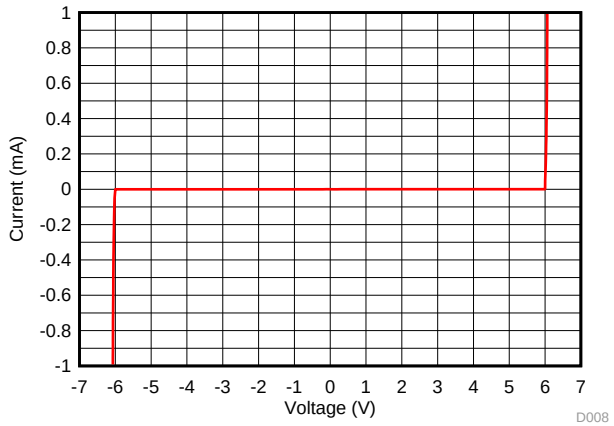


Figure 8. DC Voltage Sweep I-V Curve

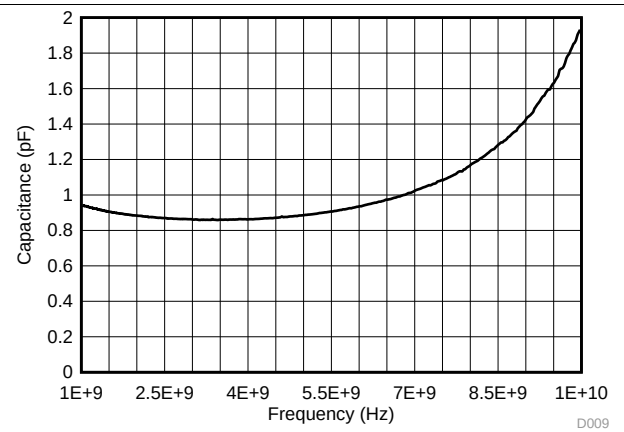


Figure 9. Capacitance vs. Frequency

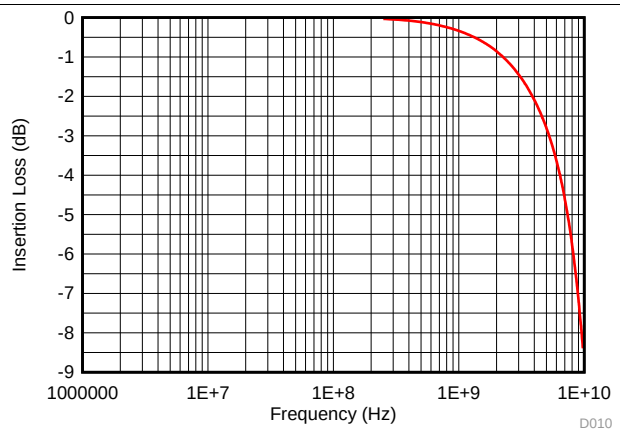


Figure 10. Insertion Loss

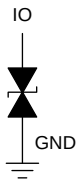
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7 Detailed Description

7.1 Overview

The TPD1E1B04 is a bidirectional ESD Protection Diode with ultra-low clamping voltage. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 International Standard. The ultra-low clamping makes this device ideal for protecting any sensitive signal pins.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events up to ±30-kV contact and ±30-kV air gap. An ESD-surge clamp diverts the current to ground.

7.3.2 IEC 61000-4-4 EFT Protection

The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50-Ω impedance). An ESD-surge clamp diverts the current to ground.

7.3.3 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 6.3 A and 50 W (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

7.3.4 IO Capacitance

The capacitance between each I/O pin to ground is 1 pF (typical) and 1.3 pF (maximum).

7.3.5 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is ±6.4 V typical. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of ±3.6 V.

7.3.6 Low Leakage Current

The I/O pins feature an low leakage current of 100 nA (maximum) with a bias of ±2.5 V.

7.3.7 Extremely Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 8.5 V (I_{PP} = 16 A).

7.3.8 Industrial Temperature Range

This device features an industrial operating range of –40°C to +125°C.

7.3.9 Industry Standard Footprint

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

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7.4 Device Functional Modes

The TPD1E1B04 is a passive integrated circuit that triggers when voltages are above V_{BRF} or below V_{BRR}. During ESD events, voltages as high as ±30 kV (contact or air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of TPD1E1B04 (usually within 10s of nano-seconds) the device reverts to passive.

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8 Application and Implementation

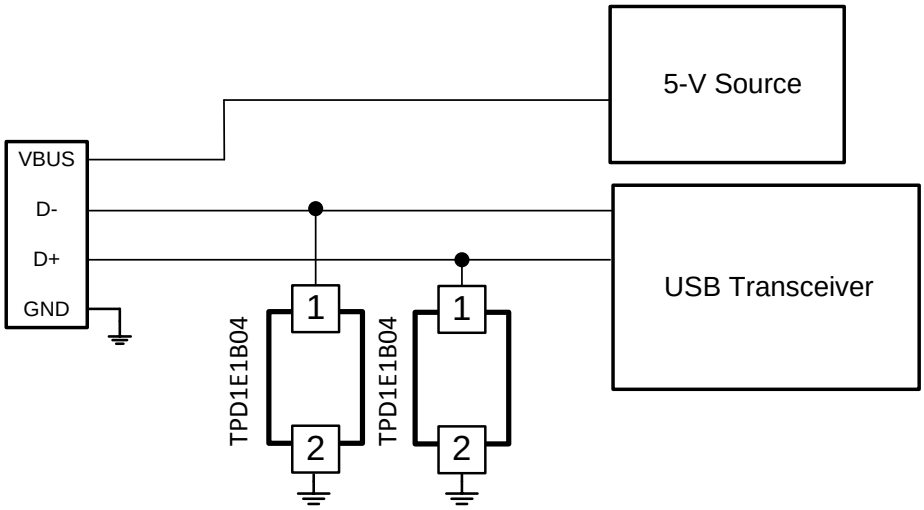
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD1E1B04 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application



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Figure 11. USB 2.0 ESD Schematic

8.2.1 Design Requirements

For this design example, two TPD1E1B04 devices are being used in a USB 2.0 application. This provides a complete ESD protection scheme.

Given the USB 2.0 application, the parameters listed in Table 1 are known.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on DP-DM lines	0 V to 3.6 V
Operating frequency on DP-DM lines	up to 240 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range

The TPD1E1B04 supports signal ranges between –3.6 V and 3.6 V, which supports the USB 2.0 signal pair on the USB 2.0 application.

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8.2.2.2 Operating Frequency

The TPD1E1B04 has a 1-pF (typical) capacitance, which supports the USB 2.0 data rates of 480 Mbps.

8.2.3 Application Curve

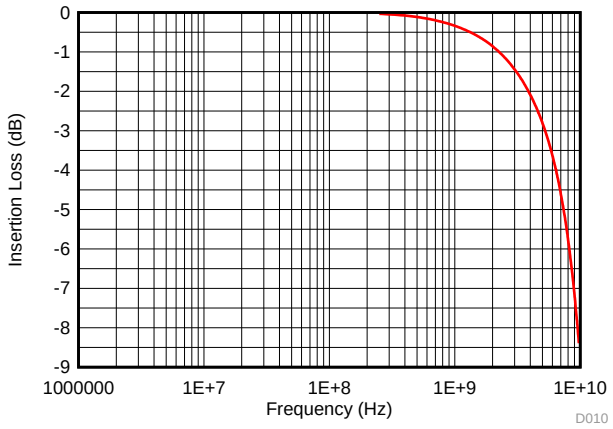


Figure 12. Insertion Loss

9 Power Supply Recommendations

The TPD1E1B04 is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification (–3.6 V to 3.6 V) to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

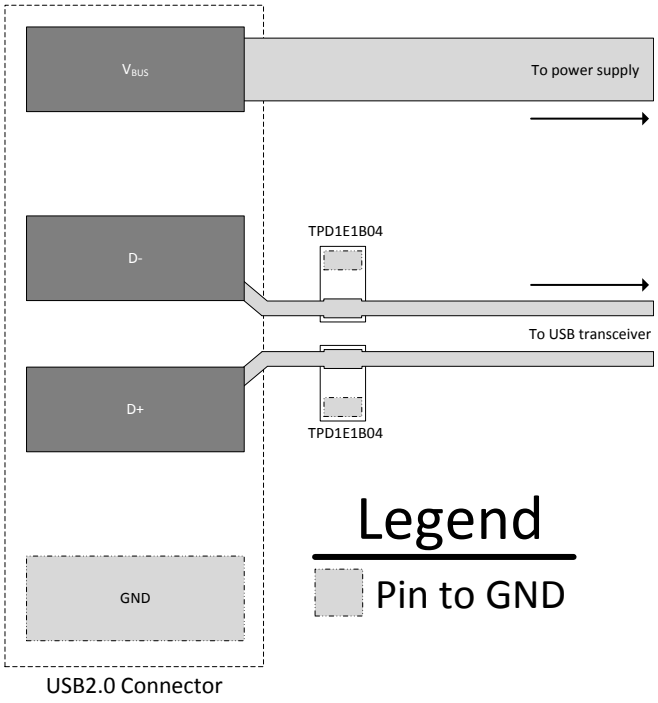


Figure 13. USB 2.0 ESD Layout

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11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档请参见以下部分：

《TPD1E1B04 评估模块》，SLVUAN7

11.2 接收文档更新通知

如需接收文档更新通知，请访问 ti.com 上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

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11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD1E1B04DPYR	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	4X
TPD1E1B04DPYR.B	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	4X
TPD1E1B04DPYRG4	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4X
TPD1E1B04DPYRG4.B	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4X
TPD1E1B04DPYT	Last Time Buy	Production	X1SON (DPY) | 2	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	4X
TPD1E1B04DPYT.B	Last Time Buy	Production	X1SON (DPY) | 2	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	4X

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

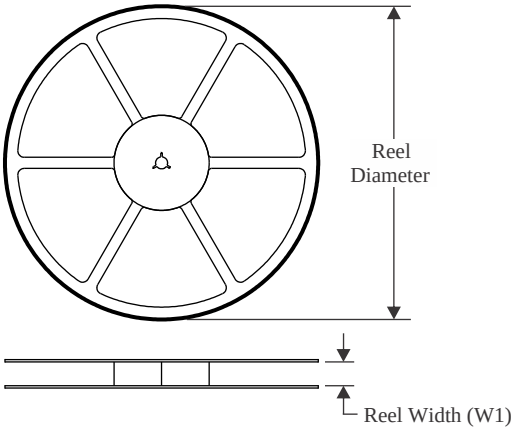
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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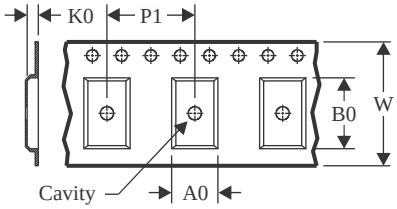
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

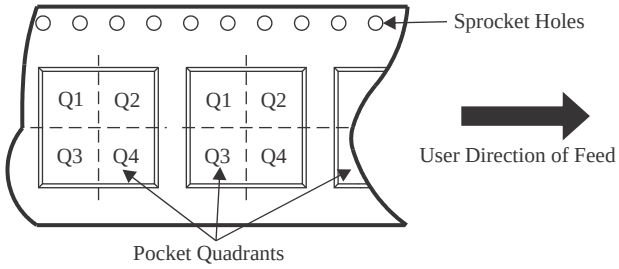


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

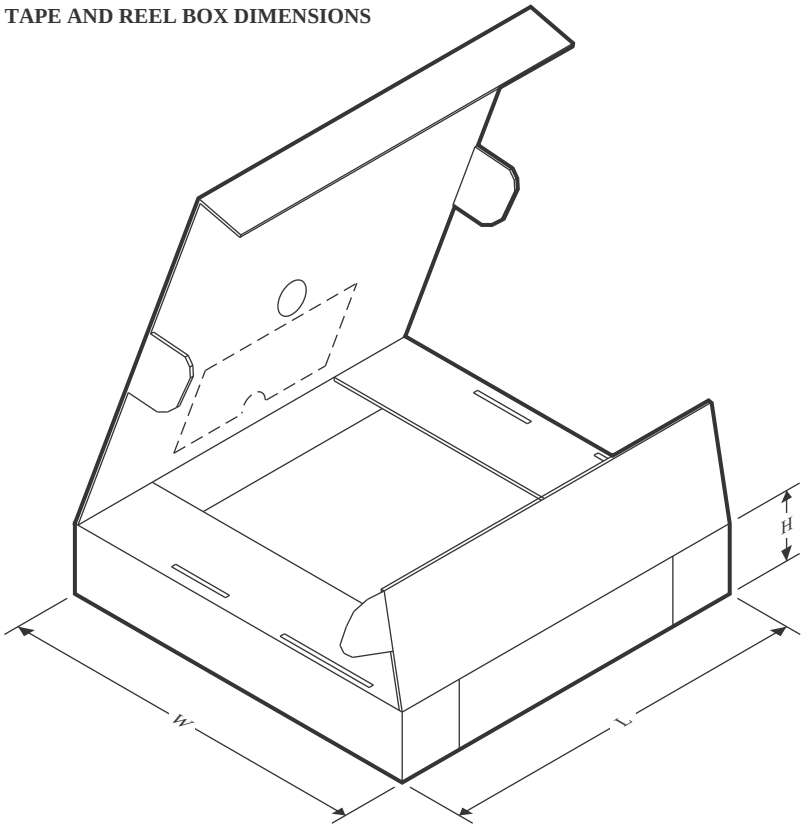
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD1E1B04DPYR	X1SON	DPY	2	10000	178.0	8.4	0.67	1.15	0.46	2.0	8.0	Q2
TPD1E1B04DPYRG4	X1SON	DPY	2	10000	180.0	8.4	0.67	1.15	0.46	2.0	8.0	Q2
TPD1E1B04DPYT	X1SON	DPY	2	250	180.0	9.5	0.73	1.13	0.5	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD1E1B04DPYR	X1SON	DPY	2	10000	208.0	191.0	35.0
TPD1E1B04DPYRG4	X1SON	DPY	2	10000	210.0	185.0	35.0
TPD1E1B04DPYT	X1SON	DPY	2	250	189.0	185.0	36.0

GENERIC PACKAGE VIEW

DPY 2

X1SON - 0.45 mm max height

1 x 0.6 mm

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



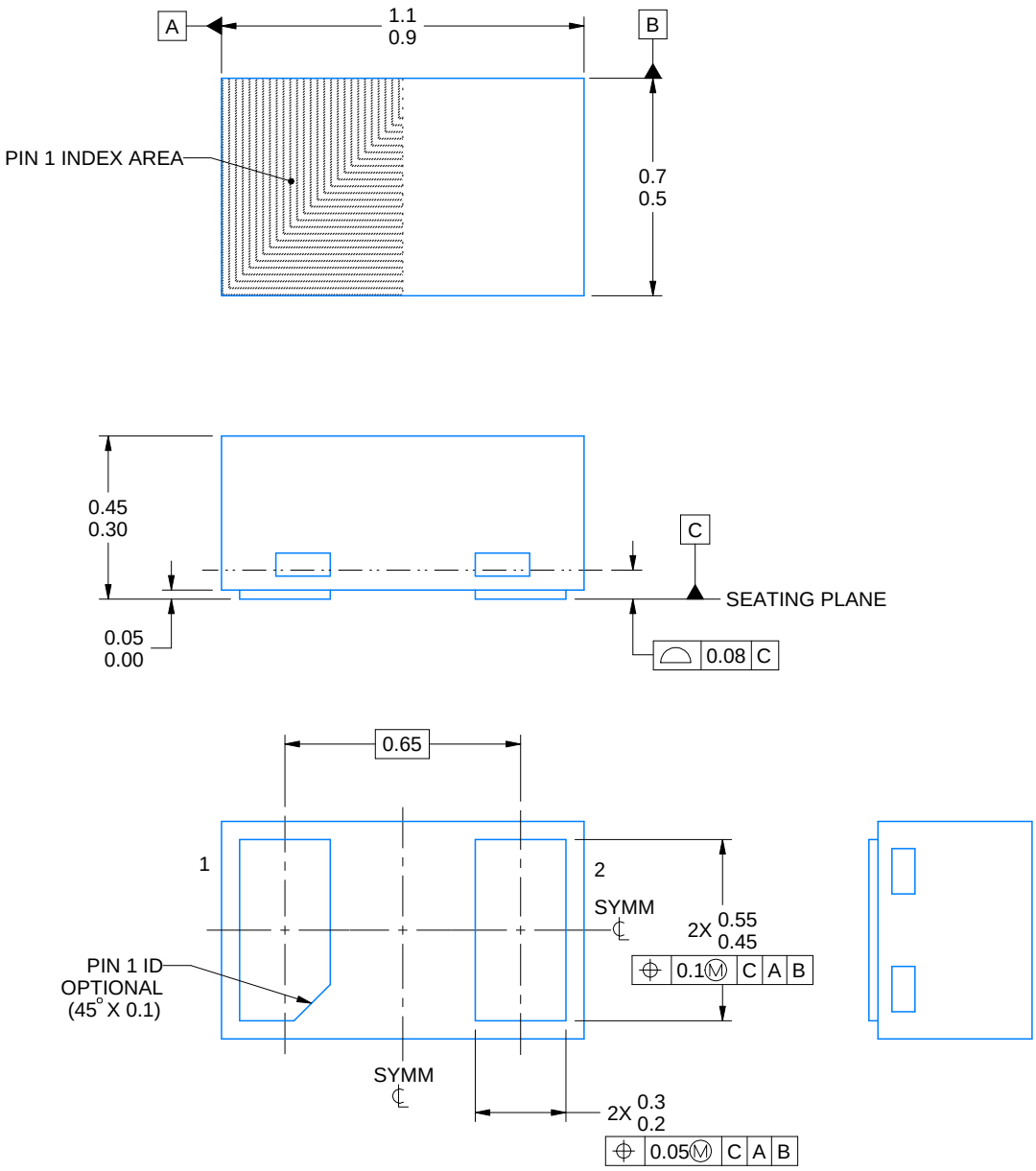
4231484/A

PACKAGE OUTLINE

DPY0002A

X1SON - 0.45 mm max height

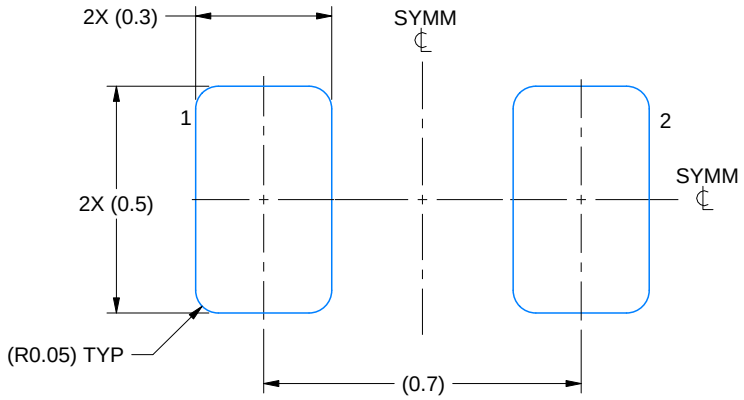
PLASTIC SMALL OUTLINE - NO LEAD



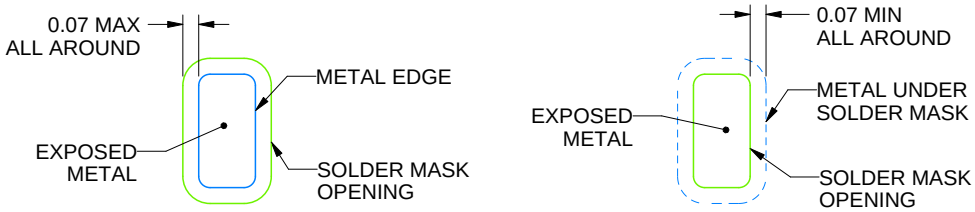
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X

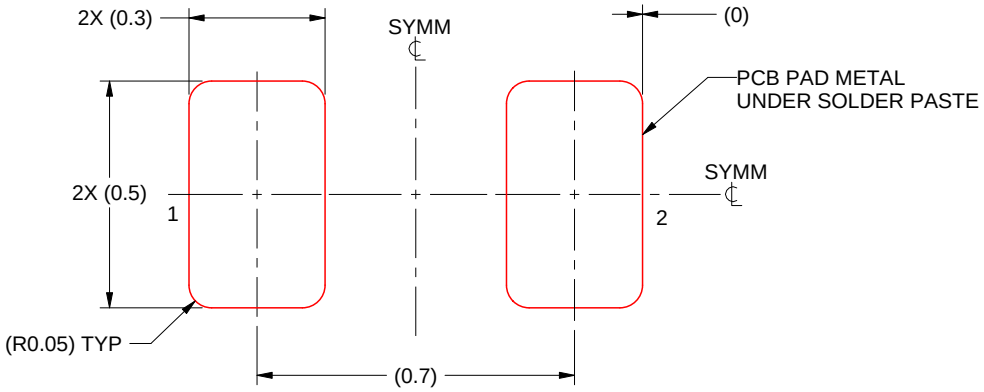


SOLDER MASK DETAILS

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NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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