TPS25924x 具有过压保护和阻断 FET 控制功能的 12V 电子熔丝

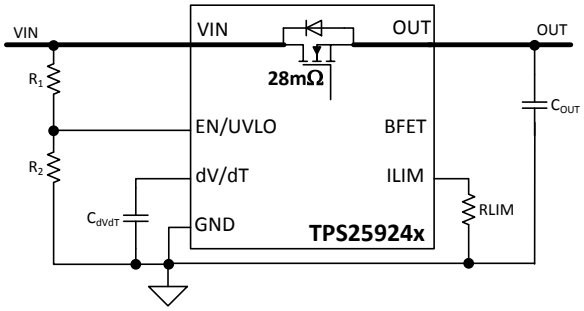
1 特性

- $V_{OPERATING}$ = 4.5V 至 13.8V，V_{ABSMAX} = 20V
- 集成 28mΩ 导通金属氧化物半导体场效应晶体管 (MOSFET)
- 15V 固定过压钳位
- 1A 至 5A 可调电流 I_{LIMIT}
- ±8% I_{LIMIT} 精度（3.7A 时）
- 支持反向电流阻断
- 可编程 OUT（输出）转换率，欠压闭锁 (UVLO)
- 内置热关断
- UL2367 认证正在处理中
- 单点故障测试期间安全 (UL60950)
- 小型封装尺寸 - 10L (3mm x 3mm) 超薄小外形尺寸无引线封装 (VSON)

2 应用

- 适配器供电器件
- 硬盘 (HDD) 和固态硬盘 (SSD)
- 机顶盒
- 服务器/辅助 (AUX) 电源
- 风扇控制
- PCI/PCIe 卡

应用电路原理图



3 说明

TPS25924x 系列电子熔丝是采用小型封装的高度集成电路保护和电源管理解决方案。 该器件使用极少的外部组件并可提供多重保护模式。 它们能够有效地防止过载、短路、电压浪涌、过高浪涌电流和反向电流。

电流限制级别可通过一个外部电阻设定。 内部钳位电路可将过电压限制在一个安全的固定最大值，无需使用外部组件。

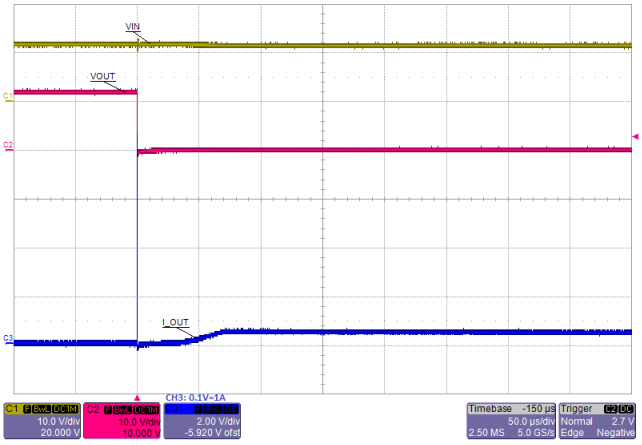
具有特殊电压斜坡要求的应用可以使用单个电容来设定 dV/dT，以确保达到适当的输出斜坡速率。 许多系统（例如 SSD）禁止将储存的电容能量通过 FET 二极管倒流到降压或短路输入总线。 BFET 引脚专用于这类系统。 外部 NFET 可与 TPS25924x 输出形成“背靠背 (B2B)”连接，而由 BFET 驱动的栅极可防止电流从负载流回电源（请参见Figure 43）。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS259241	VSON (10)	3.00mm × 3.00mm
TPS259240		

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

瞬态：输出短路



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

Changes from Original (August 2015) to Revision A **Page**

- 已更改 “产品预览”至“量产数据” ... 1

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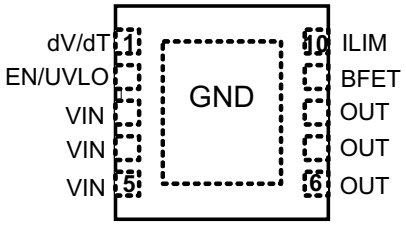
5 Device Comparison Table

PART NUMBER	UV	OV CLAMP	FAULT RESPONSE	STATUS
TPS259241	4.3 V	15 V	Auto Retry	Active
TPS259240	4.3 V	15 V	Latched	Active

6 Pin Configuration and Functions

DRC Package
10-Pin VSON
Top View



Pin Functions

PIN		DESCRIPTION
NAME	NUMBER	
BFET	9	Connect this pin to the gate of a blocking NFET. See the *Feature Description* section. This pin can be left floating if it is not used.
dV/dT	1	Tie a capacitor from this pin to GND to control the ramp rate of OUT at device turn-on.
EN/UVLO	2	This is a dual function control pin. When used as an ENABLE pin and pulled down, it shuts off the internal pass MOSFET and pulls BFET to GND. When pulled high, it enables the device and BFET. As an UVLO pin, it can be used to program different UVLO trip point via external resistor divider.
GND	Thermal Pad	GND
ILIM	10	A resistor from this pin to GND will set the overload and short circuit limit.
OUT	6-8	Output of the device
VIN	3-5	Input supply voltage

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7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
Supply voltage(1)	VIN	–0.3	20	V
	VIN (10 ms Transient)		22	
Output voltage	OUT	–0.3	VIN + 0.3	V
	OUT (Transient < 1 µs)		-1.2	V
Voltage	ILIM	–0.3	7	V
	EN/UVLO	–0.3	7	
	dV/dT	–0.3	7	
	BFET	–0.3	30	
Storage temperature range, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
Input voltage range	VIN	4.5	12	13.8	V
	BFET	0		VIN+6	
	dV/dT, EN/UVLO	0		6	
	ILIM	0		3	
Continuous output current	I_{OUT}	0		5	A
Resistance	ILIM	10	100	162	kΩ
External capacitance	OUT	0.1	1	1000	µF
	dV/dT		1	1000	nF
Operating junction temperature range, T_J		–40	25	125	°C
Operating Ambient temperature range, T_A		–40	25	85	°C

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7.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)(1)

THERMAL METRIC		TPS25924x DRC (VSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.9	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	53	
$R_{\theta JB}$	Junction-to-board thermal resistance	21.2	
ψ_{JT}	Junction-to-top characterization parameter	1.2	
ψ_{JB}	Junction-to-board characterization parameter	21.4	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	5.9	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

–40°C ≤ T_J ≤ 125°C, VIN = 12 V, $V_{EN\ /UVLO}$ = 2 V, R_{ILIM} = 100 kΩ, C_{dVdT} = OPEN. All voltages referenced to GND (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN (INPUT SUPPLY)						
V_{UVR}	UVLO threshold, rising		4.15	4.3	4.45	V
V_{UVhyst}	UVLO hysteresis(1)			5%		
IQ_{ON}	Supply current	Enabled: EN/UVLO = 2 V	0.3	0.42	0.55	mA
IQ_{OFF}		EN/UVLO = 0 V		0.13	0.225	mA
V_{OVC}	Over-voltage clamp	VIN > 16.5 V, I_{OUT} = 10 mA	13.8	15	16.5	V
EN/UVLO (ENABLE/UVLO INPUT)						
V_{ENR}	EN Threshold voltage, rising		1.37	1.4	1.44	V
V_{ENF}	EN Threshold voltage, falling		1.32	1.35	1.39	V
I_{EN}	EN Input leakage current	0 V ≤ V_{EN} ≤ 5 V	–100	0	100	nA
dV/dT (OUTPUT RAMP CONTROL)						
I_{dVdT}	dV/dT Charging current(1)	V_{dVdT} = 0 V		220		nA
R_{dVdT_disch}	dV/dT Discharging resistance	EN/UVLO = 0 V, I_{dVdT} = 10 mA sinking	50	73	100	Ω
$V_{dVdTmax}$	dV/dT Max capacitor voltage(1)			5.5		V
$GAIN_{dVdT}$	dV/dT to OUT gain(1)	ΔV_{dVdT}		4.85		V/V
ILIM (CURRENT LIMIT PROGRAMMING)						
I_{ILIM}	ILIM Bias current(1)			10		µA
I_{OL}	Overload current limit(2)	R_{ILIM} = 10 kΩ, $V_{VIN-OUT}$ = 1 V		1.02		A
		R_{ILIM} = 45.3 kΩ, $V_{VIN-OUT}$ = 1 V	1.79	2.10	2.42	
		R_{ILIM} = 100 kΩ, $V_{VIN-OUT}$ = 1 V	3.46	3.75	4.03	
		R_{ILIM} = 150 kΩ, $V_{VIN-OUT}$ = 1 V	4.5	5.1	5.7	
$I_{OL-R-Short}$		R_{ILIM} = 0 Ω, Shorted Resistor Current Limit (Single Point Failure Test: UL60950)(1)		0.84		A
$I_{OL-R-Open}$		R_{ILIM} = OPEN, Open Resistor Current Limit (Single Point Failure Test: UL60950)(1)		0.73		A
I_{SCL}	Short-circuit current limit(2)	R_{ILIM} = 10 kΩ, $V_{VIN-OUT}$ = 12 V		1		A
		R_{ILIM} = 45.3 kΩ, $V_{VIN-OUT}$ = 12 V	1.66	1.98	2.37	
		R_{ILIM} = 100 kΩ, $V_{VIN-OUT}$ = 12 V	2.90	3.32	3.85	
		R_{ILIM} = 150 kΩ, $V_{VIN-OUT}$ = 12 V	3.7	4.5	5.5	
$RATIO_{FASTRIP}$	Fast-Trip comparator level w.r.t. overload current limit(1)	$I_{FASTRIP}$: I_{OL}		160%		
$V_{OpenILIM}$	ILIM Open resistor detect threshold(1)	V_{ILIM} Rising, R_{ILIM} = OPEN		3.1		V

(1) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.
(2) Pulsed testing techniques used during this test maintain junction temperature approximately equal to ambient temperature.

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Electrical Characteristics (continued)

–40°C ≤ T_J ≤ 125°C, VIN = 12 V, $V_{EN\ /UVLO}$ = 2 V, R_{ILIM} = 100 kΩ, C_{dVdT} = OPEN. All voltages referenced to GND (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUT (PASS FET OUTPUT)						
$R_{DS(on)}$	FET ON resistance	T_J = 25°C	21	28	37	mΩ
		T_J = 125°C		39	48	
$I_{OUT-OFF-LKG}$	OUT Bias current in off state	$V_{EN/UVLO}$ = 0 V, V_{OUT} = 0 V (Sourcing)	–5	0	1.2	µA
$I_{OUT-OFF-SINK}$		$V_{EN/UVLO}$ = 0 V, V_{OUT} = 300 mV (Sinking)	10	15	20	
BFET (BLOCKING FET GATE DRIVER)						
I_{BFET}	BFET Charging current(1)	V_{BFET} = V_{OUT}		2		µA
$V_{BFETmax}$	BFET Clamp voltage(1)			V_{VIN} + 6.4		V
$R_{BFETdisch}$	BFET Discharging resistance to GND	$V_{EN/UVLO}$ = 0 V, I_{BFET} = 100 mA	15	26	36	Ω
TSD (THERMAL SHUT DOWN)						
T_{SHDN}	TSD Threshold, rising(1)			150		°C
$T_{SHDNhyst}$	TSD Hysteresis(1)			10		°C
	Thermal fault: latched or autoretry	TPS259240		LATCHED		
		TPS259241		AUTO-RETRY		

7.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{ON}	Turn-on delay(1)	EN/UVLO → H to I_{VIN} = 100 mA, 1-A resistive load at OUT		220		µs
t_{OFFdly}	Turn Off delay(1)	EN/UVLO↓ to BFET↓, C_{BFET} = 0		0.4		µs
dV/dT (OUTPUT RAMP CONTROL)						
t_{dVdT}	Output ramp time	EN/UVLO → H to OUT = 11.7 V, C_{dVdT} = 0	0.7	1	1.3	ms
		EN/UVLO → H to OUT = 11.7 V, C_{dVdT} = 1 nF(1)		12		
ILIM (CURRENT LIMIT PROGRAMMING)						
$t_{FastOffDly}$	Fast-Trip comparator delay(1)	I_{OUT} > $I_{FASTRIP}$ to I_{OUT}= 0 (Switch Off)		300		ns
BFET (BLOCKING FET GATE DRIVER)						
$t_{BFET-ON}$	BFET Turn-On duration(1)	EN/UVLO → H to V_{BFET} = 12 V, C_{BFET} = 1 nF		4.2		ms
		EN/UVLO → H to VB_{FET} = 12 V, C_{BFET} = 10 nF		42		
$t_{BFET-OFF}$	BFET Turn-Off duration(1)	EN/UVLO → L to $_{VBFET}$ = 1 V, C_{BFET} = 1 nF		0.4		µs
		EN/UVLO → L to V_{BFET} = 1 V, C_{BFET} = 10 nF		1.4		
THERMAL SHUTDOWN (TSD)						
t_{TSDdly}	Retry delay after TSD recovery, T_J < [T_{SHDN} - 10°C](1)	TPS259241 only		100		µs

(1) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

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7.7 Typical Characteristics

T_J = 25°C, V_{VIN} = 12 V, $V_{EN/UVLO}$ = 2 V, R_{ILIM} = 100 kΩ, C_{VIN} = 0.1 µF, C_{OUT} = 1 µF, C_{dVdT} = OPEN (unless stated otherwise)

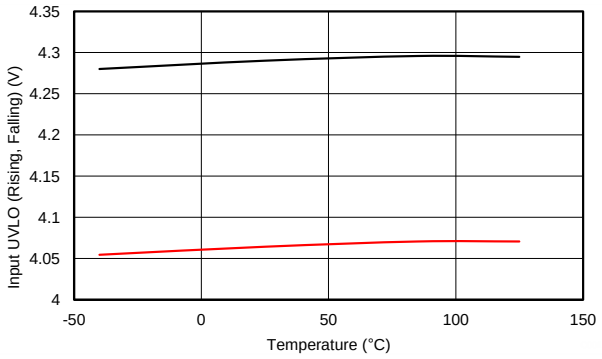


Figure 1. Input UVLO vs Temperature

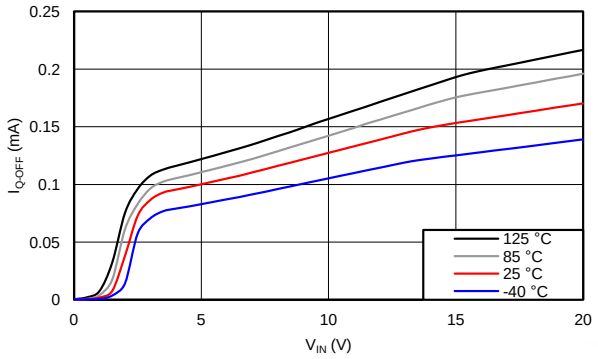


Figure 2. I_{Q-OFF} vs V_{IN}

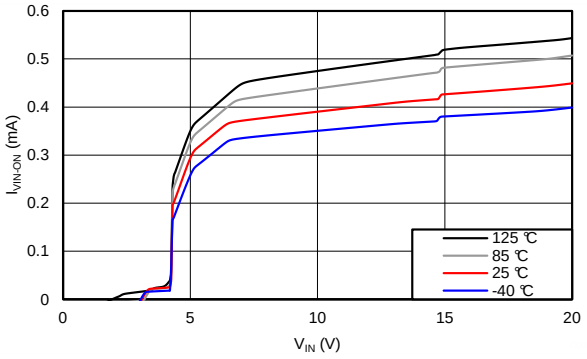


Figure 3. I_{VIN-ON} vs V_{IN}

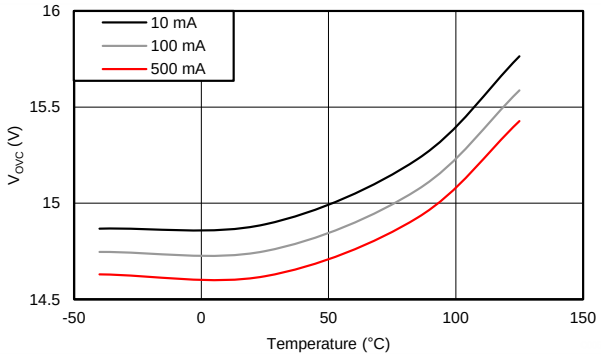


Figure 4. V_{OVC} vs Temperature Across I_{OUT}

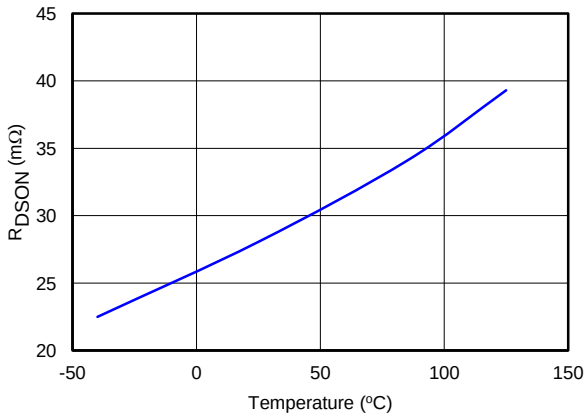


Figure 5. R_{DSON} vs Temperature

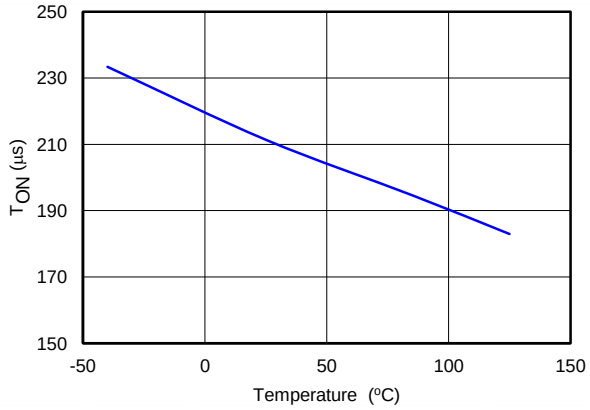


Figure 6. T_{ON} vs Temperature

Typical Characteristics (continued)

T_J = 25°C, V_{VIN} = 12 V, $V_{EN/UVLO}$ = 2 V, R_{ILIM} = 100 kΩ, C_{VIN} = 0.1 µF, C_{OUT} = 1 µF, C_{dVdT} = OPEN (unless stated otherwise)

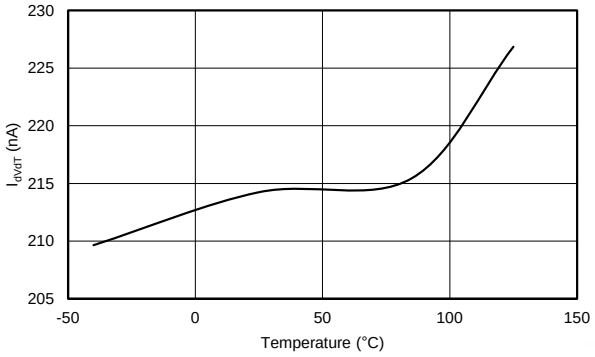


Figure 7. I_{dVdT} vs Temperature

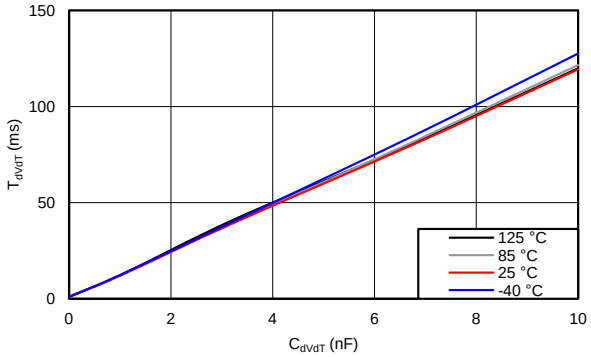


Figure 8. T_{dVdT} vs C_{dVdT}

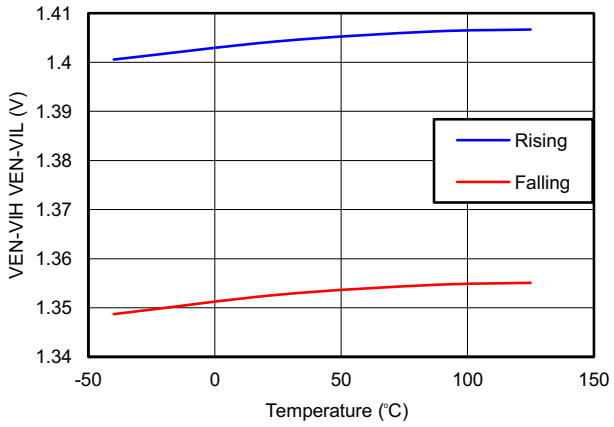


Figure 9. V_{EN-VIH}, V_{EN-VIL} vs Temperature

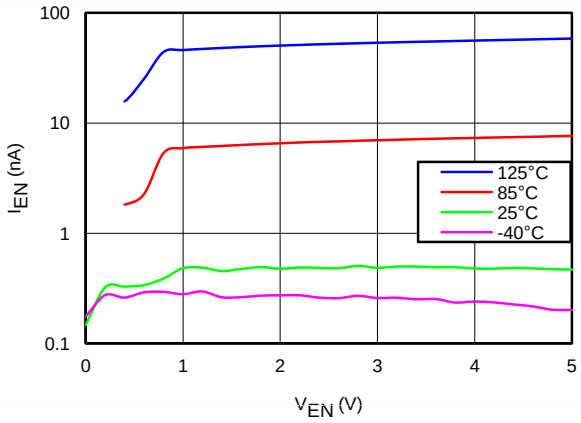
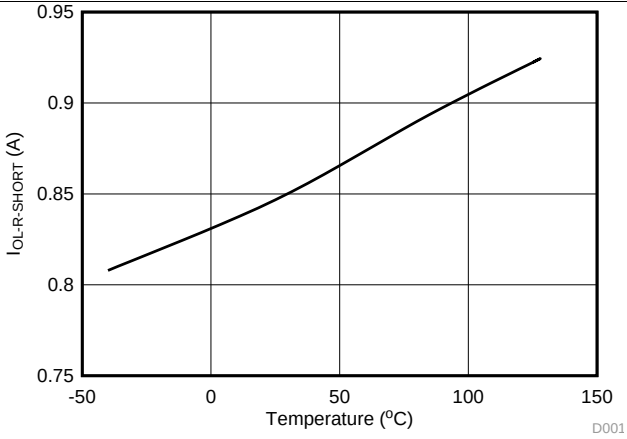
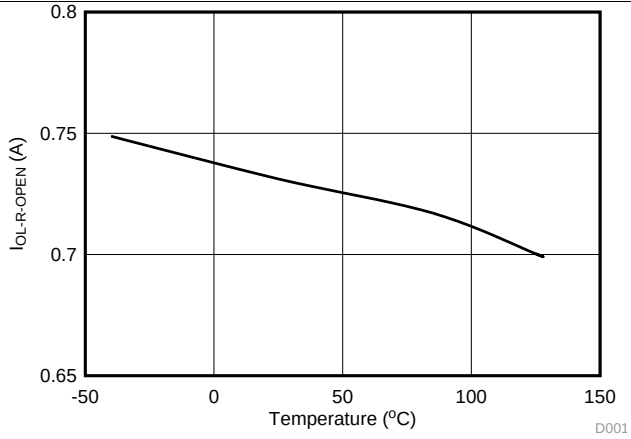


Figure 10. I_{EN} (Leakage Current) vs V_{EN}



R_{ILIM} = 0 Ω

Figure 11. $I_{OL-R-Short}$ vs Temperature



R_{ILIM} = OPEN

Figure 12. $I_{OL-R-Open}$ vs Temperature

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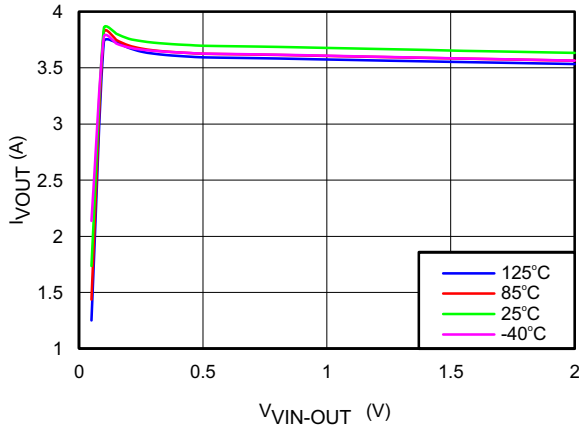
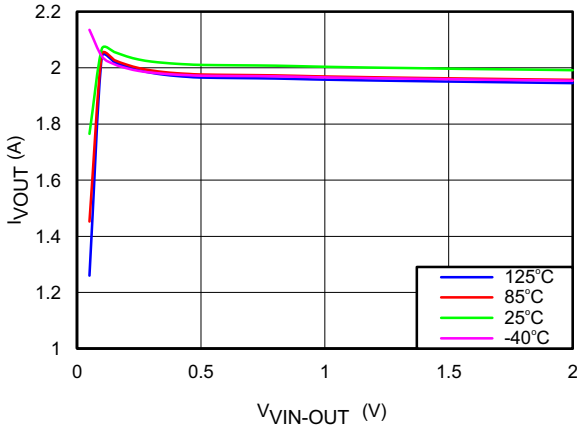
Typical Characteristics (continued)

T_J = 25°C, V_{VIN} = 12 V, $V_{EN/UVLO}$ = 2 V, R_{ILIM} = 100 kΩ, C_{VIN} = 0.1 µF, C_{OUT} = 1 µF, C_{dVdT} = OPEN (unless stated otherwise)



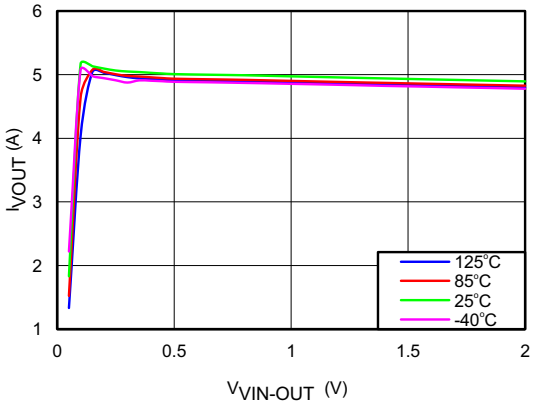
R_{ILIM} = 100 kΩ

Figure 13. I_{VOUT} vs $V_{VIN-OUT}$



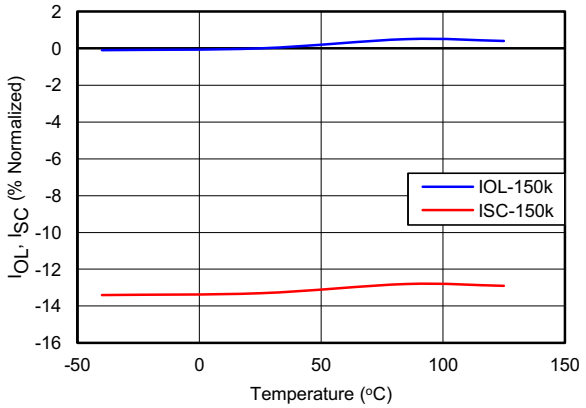
R_{ILIM} = 45.3 kΩ

Figure 14. I_{VOUT} vs $V_{VIN-OUT}$



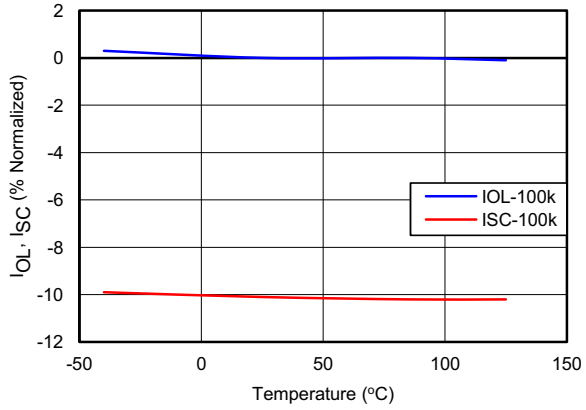
R_{ILIM} = 150 kΩ

Figure 15. I_{VOUT} vs $V_{VIN-OUT}$



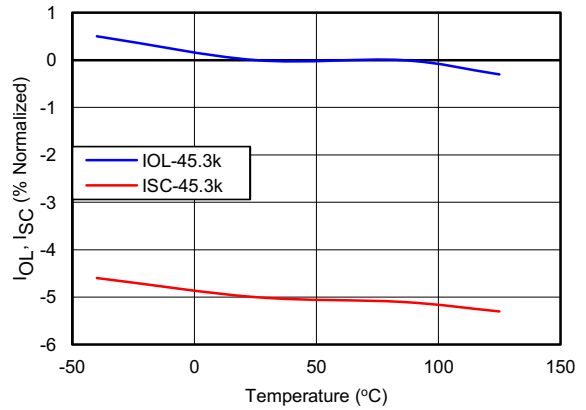
R_{ILIM} = 150 kΩ

Figure 16. I_{OL}, I_{SC} vs Temperature



R_{ILIM} = 100 kΩ

Figure 17. I_{OL}, I_{SC} vs Temperature



R_{ILIM} = 45.3 kΩ

Figure 18. I_{OL}, I_{SC} vs Temperature

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Typical Characteristics (continued)

T_J = 25°C, V_{VIN} = 12 V, $V_{EN/UVLO}$ = 2 V, R_{ILIM} = 100 kΩ, C_{VIN} = 0.1 µF, C_{OUT} = 1 µF, C_{dVdT} = OPEN (unless stated otherwise)

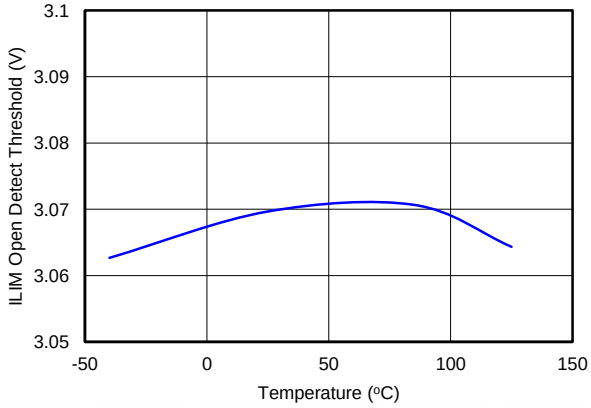


Figure 19. $V_{OpenILIM}$ vs Temperature

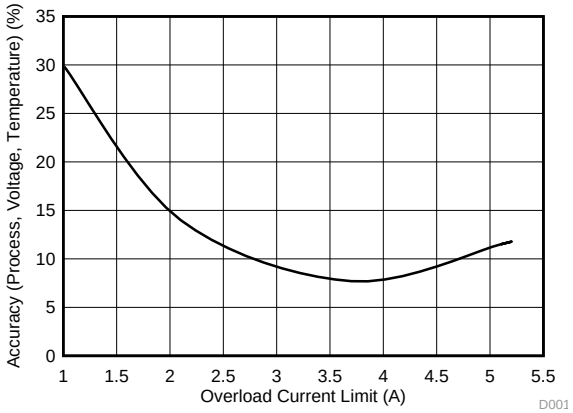


Figure 20. Accuracy vs Overload Current Limit

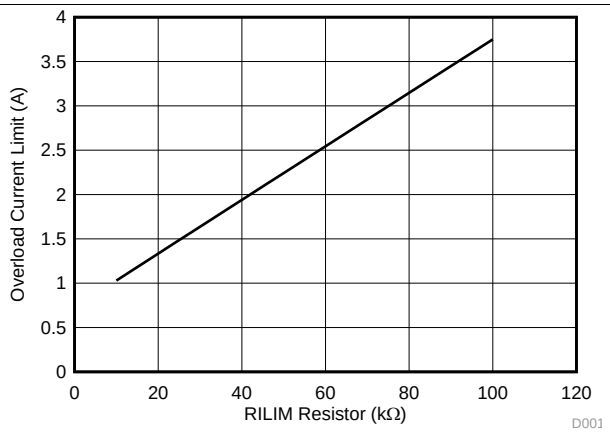


Figure 21. Overload Current Limit vs RILIM Resistor

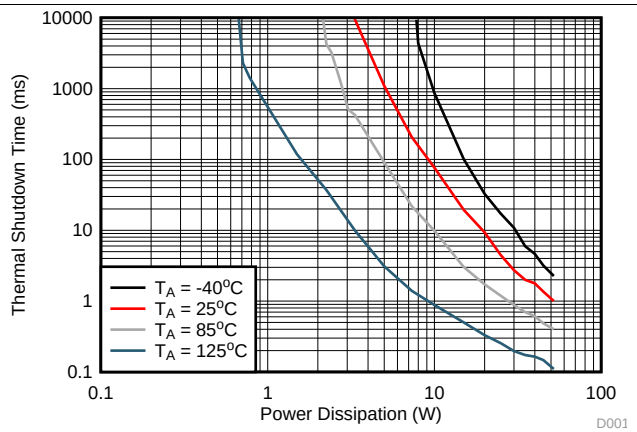


Figure 22. Thermal Shutdown Time vs Power Dissipation

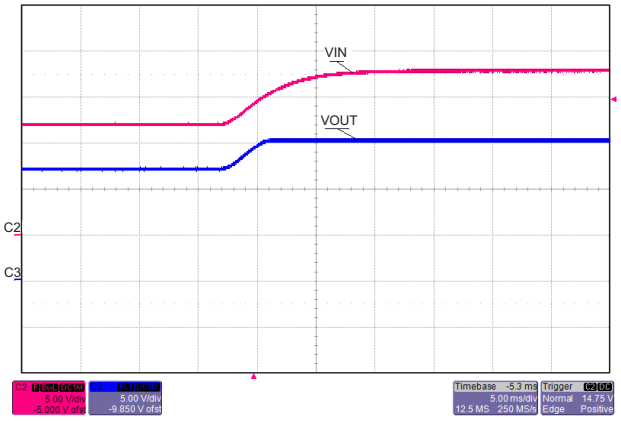
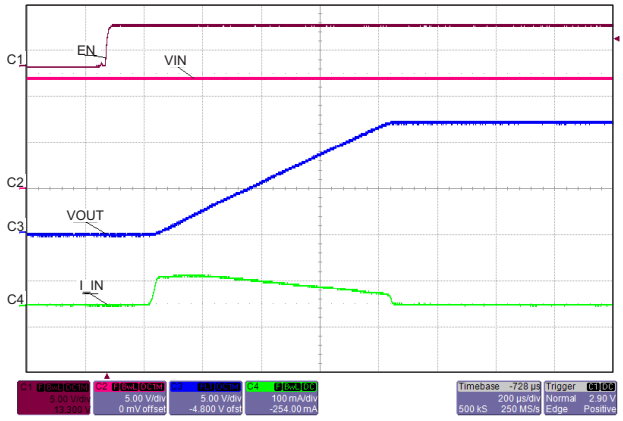


Figure 23. Transient: Over-Voltage Clamp



C_{dVdT} = OPEN, C_{OUT} = 4.7 µF

Figure 24. Transient: Output Ramp

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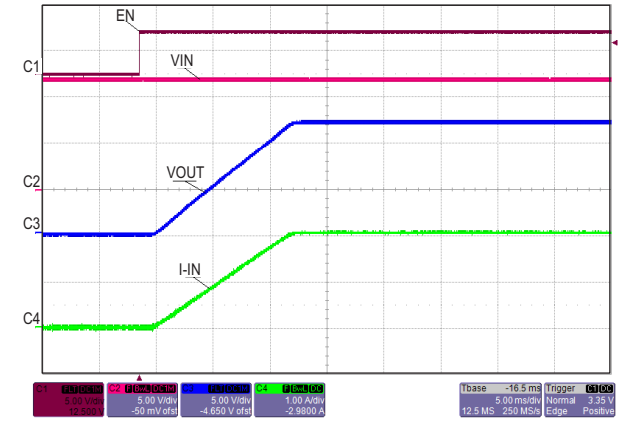
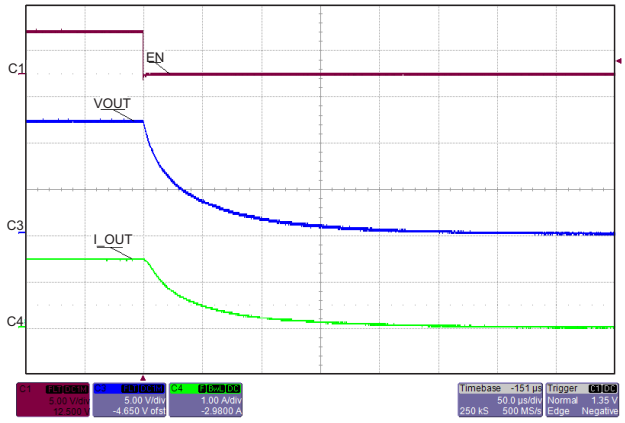
Typical Characteristics (continued)

T_J = 25°C, V_{VIN} = 12 V, $V_{EN/UVLO}$ = 2 V, R_{ILIM} = 100 kΩ, C_{VIN} = 0.1 µF, C_{OUT} = 1 µF, C_{dVdT} = OPEN (unless stated otherwise)



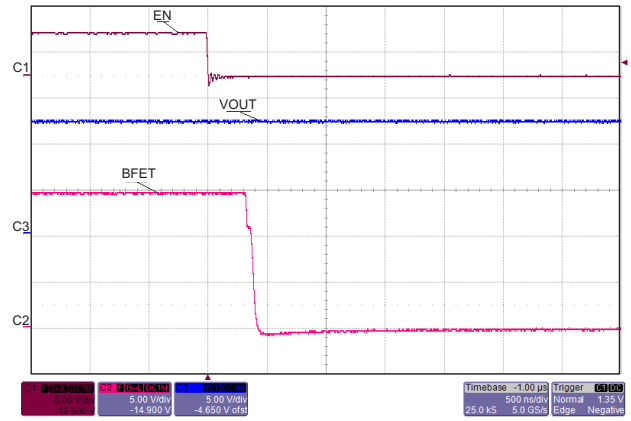
C_{dVdT} = 1nF, C_{OUT} = 10 µF, R_{OUT} = 5.7Ω

Figure 25. Transient: Output Ramp



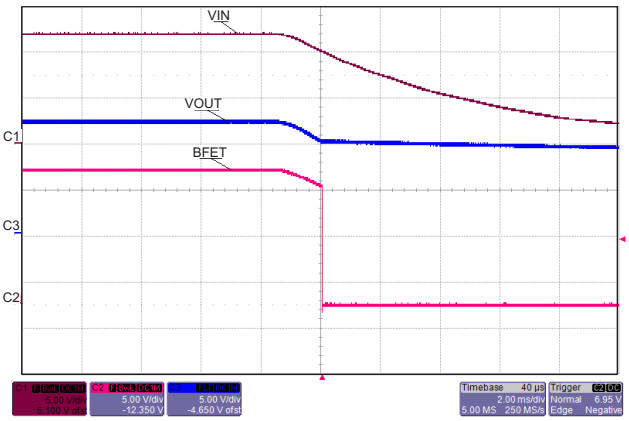
EN ↓

Figure 26. Transient: Turn Off Delay



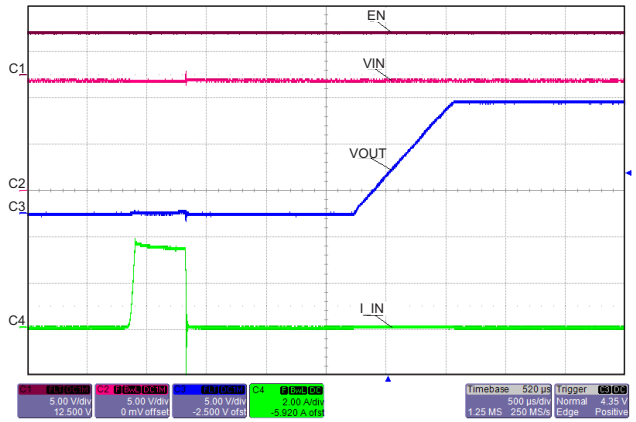
EN ↓

Figure 27. Turn Off Delay to BFET



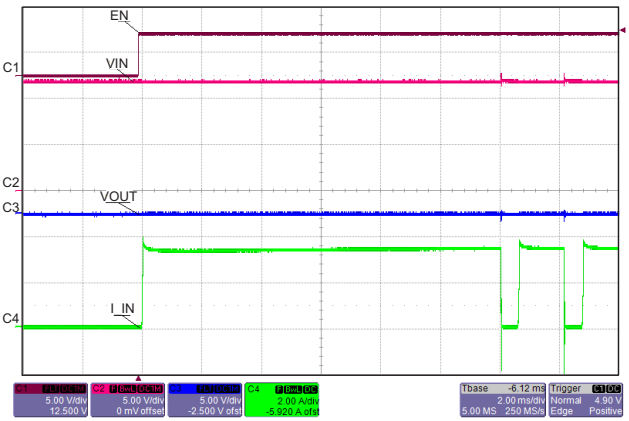
VIN↓

Figure 28. Turn Off Delay to BFET



TPS259241

Figure 29. Transient: Recovery From Short Circuit / Over Current



TPS259241

Figure 30. Transient: Wake Up to Short Circuit

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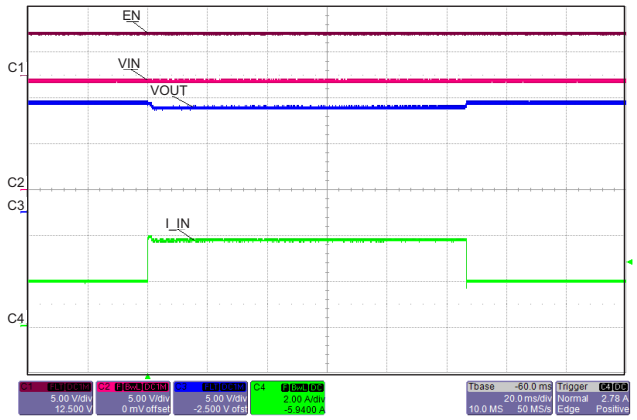
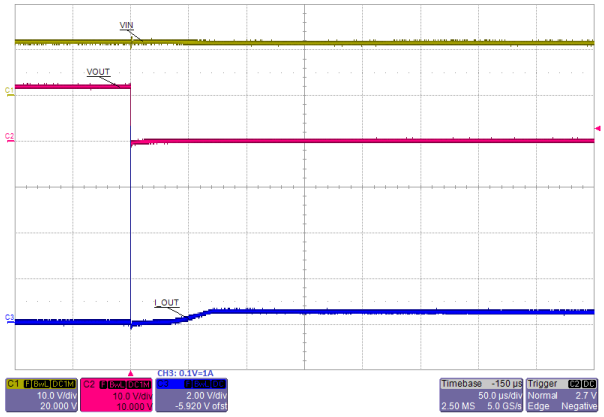
Typical Characteristics (continued)

T_J = 25°C, V_{VIN} = 12 V, $V_{EN/UVLO}$ = 2 V, R_{ILIM} = 100 kΩ, C_{VIN} = 0.1 µF, C_{OUT} = 1 µF, C_{dVdT} = OPEN (unless stated otherwise)



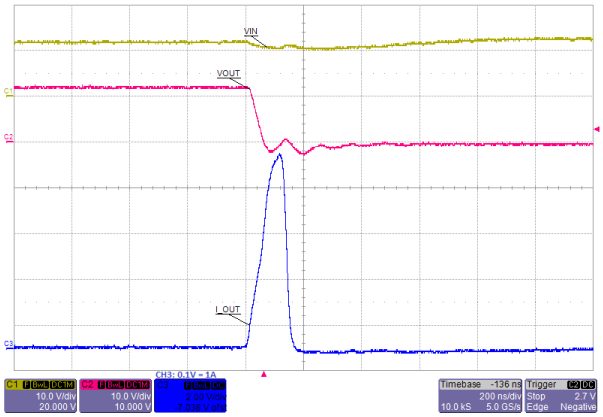
I_{LOAD} Stepped From 50% to 120%, back to 50%

Figure 31. Transient: Overload Current Limit



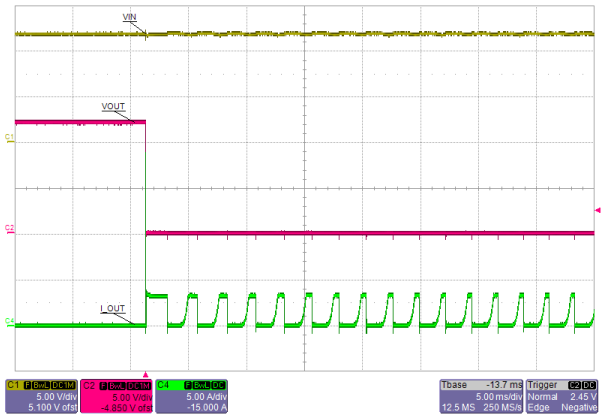
R_{ILIM} = 150 kΩ

Figure 32. Transient: Output Short Circuit



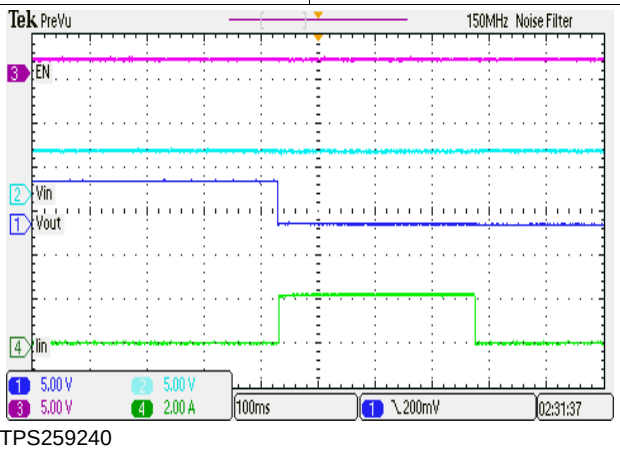
R_{ILIM} = 150 kΩ

Figure 33. Short Circuit (Zoom): Fast-Trip Comparator



TPS259241

Figure 34. Transient: Thermal Fault Auto-Retry



TPS259240

Figure 35. Transient: Thermal Fault Latched

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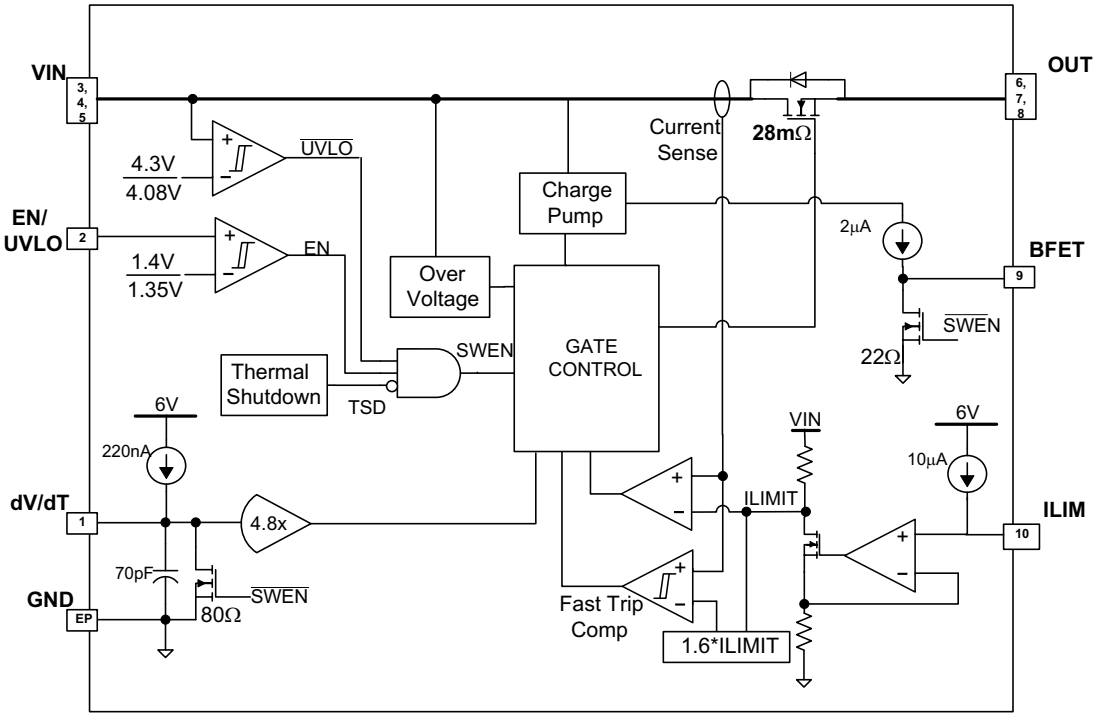
8 Detailed Description

8.1 Overview

The TPS25924x is an e-fuse with integrated power switch that is used to manage current/voltage/start-up voltage ramp to a connected load. The device starts its operation by monitoring the VIN bus. When VIN exceeds the undervoltage-lockout threshold (V_{UVR}), the device samples the EN/UVLO pin. A high level on this pin enables the internal MOSFET. As VIN rises, the internal MOSFET of the device will start conducting and allow current to flow from VIN to OUT. When EN/UVLO is held low (below V_{ENF}), internal MOSFET is turned off. User also has the ability to modify the output voltage ramp time by connecting a capacitor between dV/dT pin and GND.

After a successful start-up sequence, the device now actively monitors its load current and input voltage, ensuring that the adjustable overload current limit I_{OL} is not exceeded and input voltage spikes are safely clamped to V_{OVC} level at the output. This keeps the output device safe from harmful voltage and current transients. The device also has built-in thermal sensor. In the event device temperature (T_J) exceeds T_{SHDN}, typically 150°C, the thermal shutdown circuitry will shut down the internal MOSFET thereby disconnecting the load from the supply. In TPS259240, the output will remain disconnected (MOSFET open) until power to device is recycled or EN/UVLO is toggled (pulled low and then high). The TPS259241 device will remain off during a cooling period until device temperature falls below T_{SHDN} – 10°C, after which it will attempt to restart. This ON and OFF cycle will continue until fault is cleared.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 GND

This is the most negative voltage in the circuit and is used as a reference for all voltage measurements unless otherwise specified.

Feature Description (continued)

8.3.2 VIN

Input voltage to the TPS25924x. A ceramic bypass capacitor close to the device from VIN to GND is recommended to alleviate bus transients. The recommended operating voltage range is 4.5 V to 13.8 V for TPS25924x. The device can continuously sustain a voltage of 20 V on VIN pin. However, above the recommended maximum bus voltage, the device will be in over-voltage protection (OVP) mode, limiting the output voltage to V_{OVC}. The power dissipation in OVP mode is P_{D_OVP} = (V_{VIN} – V_{OVC}) x I_{OUT}, which can potentially heat up the device and cause thermal shutdown.

8.3.3 dV/dT

Connect a capacitor from this pin to GND to control the slew rate of the output voltage at power-on. This pin can be left floating to obtain a predetermined slew rate (minimum T_{dVdT}) on the output. Equation governing slew rate at start-up is shown below:

$$\frac{dV_{OUT}}{dt} = \frac{I_{dVdT} \times GAIN_{dVdT}}{C_{dVdT} + C_{INT}} \quad (1)$$

Where:

I_{dVdT} = 220 nA (TYP)
C_{INT} = 70 pF (TYP)
$GAIN_{dVdT}$ = 4.85
$\frac{dV_{OUT}}{dT}$ = Desired output slew rate

The total ramp time (T_{dVdT}) for 0 to VIN can be calculated using the following equation:

$$T_{dVdT} = 10^6 \times V_{IN} \times (C_{dVdT} + 70\ pF) \quad (2)$$

For details on how to select an appropriate charging time/rate, refer to the applications section *Setting Output Voltage Ramp Time (T_{dVdT})*.

8.3.4 BFET

Connect this pin to an external NFET that can be used to disconnect input supply from rest of the system in the event of power failure at VIN. The BFET pin is controlled by either input UVLO (V_{UVR}) event or EN/UVLO (see Table 1). BFET can source charging current of 2 µA (TYP) and sink (discharge) current from the gate of the external FET via a 26-Ω internal discharge resistor to initiate fast turn-off, typically <1 µs. Due to 2 µA charging current, it is recommended to use >10 MΩ impedance when probing the BFET node.

Table 1. BFET

EN/UVLO > V_{ENR}	VIN>V_{UVR}	BFET MODE
H	H	Charge
X	L	Discharge
L	X	Discharge

8.3.5 EN/UVLO

As an input pin, it controls both the ON/OFF state of the internal MOSFET and that of the external blocking FET. In its high state, the internal MOSFET is enabled and charging begins for the gate of external FET. A low on this pin will turn off the internal MOSFET and pull the gate of the external FET to GND via the built-in discharge resistor. High and Low levels are specified in the parametric table of the datasheet. The EN/UVLO pin is also used to clear a thermal shutdown latch in the TPS259240 by toggling this pin (H→L).

The internal de-glitch delay on EN/UVLO falling edge is intentionally kept low (1 us typical) for quick detection of power failure. When used with a resistor divider from supply to EN/UVLO to GND, power-fail detection on EN/UVLO helps in quick turn-off of the BFET driver, thereby stopping the flow of reverse current (see typical application diagram, Figure 43). For applications where a higher de-glitch delay on EN/UVLO is desired, or when the supply is particularly noisy, it is recommended to use an external bypass capacitor from EN/UVLO to GND.

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8.3.6 ILIM

The device continuously monitors the load current and keeps it limited to the value programmed by R_{ILIM}. After start-up event and during normal operation, current limit is set to I_{OL} (over-load current limit).

$$I_{OL} = \left(0.7 + 3 \times 10^{-5} \times R_{ILIM}\right) \quad (3)$$

When power dissipation in the internal MOSFET [$P_D = (V_{VIN} - V_{OUT}) \times I_{OUT}$] exceeds 10 W, there is a 2% – 12% thermal foldback in the current limit value so that I_{OL} drops to I_{SC}. In each of the two modes, MOSFET gate voltage is regulated to throttle short-circuit and overload current flowing to the load. Eventually, the device shuts down due to over temperature.

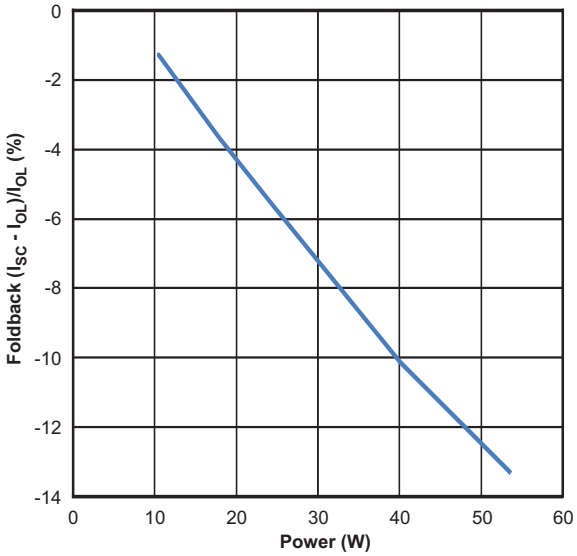

Figure 36. Thermal Foldback in Current Limit

During a transient short circuit event, the current through the device increases very rapidly. The current-limit amplifier cannot respond very quickly to this event due to its limited bandwidth. Therefore, the TPS25924x incorporates a fast-trip comparator, which shuts down the pass device very quickly when $I_{OUT} > I_{FASTRIP}$, and terminates the rapid short-circuit peak current. The trip threshold is set to 60% higher than the programmed over-load current limit ($I_{FASTRIP} = 1.6 \times I_{OL}$). After the transient short-circuit peak current has been terminated by the fast-trip comparator, the current limit amplifier smoothly regulates the output current to I_{OL} (see figure below).

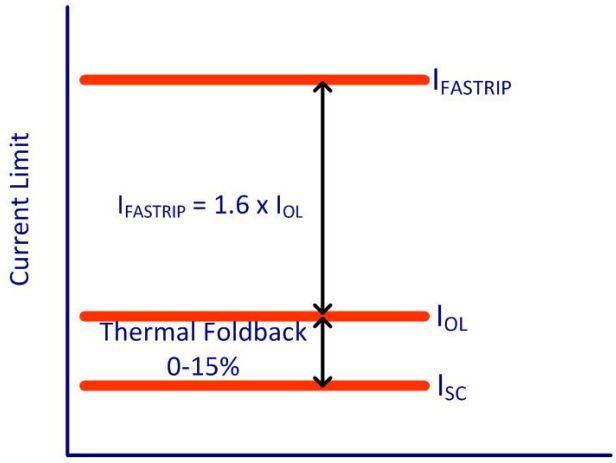

Figure 37. Fast-Trip Current

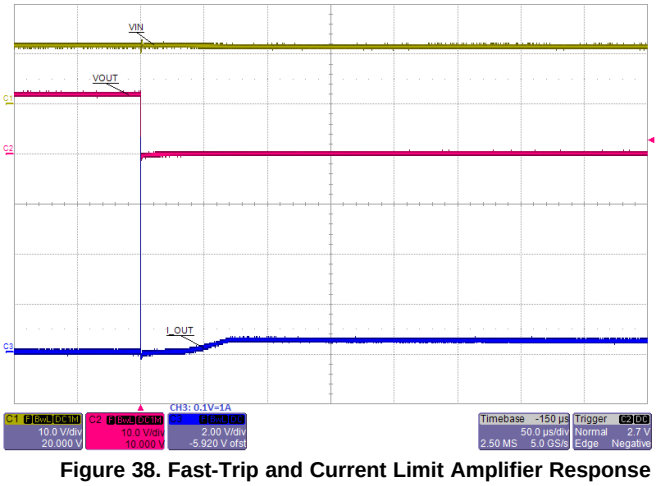

Figure 38. Fast-Trip and Current Limit Amplifier Response for Short Circuit

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8.4 Device Functional Modes

The TPS25924x is a hot-swap controller with integrated power switch that is used to manage current/voltage/start-up voltage ramp to a connected load. The device starts its operation by monitoring the VIN bus. When V_{VIN} exceeds the undervoltage-lockout threshold (V_{UVR}), the device samples the EN/UVLO pin. A high level on this pin enables the internal MOSFET and also start charging the gate of external blocking FET (if connected) via the BFET pin. As VIN rises, the internal MOSFET of the device and external FET (if connected) will start conducting and allow current to flow from VIN to OUT. When EN/UVLO is held low (that is, below V_{ENF}), the internal MOSFET is turned off and BFET pin is discharged, thereby, blocking the flow of current from VIN to OUT. User also has the ability to modify the output voltage ramp time by connecting a capacitor between dV/dT pin and GND.

Having successfully completed its start-up sequence, the device now actively monitors its load current and input voltage, ensuring that the adjustable overload current limit I_{OL} is not exceeded and input voltage spikes are safely clamped to V_{OVC} level at the output. This keeps the output device safe from harmful voltage and current transients. The device also has built-in thermal sensor. In the event device temperature (T_J) exceeds T_{SHDN}, typically 150°C, the thermal shutdown circuitry will shut down the internal MOSFET thereby disconnecting the load from the supply. In the TPS259240, the output will remain disconnected (MOSFET open) until power to device is recycled or EN/UVLO is toggled (pulled low and then high). The TPS259241 device will remain off during a cooling period until device temperature falls below T_{SHDN} – 10°C, after which it will attempt to restart. This ON and OFF cycle will continue until fault is cleared.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS25924x is a smart eFuse. It is typically used for Hot-Swap and Power rail protection applications. It operates from 4.5 V to 18 V with programmable current limit and undervoltage protection. The device aids in controlling the in-rush current and provides precise current limiting during overload conditions for systems such as Set-Top-Box, DTVs, Gaming Consoles, SSDs/HDDs and Smart Meters. The device also provides robust protection for multiple faults on the sub-system rail.

The following design procedure can be used to select component values for the device. Alternatively, the WEBENCH® software may be used to generate a complete design. The WEBENCH® software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. Additionally, a spreadsheet design tool *TPS2592xx Design Calculator* (SLUC570) is available on web folder. This section presents a simplified discussion of the design process.

9.2 Typical Applications

9.2.1 Simple 3.7-A eFuse Protection for Set Top Boxes

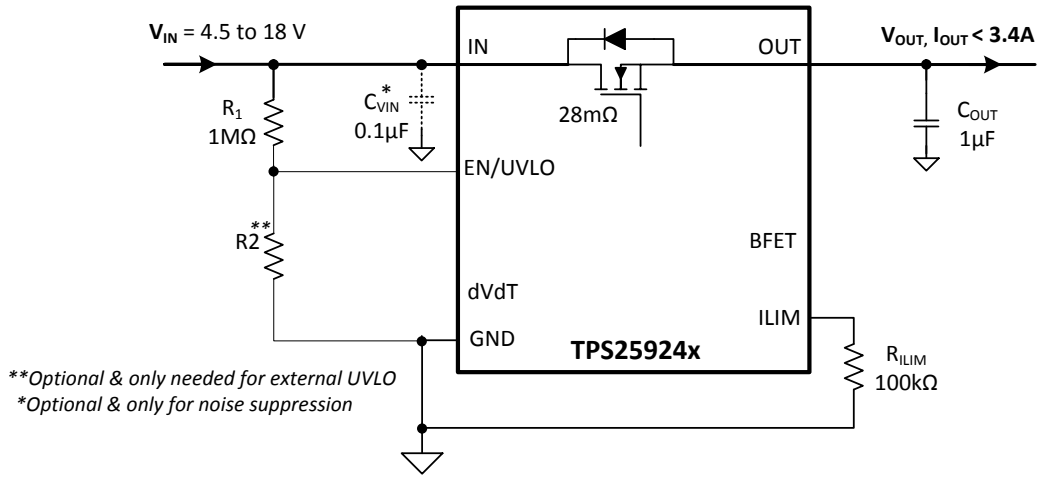

Figure 39. Typical Application Schematic: Simple 3.7-A e-Fuse for STBs

9.2.1.1 Design Requirements

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range, V_{IN}	12 V
Undervoltage lockout set point, $V_{(UV)}$	Default: V_{UVR} = 4.3 V
Overvoltage protection set point, $V_{(OV)}$	Default: V_{OVC} = 15 V
Load at start-up, $R_{L(SU)}$	4 Ω
Current limit, $I_{OL} = I_{ILIM}$	3.7 A
Load capacitance, C_{OUT}	1 µF
Maximum ambient temperature, T_A	85°C

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9.2.1.2 Detailed Design Procedure

The following design procedure can be used to select component values for the TPS25924x.

9.2.1.2.1 Step by Step Design Procedure

This design procedure below seeks to control the junction temperature of device under both static and transient conditions by proper selection of output ramp-up time and associated support components. The designer can adjust this procedure to fit the application and design criteria.

9.2.1.2.2 Programming the Current-Limit Threshold: R_{ILIM} Selection

The R_{ILIM} resistor at the ILIM pin sets the over load current limit, this can be set using Equation 4.

$$R_{ILIM} = \frac{I_{ILIM} - 0.7}{3 \times 10^{-5}} \quad (4)$$

For $I_{OL} = I_{ILIM}$ = 3.7 A, from Equation 4, R_{ILIM} = 100 kΩ, choose closest standard value resistor with 1% tolerance.

9.2.1.2.3 Undervoltage Lockout Set Point

The undervoltage lockout (UVLO) trip point is adjusted using the external voltage divider network of R_1 and R_2 as connected between IN, EN/UVLO and GND pins of the device. The values required for setting the undervoltage are calculated solving Equation 5.

$$V_{(UV)} = \frac{R_1 + R_2}{R_2} \times V_{ENR} \quad (5)$$

Where V_{ENR} = 1.4 V is enable voltage rising threshold.

Since R_1 and R_2 will leak the current from input supply (VIN), these resistors should be selected based on the acceptable leakage current from input power supply (VIN). The current drawnby R_1 and R_2 from the power supply {$I_{R12} = V_{IN}/(R_1 + R_2)$}.

However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, I_{R12} must be chosen to be 20x greater than the leakage current expected.

For default UVLO of V_{UVR} = 4.3 V, select R_2 = OPEN, and R_1 = 1 MΩ. Since EN/UVLO pin is rated only to 7 V, it cannot be connected directly to V_{IN}= 12 V. It has to be connected through R_1 = 1 MΩ only, so that the pull-up current for EN/UVLO pin is limited to < 20 µA.

The power failure threshold is detected on the falling edge of supply. This threshold voltage is 4% lower than the rising threshold, V_{UVR}. This is calculated using Equation 6.

$$V_{(PFAIL)} = 0.96 \times V_{UVR} \quad (6)$$

Where V_{UVR} is 4.3 V, Power fail threshold set is 4.1 V.

9.2.1.2.4 Setting Output Voltage Ramp Time (T_{dVdT})

For a successful design, the junction temperature of device should be kept below the absolute-maximum rating during both dynamic (start-up) and steady state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and in-rush current limit required with system capacitance to avoid thermal shutdown during start-up with and without load.

The ramp-up capacitor C_{dVdT} needed is calculated considering the two possible cases:

9.2.1.2.4.1 Case 1: Start-Up without Load: Only Output Capacitance C_{OUT} Draws Current During Start-Up

During start-up, as the output capacitor charges, the voltage difference as well as the power dissipated across the internal FET decreases. The average power dissipated in the device during start-up is calculated using Equation 8.

For TPS25924x, the inrush current is determined as:

$$I_{(INRUSH)} = C_{(OUT)} \times \frac{V_{(IN)}}{T_{dVdT}} \quad (7)$$

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Power dissipation during start-up is:

$$P_{D(INRUSH)} = 0.5 \times V_{(IN)} \times I_{(INRUSH)} \quad (8)$$

Equation 8 assumes that load does not draw any current until the output voltage has reached its final value.

9.2.1.2.4.2 Case 2: Start-Up with Load: Output Capacitance C_{OUT} and Load Draws Current During Start-Up

When load draws current during the turn-on sequence, there will be additional power dissipated. Considering a resistive load during start-up ($R_{L(SU)}$), load current ramps up proportionally with increase in output voltage during T_{dVdT} time. The average power dissipation in the internal FET during charging time due to resistive load is given by:

$$P_{D(LOAD)} = \left(\frac{1}{6}\right) \times \frac{V^2_{(IN)}}{R_{L(SU)}} \quad (9)$$

Total power dissipated in the device during startup is:

$$P_{D(STARTUP)} = P_{D(INRUSH)} + P_{D(LOAD)} \quad (10)$$

Total current during startup is given by:

$$I_{(STARTUP)} = I_{(INRUSH)} + I_L(t) \quad (11)$$

If $I_{(STARTUP)} > I_{OL}$, the device limits the current to I_{OL} and the current limited charging time is determined by:

$$T_{dVdT(Current\text{-}Limited)} = C_{OUT} \times R_{L(SU)} \times \left[\frac{I_{OL}}{I_{(INRUSH)}} - 1 + LN\left(\frac{I_{(INRUSH)}}{I_{OL} - \frac{V_{(IN)}}{R_{L(SU)}}}\right)\right] \quad (12)$$

The power dissipation, with and without load, for selected start-up time should not exceed the shutdown limits as shown in Figure 40.

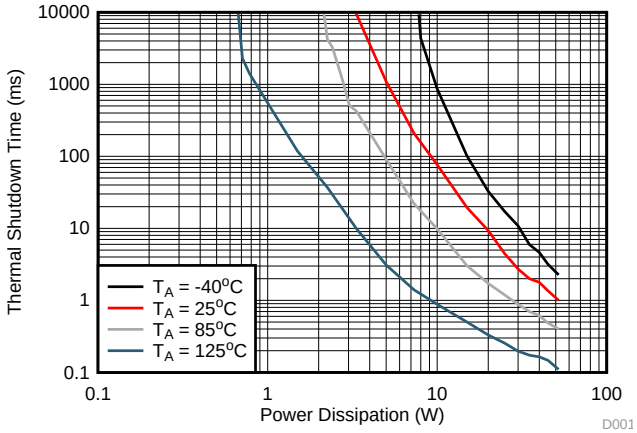

Figure 40. Thermal Shutdown Limit Plot

For the design example under discussion, select ramp-up capacitor C_{dVdT} = OPEN. Then, using Equation 2.

$$T_{dVdT} = 10^6 \times 12 \times (0 + 70\ pF) = 840\ \mu s \quad (13)$$

The inrush current drawn by the load capacitance (C_{OUT}) during ramp-up using Equation 7.

$$I_{(INRUSH)} = 1\ \mu F \times \frac{12}{840\ \mu s} = 15\ mA \quad (14)$$

The inrush Power dissipation is calculated, using Equation 8.

$$P_{D(INRUSH)} = 0.5 \times 12 \times 15\ m = 90\ mW \quad (15)$$

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For 90 mW of power loss, the thermal shut down time of the device should not be less than the ramp-up time T_{dVdT} to avoid the false trip at maximum operating temperature. From thermal shutdown limit graph Figure 40 at T_A = 85°C, for 90 mW of power, the shutdown time is infinite. So it is safe to use 0.79 ms as start-up time without any load on output.

Considering the start-up with load 4 Ω, the additional power dissipation, when load is present during start up is calculated, using Equation 9.

$$P_{D(LOAD)} = \frac{12 \times 12}{6 \times 4} = 6 \text{ W} \quad (16)$$

The total device power dissipation during start up, using Equation 10 is:

$$P_{D(STARTUP)} = 6 + 90 \text{ m} = 6.09 \text{ W} \quad (17)$$

From thermal shutdown limit graph at T_A = 85°C, the thermal shutdown time for 6.09 W is more than 10 ms. So it is well within acceptable limits to not use an external capacitor ($C_{dV/dT}$) with start-up load of 4 Ω.

If, due to large C_{OUT}, there is a need to decrease the power loss during start-up, it can be done with increase of C_{dVdT} capacitor.

9.2.1.2.5 Support Component Selection - C_{VIN}

C_{VIN} is a bypass capacitor to help control transient voltages, unit emissions, and local supply noise. Where acceptable, a value in the range of 0.001 µF to 0.1 µF is recommended for C_{VIN}.

9.2.1.3 Application Curves

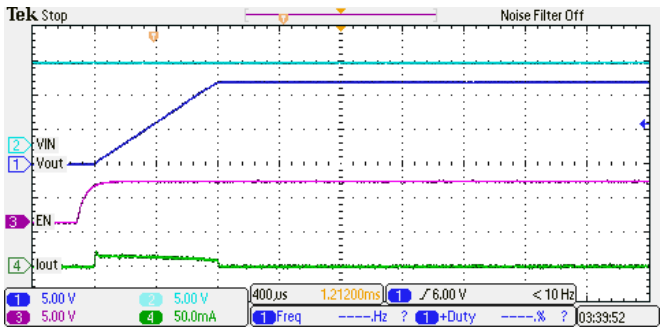

Figure 41. Output Ramp without Load on Output

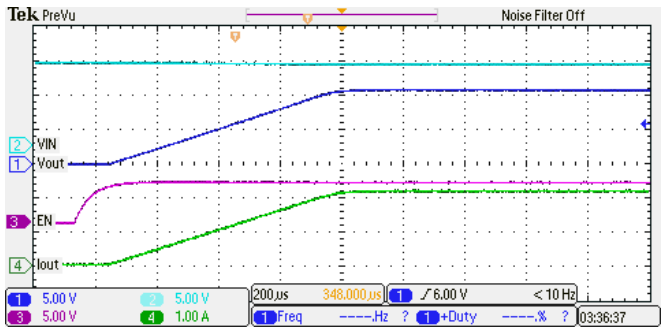

Figure 42. Output Ramp with 4-Ω Load at Start Up

9.2.2 Inrush and Reverse Current Protection for Hold-Up Capacitor Application (for example, SSD)

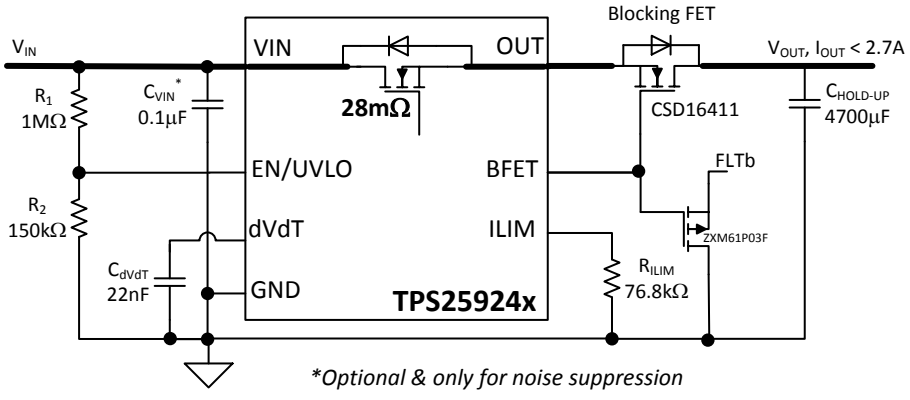

Figure 43. Inrush and Reverse Current Protection for Hold-Up Capacitor Application (for example, SSD) (TPS25924x UVLO is used as power fail comparator)

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9.2.2.1 Design Requirements

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range, V_{IN}	12 V
Undervoltage lockout set point, $V_{(UV)}$	10.8 V
Overvoltage protection set point, $V_{(OV)}$	Default: V_{OVC} = 15 V
Load at start-up, $R_{L(SU)}$	1000 Ω
Current limit, I_{OL}= I_{ILIM}	3 A
Load capacitance, C_{OUT}	4700 µF
Maximum ambient temperature, T_A	85°C

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Programming the Current-Limit Threshold: R_{ILIM} Selection

The R_{ILIM} resistor at the ILIM pin sets the over load current limit, this can be set using Equation 4.

For I_{OL} = I_{ILIM} = 3 A, from Equation 4, R_{ILIM} = 76.8 kΩ. Choose closest standard value resistor with 1% tolerance.

9.2.2.2.2 Undervoltage Lockout Set Point

The undervoltage lockout (UVLO) trip point is adjusted using the external voltage divider network of R_1 and R_2 as connected between IN, EN/UVLO and GND pins of the device. The values required for setting the undervoltage are calculated solving Equation 5.

For UVLO of $V_{(UV)}$ = 10.8 V, select R_2 = 150 kΩ, and R_1 = 1 MΩ.

The power failure threshold is detected on the falling edge of supply. This threshold voltage is 4% lower than the rising threshold, $V_{(UV)}$. This is calculated using Equation 6.

Where $V_{(UV)}$ = 10.73 V, Power fail threshold set is $V_{(PFAIL)}$ = 10.35 V.

9.2.2.2.3 Setting Output Voltage Ramp Time (T_{dVdT})

For a successful design, the junction temperature of device should be kept below the absolute-maximum rating during both dynamic (start-up) and steady state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and in-rush current limit required with system capacitance to avoid thermal shutdown during start-up with and without load.

For the design example under discussion, select ramp-up capacitor C_{dVdT} = 22 nF. Then, using Equation 2.

$$T_{dVdT} = 10^6 \times 12 \times (22\ nF + 70\ pF) = 265\ ms \quad (18)$$

The inrush current drawn by the load capacitance (C_{OUT}) during ramp-up using Equation 7.

$$I_{(INRUSH)} = 4700\ \mu F \times \frac{12}{265\ ms} = 213\ mA \quad (19)$$

The inrush Power dissipation is calculated, using Equation 8.

$$P_{D(INRUSH)} = 0.5 \times 12 \times 213\ m = 1278\ mW \quad (20)$$

Considering the start-up with load 1000 Ω, the additional power dissipation, when load is present during start up is calculated, using Equation 9.

$$P_{D(LOAD)} = \frac{12 \times 12}{6 \times 1000} = 24\ mW \quad (21)$$

The total device power dissipation during start up is:

$$P_{D(STARTUP)} = 1278 + 24 = 1302\ mW \quad (22)$$

From thermal shutdown limit graph at T_A = 85°C, the thermal shutdown time for 1.3 W is more than 300 ms. So the device will start safely.

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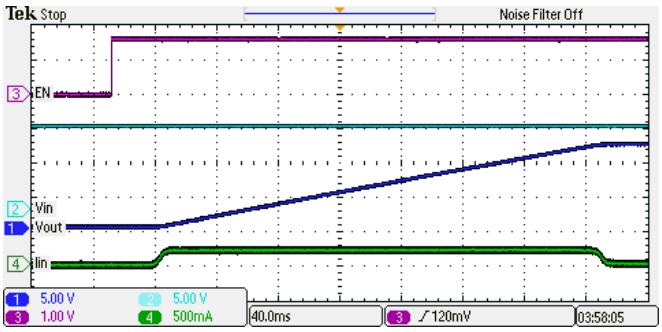
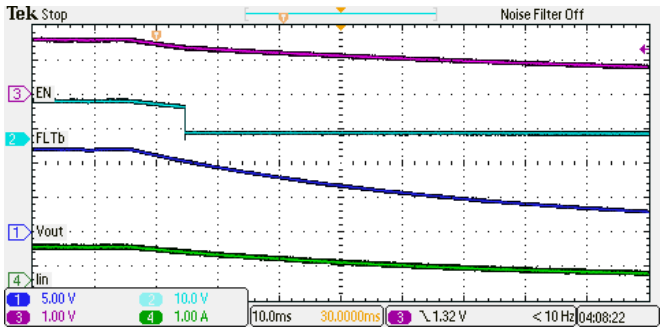
If CdVdT = 4.7 nF was used, the device would have tried to charge the 4700-µF output cap with inrush current of 986 mA in 57.24 ms, dissipating power of 5.94 W. This is outside the safe starting condition of the device, and would have led the device to enter thermal shutdown during start-up.

9.2.2.3 Application Curves



C_{OUT} = $C_{HOLD-UP}$ = 4700 µF C_{dVdT} = 22 nF

Figure 44. Output Ramp Up



C_{OUT} = $C_{HOLD-UP}$ = 4700 µF $V_{(PFAIL)}$ = 10.35 V R_{LOAD} = 12 Ω

Figure 45. Hold-up Power When VIN Fails

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10 Power Supply Recommendations

The device is designed for supply voltage range of 4.5 V ≤ V_{IN} ≤ 18 V. If the input supply is located more than a few inches from the device an input ceramic bypass capacitor higher than 0.1 µF is recommended. Power supply should be rated higher than the current limit set to avoid voltage droops during over current and short-circuit conditions.

10.1 Transient Protection

In case of short circuit and over load current limit, when the device interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on value of inductance in series to the input or output of the device. Such transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue.

Typical methods for addressing transients include:

- Minimizing lead length and inductance into and out of the device
- Using large PCB GND plane
- Schottky diode across the output to absorb negative spikes
- A low value ceramic capacitor ($C_{(IN)}$ = 0.001 µF to 0.1 µF) to absorb the energy and dampen the transients. The approximate value of input capacitance can be estimated with Equation 23.

$$V_{SPIKE(Absolute)} = V_{(IN)} + I_{(LOAD)} \times \sqrt{\frac{L_{(IN)}}{C_{(IN)}}} \quad (23)$$

Where:

- $V_{(IN)}$ is the nominal supply voltage
- $I_{(LOAD)}$ is the load current
- $L_{(IN)}$ equals the effective inductance seen looking into the source
- $C_{(IN)}$ is the capacitance present at the input

Some applications may require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the *Absolute Maximum Ratings* of the device.

The circuit implementation with optional protection components (a ceramic capacitor, TVS and schottky diode) is shown in Figure 46.

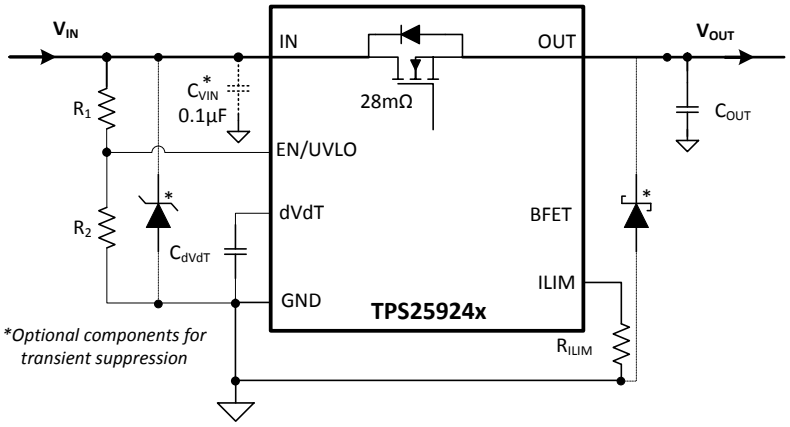

Figure 46. Circuit Implementation with Optional Protection Components

10.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. Source bypassing, input leads, circuit layout and component selection, output shorting method, relative location of the short, and instrumentation all contribute to variation in results. The actual short itself exhibits a certain degree of randomness as it microscopically bounces and arcs. Care in configuration and methods must be used to obtain realistic results. Do not expect to see waveforms exactly like those in the data sheet; every setup differs.

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11 Layout

11.1 Layout Guidelines

- For all applications, a 0.01-µF or greater ceramic decoupling capacitor is recommended between IN terminal and GND. For hot-plug applications, where input power path inductance is negligible, this capacitor can be eliminated/minimized.
- The optimum placement of decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC. See Figure 47 for a PCB layout example.
- High current carrying power path connections should be as short as possible and should be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC. The PCB ground should be a copper plane or island on the board.
- Locate all support components: R_{ILIM}, C_{dVdT} and resistors for EN/UVLO, close to their connection pin. Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the R_{ILIM} and C_{dVdT} components to the device should be as short as possible to reduce parasitic effects on the current limit and soft start timing. These traces should not have any coupling to switching signals on the board.
- Protection devices such as TVS, snubbers, capacitors, or diodes should be placed physically close to the device they are intended to protect, and routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it should be physically close to the OUT pins.
- Obtaining acceptable performance with alternate layout schemes is possible; however this layout has been shown to produce good results and is intended as a guideline.

11.2 Layout Example

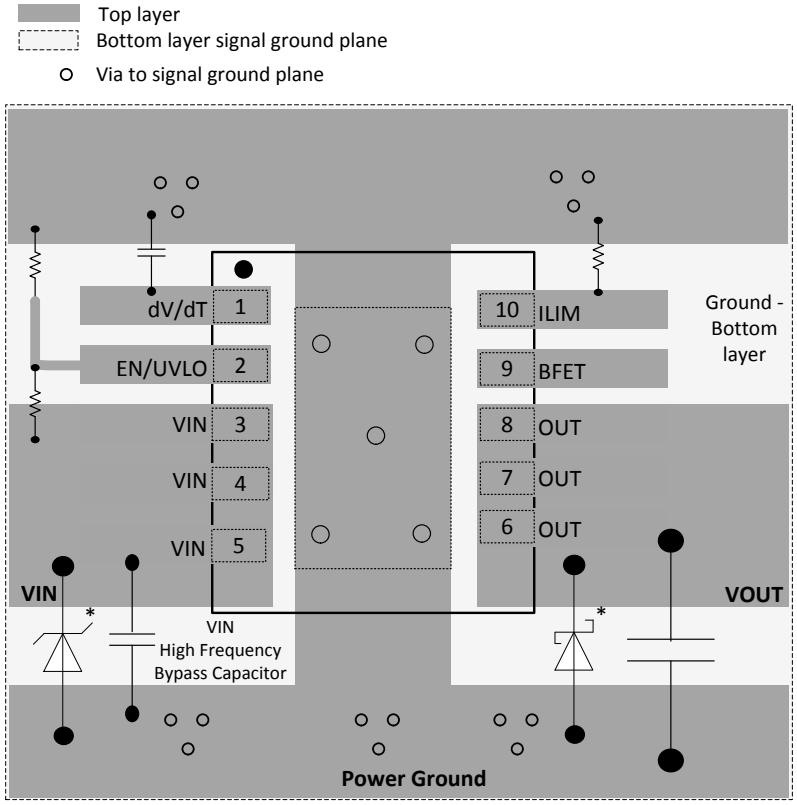

Figure 47. Layout Example

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12 器件和文档支持

12.1 器件支持

12.1.1 Third-Party Products Disclaimer

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12.2 文档支持

12.2.1 相关文档

《TPS2592xx 设计计算器》（文献编号：SLUC570）

12.3 相关链接

以下表格列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **4.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS259241	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS259240	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS259240DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	259240
TPS259240DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	259240
TPS259240DRCRG4	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	259240
TPS259240DRCRG4.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	259240
TPS259240DRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	259240
TPS259240DRCT.A	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	259240
TPS259241DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	259241
TPS259241DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	259241
TPS259241DRCRG4	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	259241
TPS259241DRCRG4.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	259241
TPS259241DRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	259241
TPS259241DRCT.A	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	259241

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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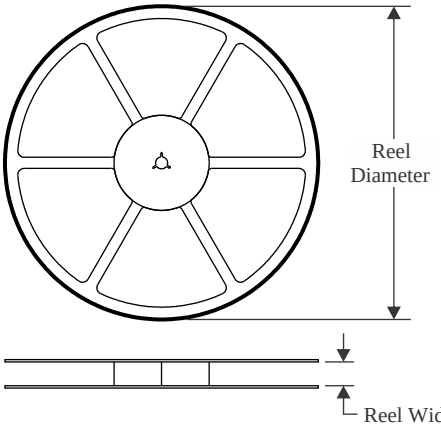
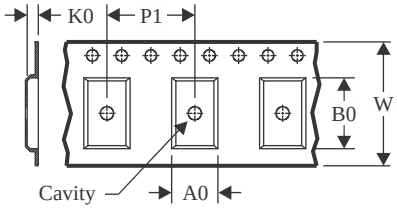
TAPE AND REEL INFORMATION

REEL DIMENSIONS

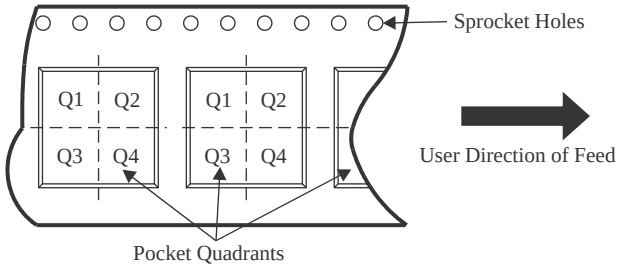


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

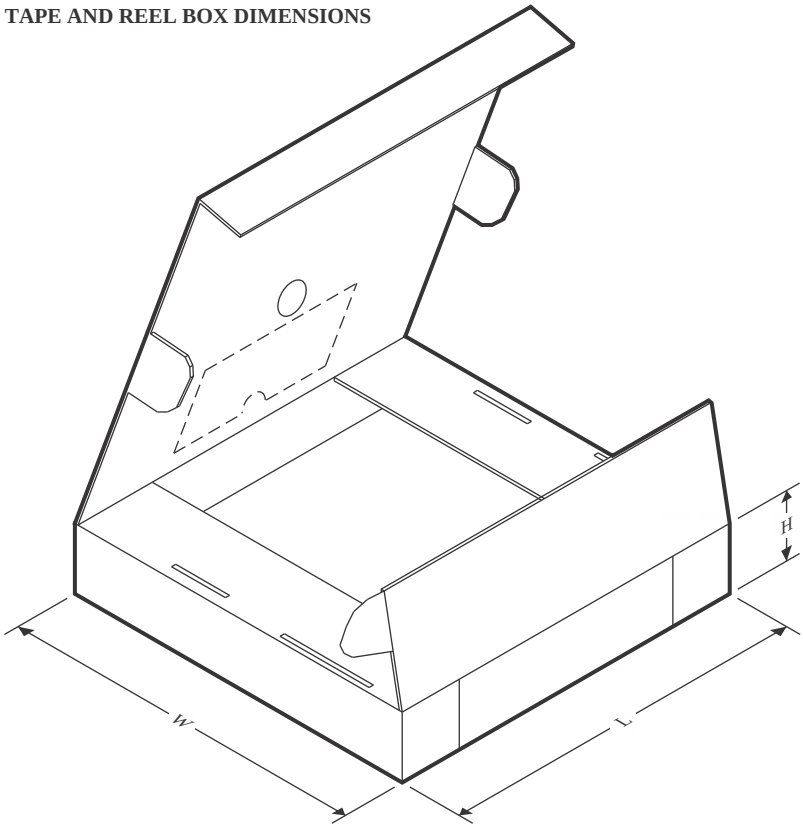
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS259240DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS259240DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS259240DRCRG4	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS259240DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS259241DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS259241DRCRG4	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS259241DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS259240DRCR	VSON	DRC	10	3000	353.0	353.0	32.0
TPS259240DRCR	VSON	DRC	10	3000	335.0	335.0	25.0
TPS259240DRCRG4	VSON	DRC	10	3000	367.0	367.0	35.0
TPS259240DRCT	VSON	DRC	10	250	182.0	182.0	20.0
TPS259241DRCR	VSON	DRC	10	3000	346.0	346.0	33.0
TPS259241DRCRG4	VSON	DRC	10	3000	346.0	346.0	33.0
TPS259241DRCT	VSON	DRC	10	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

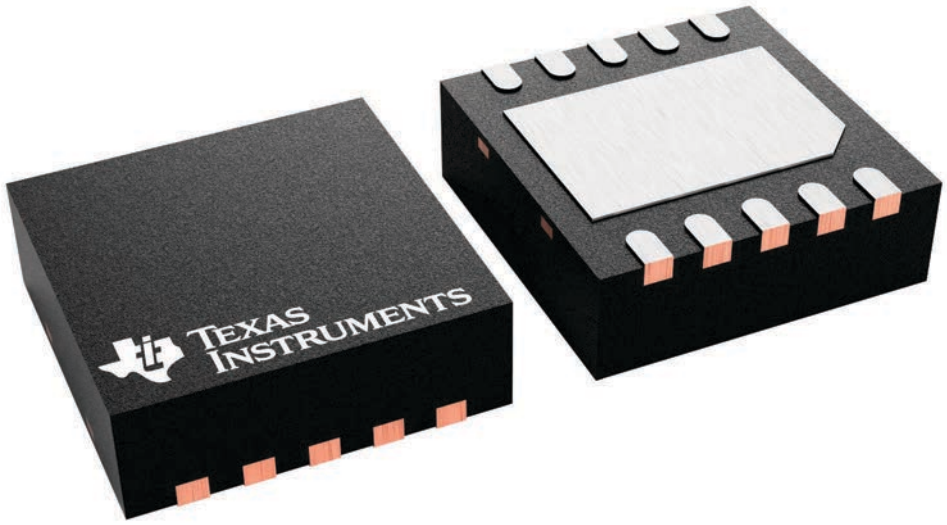
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



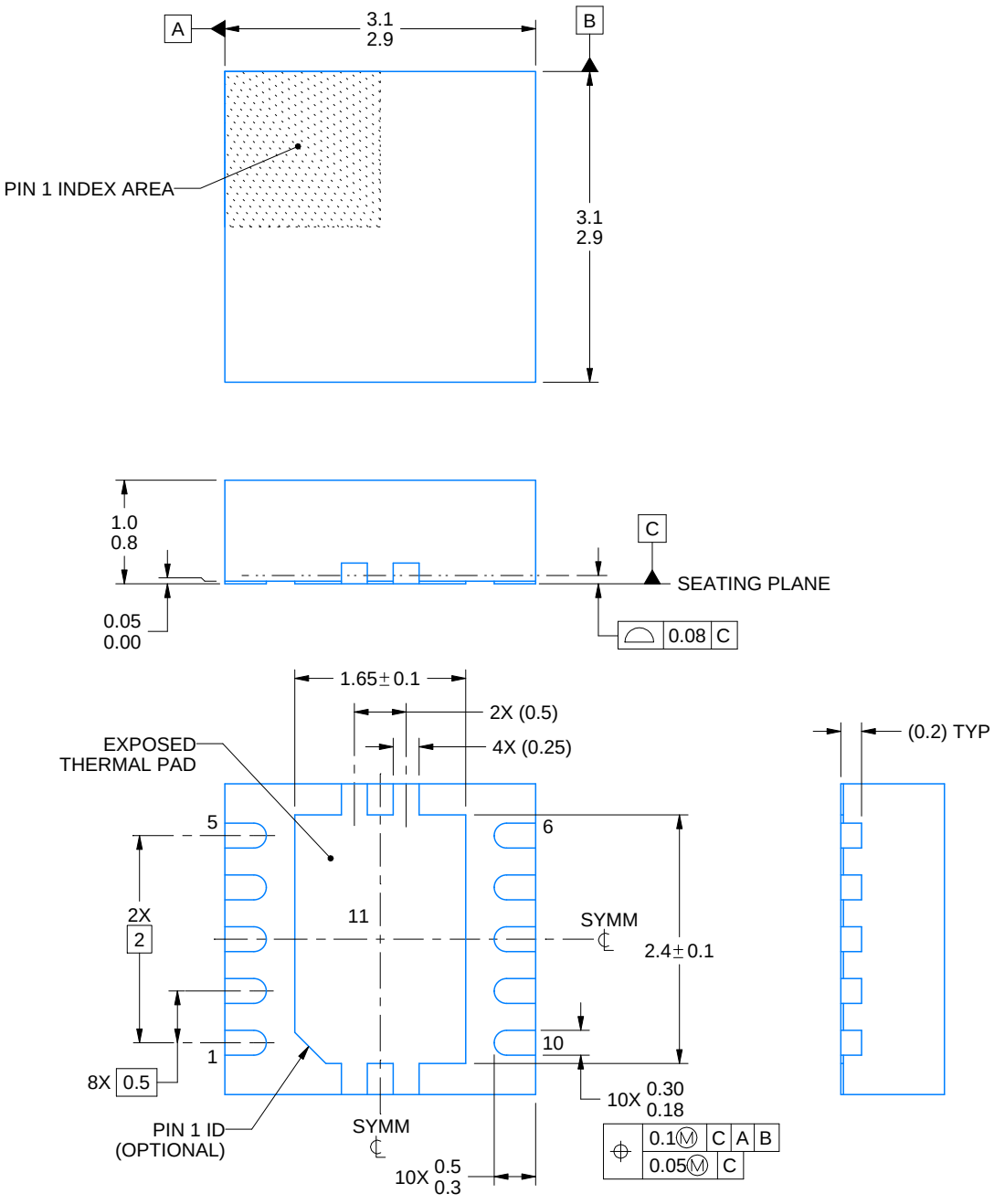
4226193/A

DRC0010J

PACKAGE OUTLINE

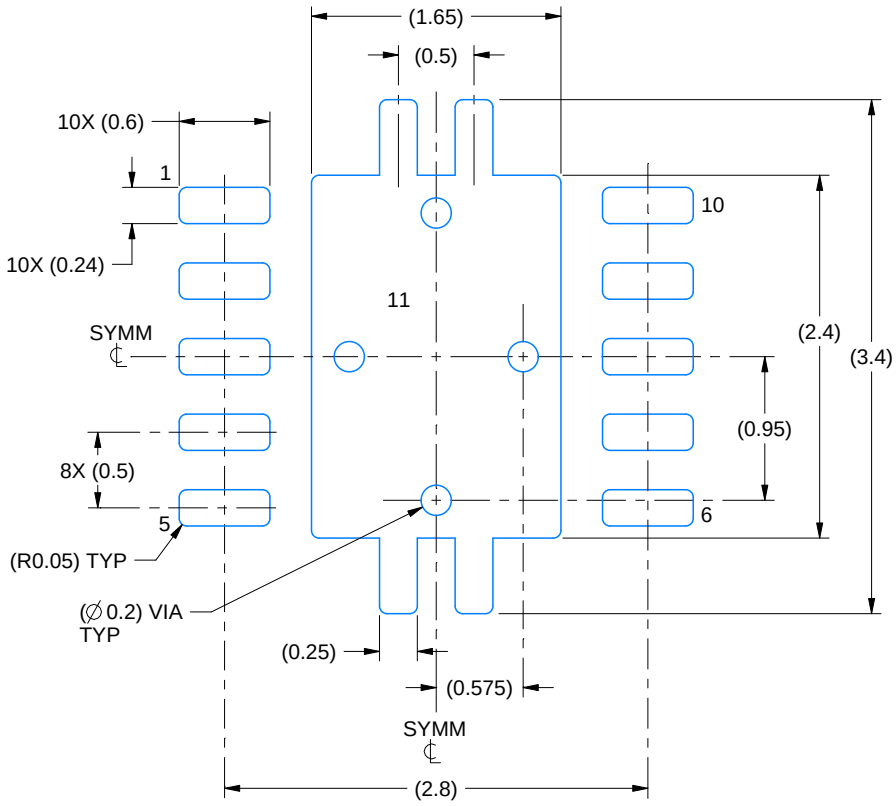
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

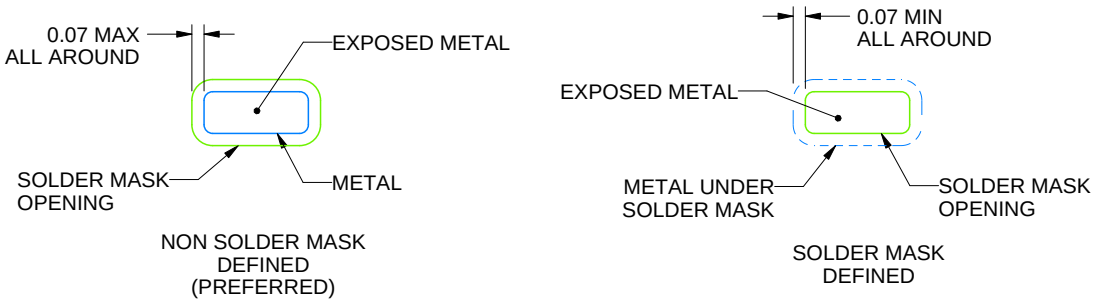


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

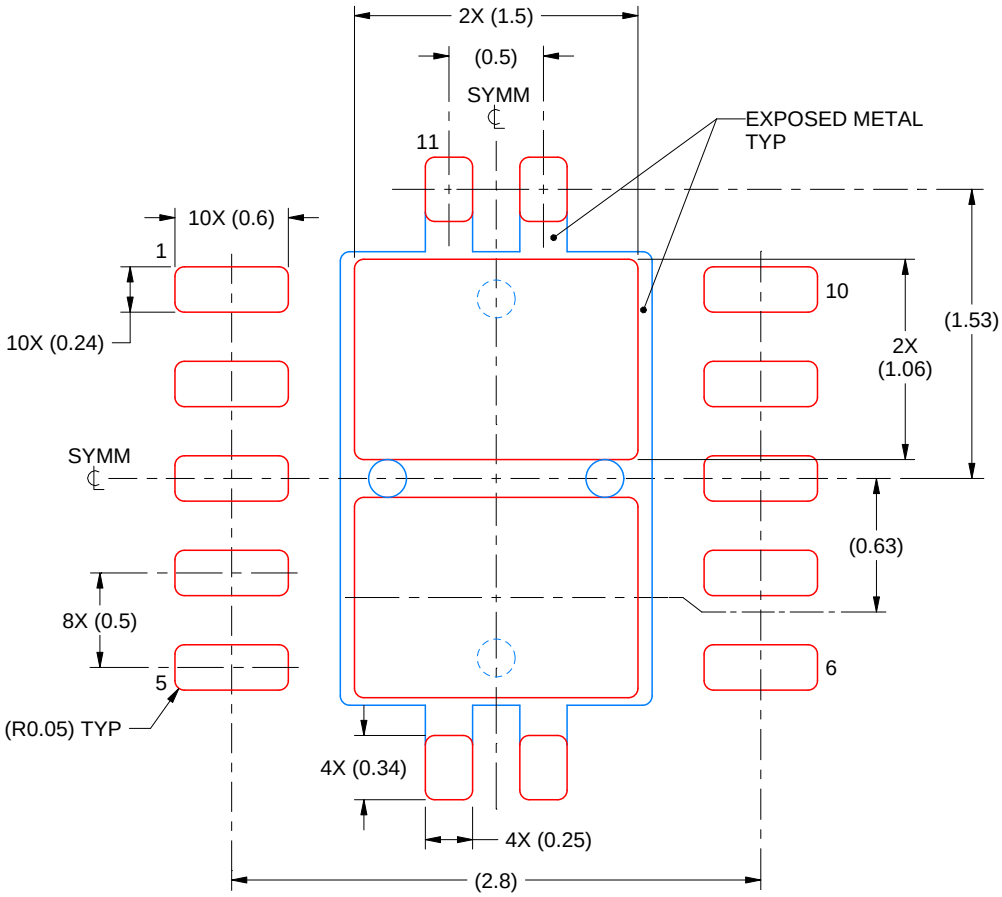
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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