TPS766 250mA 16V 低压降稳压器

1 特性

- 输入电压范围：
  - 旧芯片：2.7V 至 10V（绝对最大值 13.5V）
  - 新芯片：2.5V 至 16V（绝对最大值 18V）
- 输出电压范围：
  - 旧芯片：1.5V 至 5V（固定）和 1.25V 至 5.5V（可调）
  - 新芯片：1.2V 至 12V（固定）和 0.8V 至 14.6V（可调）
- 输出电流：最高 250mA
- 输出精度：
  - 旧芯片：3%（整个负载和温度范围）
  - 新芯片：1%（整个负载和温度范围）
- 低静态电流 (I_Q)：
  - 旧芯片：空载时典型值为 35μA
  - 新芯片：空载时典型值为 55μA
- I_Q（禁用状态）：
  - 旧芯片：10μA（最大值）
  - 新芯片：4μA（最大值）
- 压降（新芯片）：
  - 250mA 时高达 225mV（典型值）(TPS76650)
- 高 PSRR（新芯片）：1MHz 时为 46dB
- 内部软启动时间（新芯片）：750μs（典型值）
- 过流限制和热保护
- 与 2.2μF 或更高的电容器搭配使用时可保持稳定（新芯片）
- 开漏电源正常
- 封装：8 引脚，4.9mm × 6mm SOIC (D)

2 应用

- 家用空调
- 车身电子装置和照明
- HVAC 系统
- 洗衣机和烘干机

3 说明

TPS766 是一款低压降 (LDO) 线性稳压器，支持 2.5V 至 16V 的输入电压范围（新芯片）和高达 250mA 的负载电流。对于新芯片，支持的输出范围为 1.2V 至 12V（固定版本）或 0.8V 至 14.6V（可调版本）。

输入电压范围高达 16V（新芯片），这使得该器件非常适合由变压器次级绕组和稳压电源轨（例如 10V 或 12V）供电。此外，该器件具有宽输出电压范围，因此能够为碳化硅 (SiC) 栅极驱动器和麦克风产生偏置电压，以及为微控制器 (MCU) 和处理器供电。

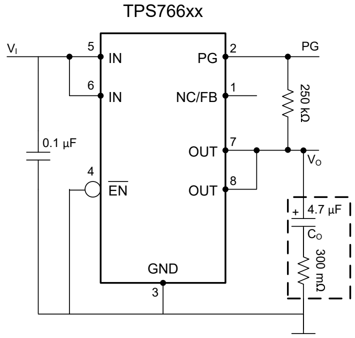
高带宽 PSRR 性能在 1kHz 时大于 70dB，在 1MHz 时大于 46dB（新芯片），因此有助于衰减上游直流/直流转换器的开关频率，并更大限度减少后置稳压器滤波。新芯片支持内部软启动电路机制，该机制可减小启动期间的浪涌电流，从而降低输入电容。

旧芯片支持在整个负载电流范围内提供恒定静态电流（对于 0mA 至 250mA 的整个输出电流范围，通常为 35μA）。

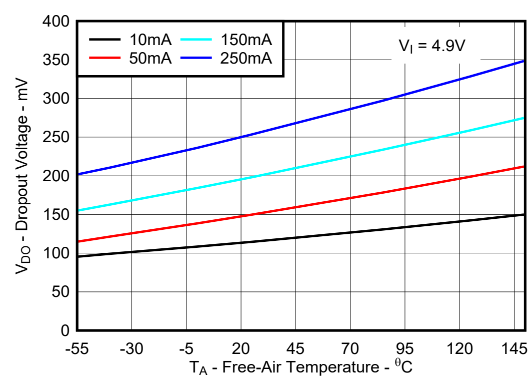
封装信息

器件型号	封装[1]	封装尺寸[2]
TPS766	D（SOIC，8）	4.9mm × 6mm

(1) 如需更多信息，请参阅*机械、封装和可订购信息*。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



典型应用电路



TPS76633 压降电压与温度间的关系（新芯片）

TPS766 LDO 还具有睡眠模式，在该模式下，向 $\overline{EN}$（使能）施加 TTL 高电平信号可关闭稳压器。在禁用模式下，旧芯片的静态电流小于 1μA（典型值），而新芯片的静态电流约为 1.6μA（典型值）。

电源正常 (PG) 是高电平有效输出，用于实现上电复位或低电池电量指示。

对于固定输出版本，TPS766 提供 1.5V 至 5.0V（旧芯片）和 1.2V 至 12V（新芯片）的输出范围。对于可调版本，输出电压可在 1.25V 至 5.5V（旧芯片）和 0.8V 至 14.6V（新芯片）范围内编程。TPS766 采用 8 引脚 SOIC 封装。

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4 Pin Configuration and Functions

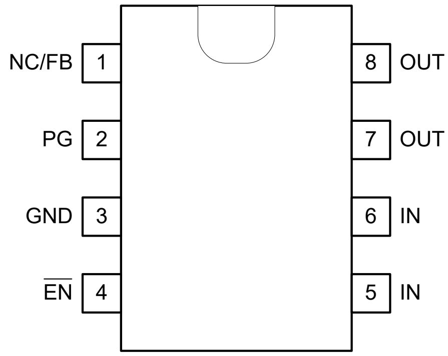


图 4-1. D Package, 8-Pin SOIC (Top View)

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
$\overline{EN}$	4	I	Enable pin. Driving the enable pin low enables the device. Driving this pin high disables the device. Low and high thresholds are listed in the *Electrical Characteristics* table.
FB/NC	1	I	Adjustable version: Feedback pin. Input to the control-loop error amplifier. This pin sets the output voltage of the device by using external resistors. Do not float this pin. Fixed version: Not internally connected. Leave this pin open or tied to ground for improved thermal performance.
GND	3		Ground pin.
IN	5, 6	I	Input pin. Use the recommended capacitor value as listed in the *Recommended Operating Conditions*. Place the input capacitor as close to the IN and GND pins of the device as possible.
OUT	7, 8	O	Output pin. Use the recommended capacitor value as listed in the *Recommended Operating Conditions*. Place the output capacitor as close to the OUT and GND pins of the device as possible.
PG	2	O	Power-good output. Available in the open-drain output. A pullup resistor is required for the open-drain output type. If the power-good functionality is not used, ground this pin or leave floating. See the *Power-Good Function* section for more information.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Voltage[(2)]	V_{IN} (for legacy chip)	–0.3	13.5	V
	V_{IN} (for new chip)	–0.3	18	
	V_{OUT} (for legacy chip)	–0.3	7	
	V_{OUT} (for new chip)	–0.3	V_{IN} + 0.3	
	V_{FB} (for legacy chip)	–0.3	7	
	V_{FB} (for new chip)	–0.3	3	
	Voltage range at $\overline{EN}$ (for legacy chip)	–0.3	13.5	
	Voltage range at $\overline{EN}$ (for new chip)	–0.3	18	
	PG pin voltage (for legacy chip)	–0.3	16.5	
	PG pin voltage (for new chip)	–0.3	18	
Current	Maximum output current	Internally Limited		A
Temperature	Operating junction (T_J)	–50	150	°C
	Storage (T_{STG})	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages with respect to GND.

5.2 ESD Ratings

			VALUE (Legacy Chip)	VALUE (New Chip)	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±2000	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	N/A	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage (for legacy chip)	2.7		10	V
	Input voltage (for new chip)	2.5		16	
EN	Enable voltage (for legacy chip)	0		16	
	Enable voltage (for new chip)	0		16	
V_{OUT}	Output voltage (for legacy chip)	1.2		5.5	
	Output voltage (for new chip)	1.2		14.6	
I_{OUT}	Output current	0		250	mA
C_{OUT}	Output capacitor (for legacy chip)	4.7			μF
	Output capacitor (for new chip)	1	2.2	220	
C_{OUT} ESR	Output capacitor ESR (for legacy chip)	0.3		10	Ω
	Output capacitor ESR (for new chip)	0		2	
C_{IN}	Input capacitor		1		μF
T_J	Junction temperature	–40		125	°C

5.4 Thermal Information (Legacy Chip)

DISSIPATION RATINGS			UNIT
THERMAL METRIC	D (SOIC) 8 PINS		
	AIR FLOW = 0 CFM	AIR FLOW = 250 CFM	
$R_{\theta JA}$ (Junction-to-ambient thermal resistance)	176.05	110.62	℃/W
Derating factor above T_A = +25℃	5.68	9.04	mW/℃
Power rating (T_A < 25℃)	568	904	mW
Power rating (T_A = 70℃)	312	497	
Power rating (T_A = 85℃)	227	361	

5.5 Thermal Information (New Chip)

THERMAL METRIC(1)		TPS766 (2)	UNIT
		D (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	75.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	18.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	74.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) Thermal performance results are based on the JEDEC standard of 2s2p PCB configuration. These thermal metric parameters can be further improved by 35-55% based on thermally optimized PCB layout designs. See the analysis of the *Impact of board layout on LDO thermal performance* application note.

5.6 Electrical Characteristics

specified at T_J = –40°C to 125°C, $V_{IN} = V_{OUT(nom)}$ + 1.0V or V_{IN} = 2.5V (whichever is greater), I_{OUT} = 10μA, $\overline{EN}$ = 0V, C_{IN} = 1.0μF, C_{OUT} = 4.7μF (unless otherwise noted); typical values are at T_J = 25ºC

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage (10 μA to 250 mA load)	TPS76601 (for legacy chip)	1.25 V ≤ V_{OUT} ≤ 5.5 V, T_J = +25°C		V_{OUT}		V
			1.25 V ≤ V_{OUT} ≤ 5.5 V, T_J = –40 ℃ to 125°C	0.97 × V_{OUT}		1.03 × V_{OUT}	
		TPS76615 (for legacy chip)	T_J = +25°C, 2.7 V < V_{IN} < 10 V		1.5		
			T_J = –40°C to +125°C, 2.7 V < V_{IN} < 10 V	1.455		1.545	
		TPS76618 (for legacy chip)	T_J = +25°C, 2.8 V < V_{IN} < 10 V		1.8		
			T_J = –40°C to +125°C, 2.7 V < V_{IN} < 10 V	1.746		1.854	
		TPS76625 (for legacy chip)	T_J = +25°C, 3.5 V < V_{IN} < 10 V		2.5		
			T_J = –40°C to +125°C, 3.5 V < V_{IN} < 10 V	2.425		2.575	
		TPS76627 (for legacy chip)	T_J = +25°C, 3.7 V < V_{IN} < 10 V		2.7		
			T_J = –40°C to +125°C, 3.7 V < V_{IN} < 10 V	2.619		2.781	
		TPS76628 (for legacy chip)	T_J = +25°C, 3.8 V < V_{IN} < 10 V		2.8		
			T_J = –40°C to +125°C, 3.8 V < V_{IN} < 10 V	2.716		2.884	
		TPS76630 (for legacy chip)	T_J = +25°C, 4.0 V < V_{IN} < 10 V		3.0		
			T_J = –40°C to +125°C, 4.0 V < V_{IN} < 10 V	2.910		3.090	
		TPS76633 (for legacy chip)	T_J = +25°C, 4.3 V < V_{IN} < 10 V		3.3		
			T_J = –40°C to +125°C, 4.3 V < V_{IN} < 10 V	3.201		3.399	
		TPS76650 (for legacy chip)	T_J = +25°C, 6.0 V < V_{IN} < 10 V		5.0		
			T_J = –40°C to +125°C, 6.0 V < V_{IN} < 10 V	4.850		5.150	
		TPS766xx (for new chip), V_{OUT} = 1.8 V	T_J = –40 ℃ to 125 ℃, V_{OUT} + 1 V ≤ V_{IN} ≤ 16 V	0.9785		1.01	× V_{OUT}
		TPS766xx (for new chip), V_{OUT} ≥ 3.3 V	T_J = –40 ℃ to 125 ℃, V_{OUT} + 1 V ≤ V_{IN} ≤ 16 V	0.982		1.009	× V_{OUT}
V_{FB}	Feedback voltage	TPS76601 (for legacy chip)			1.25		V
		TPS76601 (for new chip)			0.8		
I_Q	Quiescent current (GND current), $\overline{EN}$ = 0 V	For legacy chip	10 μA < I_{OUT} < 250 mA, T_J = +25°C		35		μA
			I_{OUT} = 250 mA, T_J = –40 ℃ to 125 °C			50	
		For new chip	I_{OUT} = 0 mA (for adjustable only)		50	80	
			I_{OUT} = 0 mA (for fixed only)		55	90	
			I_{OUT} = 250 mA		1080		
$\Delta V_{OUT(\Delta VOUT)}$	Output voltage line regulation ($\Delta V_{OUT}/V_{OUT}$)	For legacy chip	$V_{OUT(NOM)}$ +1.0 V ≤ V_{IN} ≤ 10 V, I_{OUT} = 10 μA		0.01		%/V
		For new chip	$V_{OUT(NOM)}$ +1.0 V ≤ V_{IN} ≤ 16 V, I_{OUT} = 10 μA			0.005	

5.6 Electrical Characteristics（续）

specified at T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 1.0V or V_{IN} = 2.5V (whichever is greater), I_{OUT} = 10µA, $\overline{EN}$ = 0V, C_{IN} = 1.0µF, C_{OUT} = 4.7µF (unless otherwise noted); typical values are at T_J = 25ºC

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta V_{OUT(\Delta IOUT)}$	Output voltage load regulation	For legacy chip	10 µA ≤ I_{OUT} ≤ 250 mA		0.5		%
		For new chip	10 µA ≤ I_{OUT} ≤ 250 mA		0.55	1.6	%
			10 µA ≤ I_{OUT} ≤ 250 mA		20	35	mV
V_n	Output noise voltage	For legacy chip	BW = 300 Hz to 50 kHz, V_{OUT} = 3.3 V , C_{OUT} = 4.7 µF		200		μV_{RMS}
		For new chip	BW = 300 Hz to 50 kHz, V_{OUT} = 3.3 V , I_{OUT} = 100 mA, C_{OUT} = 4.7 µF		165		
			BW = 10 Hz to 100 kHz, V_{OUT} = 3.3 V, I_{OUT} = 100 mA , C_{OUT} = 4.7 µF		195		
$T_{SD(shutdown)}$	Thermal shutdown junction temperature	For legacy chip			150		ºC
	Thermal shutdown temperature	For new chip	Temperature increasing		173		
$T_{SD(reset)}$	Thermal shutdown reset temperature		Temperature falling		157		
I_{CL}	Output current limit	For legacy chip	V_{OUT} = 0 V		0.8	1.2	A
		For new chip			0.725	0.8	
$I_{STANDBY}$	Standby current	For legacy chip	$\overline{EN}$ = V_{IN} , 2.7 V < V_{IN} < 10 V		1		µA
			$\overline{EN}$ = V_{IN} , 2.7 V < V_{IN} < 10 V & T_J = –40 ℃ to 125 ℃			10	
		For new chip	$\overline{EN}$ = V_{IN} , 2.5 V < V_{IN} < 16 V		0.9		
			$\overline{EN}$ = V_{IN} , 2.5 V < V_{IN} < 16 V & T_J = –40 ℃ to 125 ℃			6.75	
I_{FB}	Feedback pin current	For legacy chip	V_{FB} = 1.5 V		2		nA
		For newchip			10	50	nA
$\overline{EN}$	High level enable input voltage	For legacy chip		2			V
	Low level enable input voltage					0.8	
	High level enable input voltage	For new chip	2.5 V ≤ VIN ≤ 16 V	1.2			
	Low level enable input voltage					0.4	
PSRR	Power-supply ripple rejection	For legacy chip	V_{OUT} = 3.3 V, I_{OUT} = 10 µA, f = 1 kHz, T_J = 25 ℃		63		dB
		For new chip	V_{OUT} = 3.3 V, I_{OUT} = 250 mA, f = 1 kHz, T_J = 25 ℃		58		
PG	Minimum input voltage for valid PG	For legacy chip	$I_{O(PG)}$ = 300 µA		1.1		
	Trip threshold voltage (PG_{TH})		V_{OUT} decreasing	92		98	$\%V_O$
	Hysteresis voltage ($PG_{Hysteresis}$)		Measured at V_{OUT}		0.5		
	Output low voltage		V_{IN} = 2.7 V, $I_{OUT(PG)}$ = 1 mA		0.15	0.4	V
	Leakage current		$V_{(PG)}$ = 5 V			1	µA
	Minimum input voltage for valid PG	For new chip	$I_{O(PG)}$ = 300 µA		1.0		
	Trip threshold voltage (PG_{TH})		V_{OUT} decreasing	91		98.5	$\%V_O$
	Hysteresis voltage ($PG_{Hysteresis}$)		Measured at V_{OUT}		0.45		
	Output low voltage		V_{IN} = 2.7 V, $I_{OUT(PG)}$ = 1 mA		0.12	0.3	V
	Leakage current		$V_{(PG)}$ = 5 V			2.1	µA

5.6 Electrical Characteristics（续）

specified at T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 1.0V or V_{IN} = 2.5V (whichever is greater), I_{OUT} = 10μA, $\overline{EN}$ = 0V, C_{IN} = 1.0μF, C_{OUT} = 4.7μF (unless otherwise noted); typical values are at T_J = 25ºC

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{EN}	Input current ($\overline{EN}$)	For legacy chip	$\overline{EN}$ = 0V	–1	0	1	μA
			$\overline{EN}$ = V_{IN}	–1	0	1	
		For new chip	$\overline{EN}$ = 0V	–1	–0.5	1	
			$\overline{EN}$ = V_{IN}	–0.6	–0.025	0.4	
V_{DO}	Dropout voltage	TPS76628 (for legacy chip)	I_{OUT} = 250 mA		310		mV
			I_{OUT} = 250 mA, T_J = –40 ℃ to 125 ℃			540	
		TPS76628 (for new chip)	I_{OUT} = 250 mA		310		
			I_{OUT} = 250 mA, T_J = –40 ℃ to 125 ℃			540	
		TPS76630 (for legacy chip)	I_{OUT} = 250 mA		270		
			I_{OUT} = 250 mA, T_J = –40 ℃ to 125 ℃			470	
		TPS76630 (for new chip)	I_{OUT} = 250 mA		270		
			I_{OUT} = 250 mA, T_J = –40 ℃ to 125 ℃			470	
		TPS76633 (for legacy chip)	I_{OUT} = 250 mA		230		
			I_{OUT} = 250 mA, T_J = –40 ℃ to 125 ℃			400	
		TPS76633 (for new chip)	I_{OUT} = 250 mA		260		
			I_{OUT} = 250 mA, T_J = –40 ℃ to 125 ℃			400	
		TPS76650 (for legacy chip)	I_{OUT} = 250 mA		140		
			I_{OUT} = 250 mA, T_J = –40 ℃ to 125 ℃			250	
		TPS76650 (for new chip)	I_{OUT} = 250 mA		250		
			I_{OUT} = 250 mA, T_J = –40 ℃ to 125 ℃			390	
$R_{PULLDOWN}$	Output pull-down resistance	TPS766xx (for new chip)	$\overline{EN}$ = V_{IN} = 16 V, V_{OUT} = 2.5 V		1.8		KΩ
t_{STR}	Start-up time	TPS766xx (for new chip)	T_J = 25 ℃		750		μs

5.7 Timing Diagram

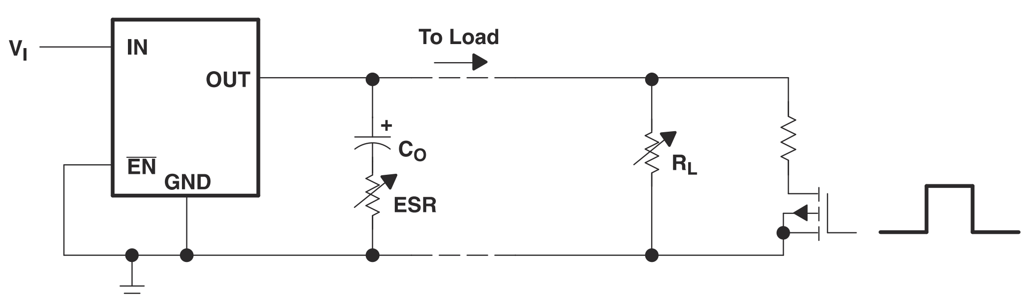


图 5-1. Test Circuit for Typical Regions of Stability
(See the *Typical Characteristics: Supported ESR Range* section)

5.8 Typical Characteristics

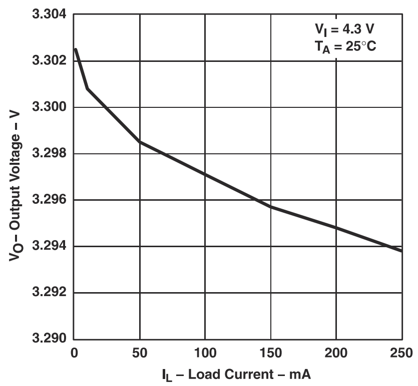


图 5-2. TPS76633 Output Voltage vs Load Current (Legacy Chip)

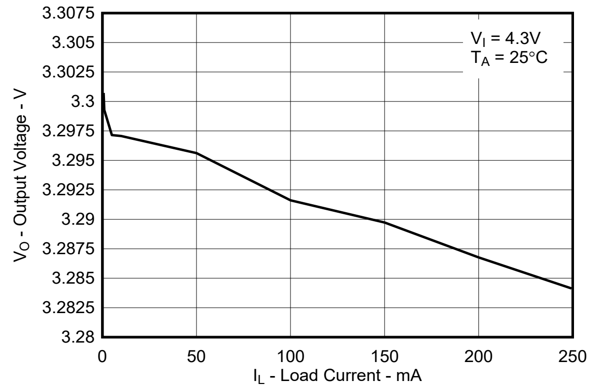


图 5-3. TPS76633 Output Voltage vs Load Current (New Chip)

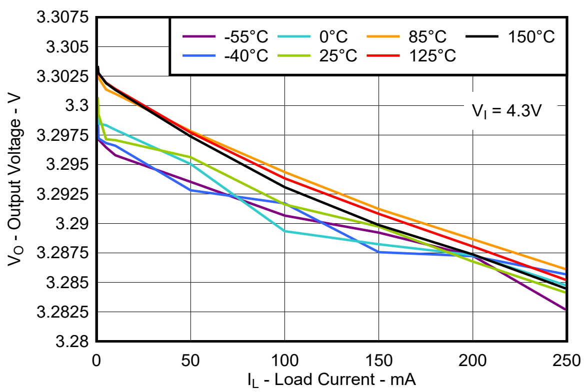


图 5-4. TPS76633 Output Voltage vs Load Current (New Chip)

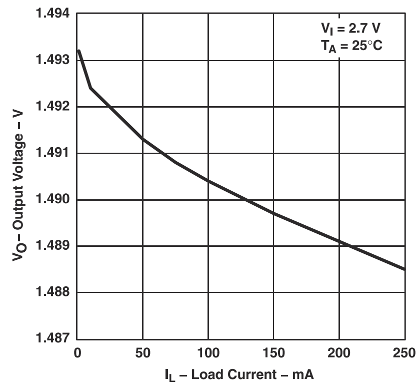


图 5-5. TPS76615 Output Voltage vs Load Current (Legacy Chip)

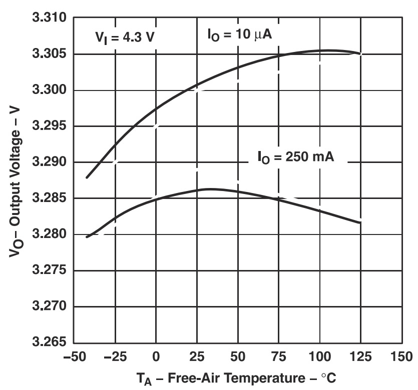


图 5-6. TPS76633 Output Voltage vs Free-Air Temperature (Legacy Chip)

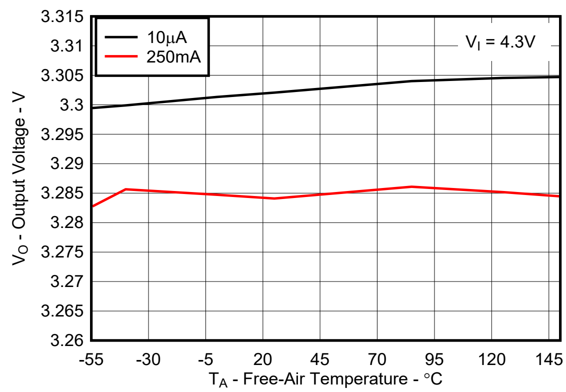


图 5-7. TPS76633 Output Voltage vs Free-Air Temperature (New Chip)

5.8 Typical Characteristics (continued)

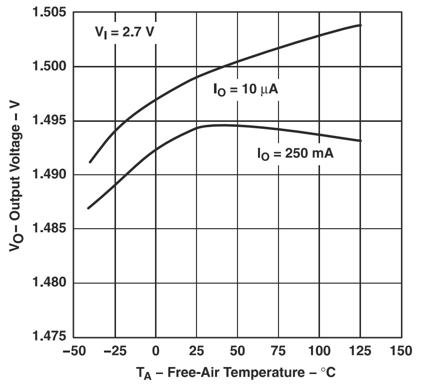


图 5-8. TPS76615 Output Voltage vs Free-Air Temperature (Legacy Chip)

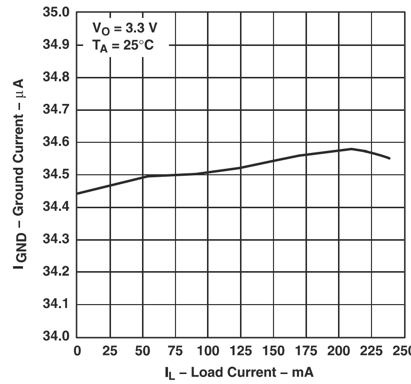


图 5-9. TPS76633 Ground Current vs Load Current (Legacy Chip)

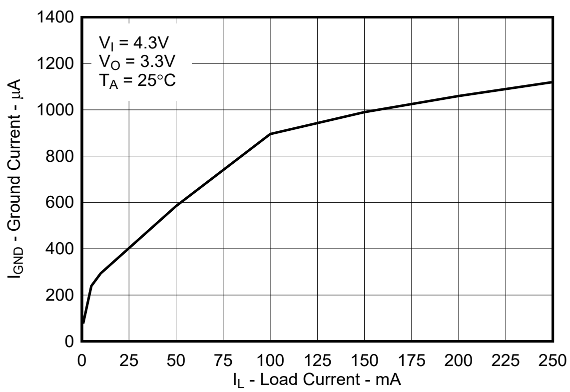


图 5-10. TPS76633 Ground Current vs Load Current (New Chip)

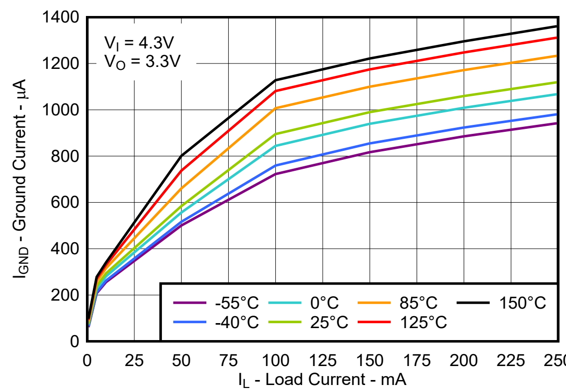


图 5-11. TPS76633 Ground Current vs Load Current (New Chip)

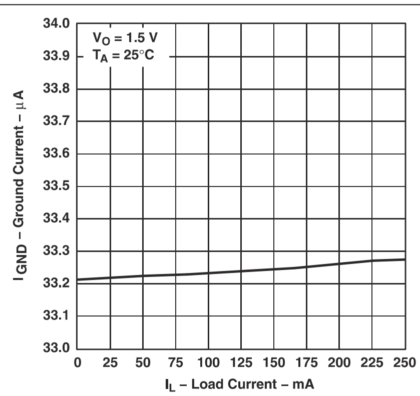


图 5-12. TPS76615 Ground Current vs Load Current (Legacy Chip)

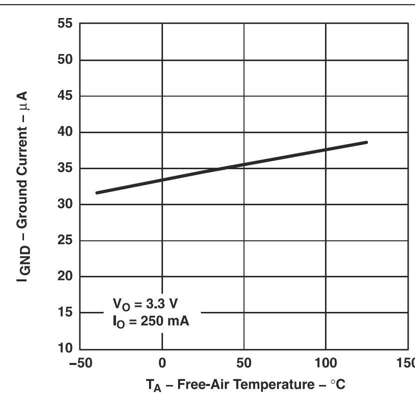


图 5-13. TPS76633 Ground Current vs Free-Air Temperature (Legacy Chip)

5.8 Typical Characteristics (continued)

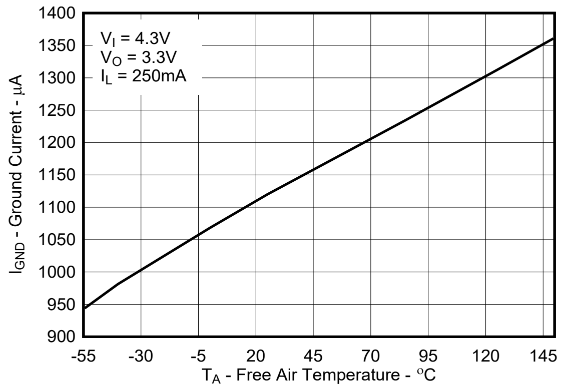


图 5-14. TPS76633 Ground Current vs Free-Air Temperature (New Chip)

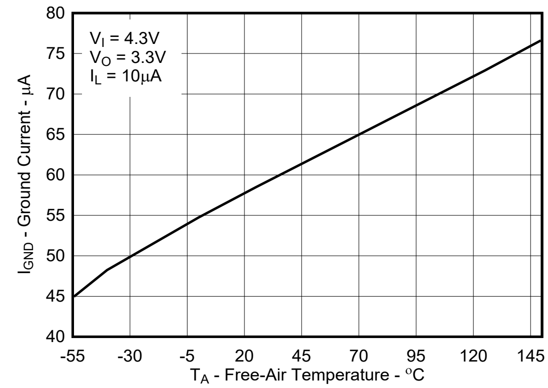


图 5-15. TPS76633 Ground Current vs Free-Air Temperature (New Chip)

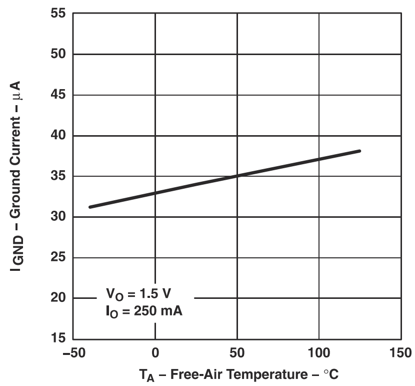


图 5-16. TPS76615 Ground Current vs Free-Air Temperature (Legacy Chip)

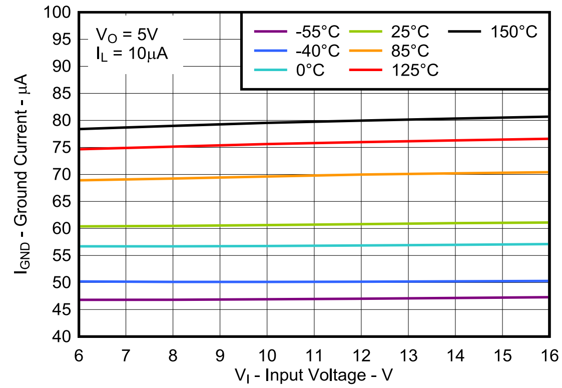


图 5-17. TPS76633 Ground Current vs Input Voltage (New Chip)

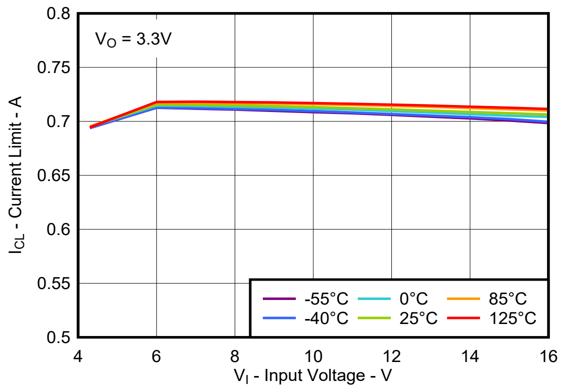
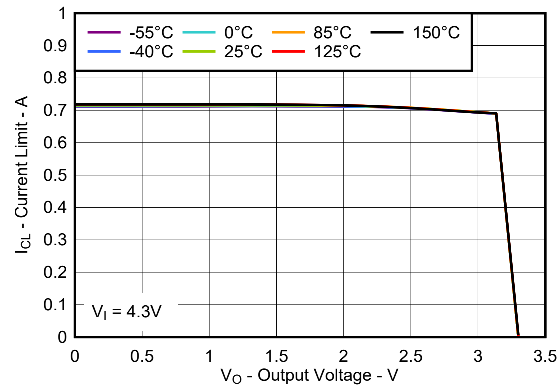


图 5-18. TPS76633 Current Limit vs Input Voltage (New Chip)



V_{OUT} = 3.3 V

图 5-19. TPS76633 Current Limit vs Output Voltage (New Chip)

5.8 Typical Characteristics (continued)

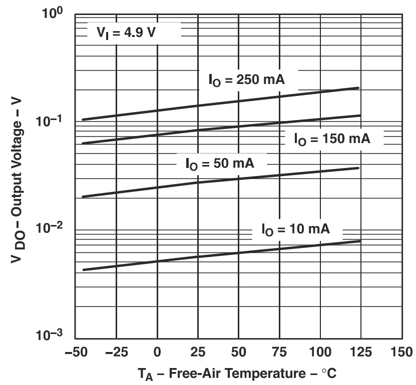


图 5-20. TPS76650 Dropout Voltage vs Free-Air Temperature (Legacy Chip)

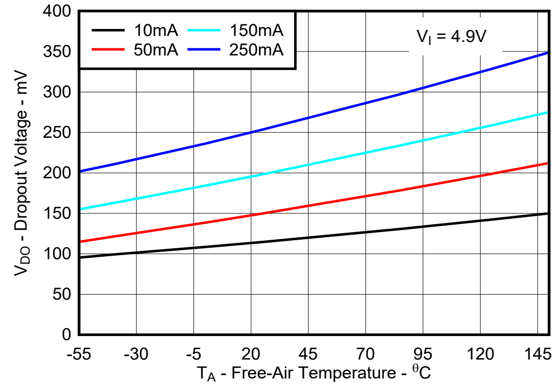


图 5-21. TPS76650 Dropout Voltage vs Free-Air Temperature (New Chip)

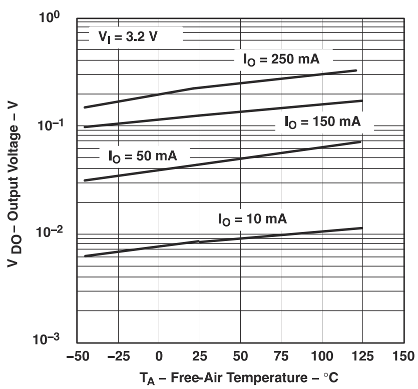


图 5-22. TPS76633 Dropout Voltage vs Free-Air Temperature (Legacy Chip)

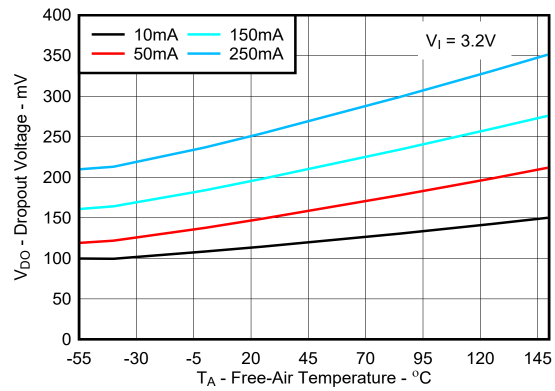


图 5-23. TPS76633 Dropout Voltage vs Free-Air Temperature (New Chip)

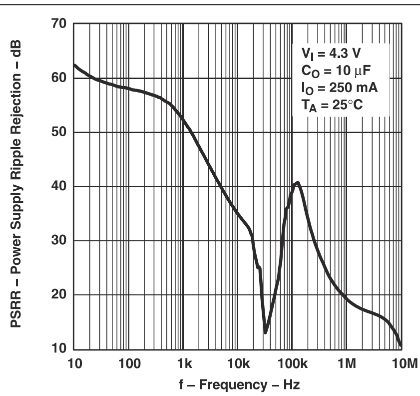


图 5-24. TPS76633 Power-Supply Ripple Rejection vs Frequency (Legacy Chip)

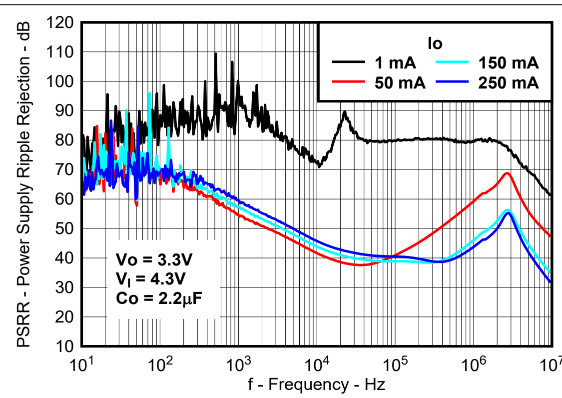


图 5-25. TPS76633 Power-Supply Ripple Rejection vs Frequency and Load Current (New Chip)

5.8 Typical Characteristics (continued)

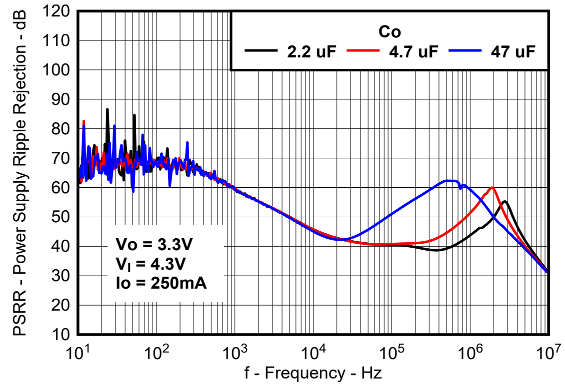


图 5-26. TPS76633 Power-Supply Ripple Rejection vs Frequency and Output Capacitor (New Chip)

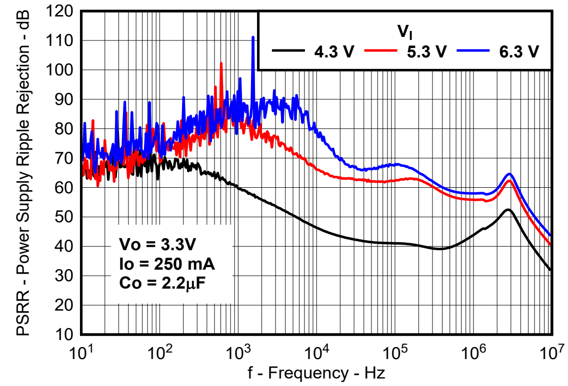


图 5-27. TPS76633 Power-Supply Ripple Rejection vs Frequency and Input Voltage (New Chip)

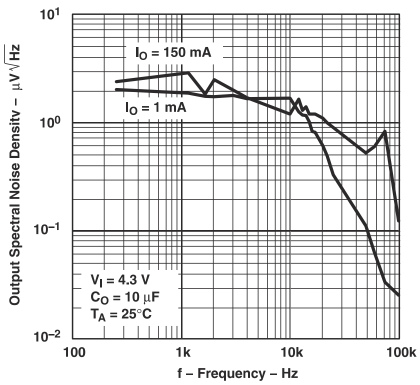


图 5-28. TPS76633 Output Spectral Noise Density vs Frequency (Legacy Chip)

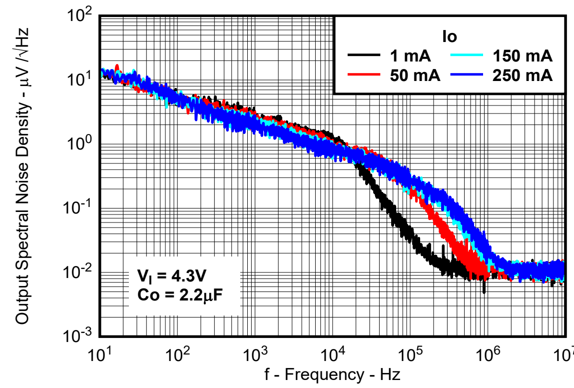


图 5-29. TPS76633 Output Spectral Noise Density vs Frequency and Load Current (New Chip)

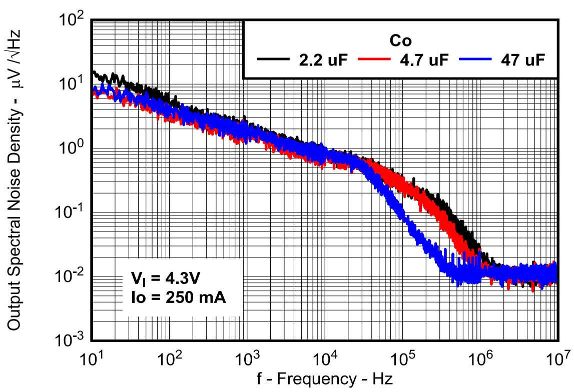


图 5-30. TPS76633 Output Spectral Noise Density vs Frequency and Output Capacitor (New Chip)

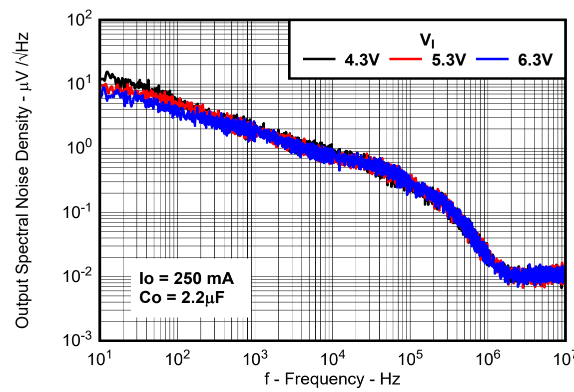


图 5-31. TPS76633 Output Spectral Noise Density vs Frequency and Input Voltage (New Chip)

5.8 Typical Characteristics (continued)

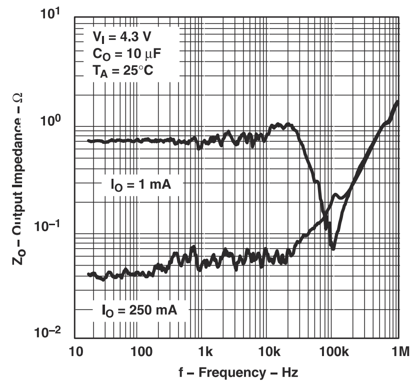


图 5-32. TPS76633 Output Impedance vs Frequency (Legacy Chip)

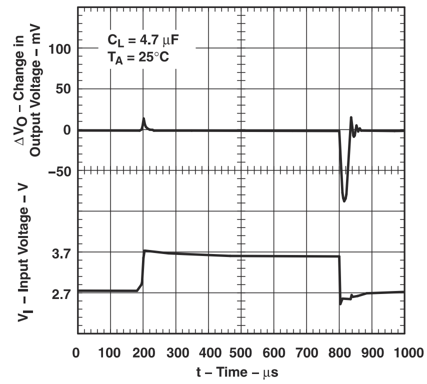


图 5-33. TPS76615 Line Transient Response (Legacy Chip)

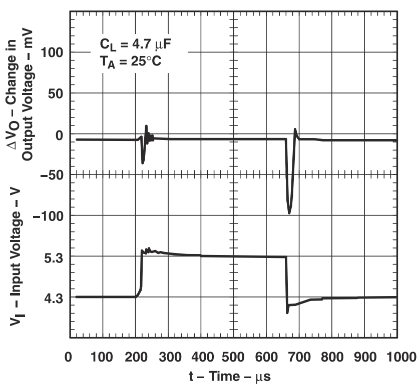


图 5-34. TPS76633 Line Transient Response (Legacy Chip)

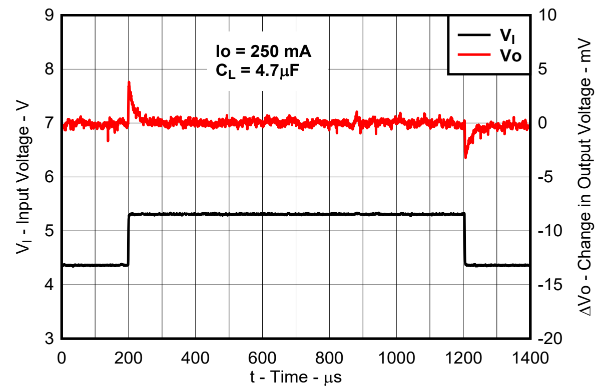


图 5-35. TPS76633 Line Transient Response (New Chip)

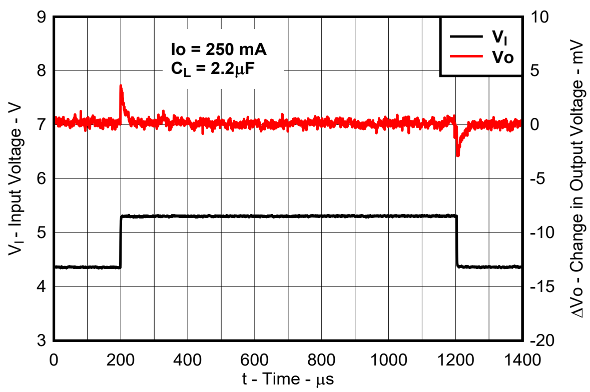


图 5-36. TPS76633 Line Transient Response (New Chip)

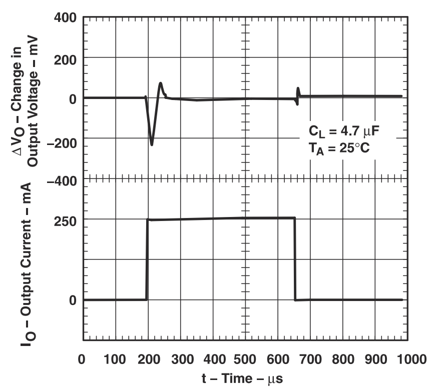


图 5-37. TPS76615 Load Transient Response (Legacy Chip)

5.8 Typical Characteristics (continued)

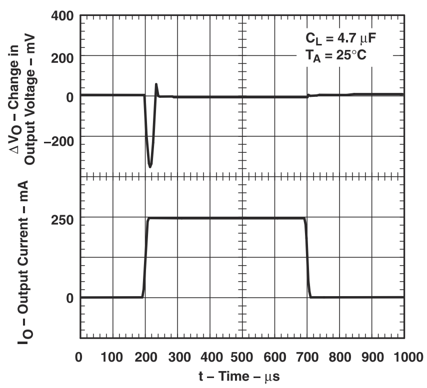


图 5-38. TPS76633 Load Transient Response (Legacy Chip)

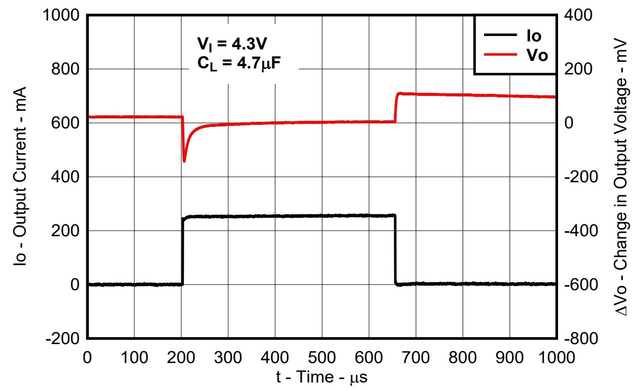


图 5-39. TPS76633 Load Transient Response (New Chip)

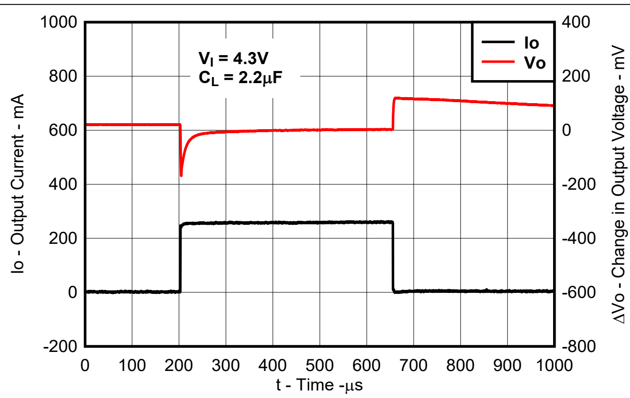


图 5-40. TPS76633 Load Transient Response (New Chip)

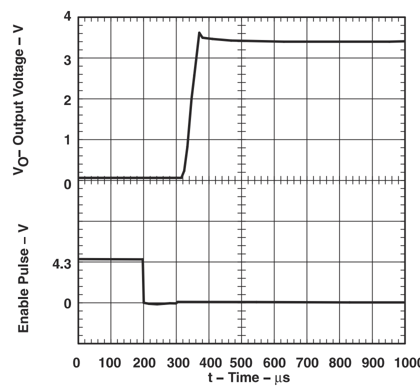
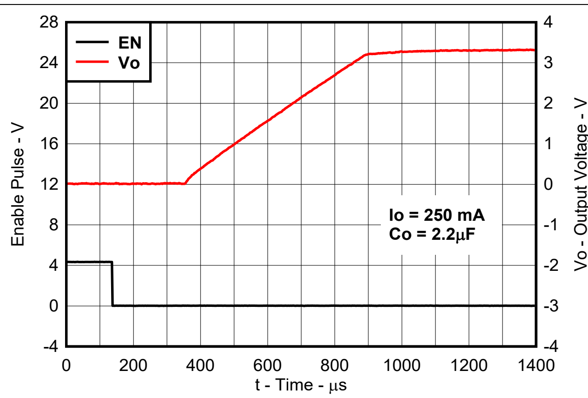
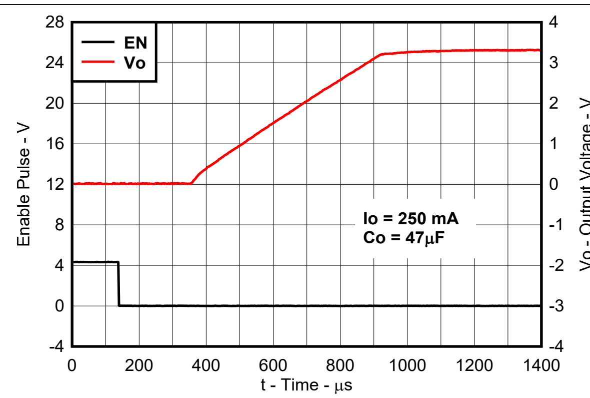


图 5-41. TPS76633 Output Voltage vs Time (Legacy Chip)



Start-up with $\overline{EN}$ sequencing

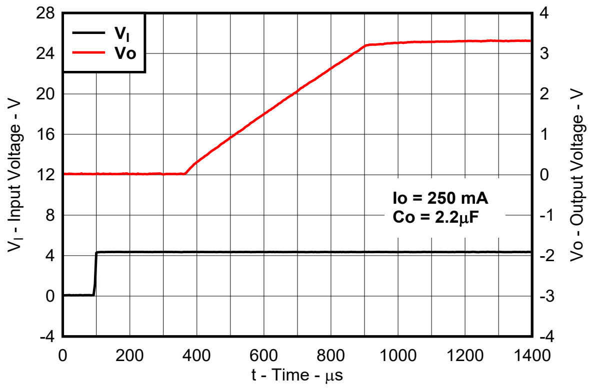
图 5-42. TPS76633 Output Voltage vs Time (New Chip)



Start-up with $\overline{EN}$ sequencing

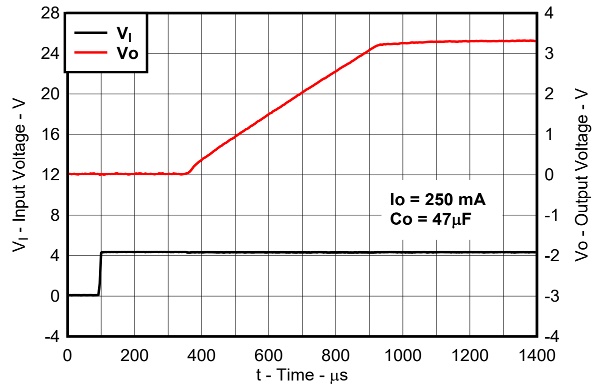
图 5-43. TPS76633 Output Voltage vs Time (New Chip)

5.8 Typical Characteristics (continued)



Start-up with V_{IN} sequencing

图 5-44. TPS76633 Output Voltage vs Time (New Chip)



Start-up with V_{IN} sequencing

图 5-45. TPS76633 Output Voltage vs Time (New Chip)

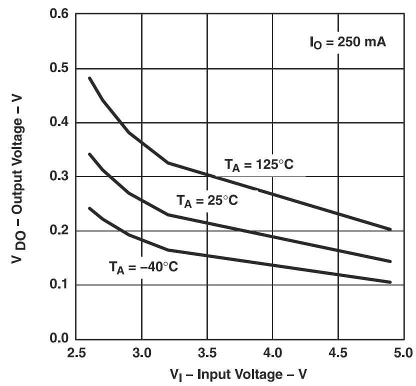


图 5-46. TPS76601 Dropout Voltage vs Input Voltage (Legacy Chip)

5.9 Typical Characteristics: Supported ESR Range

Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PCB trace resistance to C_O. The setup shown in the *Timing Diagram* section characterizes the ESR behavior across temperature.

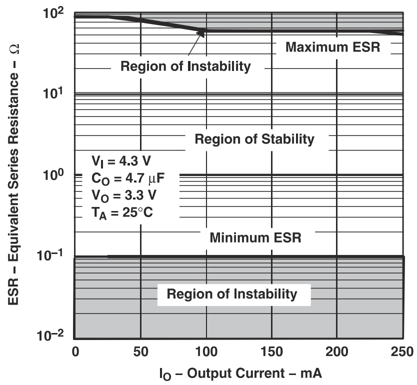


图 5-47. Typical Region of Stability ESR vs Output Current (Legacy Chip)

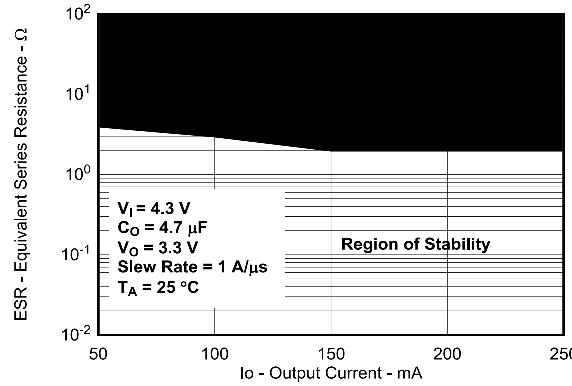


图 5-48. Typical Region of Stability ESR vs Output Current (New Chip)

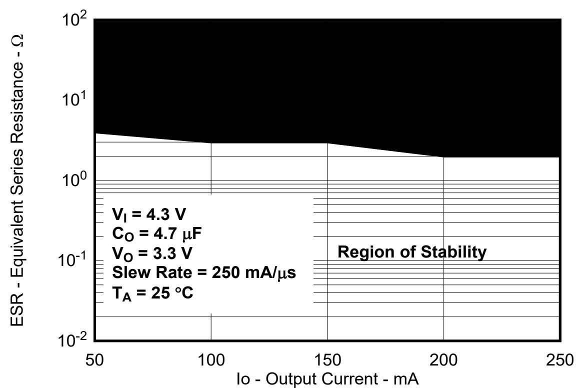


图 5-49. Typical Region of Stability ESR vs Output Current (New Chip)

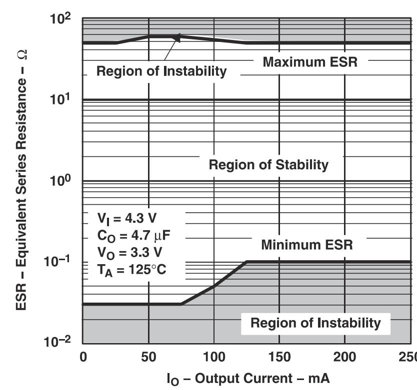


图 5-50. Typical Region of Stability ESR vs Output Current (Legacy Chip)

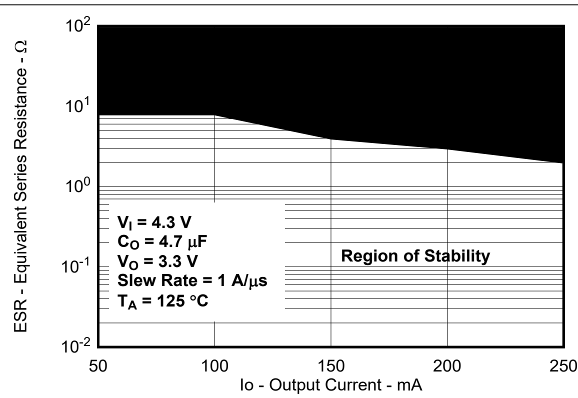


图 5-51. Typical Region of Stability ESR vs Output Current (New Chip)

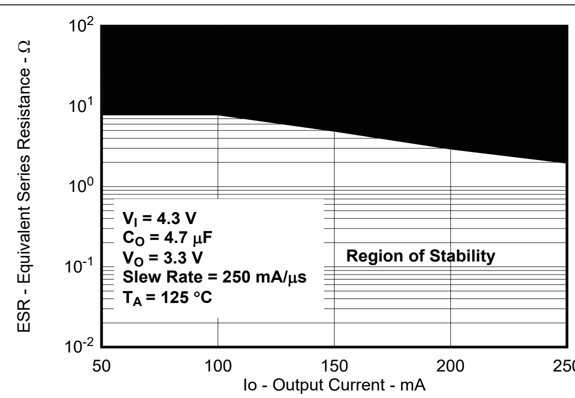


图 5-52. Typical Region of Stability ESR vs Output Current (New Chip)

5.9 Typical Characteristics: Supported ESR Range (continued)

Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PCB trace resistance to C_O. The setup shown in the *Timing Diagram* section characterizes the ESR behavior across temperature.

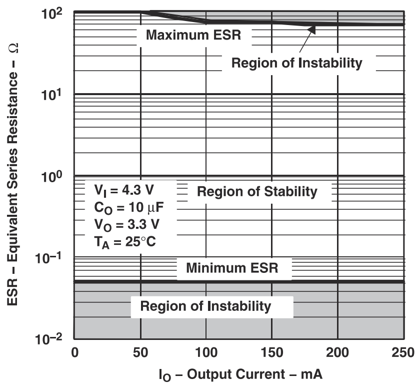


图 5-53. Typical Region of Stability ESR vs Output Current (Legacy Chip)

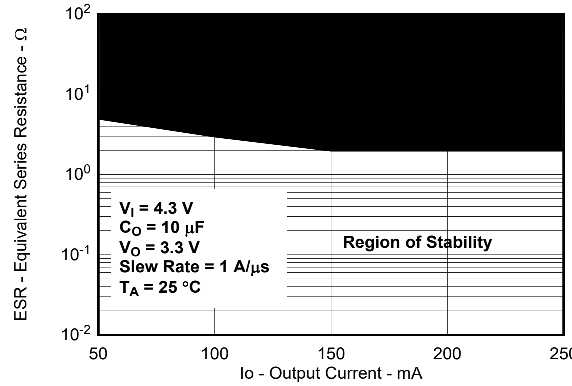


图 5-54. Typical Region of Stability ESR vs Output Current (New Chip)

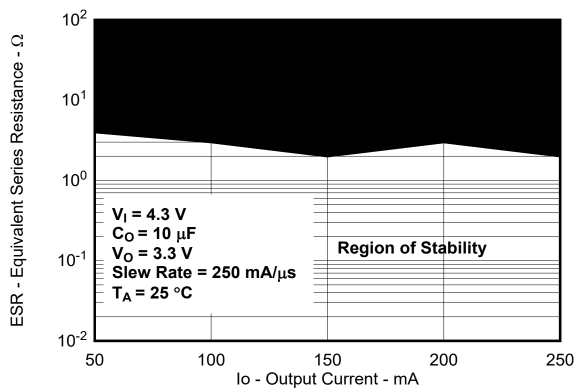


图 5-55. Typical Region of Stability ESR vs Output Current (New Chip)

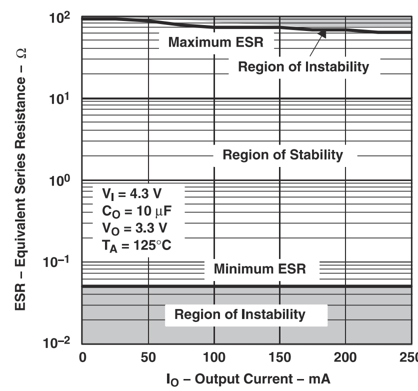


图 5-56. Typical Region of Stability ESR vs Output Current (Legacy Chip)

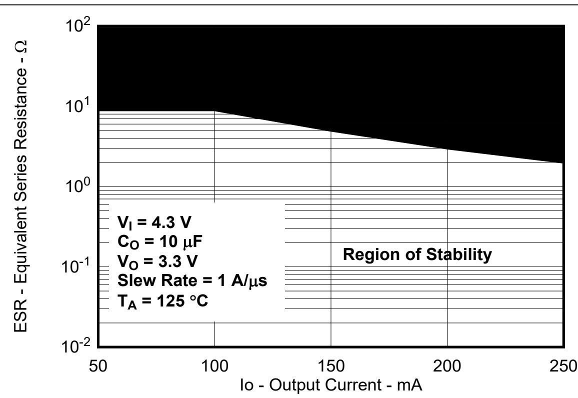


图 5-57. Typical Region of Stability ESR vs Output Current (New Chip)

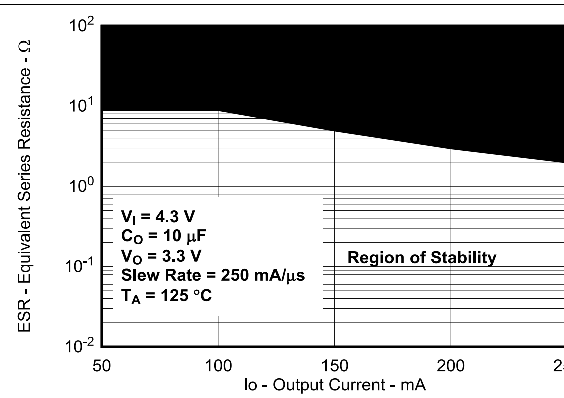


图 5-58. Typical Region of Stability ESR vs Output Current (New Chip)

5.9 Typical Characteristics: Supported ESR Range (continued)

Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PCB trace resistance to C_O. The setup shown in the *Timing Diagram* section characterizes the ESR behavior across temperature.

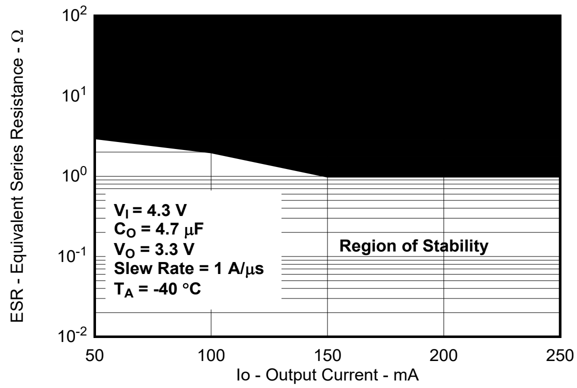


图 5-59. Typical Region of Stability ESR vs Output Current (New Chip)

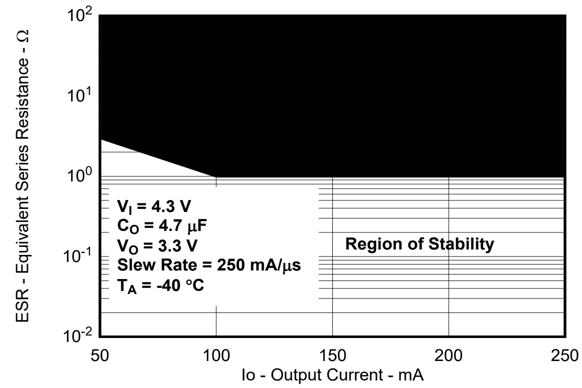


图 5-60. Typical Region of Stability ESR vs Output Current (Legacy Chip)

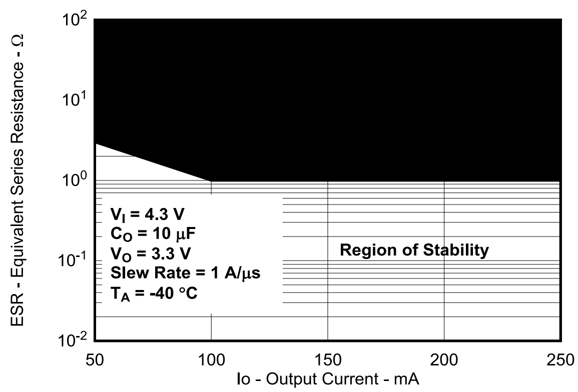


图 5-61. Typical Region of Stability ESR vs Output Current (New Chip)

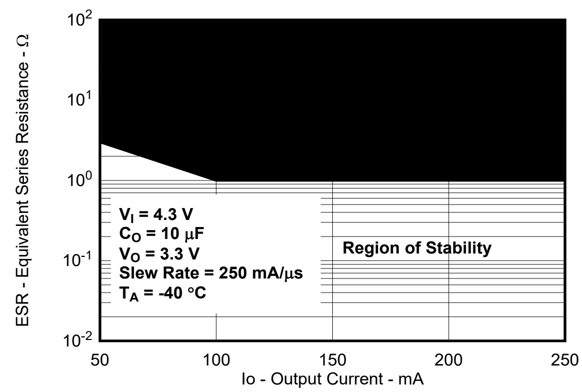


图 5-62. Typical Region of Stability ESR vs Output Current (New Chip)

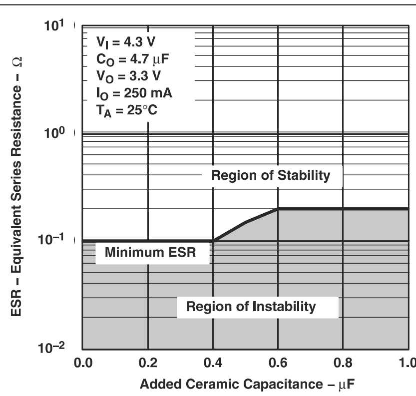


图 5-63. Typical Region of Stability ESR vs Added Ceramic Capacitance (Legacy Chip)

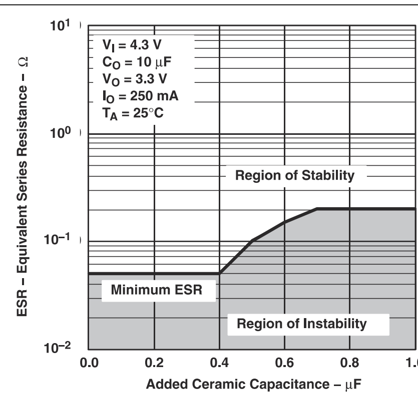


图 5-64. Typical Region of Stability ESR vs Added Ceramic Capacitance (Legacy Chip)

6 Detailed Description

6.1 Overview

The TPS766 is a low quiescent current, high PSRR, low-dropout (LDO) voltage regulator capable of handling up to 250mA of the load current. Low quiescent current consumption makes the TPS766 designed for battery-powered applications.

The TPS766 features an integrated overcurrent limit, thermal shutdown, output enable, internal output pulldown, and undervoltage lockout (UVLO). This device delivers excellent line and load transient performance and supports a wide range of ESR (up to 2Ω for the new chip). The operating ambient temperature range of the device is –40°C to +125°C.

6.2 Functional Block Diagrams

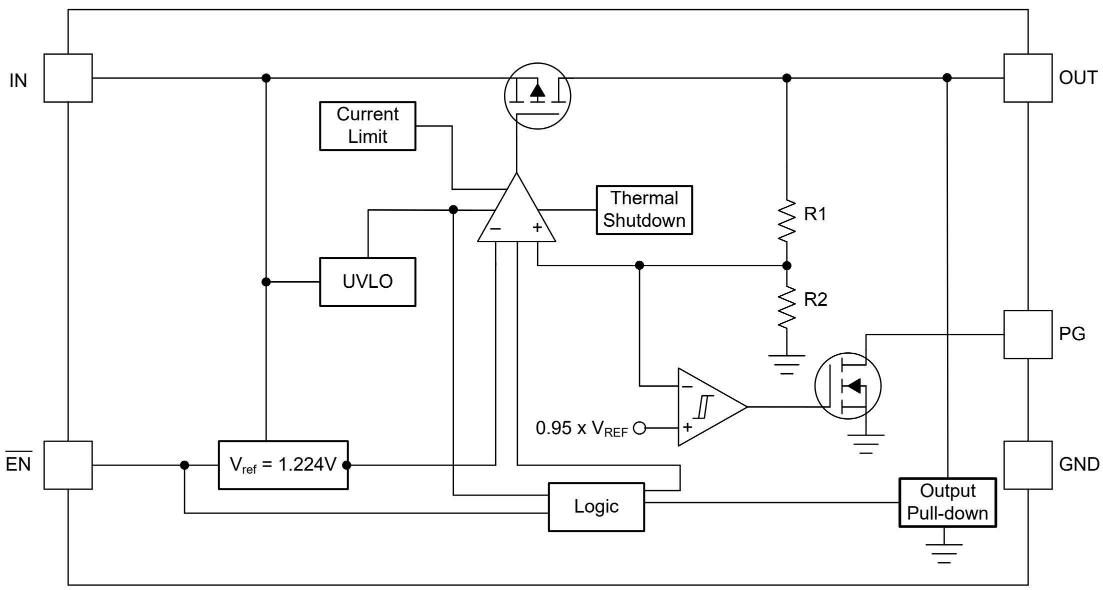


图 6-1. Fixed Version

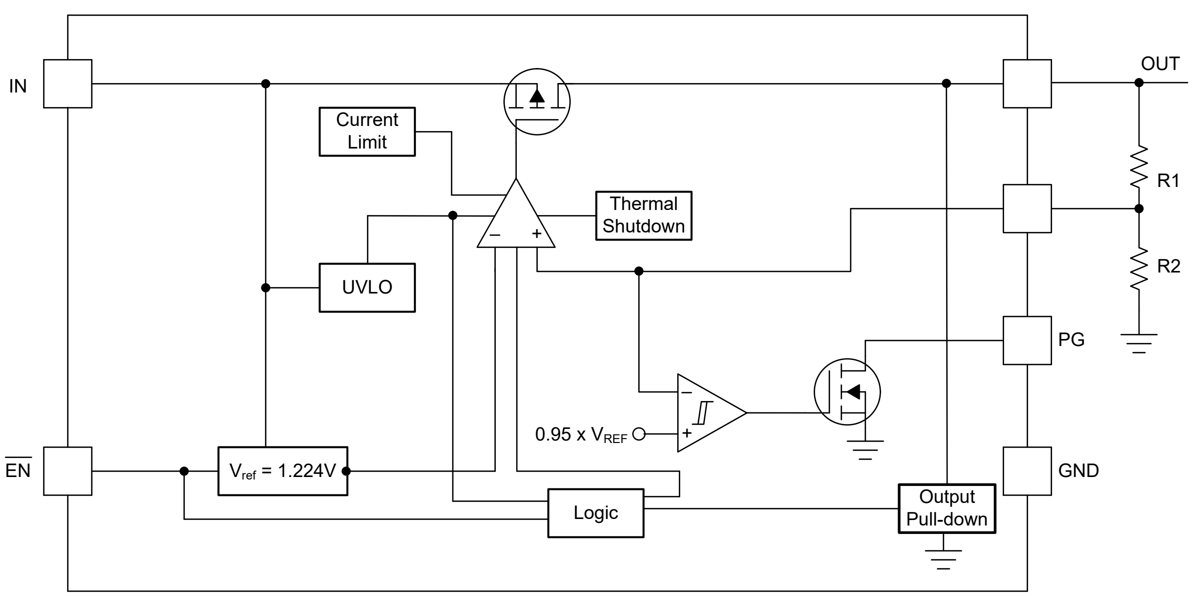


图 6-2. Adjustable Version

6.3 Feature Description

6.3.1 Output Enable

The enable pin for the device is an active-low pin. The output voltage is enabled when the voltage of the enable pin is lower than the low-level input voltage of the $\overline{EN}$ pin, and is disabled when the enable pin voltage is higher than the high-level input voltage of the $\overline{EN}$ pin. If $\overline{EN}$ functionality is not needed, connect the enable pin to the GND of the device.

For the new chip, there is an internal pullup current on the $\overline{EN}$ pin. Therefore, leave the $\overline{EN}$ pin floating. If the $\overline{EN}$ pin is left floating, the LDO is disabled.

In the new chip, the device has an internal output pulldown circuit that activates when the device is disabled to actively discharge the output voltage; see the *Output Pulldown* section.

6.3.2 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage (V_{IN} – V_{OUT}) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

6.3.3 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. For more information on current limits, see the *Know Your Limits* application note.

图 6-3 shows a diagram of the current limit.

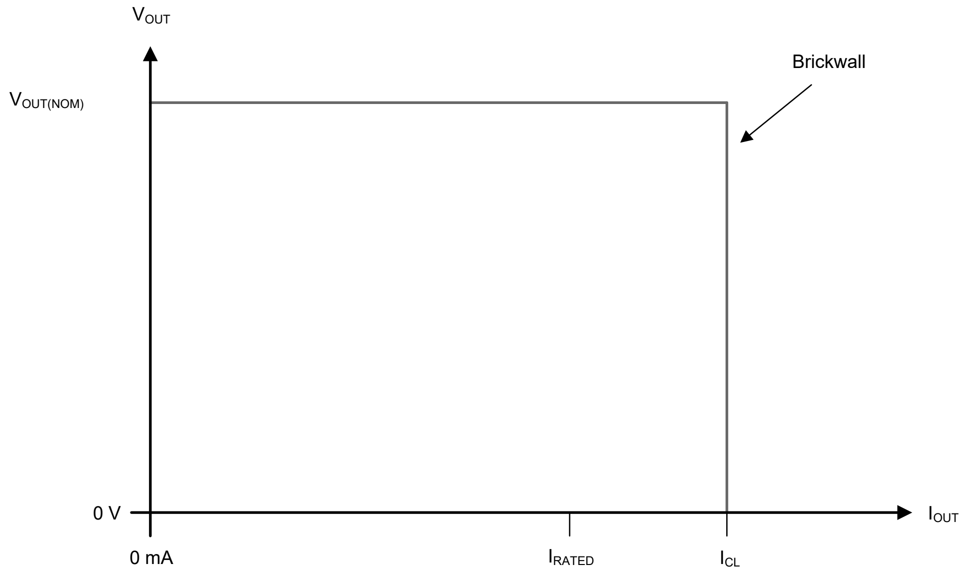


图 6-3. Current Limit

6.3.4 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. The UVLO circuit has hysteresis functionality to prevent the device from turning off if the input drops during turn on.

6.3.5 Power-Good Function

The power-good circuit monitors the voltage at the output pin to indicate the health of the LDO output. When the output voltage falls below the PG threshold voltage (PG_{TH}), the PG pin open-drain output engages and pulls the PG pin close to GND. When the output voltage exceeds PG_{TH} + $PG_{Hysteresis}$, the PG pin becomes high impedance. The open-drain output requires a pullup resistor. By connecting a pullup resistor to an external supply, any downstream device receives power-good as a logic signal for use in sequencing. Additionally, tie the open-drain output to other open-drain outputs to implement an AND logic. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device.

When using a feed-forward capacitor (C_{FF}), the time constant for the LDO start-up is increased but the power-good output time constant stays the same, possibly resulting in an invalid status of the power-good output. To avoid this issue, and to receive a valid PG output, make sure that the time constant of both the LDO start-up and the power-good output match. This matching is done by adding a capacitor in parallel with the power-good pullup resistor. For more information, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note.

The state of PG is only valid when the device operates above the minimum input voltage of the device and power-good is asserted, regardless of the output voltage state when the input voltage falls below the UVLO threshold minus the UVLO hysteresis. When the input voltage falls below approximately 0.8V, there is not enough gate drive voltage to keep the open-drain, power-good device turned on and the power-good output pulled high. Connecting the power-good pullup resistor to the output voltage helps minimize this effect.

6.3.6 Output Pulldown

The device (new chip) has an output pulldown circuit. The output pulldown circuit activates under the following conditions:

- The device is disabled with $\overline{EN}$ logic
- 1.0V < V_{IN} < V_{UVLO}

The output pulldown resistance for this device is 1.5kΩ (typ), as listed in the *Electrical Characteristics* table.

Reverse current flows from the output to the input. Thus, do not rely on the output pulldown circuit for discharging a large amount of output capacitance after the input supply collapses. This reverse current flow potentially causes damage to the device. See the *Reverse Current* section for more details.

6.3.7 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis makes sure that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time constant of the semiconductor die is fairly short, thus the device cycles on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start-up is sometimes high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.4 Device Functional Modes

6.4.1 Device Functional Mode Comparison

表 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

表 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} < V_{EN(LOW)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} < V_{EN(LOW)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} > V_{EN(HI)}$	Not applicable	$T_J > T_{SD(shutdown)}$

6.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The current sourced from OUT is less than the current limit ($I_{OUT} < I_{CL(OUT)}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage was previously lowered than the enable low level threshold voltage and has not yet increased higher than the enable high level threshold or the $\overline{EN}$ pin is connected to ground

6.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout potentially result in large output voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(nom)} + V_{DO}$, directly after being in a normal regulation state, but not during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$), the output voltage overshoots for a short period of time while the device pulls the pass transistor back into the linear region.

6.4.4 Disabled

The output of the device is shutdown by forcing the voltage of the enable pin to be more than the minimum EN pin high-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

The TPS766 LDO provides a very accurate output with high PSRR and excellent line and load transient performance and is capable of handling up to 250mA of the load current. Low quiescent current consumption makes the TPS766 designed for battery-powered applications. The TPS766 low dropout at a full load of 250mA helps extend the battery operation range.

7.2 Typical Application

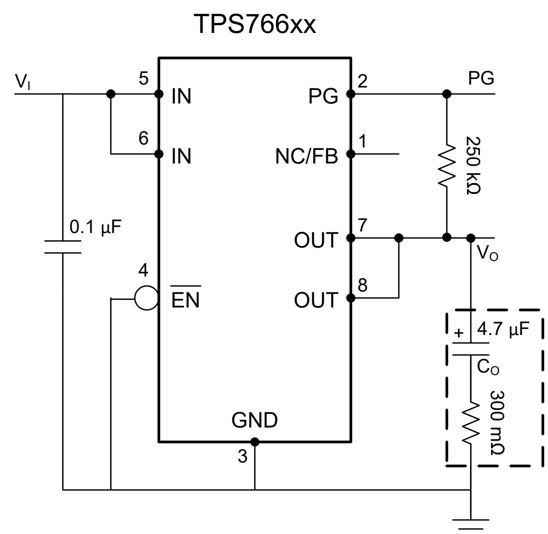
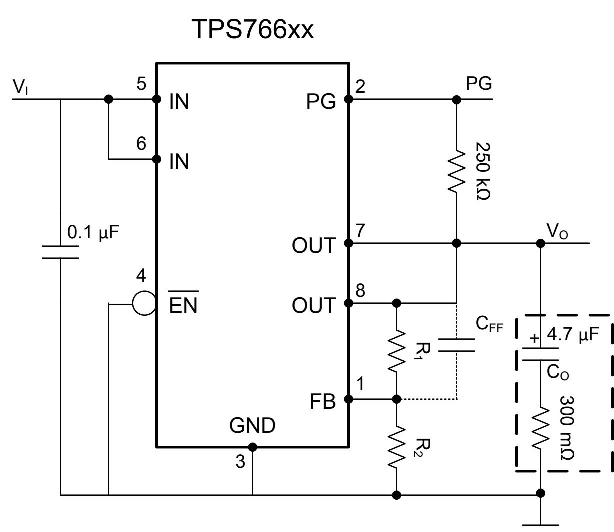


图 7-1. Typical Application Circuit (Fixed-Voltage Version)



Dotted lines indicate an optional C_{FF} capacitor (new chip). See the *Feed-Forward Capacitor (C_{FF})* section.

图 7-2. Typical Application Circuit (Adjustable-Voltage Version)

表 7-1 lists the R_1 and R_2 resistor values for the adjustable-voltage version.

表 7-1. Adjustable Output Voltage for Resistors R_1 and R_2

OUTPUT VOLTAGE	R_1 (kΩ)	R_2 (kΩ)
2.5V	174	169
3.3V	287	169
3.6V	324	169
4.0V	383	169
5.0V	523	169

7.2.1 Design Requirements

表 7-2 summarizes the design requirements of 表 7-1.

表 7-2. Design Parameters

PARAMETER	VALUE
Input voltage (V_{IN})	12V
Output voltage (V_{OUT})	3.3V
Output current (I_L)	100mA
Enable voltage ($\overline{EN}$)	0V
Weak pullup resistor for the PG pin	250kΩ

7.2.2 Detailed Design Procedure

7.2.2.1 Adjustable Device Feedback Resistors

The adjustable-version device requires external feedback divider resistors to set the output voltage. V_{OUT} is set using the feedback divider resistors, R_1 and R_2, according to the following equation:

$$V_{OUT} = V_{REF} \times (1 + R_1 / R_2) \quad (2)$$

where:

- V_{REF} = 1.224V (typ) for the internal reference voltage

To ignore the FB pin current error term in the V_{OUT} equation, set the feedback divider current to 100 times the FB pin current listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leqslant V_{OUT} / (I_{FB} \times 100) \quad (3)$$

In 表 7-1, examples of R_1 and R_2 values are given for different output voltage options with a feedback divider current designed at 7 µA.

7.2.2.2 Recommended Capacitor Types

The device (new chip) is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but use good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas using Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors discussed in the 节 5.3 table account for an effective capacitance of approximately 50% of the nominal value.

7.2.2.3 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5Ω. Use a higher value capacitor if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

As with most low-dropout regulators, the TPS766 requires an output capacitor connected between OUT and GND to stabilize the internal control loop.

Legacy chip: The minimum recommended capacitance value is 4.7μF and the equivalent series resistance (ESR) is between 300mΩ and 20Ω. Capacitor values of 4.7μF or larger are acceptable, provided the ESR is less than 20Ω. Solid tantalum electrolytic and aluminum electrolytic capacitors are all suitable, provided these capacitors meet the requirements described previously. Ceramic capacitors, with series resistors sized to meet the previously described requirements, are another option.

New chip: The device is designed to be stable using low ESR ceramic capacitors at the input and output. The minimum recommended capacitance value is 2.2μF and the ESR range is up to 2Ω. The supported ESR range depends on the output capacitance, operating junction temperature, and load current conditions. The *Typical Characteristics: Supported ESR Range* describes the supported ESR range in regards to the output capacitance across temperature for the supported load current range.

Dynamic performance of the device is improved by using an output capacitor. Use an output capacitor within the range specified in the *节 5.3* table for stability.

7.2.2.4 Reverse Current

Excessive reverse current potentially damages this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current occur are outlined in this section, all of which potentially exceed the absolute maximum rating of $V_{OUT} \leqslant V_{IN} + 0.3V$.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection is recommended to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

图 7-3 shows one approach for protecting the device.

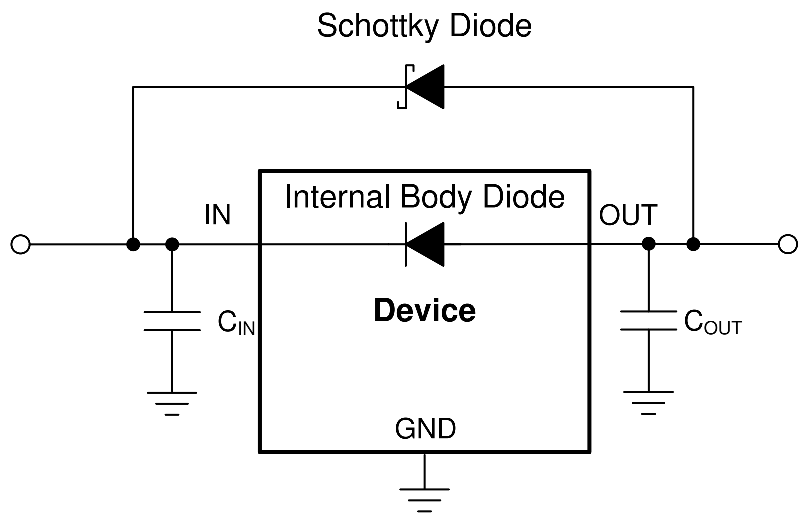


图 7-3. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.2.2.5 Feed-Forward Capacitor (C_{FF})

For the adjustable-voltage version device, connect a feed-forward capacitor (C_{FF}) from the OUT pin to the FB pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended C_{FF} values are listed in the *Recommended Operating Conditions* table. If a higher capacitance C_{FF} is used, the start-up time increases. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note.

C_{FF} and R_1 form a zero in the loop gain at frequency f_Z, while C_{FF}, R_1, and R_2 form a pole in the loop gain at frequency f_P. Calculate the C_{FF} zero and pole frequencies from the following equations:

$$f_Z = 1 / (2 \times \pi \times C_{FF} \times R_1) \quad (4)$$

$$f_P = 1 / (2 \times \pi \times C_{FF} \times (R_1 \parallel R_2)) \quad (5)$$

$C_{FF} \geqslant 10pF$ is required for stability if the feedback divider current is less than 5μA. The following equation calculates the feedback divider current.

$$I_{FB\_Divider} = V_{OUT} / (R_1 + R_2) \quad (6)$$

To avoid start-up time increases from C_{FF}, limit the product $C_{FF} \times R_1 < 50\mu s$.

For an output voltage of 1.224V with the FB pin tied to the OUT pin, no C_{FF} is used.

7.2.2.6 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. Place few or no other heat-generating devices that cause added thermal stress in the PCB area around the regulator.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (7)$$

备注

Minimize power dissipation, and therefore achieve greater efficiency, by correctly selecting the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (8)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information (New Chip)* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance. As mentioned in the *An empirical analysis of the impact of board layout on LDO thermal performance* application note, $R_{\theta JA}$ is improved by 35% to 55% compared to the *Thermal Information (New Chip)* table value by optimizing the PCB board layout.

7.2.2.7 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information (New Chip)* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (9)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (10)$$

where:

- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

7.2.3 Application Curves

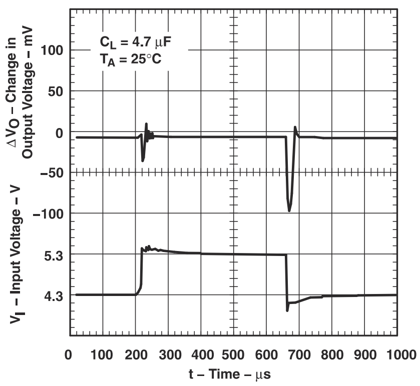


图 7-4. TPS76633 Line Transient Response (Legacy Chip)

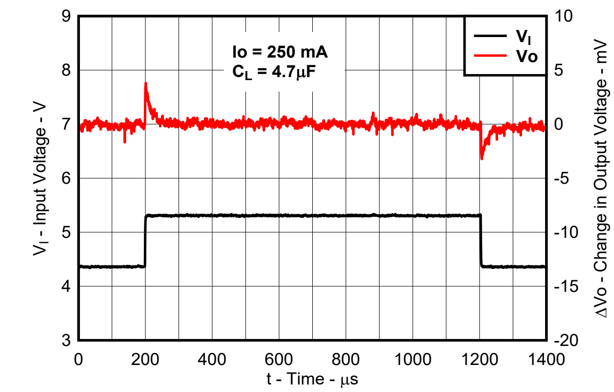


图 7-5. TPS76633 Line Transient Response (New Chip)

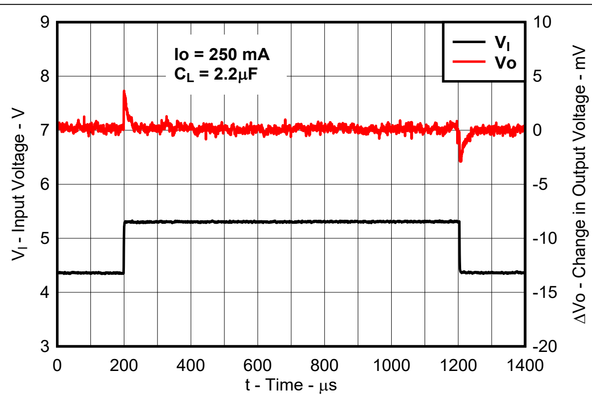


图 7-6. TPS76633 Line Transient Response (New Chip)

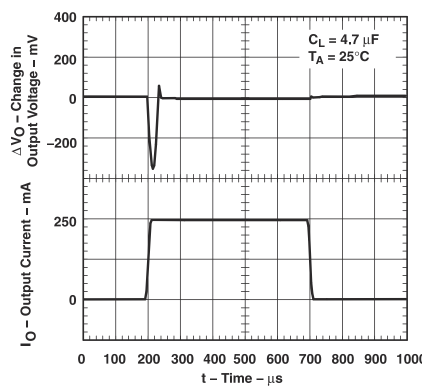


图 7-7. TPS76633 Load Transient Response (Legacy Chip)

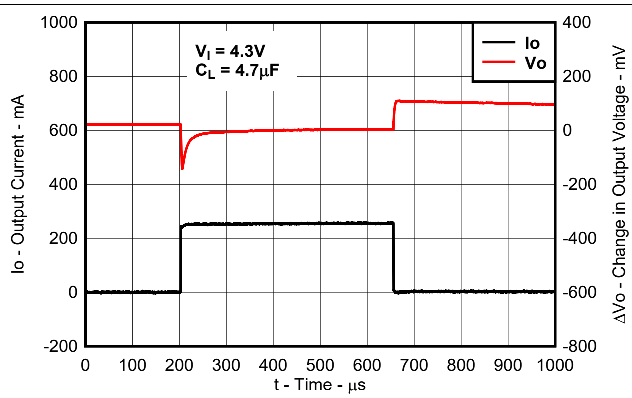


图 7-8. TPS76633 Load Transient Response (New Chip)

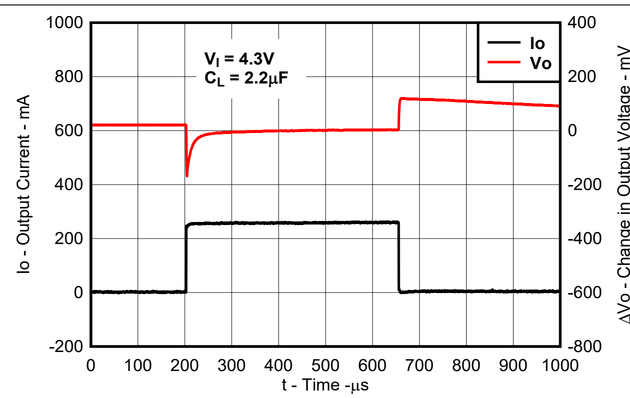


图 7-9. TPS76633 Load Transient Response (New Chip)

7.2.3 Application Curves (continued)

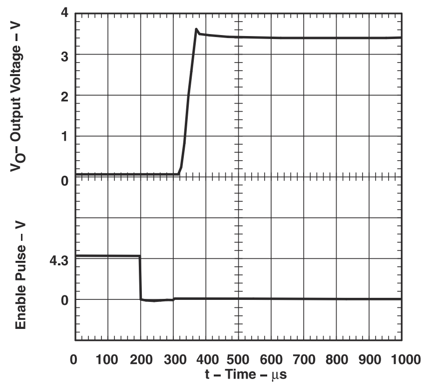
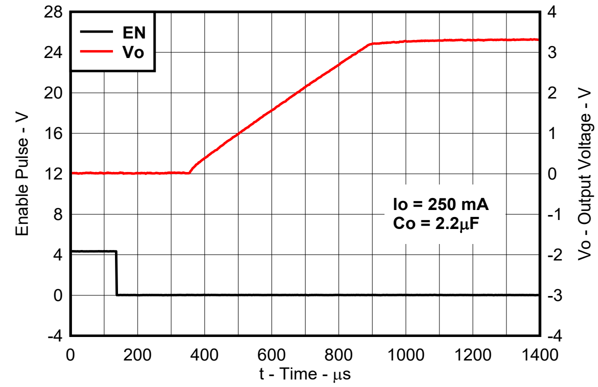
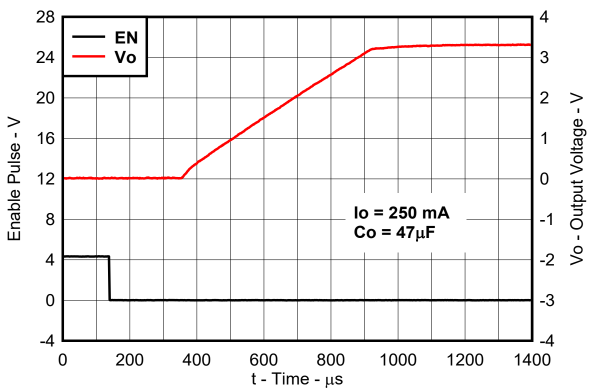


图 7-10. TPS76633 Output Voltage vs Time (Legacy Chip)



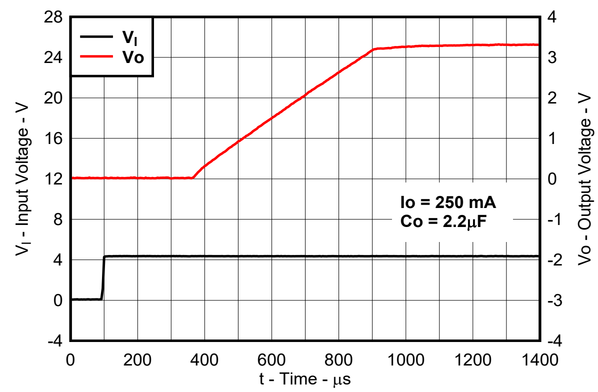
Start-up with EN sequencing

图 7-11. TPS76633 Output Voltage vs Time (New Chip)



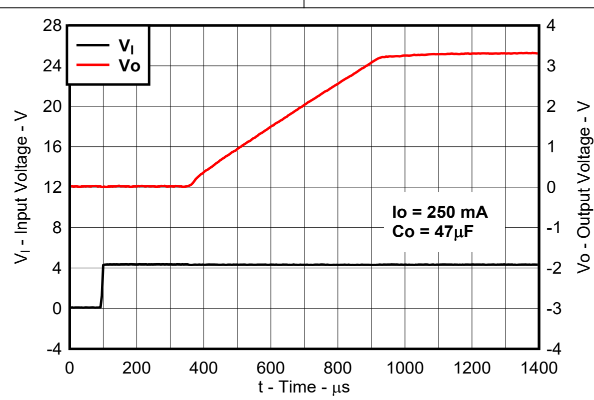
Start-up with EN sequencing

图 7-12. TPS76633 Output Voltage vs Time (New Chip)



Start-up with V_{IN} sequencing

图 7-13. TPS76633 Output Voltage vs Time (New Chip)



Start-up with V_{IN} sequencing

图 7-14. TPS76633 Output Voltage vs Time (New Chip)

7.3 Power Supply Recommendations

The TPS766 is designed to operate from an input voltage supply range between 2.5V and 16V (new chip). The input voltage range provides adequate headroom for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR help improve the output noise performance.

7.4 Layout

7.4.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the printed circuit board (PCB) and as near as practical to the respective LDO pin connections. Place ground return connections for the input and output capacitors as close to the GND pin as possible, using wide, component-side, copper planes. Do not use vias and long traces to create LDO circuit connections to the input capacitor, output capacitor, or the resistor divider because this practice negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the PCB or located on the bottom side of the PCB opposite the components. This reference plane serves to design for the accuracy of the output voltage and shield the LDO from noise.

7.4.2 Layout Example

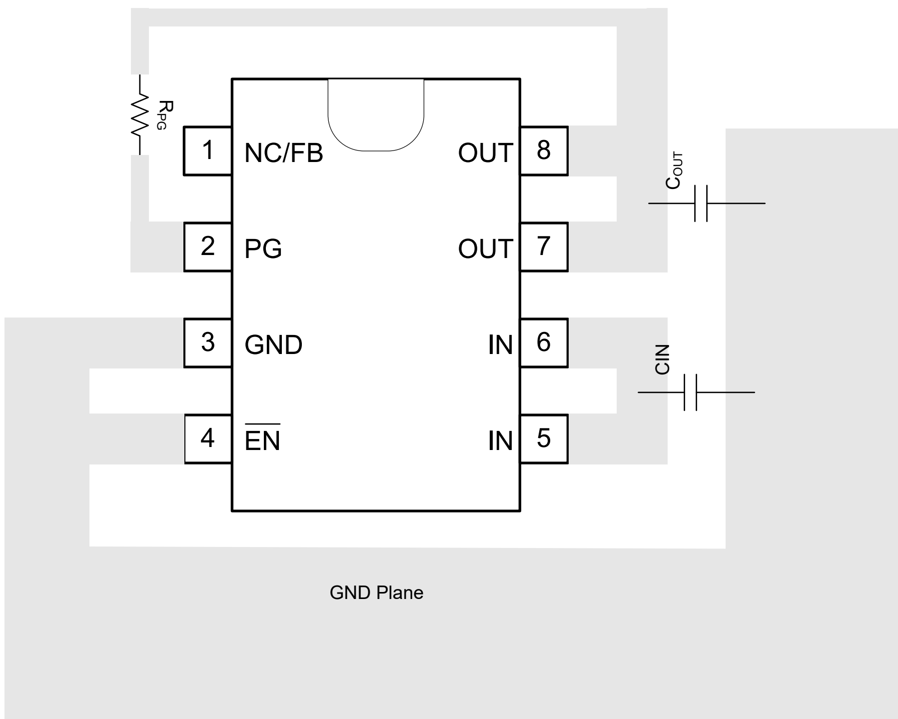


图 7-15. Fixed Version Example Layout

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed in this section.

8.1 Documentation Support

8.1.1 Device Nomenclature

表 8-1. Device Nomenclature(1)(2)

PRODUCT	V_{OUT}
TPS766**xxyz** Legacy chip	**xx** is the nominal output voltage (for example, 33 = 3.3V, 01 = adjustable). **y** is the package designator. **z** is the package quantity.
TPS766**xxyz M3** New chip	**xx** is the nominal output voltage (for example, 33 = 3.3V, 01 = adjustable). **yyy** is the package designator. **z** is the package quantity. **M3** is a suffix designator for new chip redesigns on the latest TI process technology.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Output voltages from 1.25V to 12V are available through the use of innovative factory EEPROM programming; minimum order quantities may apply. Contact factory for details and availability.

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

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8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (December 2023) to Revision E (March 2024) **Page**

- Changed ESD ratings for the new chip........ 5
- Changed > to ⩾ for inclusion of 3.3 V in the output range........ 7

Changes from Revision C (January 2009) to Revision D (December 2023) **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式............ 1
- 添加了*应用*、*ESD 等级*、*热性能信息*、*概述*、*特性说明*、*器件功能模式*、*应用和实施*、*电源相关建议*、*布局*、*器件和文档* 以及*机械、封装和可订购信息* 部分和*封装信息* 表............ 1
- 更改了整个文档，以便与当前系列格式保持一致............ 1
- 向文档添加了 M3 器件............ 1
- Added *Device Nomenclature* section............ 34

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS76601D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	76601
TPS76601DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	76601
TPS76615D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	76615
TPS76615DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	76615
TPS76618D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	76618
TPS76618DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	76618
TPS76625D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	76625
TPS76625DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	76625
TPS76628D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	76628
TPS76628DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	76628
TPS76630D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	76630
TPS76633D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	76633
TPS76633DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76633
TPS76633DRM3	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76633
TPS76650D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	76650
TPS76650DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	76650
TPS76650DRM3	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	76650

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

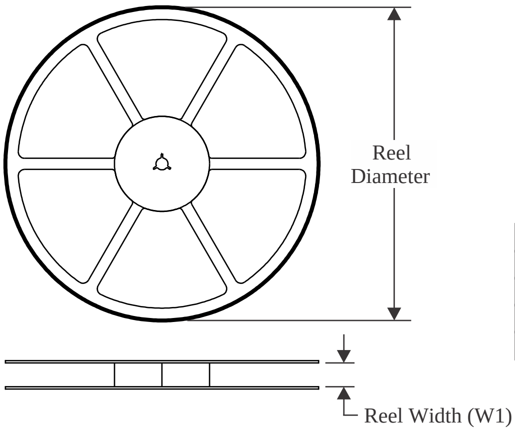
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

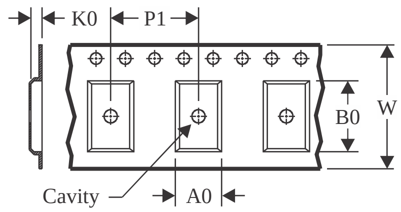
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

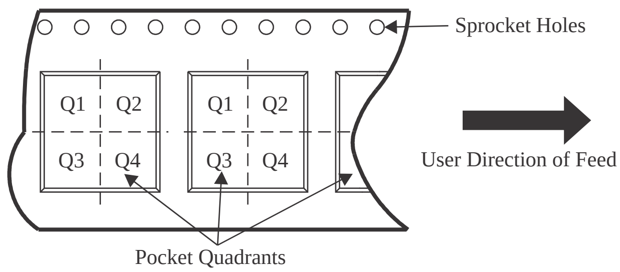


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

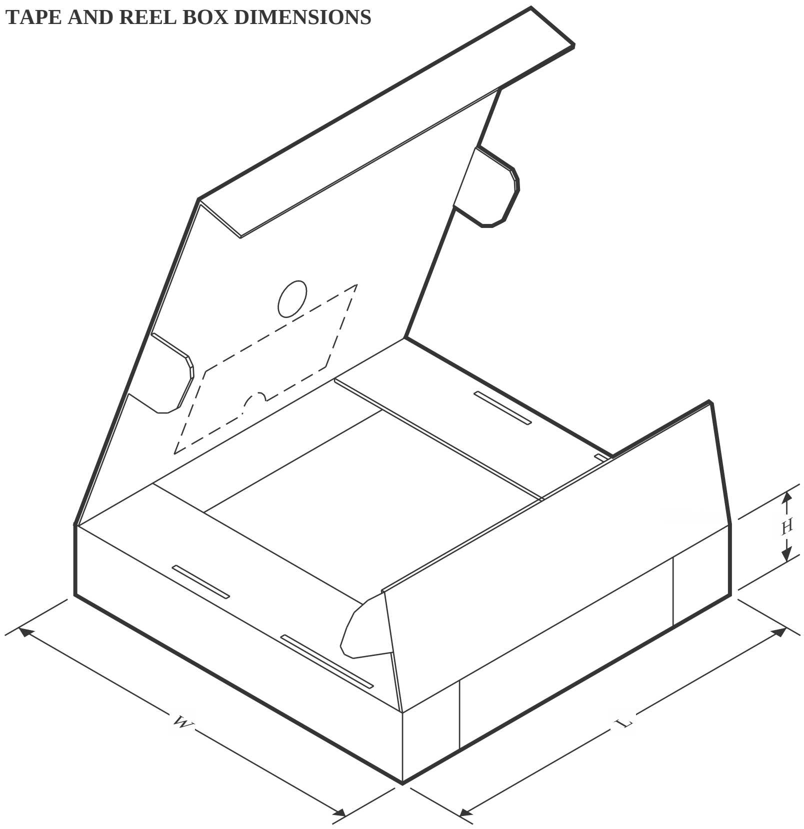
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS76601DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76615DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76618DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76625DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76628DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76633DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76633DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76633DRM3	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76650DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS76650DRM3	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

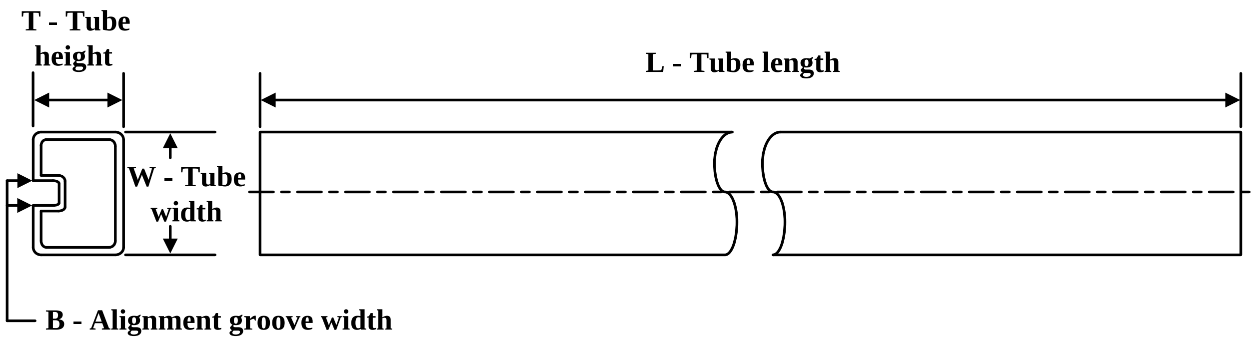
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

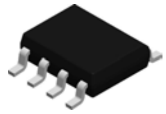
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS76601DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS76615DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS76618DR	SOIC	D	8	2500	353.0	353.0	32.0
TPS76625DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS76628DR	SOIC	D	8	2500	350.0	350.0	43.0
TPS76633DR	SOIC	D	8	2500	353.0	353.0	32.0
TPS76633DR	SOIC	D	8	2500	356.0	356.0	35.0
TPS76633DRM3	SOIC	D	8	3000	356.0	356.0	35.0
TPS76650DR	SOIC	D	8	2500	353.0	353.0	32.0
TPS76650DRM3	SOIC	D	8	3000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS76601D	D	SOIC	8	75	505.46	6.76	3810	4
TPS76601DG4	D	SOIC	8	75	505.46	6.76	3810	4
TPS76615D	D	SOIC	8	75	505.46	6.76	3810	4
TPS76618D	D	SOIC	8	75	505.46	6.76	3810	4
TPS76625D	D	SOIC	8	75	505.46	6.76	3810	4
TPS76628D	D	SOIC	8	75	505.46	6.76	3810	4
TPS76630D	D	SOIC	8	75	505.46	6.76	3810	4
TPS76650D	D	SOIC	8	75	505.46	6.76	3810	4

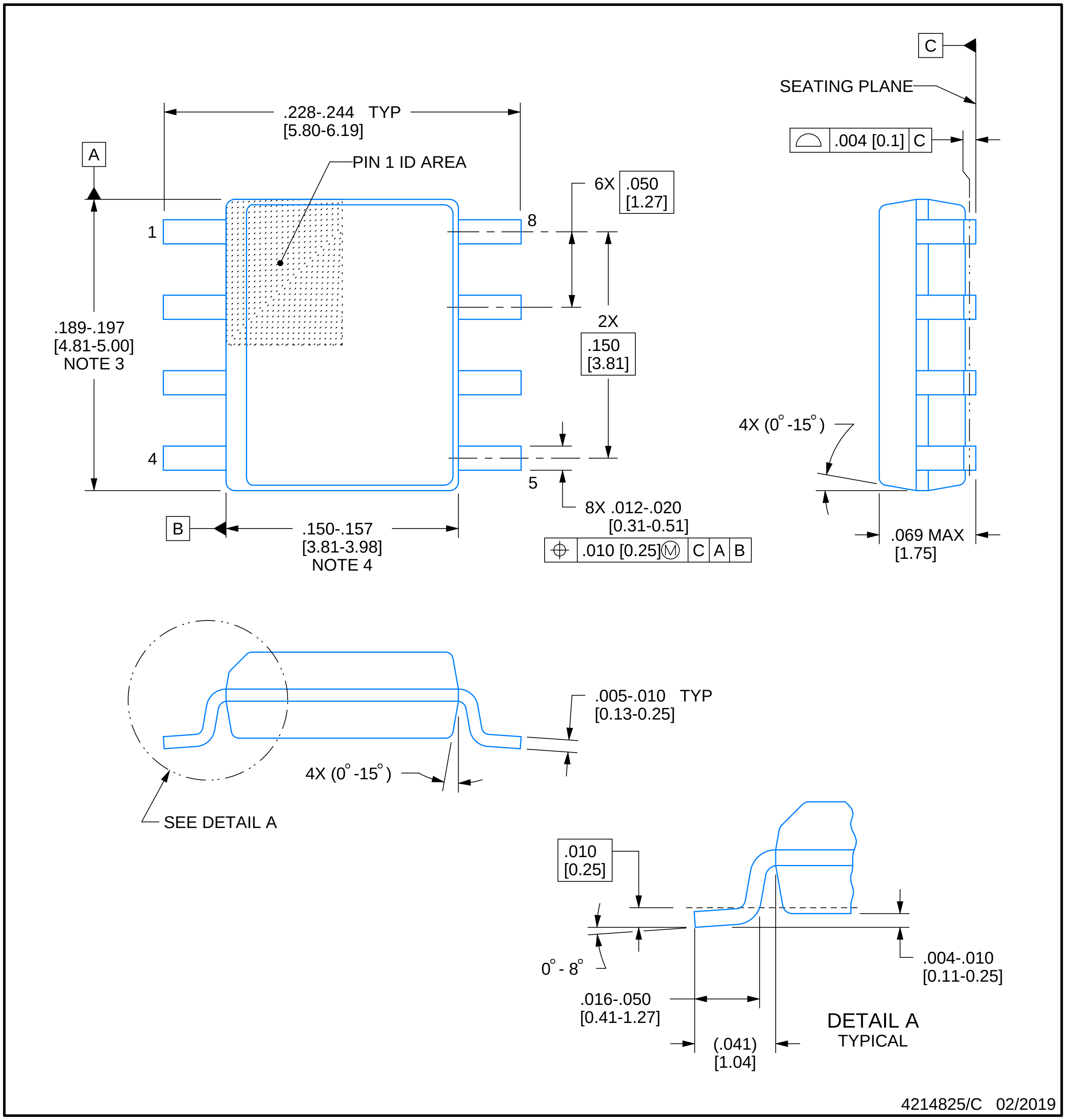


PACKAGE OUTLINE

D0008A

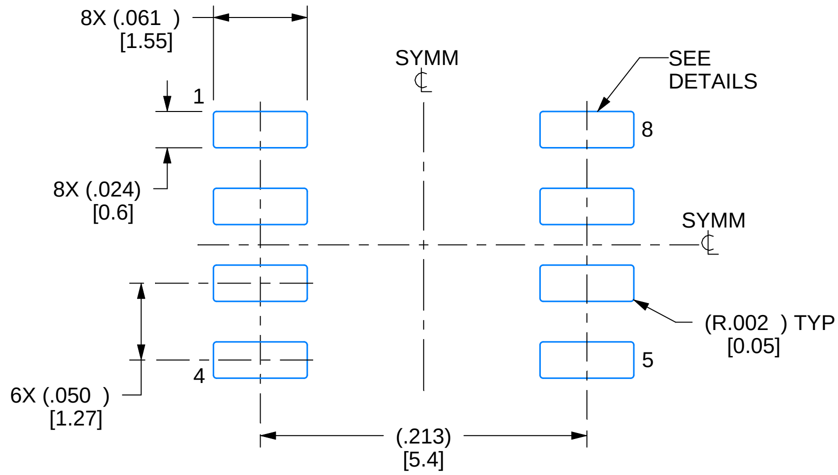
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

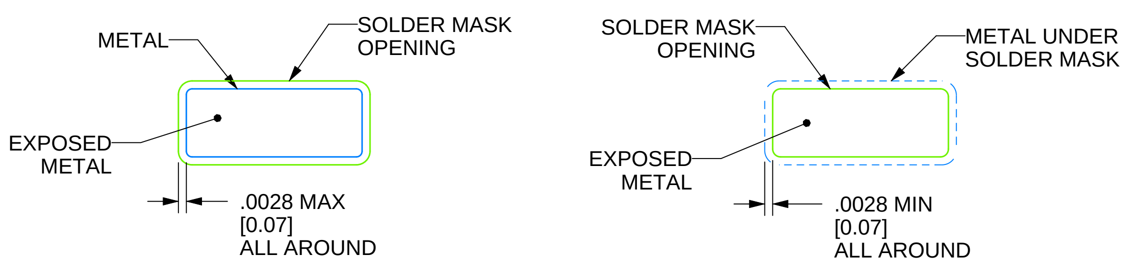


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

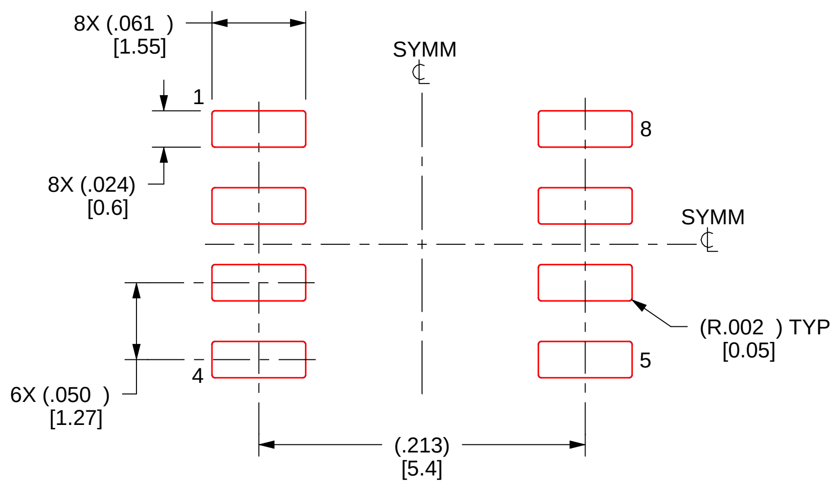
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265