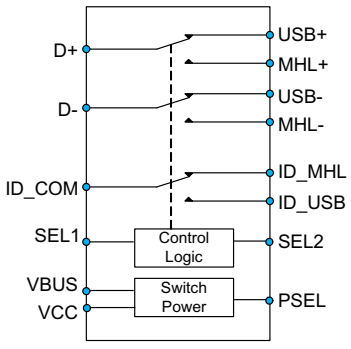
TS3USB3200 具备附加 SPDT ID 选择开关和灵活电源控制的 SPDT USB 2.0 高速 (480Mbps) 和移动高清链接 (MHL) 或移动显示端口 (MyDP) 开关

1 特性

- V_{CC} 范围：2.7V 至 4.3V
- 移动高清链接 (MHL) 或移动显示端口 (MyDP) 开关
  - 带宽 (-3dB)：-5.5GHz
  - Ron（典型值）：5.7Ω
  - Con（典型值）：2,5pF
- USB 开关
  - 带宽 (-3dB)：-5.5GHz
  - Ron（典型值）：4.6Ω
  - Con（典型值）：2,5pF
- 电流消耗：40μA（典型值）
- 特殊 特性
  - 灵活的电源控制：器件可通过 V_{BUS}（不使用 V_{CC}）或单独使用 V_{CC} 供电
  - I_{OFF} 保护防止在掉电状态（V_{CC} 和 V_{BUS} = 0V）下产生泄漏电流
  - 1.8V 兼容控制输入（SEL1、SEL2 和 PSEL）
  - 所有 I/O 引脚上的过压容限 (OVT) 高达 5.5V，而且无需使用外部组件
- 静电放电 (ESD) 性能:
  - 3.5kV 人体放电模型（A114B，II 类）
  - 1kV 带电器件模型 (C101)
- 封装：
  - 16 引脚超薄四方扁平无引线 (UQFN) 封装（2.6 mm×1.8mm，0.4mm 间距）

开关图



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2 应用范围

- USB 2.0 应用
- 移动高清链接 (MHL) 应用
- 移动显示端口 (MyDP) 应用
- 移动电话

3 说明

TS3USB3200 是一款差分单刀双掷 (DPDT) 多路复用器，在同一封装内包含一个高速移动高清链接 (MHL) 开关或移动显示端口 (MyDP) 开关以及一个 USB 2.0 高速

(480Mbps) 开关。此外，此器件还包括一个用于简化信息控制的单刀双掷 (SPDT) USB/MHL 或 MyDP ID 开关。这些配置使得系统设计人员能够为 MHL/MyDP 视频信号和 USB 数据使用一个普通 USB 或者微型 USB 连接器。

TS3USB3200 具有一个 2.7V 至 4.3V 的 V_{CC}范围，并且可选择由 V_{BUS}（不使用 V_{CC}）供电。该器件支持过压容限 (OVT) 特性，允许 I/O 引脚承受过压条件（最高可达 5.5V）。当供电消失时，断电保护特性强制所有 I/O 引脚变为高阻抗模式。这样可实现信号线路的完全隔离，从而避免的过多的泄漏电流。TS3USB3200 的选择引脚与 1.8V 控制电压兼容，允许它们直接与移动处理器的通用 I/O (GPIO) 相连。

TS3USB3200 采用小型 16 引脚 UQFN 封装（尺寸为 2.6mm × 1.8mm），是移动应用的 理想选择。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TS3USB3200	UQFN (16)	2.60mm x 1.80mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (July 2013) to Revision B **Page**

- 已添加 *ESD 额定值*表，*特性 描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分。 ... 1
- 已删除*订购信息*表，请参见数据表末尾的 POA ... 1
- Changed *Thermal Information* table ... 4

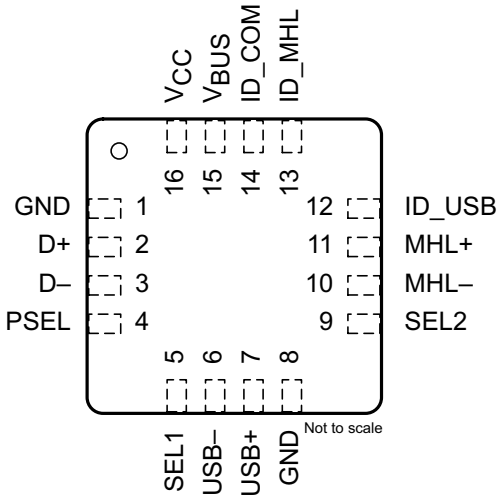
Changes from Original (June 2012) to Revision A **Page**

- 添加了移动显示端口 (MyDP) 选项功能性。 ... 1
- Changed $V_{I/O}$ MIN value from –0.3 to –0.5. ... 4
- Updated Typical Application diagrams. ... 11

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5 Pin Configuration and Functions

RSV Package
16-Pin UQFN
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	GND	Ground	Ground
2	D+	I/O	Data Signal Path (Differential +)
3	D–	I/O	Data Signal Path (Differential –)
4	PSEL	Input	Power Source Select Line
5	SEL1	Input	Control Input Select Line 1
6	USB–	I/O	USB Data Signal Path (Differential –)
7	USB+	I/O	USB Data Signal Path (Differential +)
8	GND	Ground	Ground
9	SEL2	Input	Control Input Select Line 2
10	MHL–	I/O	MHL Data Signal Path (Differential–)
11	MHL+	I/O	MHL Data Signal Path (Differential +)
12	ID_USB	I/O	ID Signal Path for USB
13	ID_MHL	I/O	ID Signal Path for MHL
14	ID_COM	I/O	ID Common Signal Path
15	V_{BUS}	Power	Alternative Device Power
16	V_{CC}	Power	Power supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
V_{CC} ,V_{BUS}	Supply voltage(3)		–0.3	5.5	V
$V_{I/O}$	Input/Output DC voltage(3)		–0.5	5.5	V
I_K	Input/Output port diode current	$V_{I/O}$ < 0	–50		mA
V_I	Digital input voltage range (SEL1, SEL2, PSEL)		–0.3	5.5	V
I_{IK}	Digital logic input clamp current(3)	V_I < 0	–50		mA
I_{CC}	Continuous current through V_{CC}			100	mA
I_{GND}	Continuous current through GND		–100		mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.7	4.3	V
V_{BUS}	V_{BUS} Supply voltage	4.3	5.5	V
$V_{I/O\ (USB)}$ $V_{I/O\ (ID)}$	Analog voltage for USB and ID signal path	0	3.6	V
$V_{I/O\ (MHL)}$	Analog voltage for MHL signal path	1.6	3.4	V
V_I	Digital input voltage (SEL1, SEL2, PSEL)	0	V_{CC}	V
$T_{RAMP\ (VCC)}$	Power supply ramp time requirement (V_{CC})	100	1000	µs/V
$T_{RAMP\ (VBUS)}$	Power supply ramp time requirement (V_{BUS})	100	1000	µs/V
T_A	Operating free-air temperature	–40	85	ºC

6.4 Thermal Information

THERMAL METRIC(1)		TS3USB3200 RSV (UQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	109.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

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6.5 Electrical Characteristics

T_A = –40°C to 85°C, Typical values are at V_{CC} = 3.3 V, T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
MHL SWITCH							
R_{ON}	ON-state resistance	V_{CC} = 2.7 V	$V_{I/O}$ = 1.6 V, I_{ON} = –8 mA		5.7		Ω
ΔR_{ON}	ON-state resistance match between + and – paths	V_{CC} = 2.7 V	$V_{I/O}$ = 1.6 V, I_{ON} = –8 mA		0.4		Ω
$R_{ON\ (FLAT)}$	ON-state resistance flatness	V_{CC} = 2.7 V	$V_{I/O}$ = 1.6 V to 3.4 V, I_{ON} = –8 mA		1		Ω
I_{OZ}	OFF leakage current	V_{CC} = 4.3 V	Switch OFF, $V_{MHL+/MHL-}$ = 1.6 V to 3.4 V, $V_{D+/D-}$ = 0 V	–2		2	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0 V	Switch ON or OFF, $V_{MHL+/MHL-}$ = 1.6 V to 3.4 V, $V_{D+/D-}$ = NC	–10		10	µA
I_{ON}	ON leakage current	V_{CC} = 4.3 V	Switch ON, $V_{MHL+/MHL-}$ = 1.6 V to 3.4 V, $V_{D+/D-}$ = NC	–2		2	µA
USB SWITCH							
R_{ON}	ON-state resistance	V_{CC} = 2.7 V	$V_{I/O}$ = 0.4 V, I_{ON} = –8 mA		4.6		Ω
ΔR_{ON}	ON-state resistance match between + and – paths	V_{CC} = 2.7 V	$V_{I/O}$ = 0.4 V, I_{ON} = –8 mA		0.4		Ω
$R_{ON\ (FLAT)}$	ON-state resistance flatness	V_{CC} = 2.7 V	$V_{I/O}$ = 0 V to 0.4 V, I_{ON} = –8 mA		1		Ω
I_{OZ}	OFF leakage current	V_{CC} = 4.3 V	Switch OFF, $V_{USB+/USB-}$ = 0 V to 4.3 V, $V_{D+/D-}$ = 0 V	–2		2	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0 V	Switch ON or OFF, $V_{USB+/USB-}$ = 0 V to 4.3 V, $V_{D+/D-}$ = NC	–10		10	µA
I_{ON}	ON leakage current	V_{CC} = 4.3 V	Switch ON, $V_{USB+/USB-}$ = 0 V to 4.3 V, $V_{D+/D-}$ = NC	–2		2	µA
ID SWITCH							
R_{ON}	ON-state resistance	V_{CC} = 2.7 V	$V_{I/O}$ = 3.3 V, I_{ON} = –8 mA		6.5		Ω
ΔR_{ON}	ON-state resistance match between + and – paths	V_{CC} = 2.7 V	$V_{I/O}$ = 3.3 V, I_{ON} = –8 mA		0.4		Ω
I_{OZ}	OFF leakage current	V_{CC} = 4.3 V	Switch OFF, V_{ID_MHL/ID_USB} = 0 V to 4.3 V, V_{ID_COM} = 0 V	–1		1	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0 V	Switch ON or OFF, V_{ID_MHL/ID_USB} = 0 V to 4.3 V, V_{ID_COM} = NC	–10		10	µA
I_{ON}	ON leakage current	V_{CC} = 4.3 V	Switch ON, V_{ID_MHL/ID_USB} = 0 V to 4.3 V, V_{ID_COM} = 0 V	–1		1	µA
DIGITAL CONTROL INPUTS (SEL1, SEL2, PSEL)							
V_{IH}	Input logic high	V_{CC} = 2.7 V to 4.3 V		1.3			V
V_{IL}	Input logic low	V_{CC} = 2.7 V to 4.3 V				0.6	V
I_{IN}	Input leakage current	V_{CC} = 4.3 V, $V_{I/O}$ = 0 V to 4.3 V, V_{IN} = 0 V to 2 V		–10		10	µA

6.6 Dynamic Characteristics

T_A = –40°C to 85°C, Typical values are at V_{CC} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
MHL(1)/USB/ ID SWITCH							
t_{pd}	Propagation Delay	R_L = 50 Ω, C_L = 5 pF	V_{CC} = 2.7 V to 4.3 V		0.1		ns
t_{ON}	Turnon time	R_L = 50 Ω, C_L = 5 pF	V_{CC} = 2.7 V to 4.3 V			400	ns
t_{OFF}	Turnoff time	R_L = 50 Ω, C_L = 5 pF	V_{CC} = 2.7 V to 4.3 V			400	ns
$t_{SK(P)}$	Skew of opposite transitions of same output	V_{CC} = 2.7 V or 3.3V	V_{CC} = 2.7 V to 4.3 V		0.1	0.2	ns
$C_{ON(MHL)}$	MHL path ON capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 or 3.3 V, f = 240 MHz	Switch ON		1.6		pF
$C_{ON(USB)}$	USB path ON capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 or 3.3 V, f = 240 MHz	Switch ON		1.4		pF
$C_{OFF(MHL)}$	MHL path OFF capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 or 3.3 V, f = 240 MHz	Switch OFF		1.4		pF
$C_{OFF(USB)}$	USB path OFF capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 or 3.3 V, f = 240 MHz	Switch OFF		1.6		pF
C_I	Digital input capacitance	V_{CC} = 3.3 V, V_I = 0 or 2V			2.2		pF

(1) Specified by Design

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Dynamic Characteristics (continued)

T_A = –40°C to 85°C, Typical values are at V_{CC} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
O_{ISO}	OFF Isolation	V_{CC} = 2.7 V to 4.3 V, R_L = 50 Ω, f = 240 MHz	Switch OFF		–37		dB
X_{TALK}	Crosstalk	V_{CC} = 2.7 V to 4.3 V, R_L = 50 Ω, f = 240 MHz	Switch ON		–37		dB
$BW_{(MHL)}$	MHL path –3-dB bandwidth	V_{CC} = 2.7 V to 4.3 V, R_L = 50 Ω	Switch ON		5.5		GHz
$BW_{(USB)}$	USB path –3-dB bandwidth	V_{CC} = 2.7 V to 4.3 V, R_L = 50 Ω	Switch ON		5.5		GHz
$BW_{(ID)}$	ID path –3-dB bandwidth	V_{CC} = 2.7 V to 4.3 V, R_L = 50 Ω	Switch ON		4		GHz
SUPPLY							
V_{BUS}	V_{BUS} Power supply voltage			4.3		5.5	V
V_{CC}	Power supply voltage			2.7		4.3	V
I_{CC}	Positive supply current	V_{CC} = 4.3 V, V_{IN} = V_{CC} or GND, $V_{I/O}$ = 0 V	Switch ON or OFF		40	70	µA
$I_{CC, VBUS}$	Positive supply current (V_{BUS} mode)	V_{CC} = 0 V, V_{BUS} = 5.5 V, V_{IN} = V_{CC} or GND, $V_{I/O}$ = 0 V	Switch ON or OFF			50	µA

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6.7 Typical Characteristics

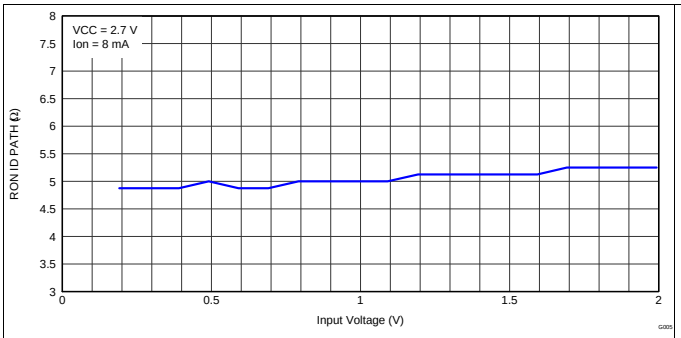


Figure 1. ON-Resistance vs VI for MHL Switch

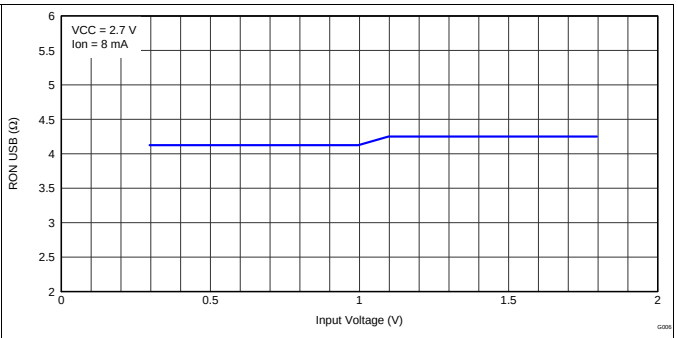


Figure 2. ON-Resistance vs VI for USB Switch

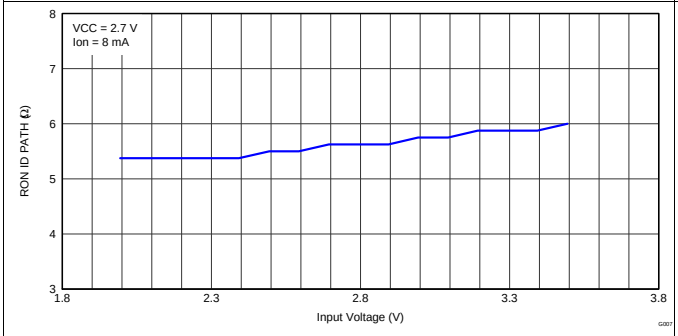


Figure 3. ON-Resistance vs VI for ID Switch

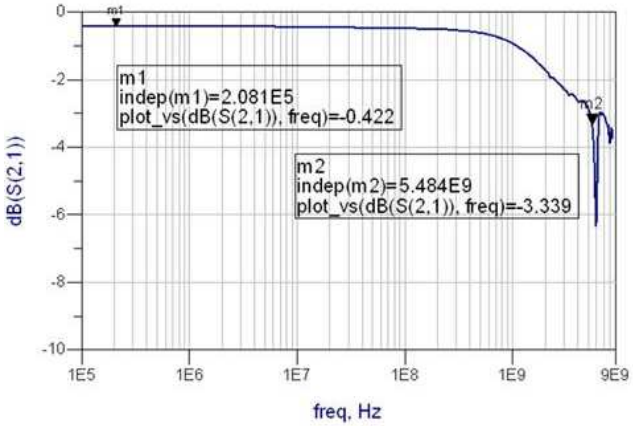


Figure 4. Gain vs Frequency for MHL Switch

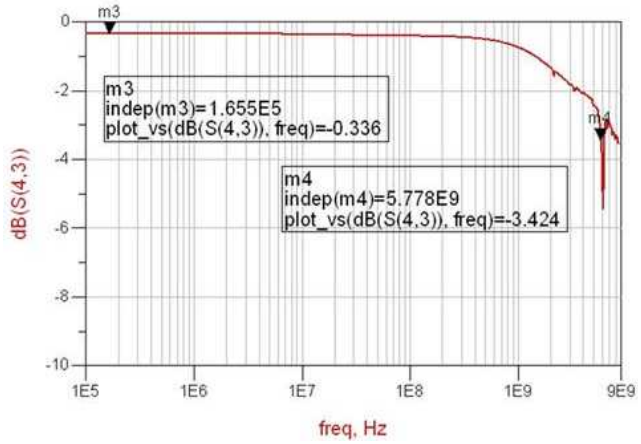


Figure 5. Gain vs Frequency for USB Switch

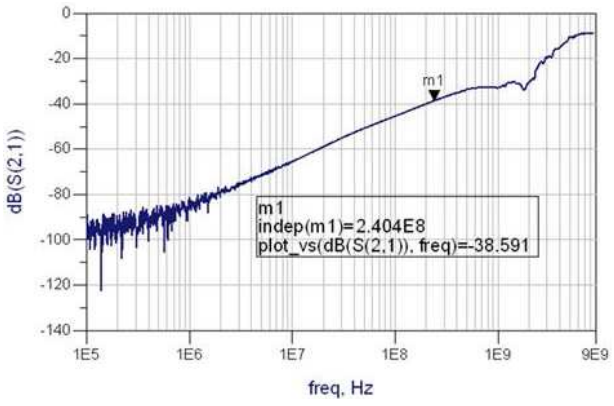


Figure 6. Off Isolation vs Frequency for MHL Path

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Typical Characteristics (continued)

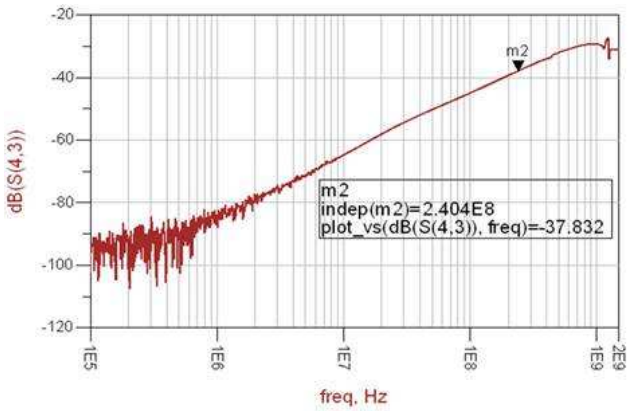


Figure 7. Off Isolation vs Frequency for USB Path

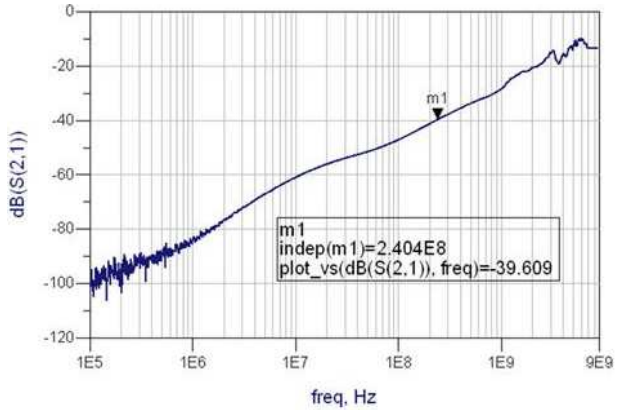


Figure 8. Crosstalk vs Frequency for MHL Path

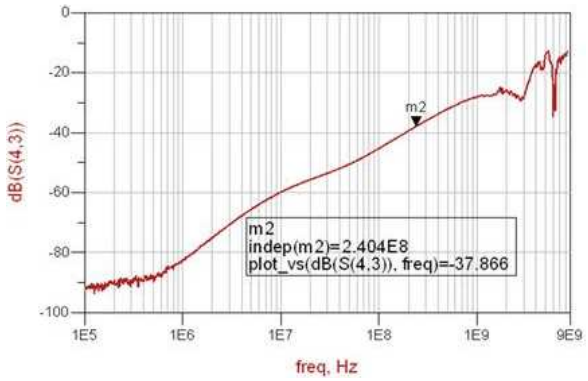


Figure 9. Crosstalk vs Frequency for USB Path

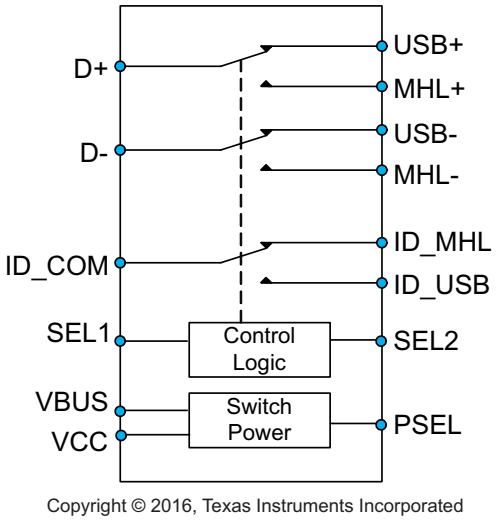
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7 Detailed Description

7.1 Overview

The TS3USB3200 supports high-speed Mobile High-Definition Link (MHL) or Mobility Display Port (MyDP) switching, as well as USB 2.0 High-Speed (480 Mbps) switching in the same package. An additional integrated ID switch is also included to support USB/MHL or MyDP ID for easy information control. These configurations allow the system designer to use a common USB or Mico-USB connector to support both MHL/MyDP video signals and USB data.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Flexible Power Control

Device can be powered by V_{BUS} or by V_{CC}. This allows the device to run off a 4.3-V battery voltage or 5 V from an external USB device. If both a battery and external USB device are supplying voltage on the V_{CC} and V_{BUS} pins the PSEL can be used to select which power supply is used to save battery power.

7.3.2 I_{OFF} Protection Prevents Current Leakage in Powered Down State (V_{CC} and V_{BUS}= 0 V)

When there is no power supplied to the IC, all of the I/O signal paths are placed in a high impedance state, which isolates the data paths when they are not being used.

7.3.3 1.8-V Compatible Control Inputs (SEL1, SEL2, and PSEL)

The TS3USB3200 logic control input pins can operate with 1.8-V logic since the V_{IH} minimum for the SEL1, SEL2, and PSEL is 1.3 V.

7.4 Device Functional Modes

The TS3USB32000 device can select which power supply pin V_{CC} or V_{BUS} will power the device when voltages are present on both pins.

Table 1. Function Table (Power Source)

V_{CC}	V_{BUS}	PSEL (1)	POWER SOURCE
L	L	X	No Power. All I/O in High-Z
L	H	X	V_{BUS}
H	L	X	V_{CC}
H	H	L	V_{CC}
H	H	H	V_{BUS}

(1) The PSEL pin has 6-MΩ weak pulldown resistor to GND to make its default value to be LOW.

Table 2. Function Table (Signal and ID Select)

SEL1 (1)	SEL2 (1)	CONNECTION	High-Z
L	L	D+/D– to USB+/USB–, ID_COM to ID_USB	MHL+/MHL–, ID_MHL
L	H	D+/D– to USB+/USB–, ID_COM to ID_MHL	MHL+/MHL–, ID_USB
H	L	D+/D– to MHL+/MHL–, ID_COM to ID_USB	USB+/USB–, ID_MHL
H	H	D+/D– to MHL+/MHL–, ID_COM to ID_MHL	USB+/USB–, ID_USB

(1) The SEL1 and SEL2 pins have 6-MΩ weak pulldown resistor to GND to make their default value to be LOW.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

For Mobility Display Port Applications (MyDP) the signal voltage must be biased to ensure that the signal never exceeds the *Recommended Operating Conditions* for the TS3USB3200. Namely the $V_{I/O}$ must never operate outside the range of 0 V to 3.6 V.

The control pins (SEL1 and SEL2) have built-in 6-MΩ pulldown resistors to ensure the USB paths are enabled for TS3USB3200 and allow connectivity to the TSU5611 USB accessory switch.

8.2 Typical Applications

8.2.1 TS3USB3200 Configured to be Powered by VBUS Through the MicroUSB Connector

During manufacturing test when battery power is not available, the TS3USB3200 can be configured, as shown in Figure 10, to be powered by VBUS through the microUSB connector.

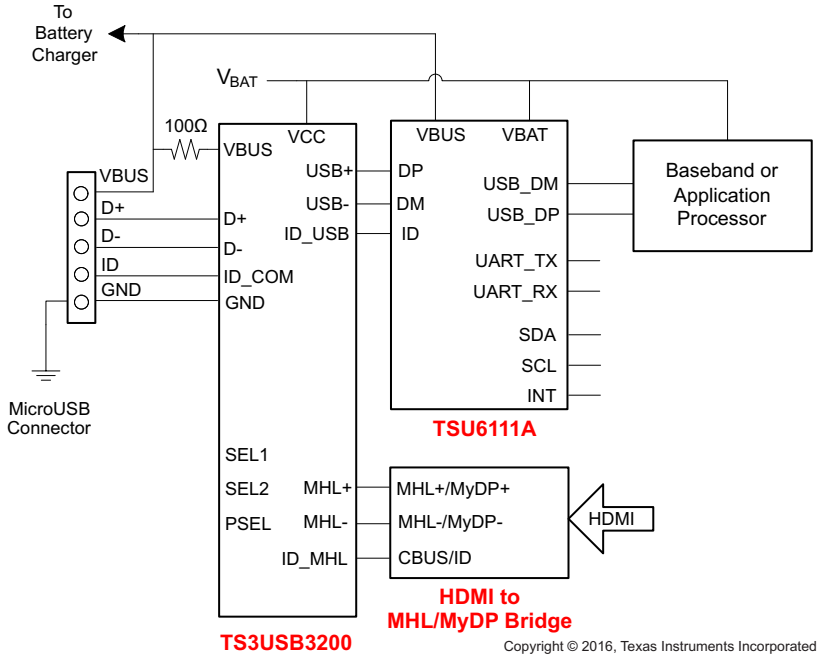


Figure 10. Typical Application Schematic Powered by VBUS

8.2.1.1 Design Requirements

Design requirements of the MHL and USB 1.0,1.1, and 2.0 standards must be followed. The TS3USB3200 has internal 6-MΩ pulldown resistors on SEL and $\overline{OE}$, so no external resistors are required on the logic pins. The internal pulldown resistor on SEL ensures the USB channel is selected by default. The internal pulldown resistor on $\overline{OE}$ enables the switch when power is applied to VCC.

Typical Applications (continued)

8.2.1.2 Detailed Design Procedure

The TS3USB3200 can be properly operated without any external components. However, TI recommends that unused pins must be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device.

8.2.1.3 Application Curves

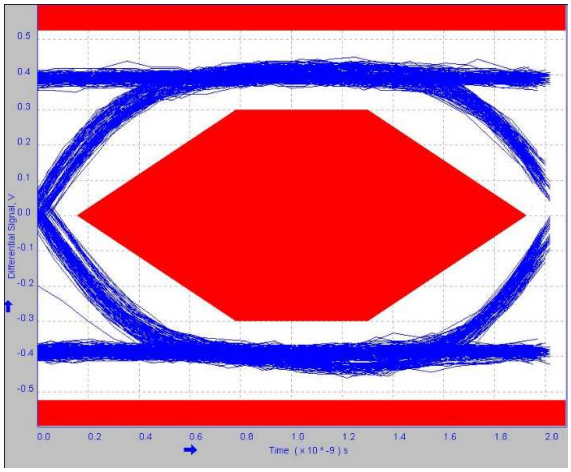


Figure 11. 480-Mbps USB 2.0 Eye Pattern With No Device

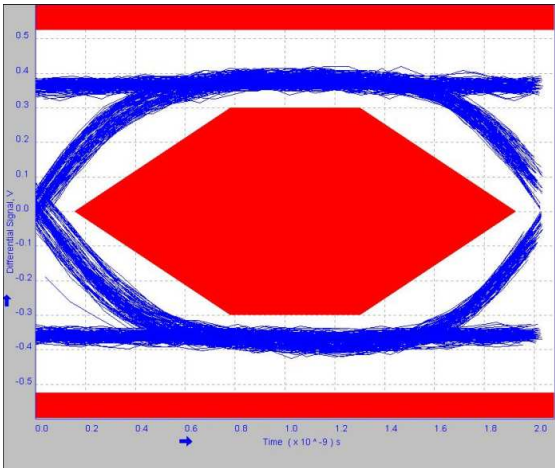


Figure 12. 480-Mbps USB 2.0 Eye Pattern for USB Switch

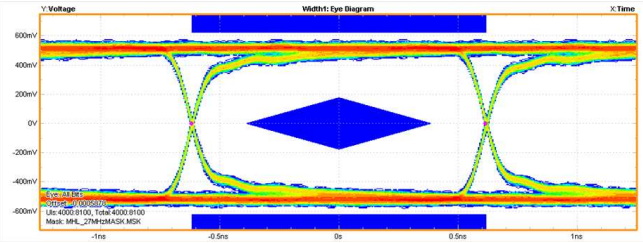


Figure 13. Eye Pattern: 0.7-Gbps MHL Eye Pattern for With No Device

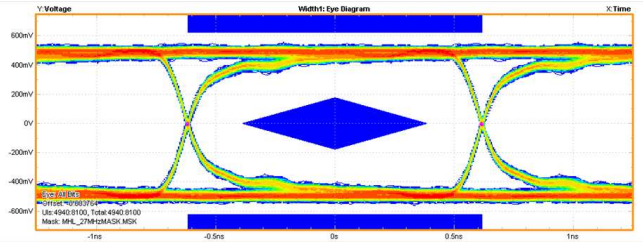


Figure 14. Eye Pattern: 0.7-Gbps MHL Eye Pattern for MHL Switch

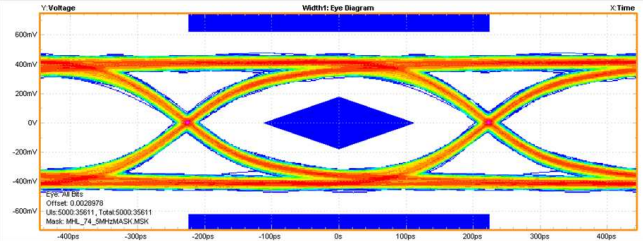


Figure 15. Eye Pattern: 2.2-Gbps MHL Eye Pattern for With No Device

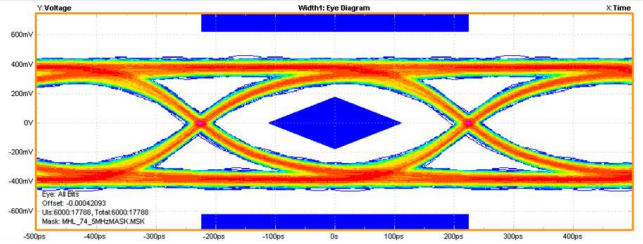


Figure 16. Eye Pattern: 2.2-Gbps MHL Eye Pattern for MHL Switch

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Typical Applications (continued)

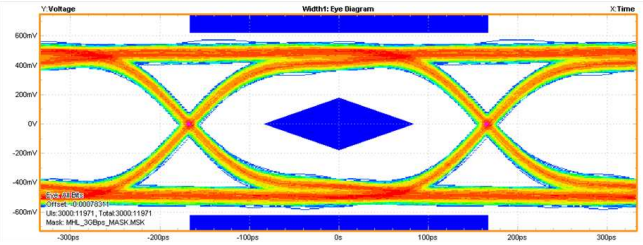


Figure 17. Eye Pattern: 3-Gbps MHL Eye Pattern for With No Device

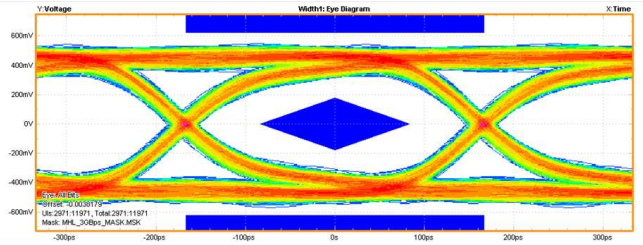


Figure 18. Eye Pattern: 3-Gbps MHL Eye Pattern for MHL Switch

8.2.2 TS3USB3200 Powered by Mobile Device's Standalone Battery

The TS3USB3200 can also be powered by the mobile device's standalone battery. Figure 19 shows a typical implementation. The VBUS pin of the TS3USB3200 can simply be grounded under such conditions.

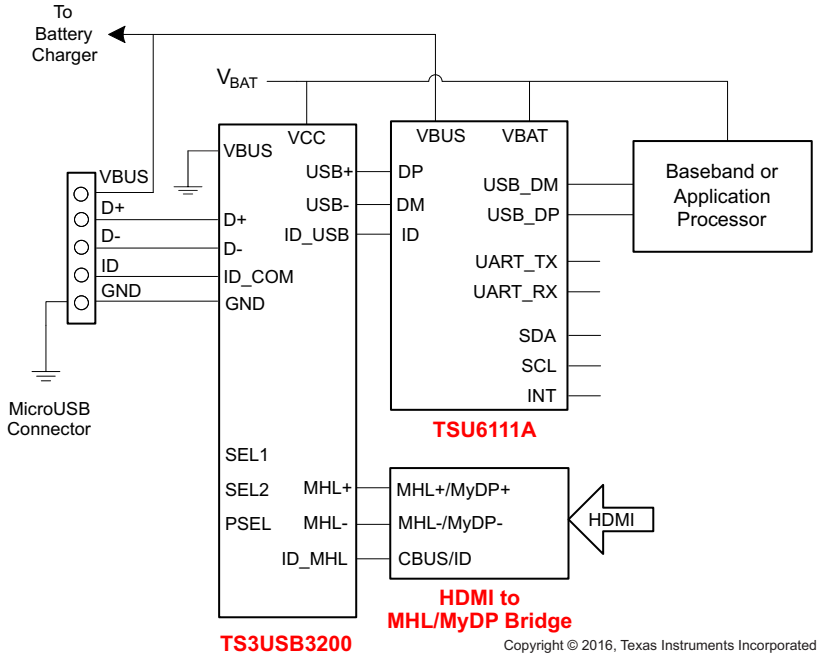


Figure 19. Typical Application Schematic Powered by Mobile Devices

8.2.2.1 Design Requirements

The TS3USB3200 can be properly operated without any external components. However, TI recommends that unused pins must be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device.

8.2.2.2 Detailed Design Procedure

The VBUS pin of the TS3USB3200 can simply be grounded under such conditions.

9 Power Supply Recommendations

Power to the device is supplied through the VCC pin and must follow the USB 1.0, 1.1, and 2.0 standards. TI recommends placing a bypass capacitor as close to the supply pin VCC as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

10 Layout

10.1 Layout Guidelines

Place supply bypass capacitors as close to VCC pin as possible and avoid placing the bypass capacitors near the D+/D– traces.

The high-speed D+/D- must match and be no more than 4 inches long; otherwise, the eye diagram performance may be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In layout, the impedance of D+ and D– traces must match the cable characteristic differential impedance for optimal performance.

Route the high-speed USB signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices, or ICs that use or duplicate clock signals.

Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub must be less than 200 mm.

Route all high-speed USB signal traces over continuous GND planes, with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

Due to high frequencies associated with the USB, a printed-circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 20.

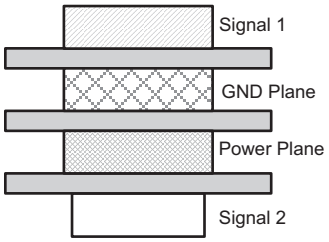


Figure 20. Four-Layer Board Stack-Up

The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

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10.2 Layout Example

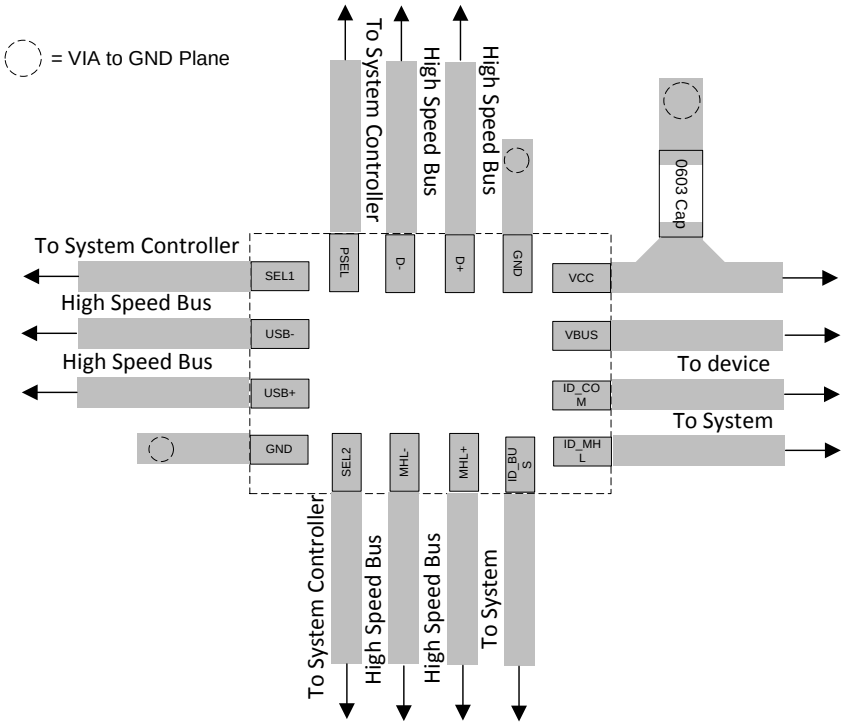


Figure 21. TS3USB3200 Layout Example

11 器件和文档支持

11.1 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

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11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS3USB32008RSVR	Active	Production	UQFN (RSV) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZTV
TS3USB32008RSVR.B	Active	Production	UQFN (RSV) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZTV
TS3USB3200RSVR	Active	Production	UQFN (RSV) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZTO
TS3USB3200RSVR.B	Active	Production	UQFN (RSV) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZTO

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

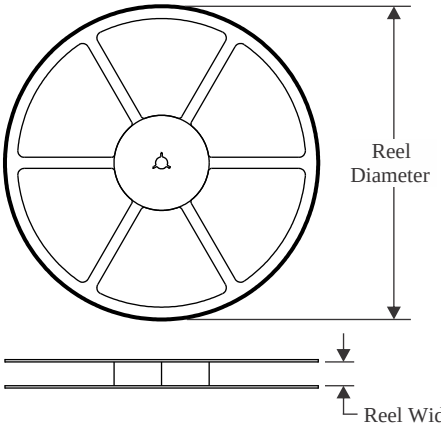
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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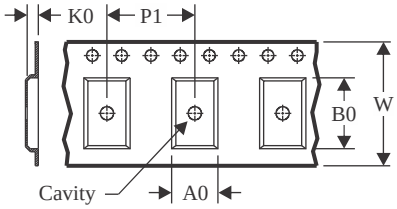
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

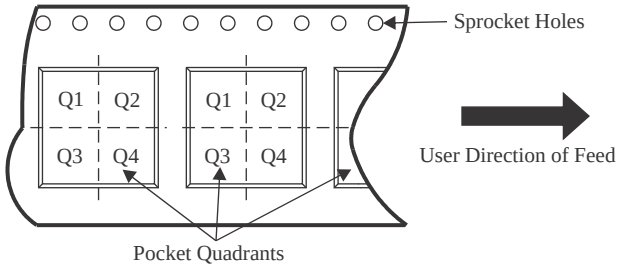


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

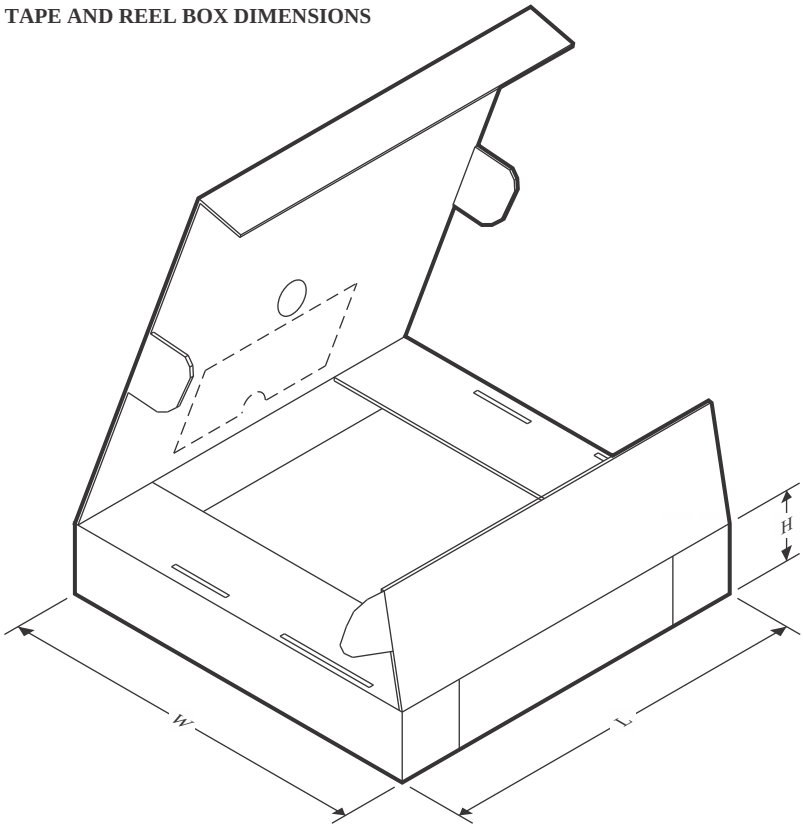
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3USB32008RSVR	UQFN	RSV	16	3000	180.0	9.5	2.1	2.9	0.75	4.0	8.0	Q1
TS3USB3200RSVR	UQFN	RSV	16	3000	180.0	12.4	2.1	2.9	0.75	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3USB32008RSVR	UQFN	RSV	16	3000	184.0	184.0	19.0
TS3USB3200RSVR	UQFN	RSV	16	3000	200.0	183.0	25.0

GENERIC PACKAGE VIEW

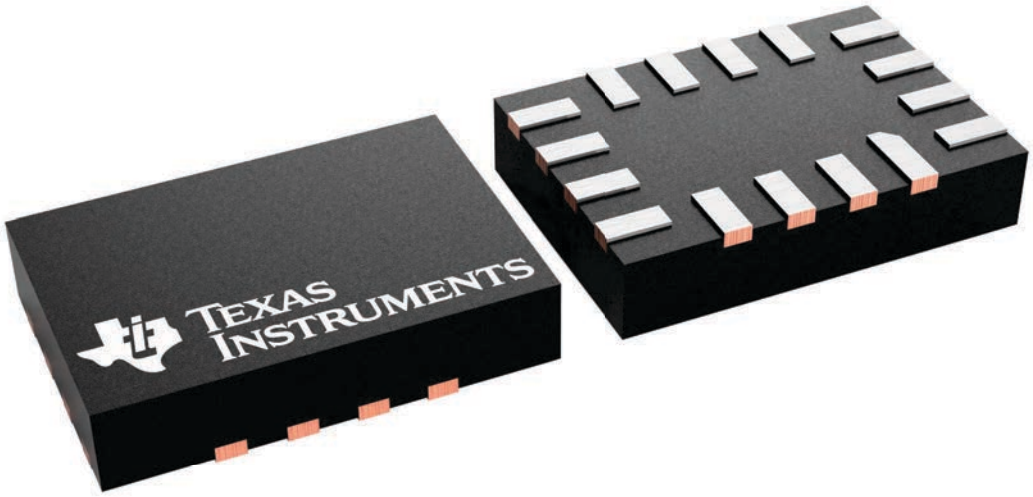
RSV 16

UQFN - 0.55 mm max height

1.8 x 2.6, 0.4 mm pitch

ULTRA THIN QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



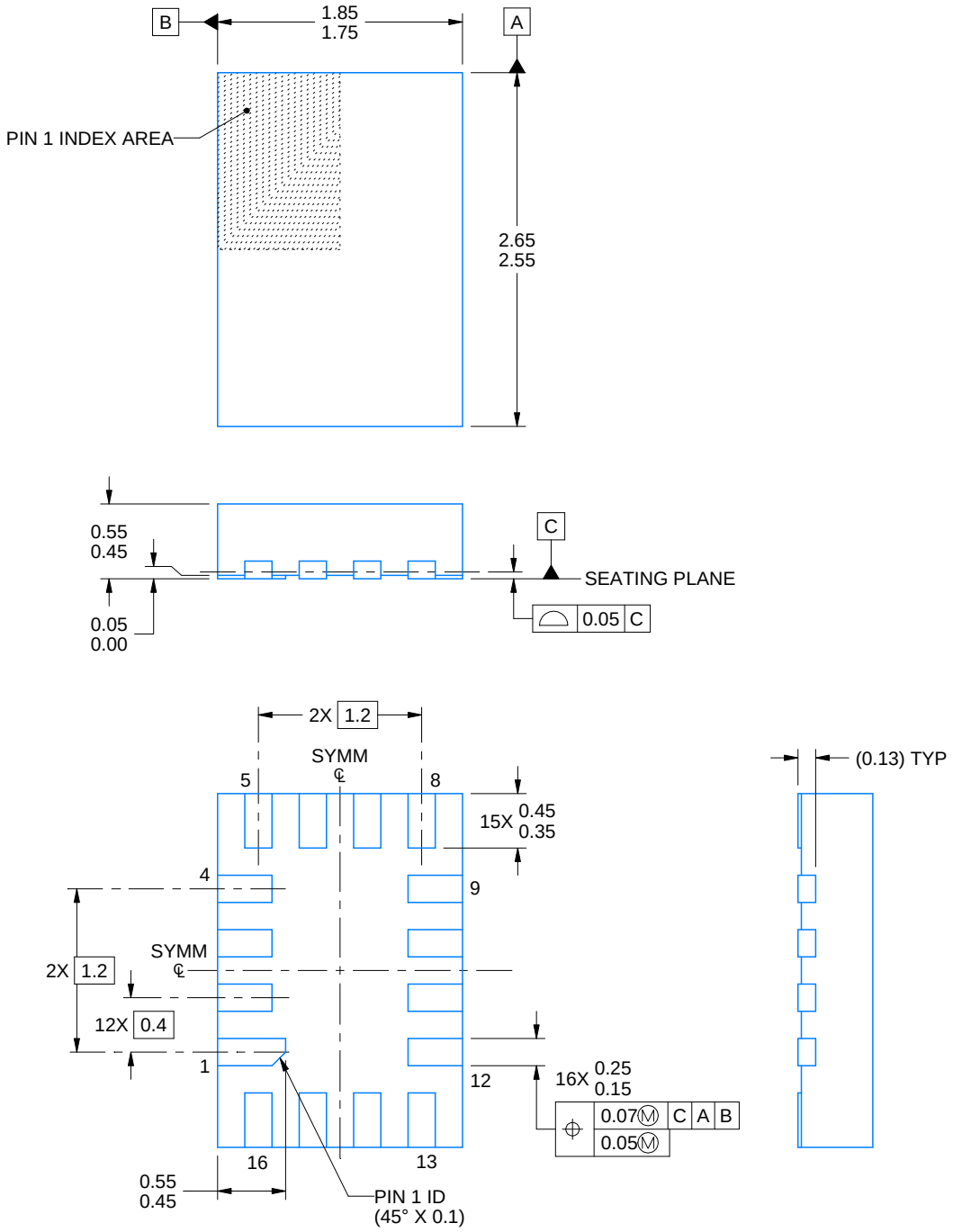
4231225/A

RSV0016A

PACKAGE OUTLINE

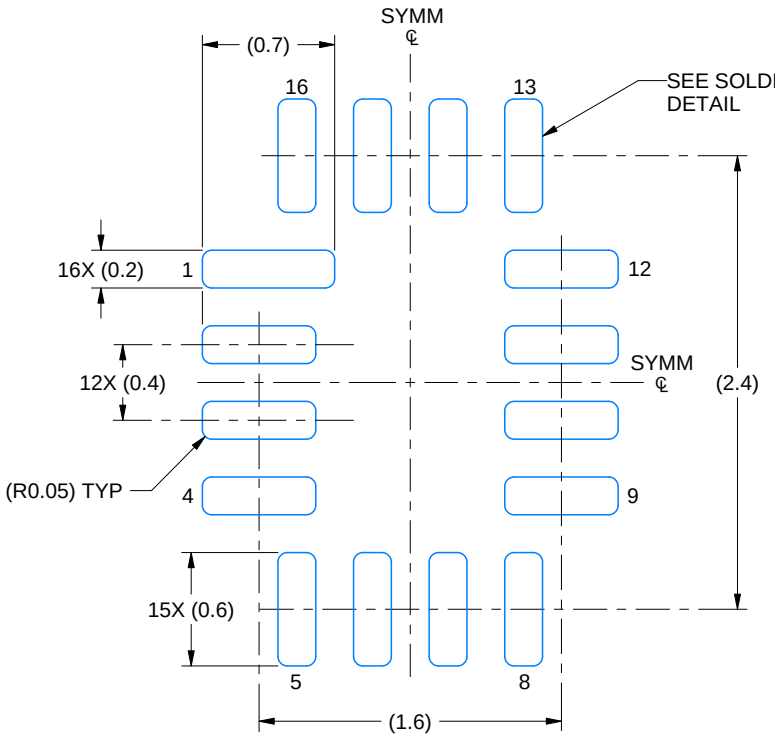
UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD

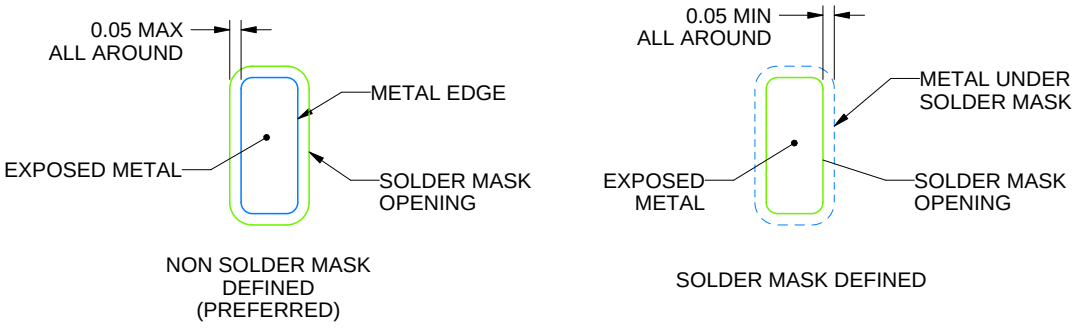


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

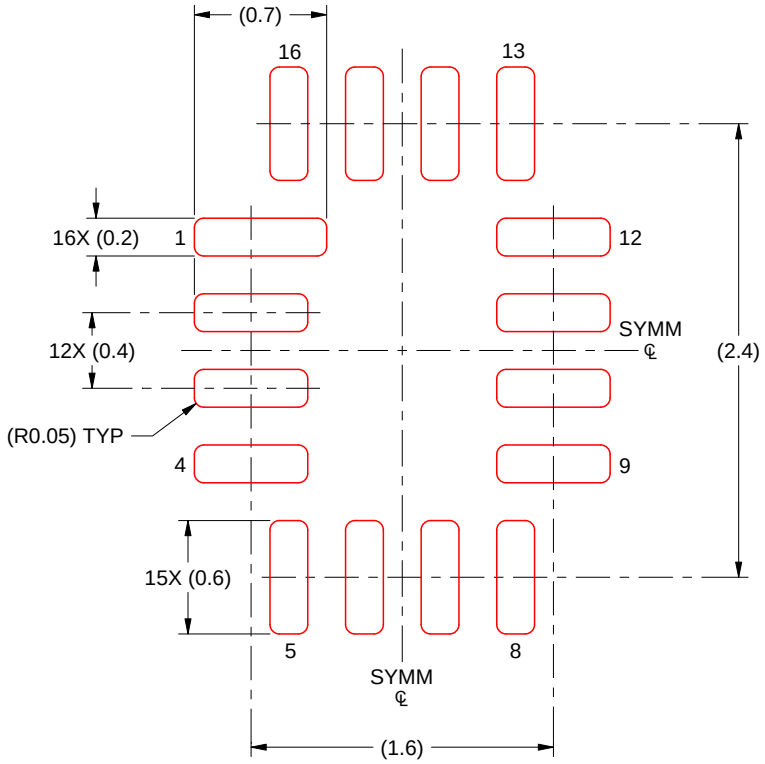


SOLDER MASK DETAILS

4220314/C 02/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

4220314/C 02/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月