SBAS417B − JUNE 2007 − REVISED JANUARY 2008

# Low Voltage I/O TOUCH SCREEN CONTROLLER

## FEATURES

- **Same Pinout as ADS7846**
- **2.2V to 5.25V Operation**
- **1.5V to 5.25V Digital I/O**
- **Internal 2.5V Reference**
- **Direct Battery Measurement (0V to 6V)**
- **On-Chip Temperature Measurement**
- **Touch-Pressure Measurement**
- **QSPI™ and SPI™ 3-Wire Interface**
- **Auto Power-Down**
- **Exceeds IEC 61000-4-2 ESD Requirements**
  - **±15kV Contact Discharge**
  - **No External Components Needed**
- **Available In TSSOP-16, QFN-16, and VFBGA-48 Packages**

## APPLICATIONS

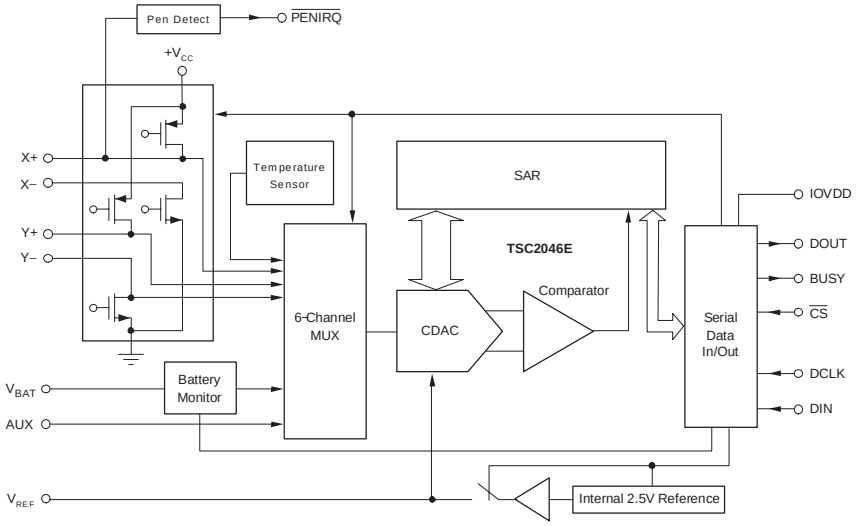
- **Personal Digital Assistants**
- **Portable Instruments**
- **Point-of-Sale Terminals**
- **Pagers**
- **Touch Screen Monitors**
- **Cellular Phones**

US Patent No. 6246394

## DESCRIPTION

The TSC2046E is the next-generation version of the ADS7846 4-wire touch screen controller, supporting a low-voltage I/O interface from 1.5V to 5.25V. The TSC2046E is 100% pin-compatible with the existing ADS7846, and drops into the same socket. This design allows for an easy upgrade of current applications to the new version. The TSC2046E also has an on-chip 2.5V reference that can be used for the auxiliary input, battery monitor, and temperature measurement modes. The reference can also be powered down when not used to conserve power. The internal reference operates down to a supply voltage of 2.7V, while monitoring the battery voltage from 0V to 6V.

The low-power consumption of < 0.75mW typ at 2.7V (reference off), high-speed (up to 125kHz sample rate), and on-chip drivers make the TSC2046E an ideal choice for battery-operated systems such as personal digital assistants (PDAs) with resistive touch screens, pagers, cellular phones, and other portable equipment. The TSC2046E is available in TSSOP-16, QFN-16, and VFBGA-48 packages and is specified over the –40°C to +85°C temperature range.




Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SPI and QSPI are trademarks of Motorola Inc.
Microwire is a trademark of National Semiconductor Corporation.
All other trademarks are the property of their respective owners.

**PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.**



Copyright © 2007−2008, Texas Instruments Incorporated

## ABSOLUTE MAXIMUM RATINGS(1)

| | |
|---|---|
| $+V_{CC}$ and IOVDD to GND | −0.3V to +6V |
| Analog Inputs to GND | −0.3V to $+V_{CC}$ + 0.3V |
| Digital Inputs to GND | −0.3V to IOVDD + 0.3V |
| Power Dissipation | 250mW |
| Maximum Junction Temperature | +150°C |
| Operating Temperature Range | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| IEC Contact Discharge (X+, X−, Y+, Y−)(2) | ±15kV |

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Test method based on IEC standard 61000−4−2. Contact Texas Instruments for test details.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION(1)

| PRODUCT | NOMINAL PENIRQ PULLUP RESISTOR VALUES | MAXIMUM INTEGRAL LINEARITY ERROR (LSB) | PACKAGE-LEAD | PACKAGE DESIGNATOR | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|---|---|---|---|---|---|---|---|---|
| TSC2046E | 50kΩ | ±2 | TSSOP-16 | PW | −40°C to +85°C | TSC2046EI | TSC2046EIPW | Rails, 100 |
| | | | | | | | TSC2046EIPWR | Tape and Reel, 2500 |
| | | | 4x4, 0.8mm Thin QFN-16 | RGV | −40°C to +85°C | TSC2046E | TSC2046EIRGVT | Tape and Reel, 250 |
| | | | | | | | TSC2046EIRGVR | Tape and Reel, 2500 |
| | | | 4x4 VFBGA-48 | ZQC | −40°C to +85°C | BC2046E | TSC2046EIZQCR | Tape and Reel, 2500 |

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or see the TI web site at www.ti.com.

## ELECTRICAL CHARACTERISTICS: $V_S$ = +2.7V to +5.5V

At $T_A$ = −40°C to +85°C, $+V_{CC}$ = +2.7V, $V_{REF}$ = 2.5V internal voltage, $f_{SAMPLE}$ = 125kHz, $f_{CLK}$ = 16 • $f_{SAMPLE}$ = 2MHz, 12-bit mode, digital inputs = GND or IOVDD, and $+V_{CC}$ must be ≥ IOVDD, unless otherwise noted.

| PARAMETER | CONDITION | TSC2046E | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **ANALOG INPUT** | | | | | |
| Full-Scale Input Span | Positive Input−Negative Input | 0 | | $V_{REF}$ | V |
| Absolute Input Range | Positive Input | −0.2 | | $+V_{CC}$ + 0.2 | V |
| | Negative Input | −0.2 | | +0.2 | V |
| Capacitance | | | 25 | | pF |
| Leakage Current | | | 0.1 | | µA |
| **SYSTEM PERFORMANCE** | | | | | |
| Resolution | | | 12 | | Bits |
| No Missing Codes | | 11 | | | Bits |
| Integral Linearity Error | | | | ±2 | LSB(1) |
| Offset Error | | | | ±6 | LSB |
| Gain Error | External $V_{REF}$ | | | ±4 | LSB |
| Noise | Including Internal $V_{REF}$ | | 70 | | µVrms |
| Power-Supply Rejection | | | 70 | | dB |
| **SAMPLING DYNAMICS** | | | | | |
| Conversion Time | | | | 12 | CLK Cycles |
| Acquisition Time | | 3 | | | CLK Cycles |
| Throughput Rate | | | | 125 | kHz |
| Multiplexer Settling Time | | | 500 | | ns |
| Aperture Delay | | | 30 | | ns |
| Aperture Jitter | | | 100 | | ps |
| Channel-to-Channel Isolation | $V_{IN}$ = 2.5$V_{PP}$ at 50kHz | | 100 | | dB |
| **SWITCH DRIVERS** | | | | | |
| On-Resistance | | | | | |
| Y+, X+ | | | 5 | | Ω |
| Y−, X− | | | 6 | | Ω |
| Drive Current(2) | Duration 100ms | | | 50 | mA |
| **REFERENCE OUTPUT** | | | | | |
| Internal Reference Voltage | | 2.45 | 2.50 | 2.55 | V |
| Internal Reference Drift | | | 15 | | ppm/°C |
| Quiescent Current | | | 500 | | µA |
| **REFERENCE INPUT** | | | | | |
| Range | | 1.0 | | $+V_{CC}$ | V |
| Input Impedance | SER/$\overline{DFR}$ = 0, PD1 = 0 | | 1 | | GΩ |
| | Internal Reference Off | | | | |
| | Internal Reference On | | 250 | | Ω |
| **BATTERY MONITOR** | | | | | |
| Input Voltage Range | | 0.5 | | 6.0 | V |
| Input Impedance | | | | | |
| Sampling Battery | | | 10 | | kΩ |
| Battery Monitor Off | | | 1 | | GΩ |
| Accuracy | $V_{BAT}$ = 0.5V to 5.5V, External $V_{REF}$ = 2.5V | −2 | | +2 | % |
| | $V_{BAT}$ = 0.5V to 5.5V, Internal Reference | −3 | | +3 | % |
| **TEMPERATURE MEASUREMENT** | | | | | |
| Temperature Range | | −40 | | +85 | °C |
| Resolution | Differential Method(3) | | 1.6 | | °C |
| | TEMP0(4) | | 0.3 | | °C |
| Accuracy | Differential Method(3) | | ±2 | | °C |
| | TEMP0(4) | | ±3 | | °C |

(1) LSB means *Least Significant Bit*. With $V_{REF}$ = +2.5V, 1 LSB is 610µV.
(2) Assured by design, but not tested. Exceeding 50mA source current may result in device degradation.
(3) Difference between TEMP0 and TEMP1 measurement, no calibration necessary.
(4) Temperature drift is −2.1mV/°C.
(5) TSC2046E operates down to 2.2V.
(6) IOVDD must be ≤ ($+V_{CC}$).
(7) Combined supply current from $+V_{CC}$ and IOVDD. Typical values obtained from conversions on AUX input with PD0 = 0.

## ELECTRICAL CHARACTERISTICS: $V_S$ = +2.7V to +5.5V (continued)

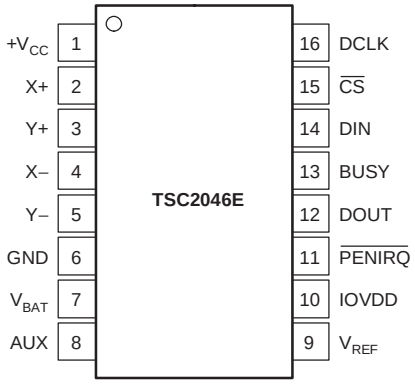
At $T_A$ = −40°C to +85°C, $+V_{CC}$ = +2.7V, $V_{REF}$ = 2.5V internal voltage, $f_{SAMPLE}$ = 125kHz, $f_{CLK}$ = 16 • $f_{SAMPLE}$ = 2MHz, 12-bit mode, digital inputs = GND or IOVDD, and $+V_{CC}$ must be ≥ IOVDD, unless otherwise noted.

| PARAMETER | CONDITION | TSC2046E | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **DIGITAL INPUT/OUTPUT** | | | | | |
| Logic Family | | | CMOS | | |
| Capacitance | All Digital Control Input Pins | | 5 | 15 | pF |
| $V_{IH}$ | $\lvert I_{IH} \rvert \le +5\mu A$ | IOVDD • 0.7 | | IOVDD + 0.3 | V |
| $V_{IL}$ | $\lvert I_{IL} \rvert \le +5\mu A$ | −0.3 | | 0.3 • IOVDD | V |
| $V_{OH}$ | $I_{OH}$ = −250µA | IOVDD • 0.8 | | | V |
| $V_{OL}$ | $I_{OL}$ = 250µA | | | 0.4 | V |
| Data Format | | | Straight Binary | | |
| **POWER-SUPPLY REQUIREMENTS** | | | | | |
| $+V_{CC}$(5) | Specified Performance | 2.7 | | 3.6 | V |
| | Operating Range | 2.2 | | 5.25 | V |
| IOVDD(6) | | 1.5 | | $+V_{CC}$ | V |
| Quiescent Current(7) | Internal Reference Off | | 280 | 650 | µA |
| | Internal Reference On | | 780 | | µA |
| | $f_{SAMPLE}$ = 12.5kHz | | 220 | | µA |
| | Power-Down Mode with $\overline{CS}$ = DCLK = DIN = IOVDD | | | 3 | µA |
| Power Dissipation | $+V_{CC}$ = +2.7V | | | 1.8 | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specified Performance | | −40 | | +85 | °C |

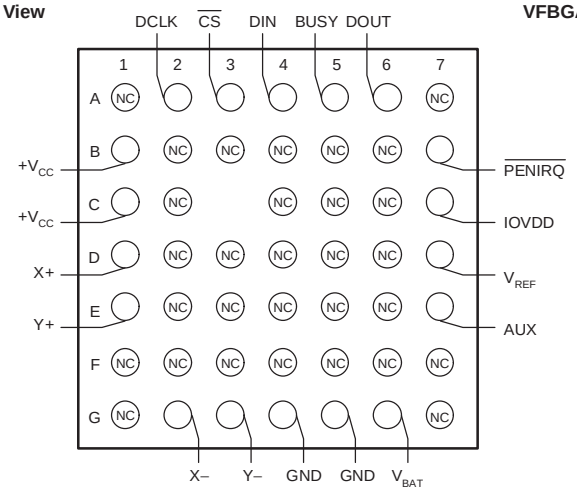
(1) LSB means *Least Significant Bit*. With $V_{REF}$ = +2.5V, 1 LSB is 610µV.
(2) Assured by design, but not tested. Exceeding 50mA source current may result in device degradation.
(3) Difference between TEMP0 and TEMP1 measurement, no calibration necessary.
(4) Temperature drift is −2.1mV/°C.
(5) TSC2046E operates down to 2.2V.
(6) IOVDD must be ≤ ($+V_{CC}$).
(7) Combined supply current from $+V_{CC}$ and IOVDD. Typical values obtained from conversions on AUX input with PD0 = 0.

## PIN CONFIGURATION

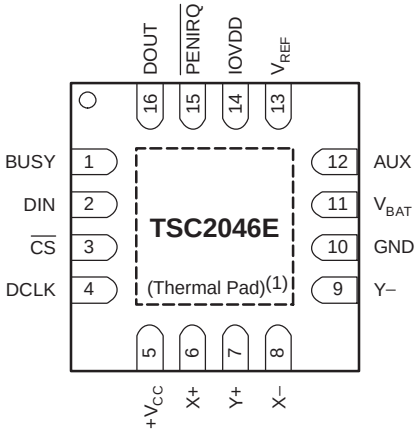
**Top View** **TSSOP**




**Top View** **VFBGA**




**Top View** **QFN**



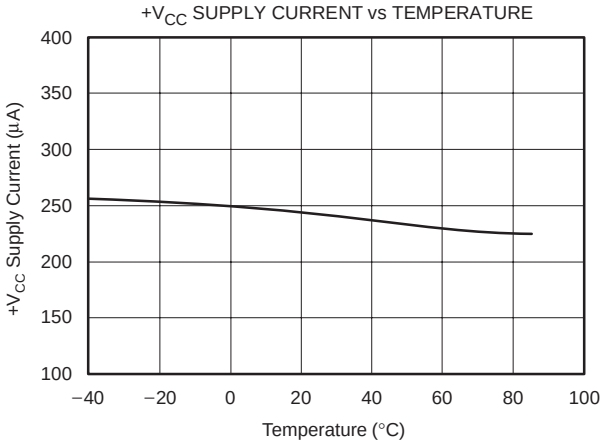

(1) The thermal pad is internally connected to the substrate. This pad can be connected to the analog ground or left floating. Keep the thermal pad separate from the digital ground, if possible.

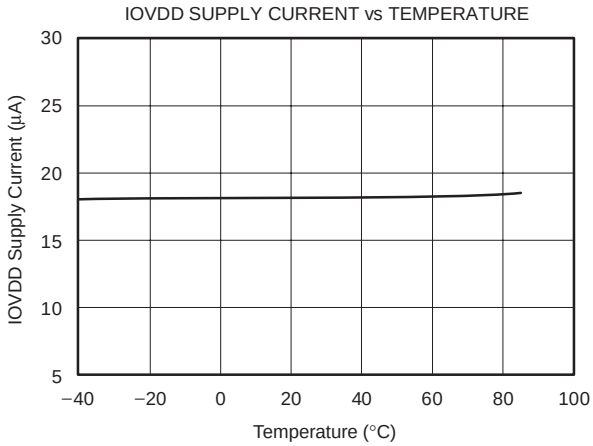
## PIN DESCRIPTION

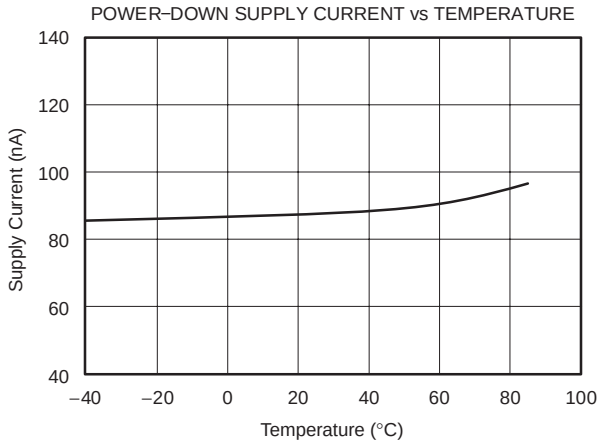
| TSSOP PIN # | VFBGA PIN # | QFN PIN # | NAME | DESCRIPTION |
|---|---|---|---|---|
| 1 | B1 and C1 | 5 | $+V_{CC}$ | Power Supply |
| 2 | D1 | 6 | X+ | X+ Position Input |
| 3 | E1 | 7 | Y+ | Y+ Position Input |
| 4 | G2 | 8 | X− | X− Position Input |
| 5 | G3 | 9 | Y− | Y− Position Input |
| 6 | G4 and G5 | 10 | GND | Ground |
| 7 | G6 | 11 | $V_{BAT}$ | Battery Monitor Input |
| 8 | E7 | 12 | AUX | Auxiliary Input to ADC |
| 9 | D7 | 13 | $V_{REF}$ | Voltage Reference Input/Output |
| 10 | C7 | 14 | IOVDD | Digital I/O Power Supply |
| 11 | B7 | 15 | $\overline{\text{PENIRQ}}$ | Pen Interrupt |
| 12 | A6 | 16 | DOUT | Serial Data Output. Data are shifted on the falling edge of DCLK. This output is high impedance when $\overline{\text{CS}}$ is high. |
| 13 | A5 | 1 | BUSY | Busy Output. This output is high impedance when $\overline{\text{CS}}$ is high. |
| 14 | A4 | 2 | DIN | Serial Data Input. If $\overline{\text{CS}}$ is low, data sre latched on the rising edge of DCLK. |
| 15 | A3 | 3 | $\overline{\text{CS}}$ | Chip Select Input. Controls conversion timing and enables the serial input/output register. $\overline{\text{CS}}$ high = power-down mode (ADC only). |
| 16 | A2 | 4 | DCLK | External Clock Input. This clock runs the SAR conversion process and synchronizes serial data I/O. |

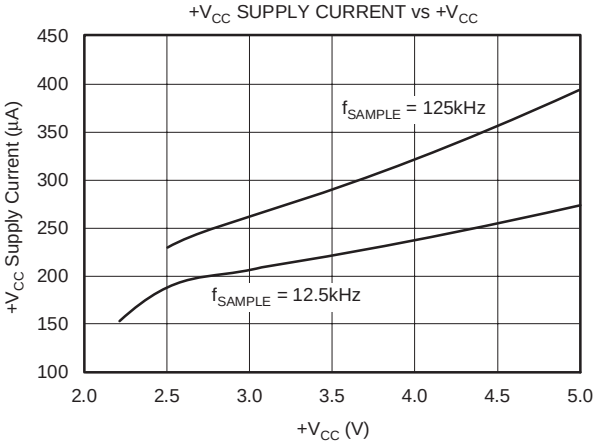
## TYPICAL CHARACTERISTICS

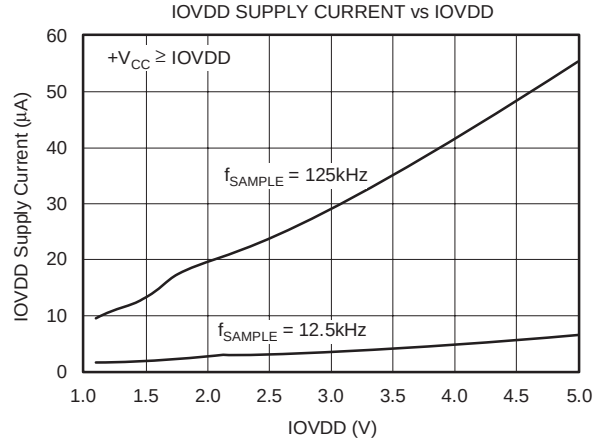
At $T_A$ = +25°C, $+V_{CC}$ = +2.7V, IOVDD = +1.8V, $V_{REF}$ = External +2.5V, 12-bit mode, PD0 = 0, $f_{SAMPLE}$ = 125kHz, and $f_{CLK}$ = 16 • $f_{SAMPLE}$ = 2MHz, unless otherwise noted.

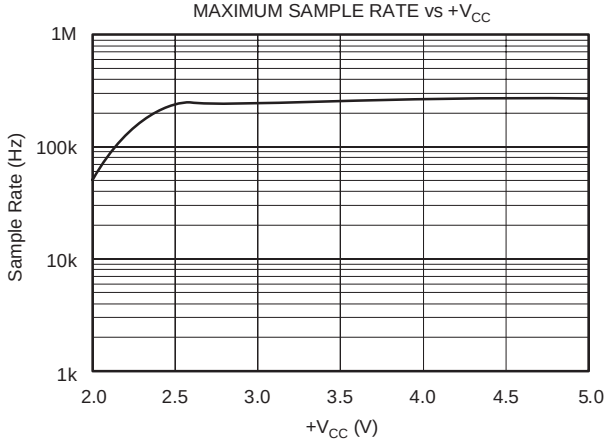


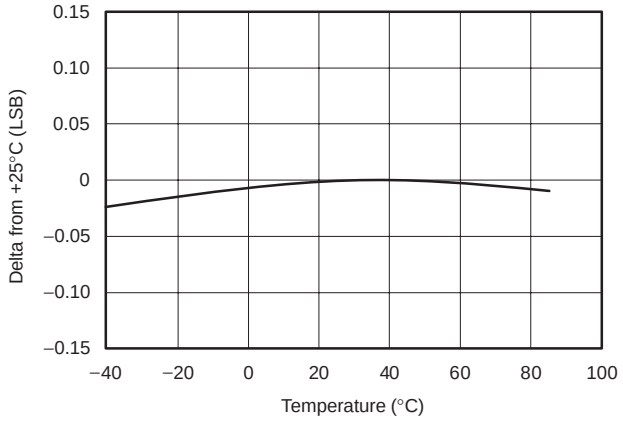



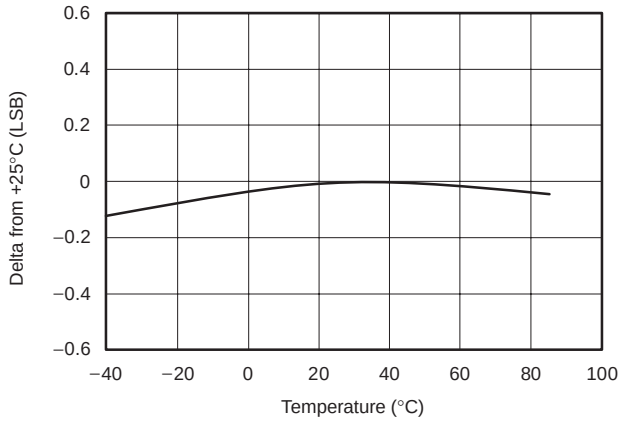
## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C, $+V_{CC}$ = +2.7V, IOVDD = +1.8V, $V_{REF}$ = External +2.5V, 12-bit mode, PD0 = 0, $f_{SAMPLE}$ = 125kHz, and $f_{CLK}$ = 16 • $f_{SAMPLE}$ = 2MHz, unless otherwise noted.

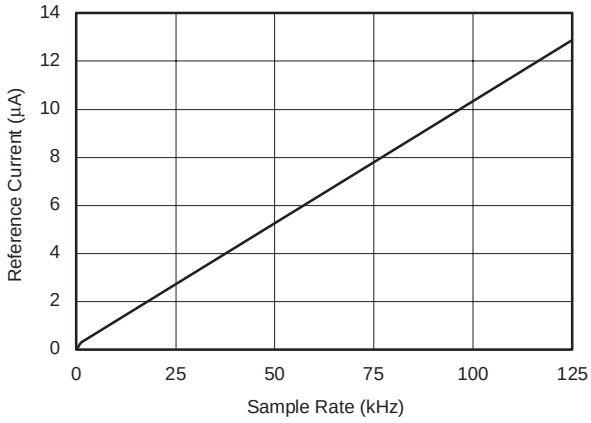
CHANGE IN GAIN vs TEMPERATURE



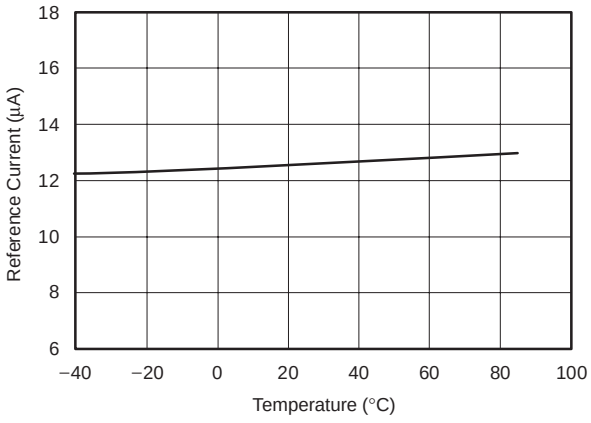

CHANGE IN OFFSET vs TEMPERATURE



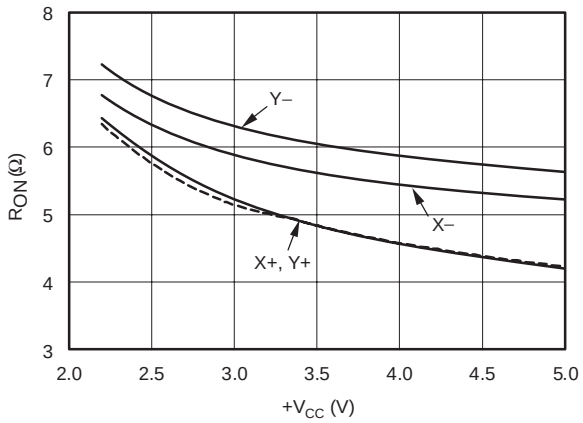

REFERENCE CURRENT vs SAMPLE RATE



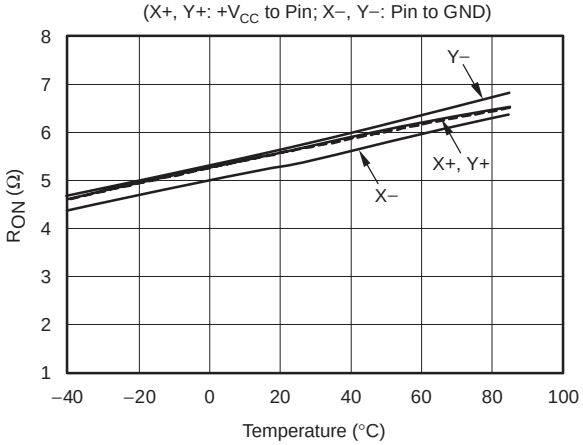

REFERENCE CURRENT vs TEMPERATURE




SWITCH ON− RESISTANCE vs $+V_{CC}$
($X+$, $Y+$: $+V_{CC}$ to Pin; $X-$, $Y-$: Pin to GND)



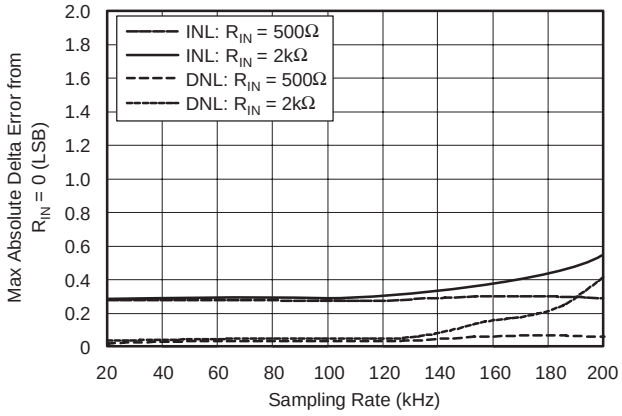

SWITCH ON−RESISTANCE vs TEMPERATURE
($X+$, $Y+$: $+V_{CC}$ to Pin; $X-$, $Y-$: Pin to GND)



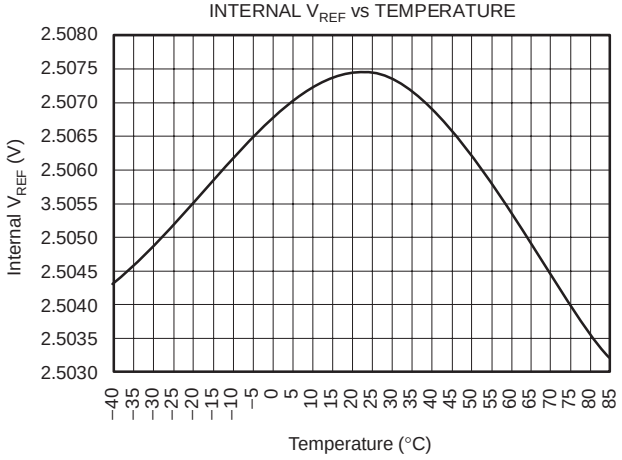
## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C, $+V_{CC}$ = +2.7V, IOVDD = +1.8V, $V_{REF}$ = External +2.5V, 12-bit mode, PD0 = 0, $f_{SAMPLE}$ = 125kHz, and $f_{CLK}$ = 16 • $f_{SAMPLE}$ = 2MHz, unless otherwise noted.

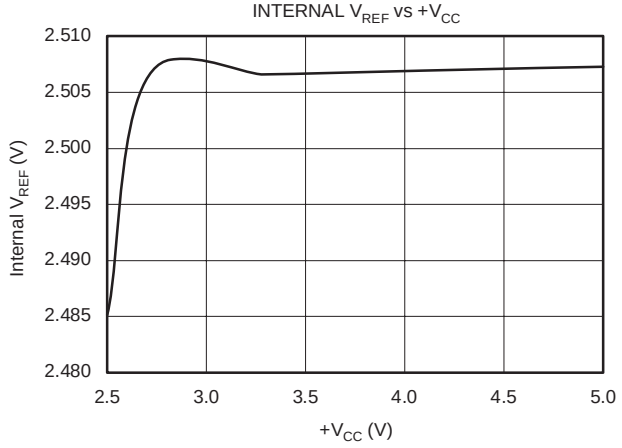
MAXIMUM SAMPLING RATE vs $R_{IN}$



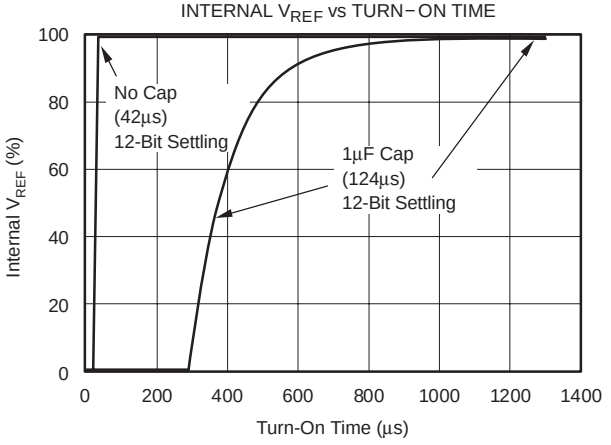

INTERNAL $V_{REF}$ vs TEMPERATURE



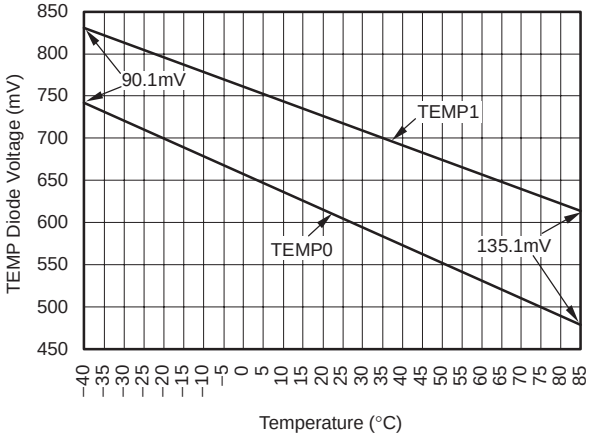

INTERNAL $V_{REF}$ vs $+V_{CC}$



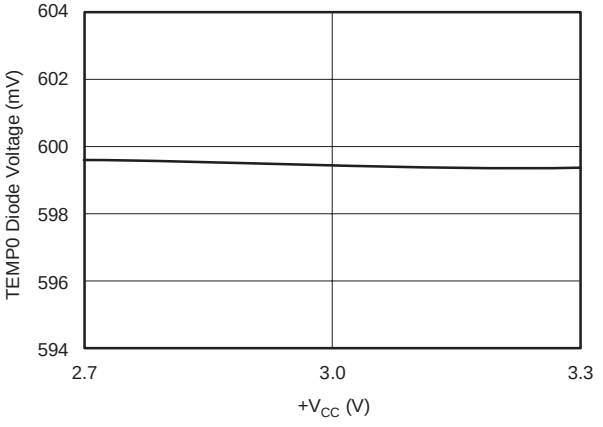

INTERNAL $V_{REF}$ vs TURN−ON TIME




TEMP DIODE VOLTAGE vs TEMPERATURE

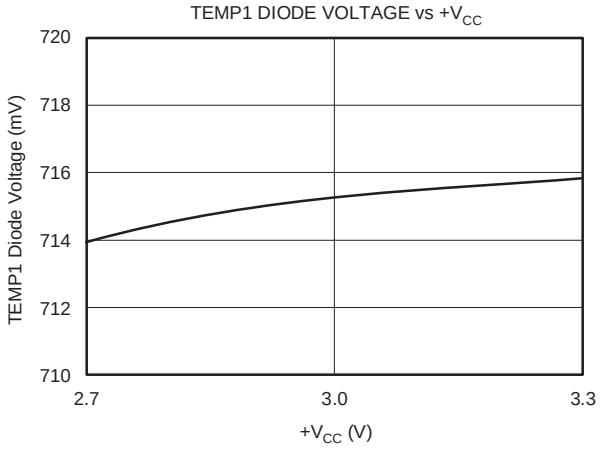



TEMP0 DIODE VOLTAGE vs $+V_{CC}$



## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C, $+V_{CC}$ = +2.7V, IOVDD = +1.8V, $V_{REF}$ = External +2.5V, 12-bit mode, PD0 = 0, $f_{SAMPLE}$ = 125kHz, and $f_{CLK}$ = 16 • $f_{SAMPLE}$ = 2MHz, unless otherwise noted.




# THEORY OF OPERATION

The TSC2046E is a classic successive approximation register (SAR) analog-to-digital converter (ADC). The architecture is based on capacitive redistribution, which inherently includes a sample-and-hold function. The converter is fabricated on a 0.6µm CMOS process.

The basic operation of the TSC2046E is shown in Figure 1. The device features an internal 2.5V reference and uses an external clock. Operation is maintained from a single supply of 2.7V to 5.25V. The internal reference can be overdriven with an external, low-impedance source between 1V and $+V_{CC}$. The value of the reference voltage directly sets the input range of the converter.

The analog input (X-, Y-, and Z-Position coordinates, auxiliary input, battery voltage, and chip temperature) to the converter is provided via a multiplexer. A unique configuration of low on-resistance touch panel driver switches allows an unselected ADC input channel to provide power and the accompanying pin to provide ground for an external device, such as a touch screen. By maintaining a differential input to the converter and a differential reference architecture, it is possible to negate the error from each touch panel driver switch on-resistance (if this is a source of error for the particular measurement).

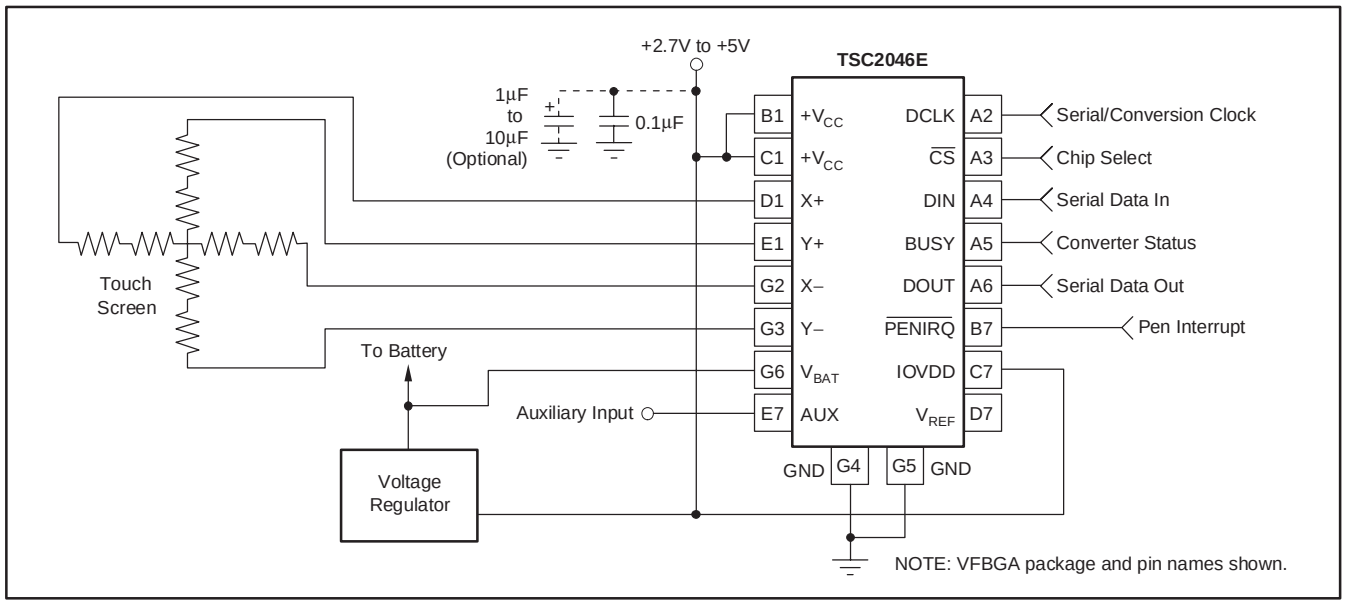



**Figure 1. Basic Operation of the TSC2046E**

## ANALOG INPUT

Figure 2 shows a block diagram of the input multiplexer on the TSC2046E, the differential input of the ADC, and the differential reference of the converter. Table 1 and Table 2 show the relationship between the A2, A1, A0, and SER/$\overline{\text{DFR}}$ control bits and the configuration of the TSC2046E. The control bits are provided serially via the DIN pin—see the *Digital Interface* section of this data sheet for more details.

When the converter enters the hold mode, the voltage difference between the +IN and –IN inputs (shown in Figure 2) is captured on the internal capacitor array. The input current into the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typically 25pF). After the capacitor is fully charged, there is no further input current. The rate of charge transfer from the analog source to the converter is a function of conversion rate.

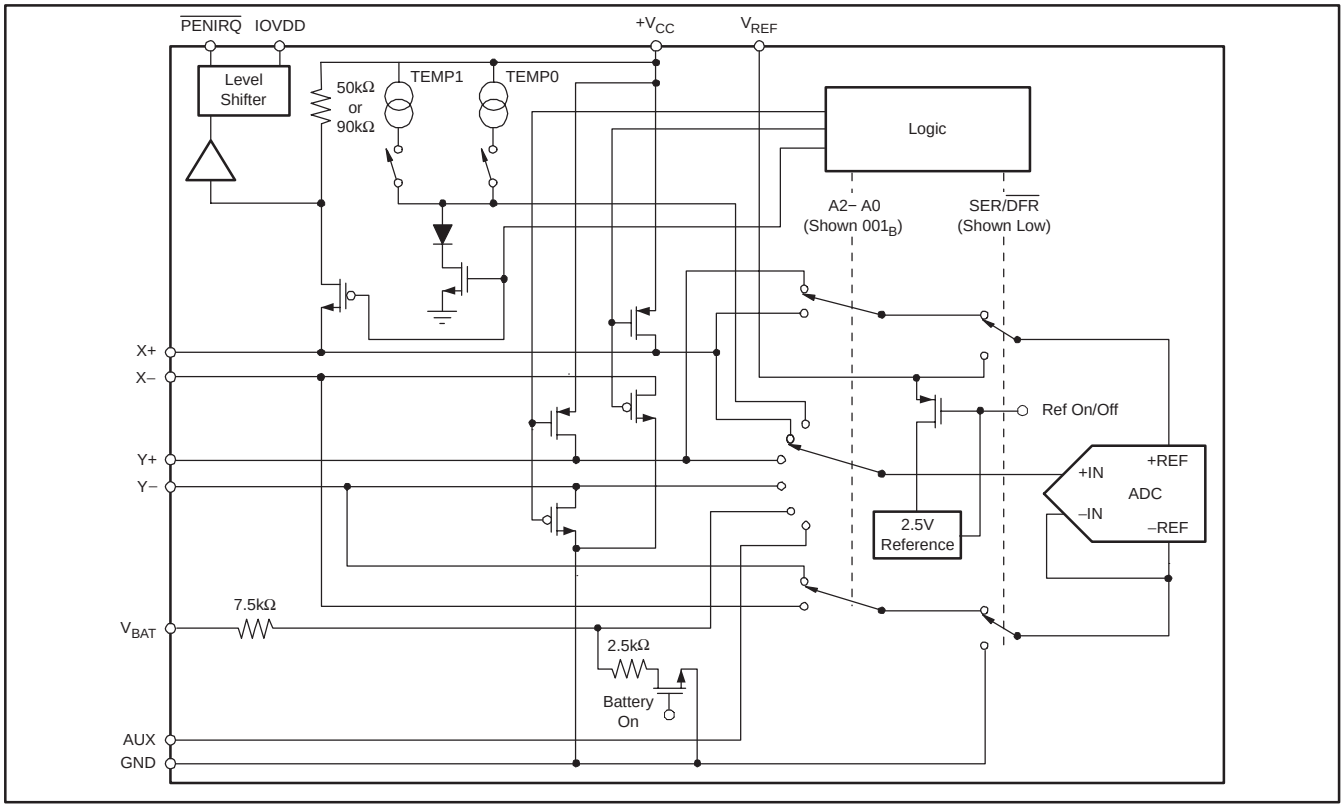



**Figure 2. Simplified Diagram of Analog Input**

| A2 | A1 | A0 | $V_{BAT}$ | $AUX_{IN}$ | TEMP | Y− | X+ | Y+ | Y-POSITION | X-POSITION | $Z_1$-POSITION | $Z_2$-POSITION | X-DRIVERS | Y-DRIVERS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | | | +IN (TEMP0) | | | | | | | | Off | Off |
| 0 | 0 | 1 | | | | | +IN | | Measure | | | | Off | On |
| 0 | 1 | 0 | +IN | | | | | | | | | | Off | Off |
| 0 | 1 | 1 | | | | | +IN | | | | Measure | | X−, On | Y+, On |
| 1 | 0 | 0 | | | | +IN | | | | | | Measure | X−, On | Y+, On |
| 1 | 0 | 1 | | | | | | +IN | | Measure | | | On | Off |
| 1 | 1 | 0 | | +IN | | | | | | | | | Off | Off |
| 1 | 1 | 1 | | | +IN (TEMP1) | | | | | | | | Off | Off |

**Table 1. Input Configuration (DIN), Single-Ended Reference Mode (SER/$\overline{\text{DFR}}$ high)**

| A2 | A1 | A0 | +REF | −REF | Y− | X+ | Y+ | Y-POSITION | X-POSITION | $Z_1$-POSITION | $Z_2$-POSITION | DRIVERS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | Y+ | Y− | | +IN | | Measure | | | | Y+, Y− |
| 0 | 1 | 1 | Y+ | X− | | +IN | | | | Measure | | Y+, X− |
| 1 | 0 | 0 | Y+ | X− | +IN | | | | | | Measure | Y+, X− |
| 1 | 0 | 1 | X+ | X− | | | +IN | | Measure | | | X+, X− |

**Table 2. Input Configuration (DIN), Differential Reference Mode (SER/$\overline{\text{DFR}}$ low)**

## INTERNAL REFERENCE

The TSC2046E has an internal 2.5V voltage reference that can be turned on or off with the control bit, PD1 (see Table 5 and Figure 3). Typically, the internal reference voltage is only used in the single-ended mode for battery monitoring, temperature measurement, and for using the auxiliary input. Optimal touch screen performance is achieved when using the differential mode. The internal reference voltage of the TSC2046E must be commanded to be off to maintain compatibility with the ADS7843. Therefore, after power-up, a write of PD1 = 0 is required to ensure the reference is off (see the Typical Characteristics for power-up time of the reference from power-down).

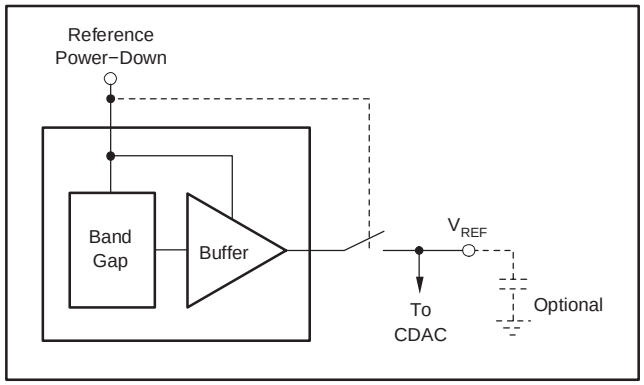



**Figure 3. Simplified Diagram of the Internal Reference**

## REFERENCE INPUT

The voltage difference between +REF and –REF (see Figure 2) sets the analog input range. The TSC2046E operates with a reference in the range of 1V to $+V_{CC}$. There are several critical items concerning the reference input and its wide voltage range. As the reference voltage is reduced, the analog voltage weight of each digital output code (referred to as LSB size) is also reduced. The LSB (least significant bit) size is equal to the reference voltage divided by 4096 in 12-bit mode. Any offset or gain error inherent in the ADC appears to increase, in terms of LSB size, as the reference voltage is reduced. For example, if the offset of a given converter is 2LSBs with a 2.5V reference, it is typically 5LSBs with a 1V reference. In each case, the actual offset of the device is the same, 1.22mV. With a lower reference voltage, more care must be taken to provide a clean layout including adequate bypassing, a clean (low-noise, low-ripple) power supply, a low-noise reference (if an external reference is used), and a low-noise input signal.

The voltage into the $V_{REF}$ input directly drives the capacitor digital-to-analog converter (CDAC) portion of the TSC2046E. Therefore, the input current is very low (typically < 13µA).

There is also a critical item regarding the reference when making measurements while the switch drivers are ON. For this discussion, it is useful to consider the basic operation of the TSC2046E (see Figure 1). This particular application shows the device being used to digitize a resistive touch screen. A measurement of the current Y-Position of the pointing device is made by connecting the X+ input to the ADC, turning on the Y+ and Y– drivers, and digitizing the voltage on X+ (Figure 4 shows a block diagram). For this measurement, the resistance in the X+ lead does not affect the conversion (it does affect the settling time, but the resistance is usually small enough that this is not a concern). However, because the resistance between Y+ and Y– is fairly low, the on-resistance of the Y drivers does make a small difference. Under the situation outlined so far, it is not possible to achieve a 0V input or a full-scale input regardless of where the pointing device is on the touch screen because some voltage is lost across the internal switches. In addition, the internal switch resistance is unlikely to track the resistance of the touch screen, providing an additional source of error.

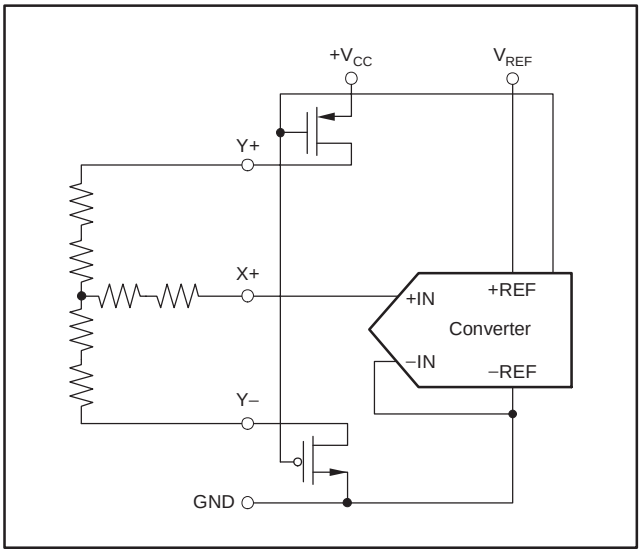



**Figure 4. Simplified Diagram of Single-Ended Reference (SER/DFR high, Y switches enabled, X+ is analog input)**

This situation can be remedied as shown in Figure 5. By setting the SER/$\overline{\text{DFR}}$ bit low, the +REF and –REF inputs are connected directly to Y+ and Y–, respectively, making the analog-to-digital conversion ratiometric. The result of the conversion is always a percentage of the external resistance, regardless of how it changes in relation to the on-resistance of the internal switches. Note that there is an important consideration regarding power dissipation when using the ratiometric mode of operation (see the *Power Dissipation* section for more details).

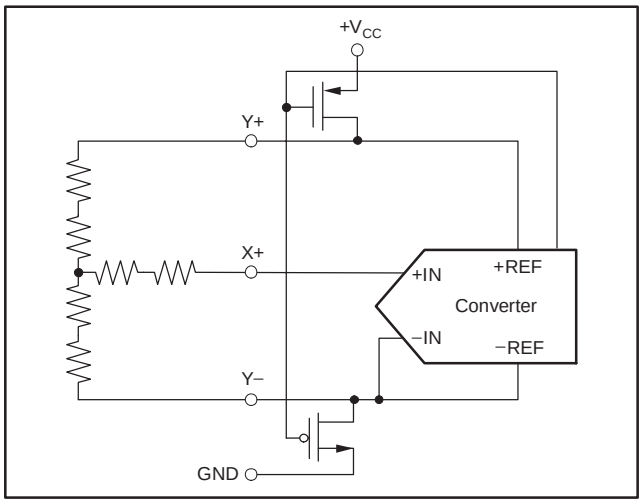



**Figure 5. Simplified Diagram of Differential Reference (SER/DFR low, Y switches enabled, X+ is analog input)**

As a final note about the differential reference mode, it must be used with $+V_{CC}$ as the source of the +REF voltage and cannot be used with $V_{REF}$. It is possible to use a high-precision reference on $V_{REF}$ and single-ended reference mode for measurements that do not need to be ratiometric. In some cases, it is possible to power the converter directly from a precision reference. Most references can provide enough power for the TSC2046E, but might not be able to supply enough current for the external load (such as a resistive touch screen).

## TOUCH SCREEN SETTLING

In some applications, external capacitors may be required across the touch screen for filtering noise picked up by the touch screen (for example, noise generated by the LCD panel or backlight circuitry). These capacitors provide a low-pass filter to reduce the noise, but cause a settling time requirement when the panel is touched that typically shows up as a gain error. There are several methods for minimizing or eliminating this issue. The problem is that the input and/or reference has not settled to the final steady-state value prior to the ADC sampling the input(s) and providing the digital output. Additionally, the reference voltage may still be changing during the measurement cycle. Option 1 is to stop or slow down the TSC2046E DCLK for the required touch screen settling time. This option allows the input and reference to have stable values for the Acquire period (3 clock cycles of the TSC2046E; see Figure 9). This option works for both the single-ended and the differential modes. Option 2 is to operate the TSC2046E in the differential mode only for the touch screen measurements and command the TSC2046E to remain on (touch screen drivers ON) and not go into power-down (PD0 = 1). Several conversions are made, depending on the settling time required and the TSC2046E data rate. Once the required number of conversions have been made, the processor commands the TSC2046E to go into its power-down state on the last measurement. This process is required for X-Position, Y-Position, and Z-Position measurements. Option 3 is to operate in the 15 Clock-per-Conversion mode, which overlaps the analog-to-digital conversions and maintains the touch screen drivers on until commanded to stop by the processor (see Figure 13).

## TEMPERATURE MEASUREMENT

In some applications, such as battery recharging, a measurement of ambient temperature is required. The temperature measurement technique used in the TSC2046E relies on the characteristics of a semiconductor junction operating at a fixed current level. The forward diode voltage ($V_{BE}$) has a well-defined characteristic versus temperature. The ambient temperature can be predicted in applications by knowing the +25°C value of the $V_{BE}$ voltage and then monitoring the delta of that voltage as the temperature changes. The TSC2046E offers two modes of operation. The first mode requires calibration at a known temperature, but only requires a single reading to predict the ambient temperature. A diode is used (turned on) during this measurement cycle. The voltage across the diode is connected through the MUX for digitizing the forward bias voltage by the ADC with an address of A2 = 0, A1 = 0, and A0 = 0 (see Table 1 and Figure 6 for details). This voltage is typically 600mV at +25°C with a 20µA current through the diode. The absolute value of this diode voltage can vary by a few millivolts. However, the temperature coefficient ($T_C$) of this voltage is very consistent at –2.1mV/°C. During the final test of the end product, the diode voltage would be stored at a known room temperature, in memory, for calibration purposes by the user. The result is an equivalent temperature measurement resolution of 0.3°C/LSB (in 12-bit mode).

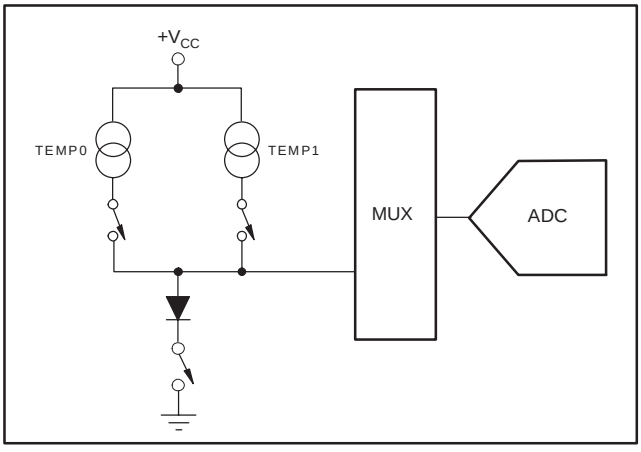



**Figure 6. Functional Block Diagram of Temperature Measurement**

The second mode of operation does not require a test temperature calibration, but uses a two-measurement method to eliminate the need for absolute temperature calibration and for achieving 2°C accuracy. This mode requires a second conversion with an address of A2 = 1, A1 = 1, and A0 = 1, with a 91 times larger current. The voltage difference between the first and second conversion using 91 times the bias current is represented by Equation (1):

$$\Delta V = \frac{kT}{q} \cdot \ln(N) \quad (1)$$

where:

N is the current ratio = 91.

k = Boltzmann's constant = $1.3807 \times 10^{-23}$ J/K (joules/kelvins).

q = the electron charge = $1.6022 \times 10^{-19}$ C (coulombs).

T = the temperature in kelvins (K).

This method can provide improved absolute temperature measurement, but at a lower resolution of 1.6°C/LSB. The resulting equation that solves for T is:

$$T = \frac{q \cdot \Delta V}{k \cdot \ln(N)} \quad (2)$$

where:

$\Delta V = V_{BE}(TEMP1) - V_{BE}(TEMP0)$ (in mV)

$\therefore T = 2.573 \cdot \Delta V$ (in K)

or $T = 2.573 \cdot \Delta V - 273$ (in °C)

**NOTE:** The bias current for each diode temperature measurement is only on for three clock cycles (during the acquisition mode) and, therefore, does not add any noticeable increase in power, especially if the temperature measurement only occurs occasionally.

## BATTERY MEASUREMENT

An added feature of the TSC2046E is the ability to monitor the battery voltage on the other side of the voltage regulator (dc/dc converter), as shown in Figure 7. The battery voltage can vary from 0V to 6V, while maintaining the voltage to the TSC2046E at 2.7V, 3.3V, etc. The input voltage ($V_{BAT}$) is divided down by four so that a 5.5V battery voltage is represented as 1.375V to the ADC. This design simplifies the multiplexer and control logic. In order to minimize the power consumption, the divider is only on during the sampling period when A2 = 0, A1 = 1, and A0 = 0 (see Table 1 for the relationship between the control bits and configuration of the TSC2046E).

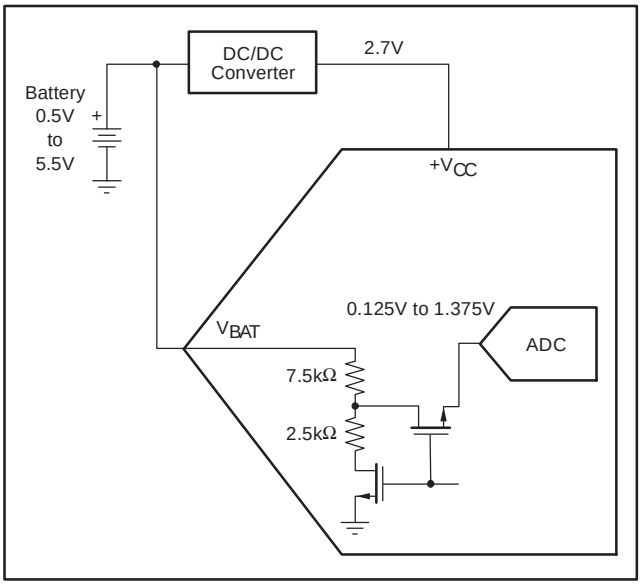



**Figure 7. Battery Measurement Functional Block Diagram**

## PRESSURE MEASUREMENT

Measuring touch pressure can also be done with the TSC2046E. To determine pen or finger touch, the pressure of the touch needs to be determined. Generally, it is not necessary to have very high performance for this test; therefore, the 8-bit resolution mode is recommended (however, calculations shown here are in the 12-bit resolution mode). There are several different ways of performing this measurement. The TSC2046E supports two methods. The first method requires knowing the X-plate resistance, measurement of the X-Position, and two additional cross panel measurements ($Z_1$ and $Z_2$) of the touch screen, as shown in Figure 8. Using Equation (3) calculates the touch resistance:

$$R_{TOUCH} = R_{X-Plate} \cdot \frac{X-Position}{4096} \left( \frac{Z_2}{Z_1} - 1 \right) \quad (3)$$

The second method requires knowing both the X-plate and Y-plate resistance, measurement of X-Position and Y-Position, and $Z_1$. Using Equation (4) also calculates the touch resistance:

$$R_{TOUCH} = \frac{R_{X-Plate} \cdot X-Position}{4096} \left( \frac{4096}{Z_1} - 1 \right) - R_{Y-Plate} \left( 1 - \frac{Y-Position}{4096} \right) \quad (4)$$

## DIGITAL INTERFACE

See Figure 9 for the typical operation of the TSC2046E digital interface. This diagram assumes that the source of the digital signals is a microcontroller or digital signal processor with a basic serial interface. Each communication between the processor and the converter, such as SPI, SSI, or Microwire™ synchronous serial interface, consists of eight clock cycles. One complete conversion can be accomplished with three serial communications for a total of 24 clock cycles on the DCLK input.

The first eight clock cycles are used to provide the control byte via the DIN pin. When the converter has enough information about the following conversion to set the input multiplexer and reference inputs appropriately, the converter enters the acquisition (sample) mode and, if needed, the touch panel drivers are turned on. After three more clock cycles, the control byte is complete and the converter enters the conversion mode. At this point, the input sample-and-hold goes into the hold mode and the touch panel drivers turn off (in single-ended mode). The next 12 clock cycles accomplish the actual analog-to-digital conversion. If the conversion is ratiometric (SER/$\overline{DFR}$ = 0), the drivers are on during the conversion and a 13th clock cycle is needed for the last bit of the conversion result. Three more clock cycles are needed to complete the last byte (DOUT will be low), which are ignored by the converter.

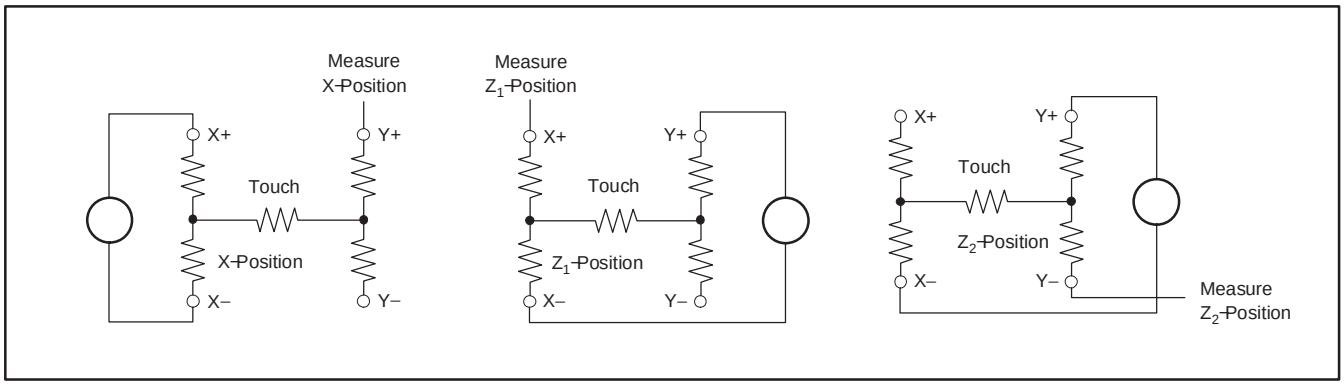



**Figure 8. Pressure Measurement Block Diagrams**

### Control Byte

The control byte (on DIN), as shown in Table 3, provides the start conversion, addressing, ADC resolution, configuration, and power-down of the TSC2046E. Figure 9, Table 3 and Table 4 give detailed information regarding the order and description of these control bits within the control byte.

**Initiate START**—The first bit, the S bit, must always be high and initiates the start of the control byte. The TSC2046E ignores inputs on the DIN pin until the start bit is detected.

**Addressing**—The next three bits (A2, A1, and A0) select the active input channel(s) of the input multiplexer (see Table 1, Table 2, and Figure 2), touch screen drivers, and the reference inputs.

**MODE**—The mode bit sets the resolution of the ADC. With this bit low, the next conversion has 12-bit resolution, whereas with this bit high, the next conversion has 8-bit resolution.

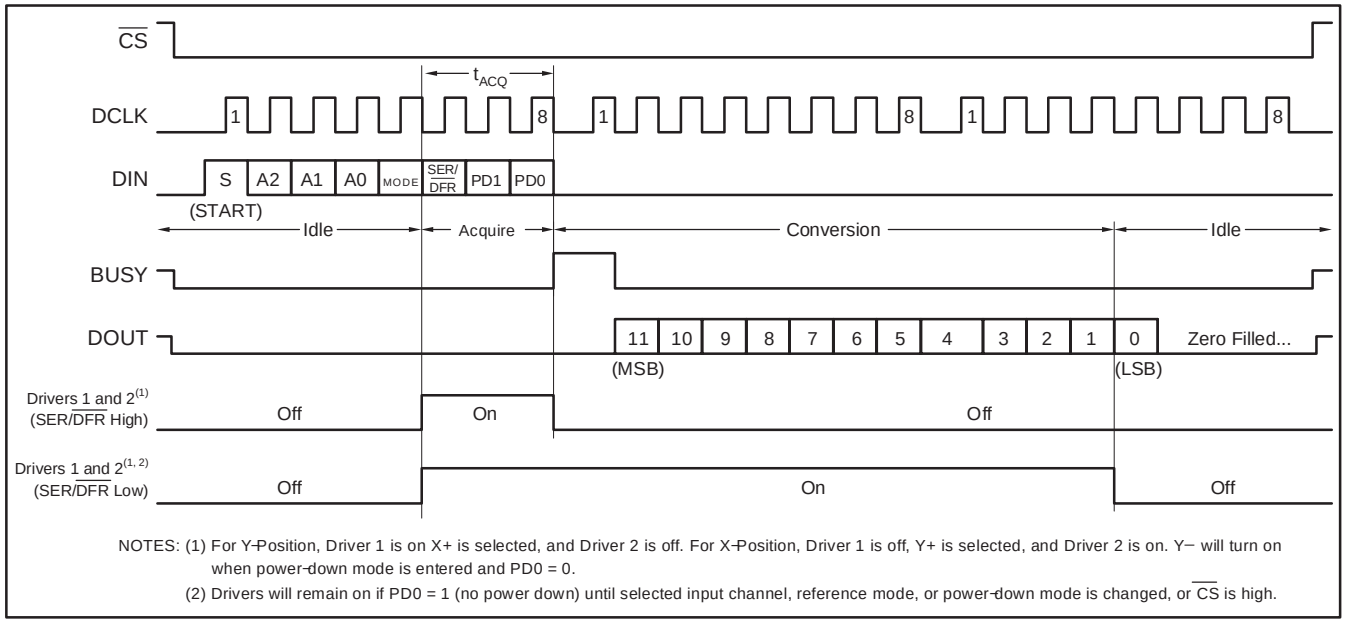
**SER/$\overline{\text{DFR}}$**—The SER/$\overline{\text{DFR}}$ bit controls the reference mode, either single-ended (high) or differential (low). The differential mode is also referred to as the ratiometric conversion mode and is preferred for X-Position, Y-Position, and Pressure-Touch measurements for optimum performance. The reference is derived from the voltage at the switch drivers, which is almost the same as the voltage to the touch screen. In this case, a reference voltage is not needed as the reference voltage to the ADC is the voltage across the touch screen. In the single-ended mode, the converter reference voltage is always the difference between the $V_{REF}$ and GND pins (see Table 1 and Table 2, and Figure 2 through Figure 5, for further information).

| BIT 7 (MSB) | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 (LSB) |
|---|---|---|---|---|---|---|---|
| S | A2 | A1 | A0 | MODE | SER/$\overline{\text{DFR}}$ | PD1 | PD0 |

**Table 3. Order of the Control Bits in the Control Byte**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 7 | S | Start bit. Control byte starts with first high bit on DIN. A new control byte can start every 15th clock cycle in 12-bit conversion mode or every 11th clock cycle in 8-bit conversion mode (see Figure 13). |
| 6-4 | A2-A0 | Channel Select bits. Along with the SER/$\overline{\text{DFR}}$ bit, these bits control the setting of the multiplexer input, touch driver switches, and reference inputs (see Table 1 and Figure 13). |
| 3 | MODE | 12-Bit/8-Bit Conversion Select bit. This bit controls the number of bits for the next conversion: 12-bits (low) or 8-bits (high). |
| 2 | SER/$\overline{\text{DFR}}$ | Single-Ended/Differential Reference Select bit. Along with bits A2-A0, this bit controls the setting of the multiplexer input, touch driver switches, and reference inputs (see Table 1 and Table 2). |
| 1-0 | PD1-PD0 | Power-Down Mode Select bits. Refer to Table 5 for details. |

**Table 4. Descriptions of the Control Bits within the Control Byte**




NOTES: (1) For Y-Position, Driver 1 is on X+ is selected, and Driver 2 is off. For X-Position, Driver 1 is off, Y+ is selected, and Driver 2 is on. Y− will turn on when power-down mode is entered and PD0 = 0.
(2) Drivers will remain on if PD0 = 1 (no power down) until selected input channel, reference mode, or power-down mode is changed, or $\overline{\text{CS}}$ is high.

**Figure 9. Conversion Timing, 24 Clocks-per-Conversion, 8-Bit Bus Interface. No DCLK delay required with dedicated serial port**

If X-Position, Y-Position, and Pressure-Touch are measured in the single-ended mode, an external reference voltage is needed. The TSC2046E must also be powered from the external reference. Caution should be observed when using the single-ended mode such that the input voltage to the ADC does not exceed the internal reference voltage, especially if the supply voltage is greater than 2.7V.

**NOTE:** The differential mode can only be used for X-Position, Y-Position, and Pressure-Touch measurements. All other measurements require the single-ended mode.

**PD0 and PD1**—Table 5 describes the power-down and the internal reference voltage configurations. The internal reference voltage can be turned on or off independently of the ADC. This feature can allow extra time for the internal reference voltage to settle to the final value prior to making a conversion. Make sure to also allow this extra wake-up time if the internal reference is powered down. The ADC requires no wake-up time and can be instantaneously used. Also note that the status of the internal reference power-down is latched into the part (internally) with BUSY going high. In order to turn the reference off, an additional write to the TSC2046E is required after the channel has been converted.

| PD1 | PD0 | $\overline{\text{PENIRQ}}$ | DESCRIPTION |
|---|---|---|---|
| 0 | 0 | Enabled | Power-Down Between Conversions. When each conversion is finished, the converter enters a low-power mode. At the start of the next conversion, the device instantly powers up to full power. There is no need for additional delays to ensure full operation, and the very first conversion is valid. The Y− switch is on when in power-down. |
| 0 | 1 | Disabled | Reference is off and ADC is on. |
| 1 | 0 | Enabled | Reference is on and ADC is off. |
| 1 | 1 | Disabled | Device is always powered. Reference is on and ADC is on. |

**Table 5. Power-Down and Internal Reference Selection**

## $\overline{\text{PENIRQ}}$ OUTPUT

The pen-interrupt output function is shown in Figure 10. While in power-down mode with PD0 = 0, the Y-driver is on and connects the Y-plane of the touch screen to GND. The $\overline{\text{PENIRQ}}$ output is connected to the X+ input through two transmission gates. When the screen is touched, the X+ input is pulled to ground through the touch screen.

In most of the TSC2046E models, the internal pullup resistor value is nominally 50kΩ, but this value may vary between 36kΩ and 67kΩ given process and temperature variations. In order to assure a logic low of 0.35 • ($+V_{CC}$) is presented to the $\overline{\text{PENIRQ}}$ circuitry, the total resistance between the X+ and Y− terminals must be less than 21kΩ.

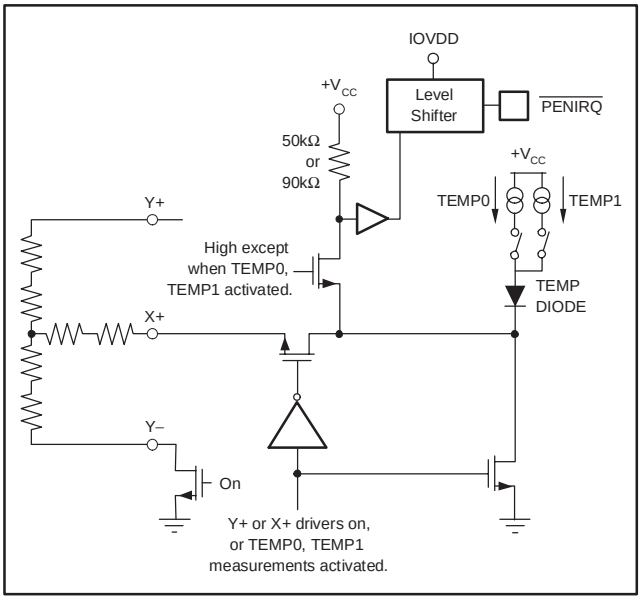



**Figure 10. $\overline{\text{PENIRQ}}$ Functional Block Diagram**

The −90 version of the TSC2046E uses a nominal 90kΩ pullup resistor that allows the total resistance between the X+ and Y− terminals to be as high as 30kΩ. Note that the higher pullup resistance causes a slower response time of the $\overline{\text{PENIRQ}}$ to a screen touch, so user software should take this into account.

The $\overline{\text{PENIRQ}}$ output goes low due to the current path through the touch screen to ground, initiating an interrupt to the processor. During the measurement cycle for X-, Y-, and Z-Position, the X+ input is disconnected from the $\overline{\text{PENIRQ}}$ internal pull-up resistor. This disconnection is done to eliminate any leakage current from the internal pull-up resistor through the touch screen, thus causing no errors.

Furthermore, the $\overline{\text{PENIRQ}}$ output is disabled and low during the measurement cycle for X-, Y-, and Z-Position. The $\overline{\text{PENIRQ}}$ output is disabled and high during the measurement cycle for battery monitor, auxiliary input, and chip temperature. If the last control byte written to the TSC2046E contains PD0 = 1, the pen-interrupt output function is disabled and is not able to detect when the screen is touched. In order to re-enable the pen-interrupt output function under these circumstances, a control byte needs to be written to the TSC2046E with PD0 = 0. If the last control byte written to the TSC2046E contains PD0 = 0, the pen-interrupt output function is enabled at the end of the conversion. The end of the conversion occurs on the falling edge of DCLK after bit 1 of the converted data is clocked out of the TSC2046E.

It is recommended that the processor mask the interrupt that $\overline{\text{PENIRQ}}$ is associated with whenever the processor sends a control byte to the TSC2046E. This masking prevents false triggering of interrupts when the $\overline{\text{PENIRQ}}$ output is disabled in the cases discussed in this section.

### 16 Clocks-per-Conversion

The control bits for conversion *n* + 1 can be overlapped with conversion *n* to allow for a conversion every 16 clock cycles, as shown in Figure 11. This figure also shows possible serial communication occurring with other serial peripherals between each byte transfer from the processor to the converter. (16 clocks cycles are possible, provided that each conversion completes within 1.6ms of starting. Otherwise, the signal that is captured on the input sample-and-hold may droop enough to affect the conversion result.) Note that the TSC2046E is fully powered while other serial communications are taking place during a conversion.

### Digital Timing

Figure 9, Figure 12, and Table 6 provide detailed timing for the digital interface of the TSC2046E.

### 15 Clocks-per-Conversion

Figure 13 provides the fastest way to clock the TSC2046E. This method does not work with the serial interface of most microcontrollers and digital signal processors, as they are generally not capable of providing 15 clock cycles per serial transfer. However, this method can be used with field-programmable gate arrays (FPGAs) or application- specific integrated circuits (ASICs). Note that this effectively increases the maximum conversion rate of the converter beyond the values given in the specification tables, which assume 16 clock cycles per conversion.

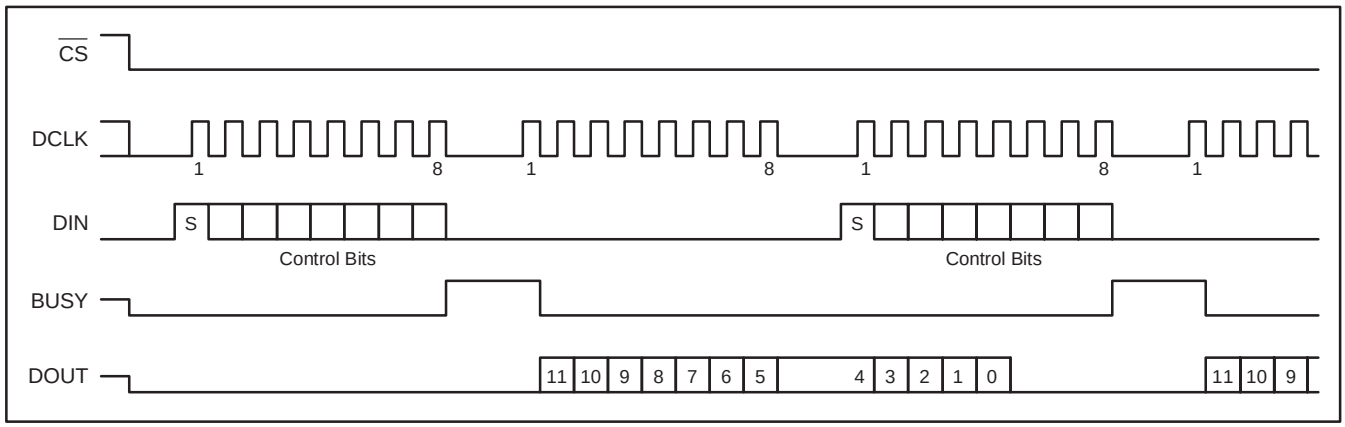



**Figure 11. Conversion Timing, 16 Clocks-per-Conversion, 8-Bit Bus Interface. No DCLK delay required with dedicated serial port**

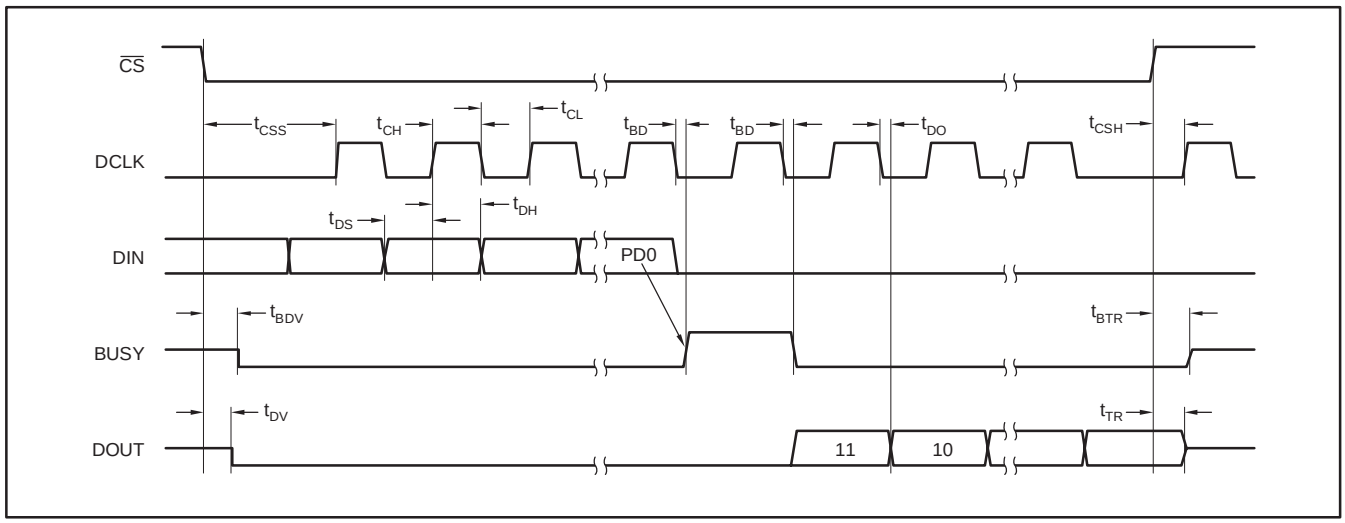



**Figure 12. Detailed Timing Diagram**

| SYMBOL | DESCRIPTION | $+V_{CC}$ • 2.7V, $+V_{CC}$ • IOVDD • 1.5V, $C_{LOAD}$ = 50pF | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $t_{ACQ}$ | Acquisition Time | 1.5 | | | µs |
| $t_{DS}$ | DIN Valid Prior to DCLK Rising | 100 | | | ns |
| $t_{DH}$ | DIN Hold After DCLK High | 50 | | | ns |
| $t_{DO}$ | DCLK Falling to DOUT Valid | | | 200 | ns |
| $t_{DV}$ | $\overline{CS}$ Falling to DOUT Enabled | | | 200 | ns |
| $t_{TR}$ | $\overline{CS}$ Rising to DOUT Disabled | | | 200 | ns |
| $t_{CSS}$ | $\overline{CS}$ Falling to First DCLK Rising | 100 | | | ns |
| $t_{CSH}$ | $\overline{CS}$ Rising to DCLK Ignored | 10 | | | ns |
| $t_{CH}$ | DCLK High | 200 | | | ns |
| $t_{CL}$ | DCLK Low | 200 | | | ns |
| $t_{BD}$ | DCLK Falling to BUSY Rising/Falling | | | 200 | ns |
| $t_{BDV}$ | $\overline{CS}$ Falling to BUSY Enabled | | | 200 | ns |
| $t_{BTR}$ | $\overline{CS}$ Rising to BUSY Disabled | | | 200 | ns |

**Table 6. Timing Specifications, $T_A$ = −40°C to +85°C**

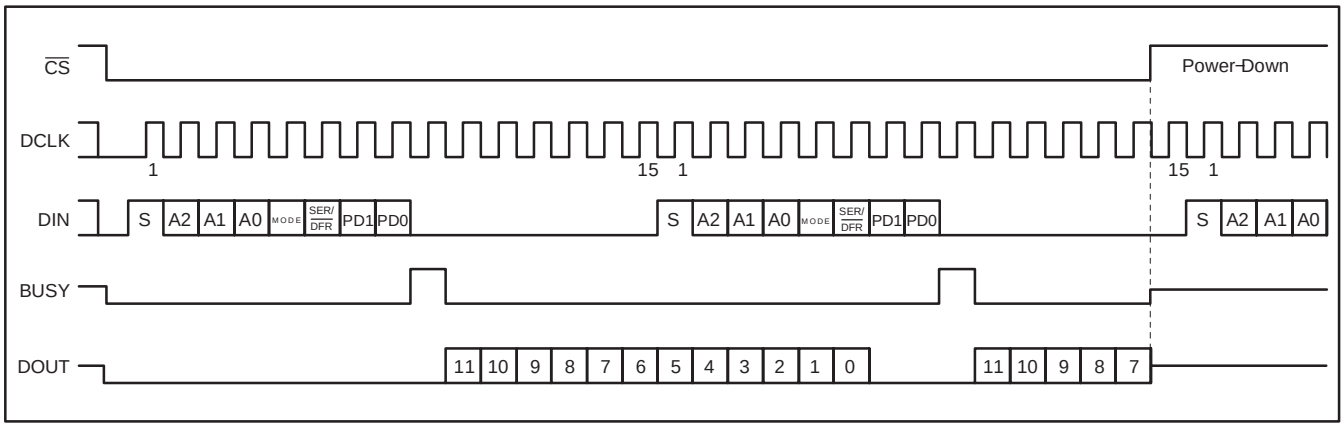


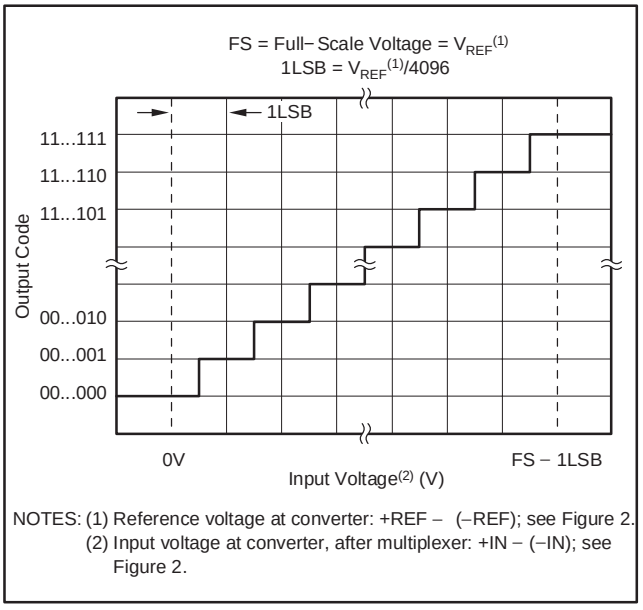

**Figure 13. Maximum Conversion Rate, 15 Clocks-per-Conversion**

## Data Format

The TSC2046E output data is in Straight Binary format, as shown in Figure 14. This figure shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.

## 8-Bit Conversion

The TSC2046E provides an 8-bit conversion mode that can be used when faster throughput is needed and the digital result is not as critical. By switching to the 8-bit mode, a conversion is complete four clock cycles earlier. Not only does this shorten each conversion by four bits (25% faster throughput), but each conversion can actually occur at a faster clock rate. This faster rate occurs because the internal settling time of the TSC2046E is not as critical—settling to better than 8 bits is all that is needed. The clock rate can be as much as 50% faster. The faster clock rate and fewer clock cycles combine to provide a 2x increase in conversion rate.




NOTES: (1) Reference voltage at converter: +REF − (−REF); see Figure 2.
(2) Input voltage at converter, after multiplexer: +IN − (−IN); see Figure 2.

**Figure 14. Ideal Input Voltages and Output Codes**

## POWER DISSIPATION

There are two major power modes for the TSC2046E: full-power (PD0 = 1) and auto power-down (PD0 = 0). When operating at full speed and 16 clocks-per-conversion (see Figure 11), the TSC2046E spends most of the time acquiring or converting. There is little time for auto power-down, assuming that this mode is active. Therefore, the difference between full-power mode and auto power-down is negligible. If the conversion rate is decreased by slowing the frequency of the DCLK input, the two modes remain approximately equal. However, if the DCLK frequency is kept at the maximum rate during a conversion but conversions are done less often, the difference between the two modes is dramatic.

Figure 15 shows the difference between reducing the DCLK frequency (scaling DCLK to match the conversion rate) or maintaining DCLK at the highest frequency and reducing the number of conversions per second. In the latter case, the converter spends an increasing percentage of time in power-down mode (assuming the auto power-down mode is active).

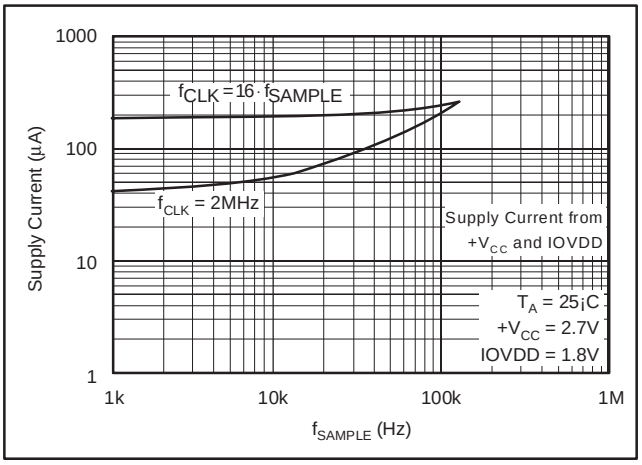



**Figure 15. Supply Current versus Directly Scaling the Frequency of DCLK with Sample Rate or Maintaining DCLK at the Maximum Possible Frequency**

Another important consideration for power dissipation is the reference mode of the converter. In the single-ended reference mode, the touch panel drivers are ON only when the analog input voltage is being acquired (see Figure 9 and Table 1). The external device (for example, a resistive touch screen), therefore, is only powered during the acquisition period. In the differential reference mode, the external device must be powered throughout the acquisition and conversion periods (see Figure 9). If the conversion rate is high, it could substantially increase power dissipation.

$\overline{CS}$ also puts the TSC2046E into power-down mode. When $\overline{CS}$ goes high, the TSC2046E immediately goes into power-down mode and does not complete the current conversion. The internal reference, however, does not turn off with $\overline{CS}$ going high. To turn the reference off, an additional write is required before $\overline{CS}$ goes high (PD1 = 0).

When the TSC2046E first powers up, the device draws about 20µA of current until a control byte is written to it with PD0 = 0 to put it into power-down mode. This current draw can be avoided if the TSC2046E is powered up with $\overline{CS}$ = 0 and DCLK = IOVDD.

# LAYOUT

The following layout suggestions provide the most optimum performance from the TSC2046E. Many portable applications, however, have conflicting requirements concerning power, cost, size, and weight. In general, most portable devices have fairly clean power and grounds because most of the internal components are very low power. This situation means less bypassing for the converter power and less concern regarding grounding. Still, each situation is unique and the following suggestions should be reviewed carefully.

For optimum performance, care should be taken with the physical layout of the TSC2046E circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Therefore, during any single conversion for an *n*-bit SAR converter, there are *n* windows in which large external transient voltages can easily affect the conversion result. Such glitches can originate from switching power supplies, nearby digital logic, and high-power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the DCLK input.

Because of the SAR architecture sensitvity, power to the TSC2046E should be clean and well bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. A 1µF to 10µF capacitor may also be needed if the impedance of the connection between $+V_{CC}$ or IOVDD and the power supplies is high. Low-leakage capacitors should be used to minimize power dissipation through the bypass capacitors when the TSC2046E is in power-down mode.

A bypass capacitor is generally not needed on the $V_{REF}$ pin because the internal reference is buffered by an internal op amp. If an external reference voltage originates from an op amp, make sure that it can drive any bypass capacitor that is used without oscillation.

The TSC2046E architecture offers no inherent rejection of noise or voltage variation in regards to using an external reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply appears directly in the digital results. Whereas high-frequency noise can be filtered out, voltage variation bacause of line frequency (50Hz or 60Hz) can be difficult to remove.

The GND pin must be connected to a clean ground point. In many cases, this is the *analog ground*. Avoid connections which are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply entry or battery connection point. The ideal layout includes an analog ground plane dedicated to the converter and associated analog circuitry.

In the specific case of use with a resistive touch screen, care should be taken with the connection between the converter and the touch screen. Although resistive touch screens have fairly low resistance, the interconnection should be as short and robust as possible. Longer connections are a source of error, much like the on-resistance of the internal switches. Likewise, loose connections can be a source of error when the contact resistance changes with flexing or vibrations.

As indicated previously, noise can be a major source of error in touch screen applications (such as in applications that require a backlit LCD panel). This EMI noise can be coupled through the LCD panel to the touch screen and cause *flickering* of the converted data. Several things can be done to reduce this error; for instance, using a touch screen with a bottom-side metal layer connected to ground to shunt the majority of noise to ground. Additionally, filtering capacitors from Y+, Y–, X+, and X− pins to ground can also help. Caution should be observed under these circumstances for settling time of the touch screen, especially operating in the single-ended mode and at high data rates.

## Revision History

| DATE | REV | PAGE | SECTION | DESCRIPTION |
|---|---|---|---|---|
| 1/08 | B | 3, 4 | Electrical Characteristics | Fixed typos in conditions header and in Note (6). |
| | | 13 | Temperature Measurement | Fixed typos in Equations (1) and (2). |
| 8/07 | A | 5 | Pin Configuration | Added note to QFN package. |

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TSC2046EIPW | Active | Production | TSSOP (PW) \| 16 | 90 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TSC 2046EI |
| TSC2046EIPW.B | Active | Production | TSSOP (PW) \| 16 | 90 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TSC 2046EI |
| TSC2046EIPWG4 | Active | Production | TSSOP (PW) \| 16 | 90 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TSC 2046EI |
| TSC2046EIPWR | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TSC 2046EI |
| TSC2046EIPWR.B | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TSC 2046EI |
| TSC2046EIPWRG4 | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TSC 2046EI |
| TSC2046EIRGVR | Active | Production | VQFN (RGV) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TSC 2046E |
| TSC2046EIRGVR.B | Active | Production | VQFN (RGV) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TSC 2046E |
| TSC2046EIRGVRG4 | Active | Production | VQFN (RGV) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TSC 2046E |
| TSC2046EIRGVRG4.B | Active | Production | VQFN (RGV) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TSC 2046E |
| TSC2046EIRGVT | Active | Production | VQFN (RGV) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TSC 2046E |
| TSC2046EIRGVT.B | Active | Production | VQFN (RGV) \| 16 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | TSC 2046E |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TSC2046E :**

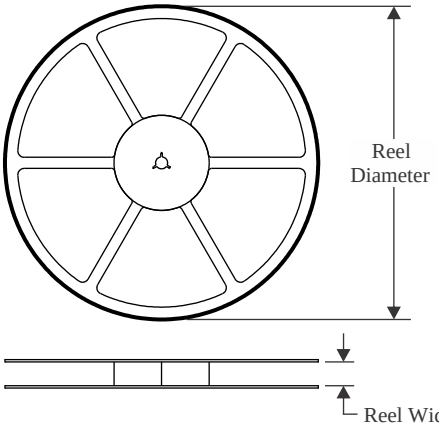
- Automotive : TSC2046E-Q1

NOTE: Qualified Version Definitions:

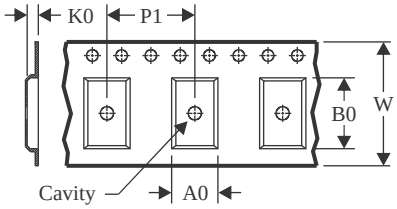
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

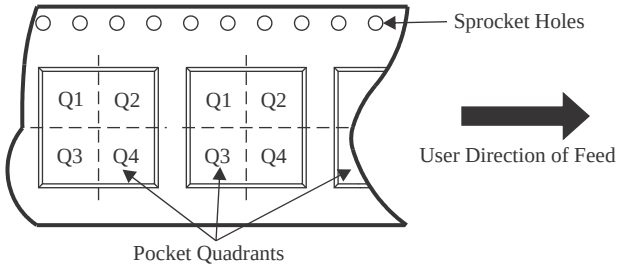



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

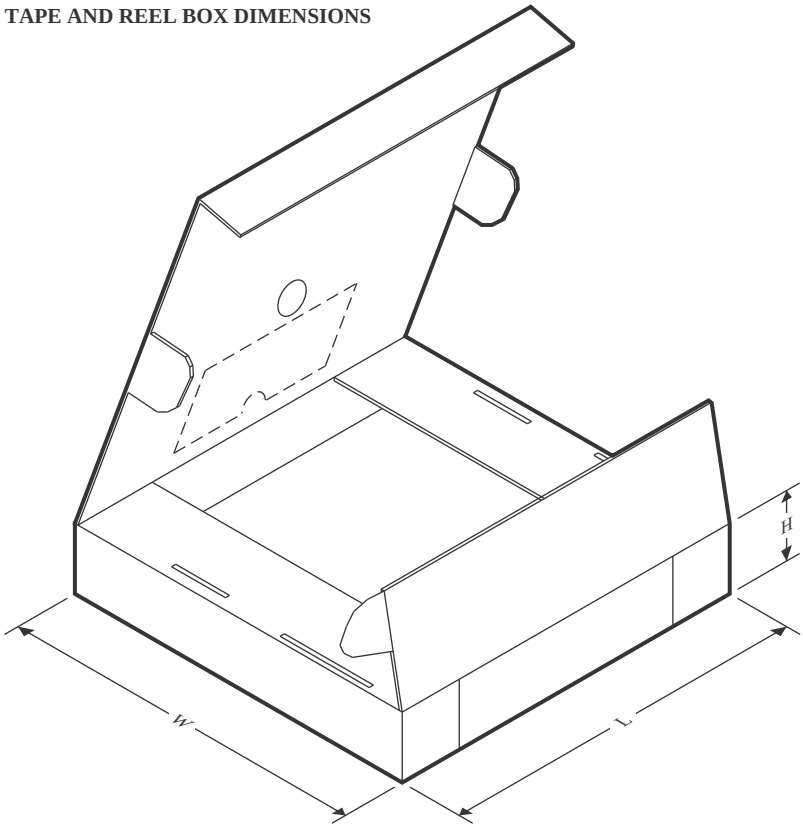
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TSC2046EIPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TSC2046EIRGVR | VQFN | RGV | 16 | 2500 | 330.0 | 12.4 | 4.3 | 4.3 | 1.5 | 8.0 | 12.0 | Q2 |
| TSC2046EIRGVRG4 | VQFN | RGV | 16 | 2500 | 330.0 | 12.4 | 4.3 | 4.3 | 1.5 | 8.0 | 12.0 | Q2 |
| TSC2046EIRGVT | VQFN | RGV | 16 | 250 | 180.0 | 12.4 | 4.3 | 4.3 | 1.5 | 8.0 | 12.0 | Q2 |

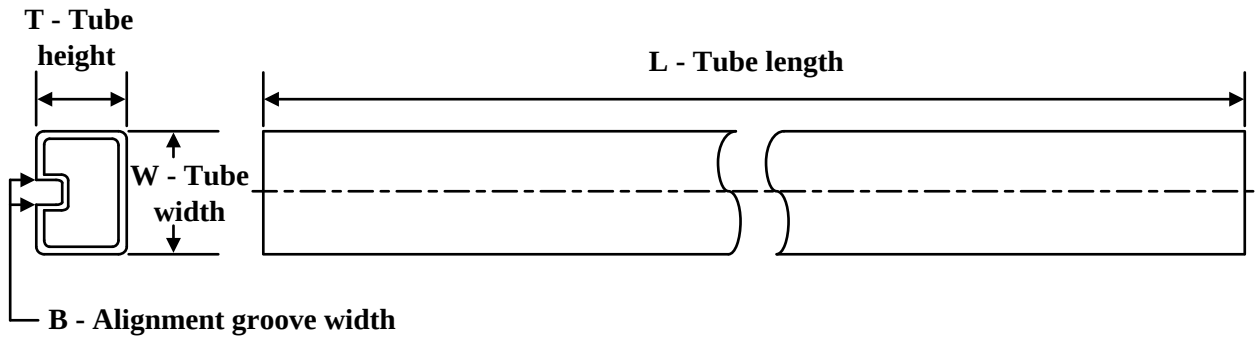
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TSC2046EIPWR | TSSOP | PW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| TSC2046EIRGVR | VQFN | RGV | 16 | 2500 | 350.0 | 350.0 | 43.0 |
| TSC2046EIRGVRG4 | VQFN | RGV | 16 | 2500 | 350.0 | 350.0 | 43.0 |
| TSC2046EIRGVT | VQFN | RGV | 16 | 250 | 210.0 | 185.0 | 35.0 |

## TUBE




*All dimensions are nominal

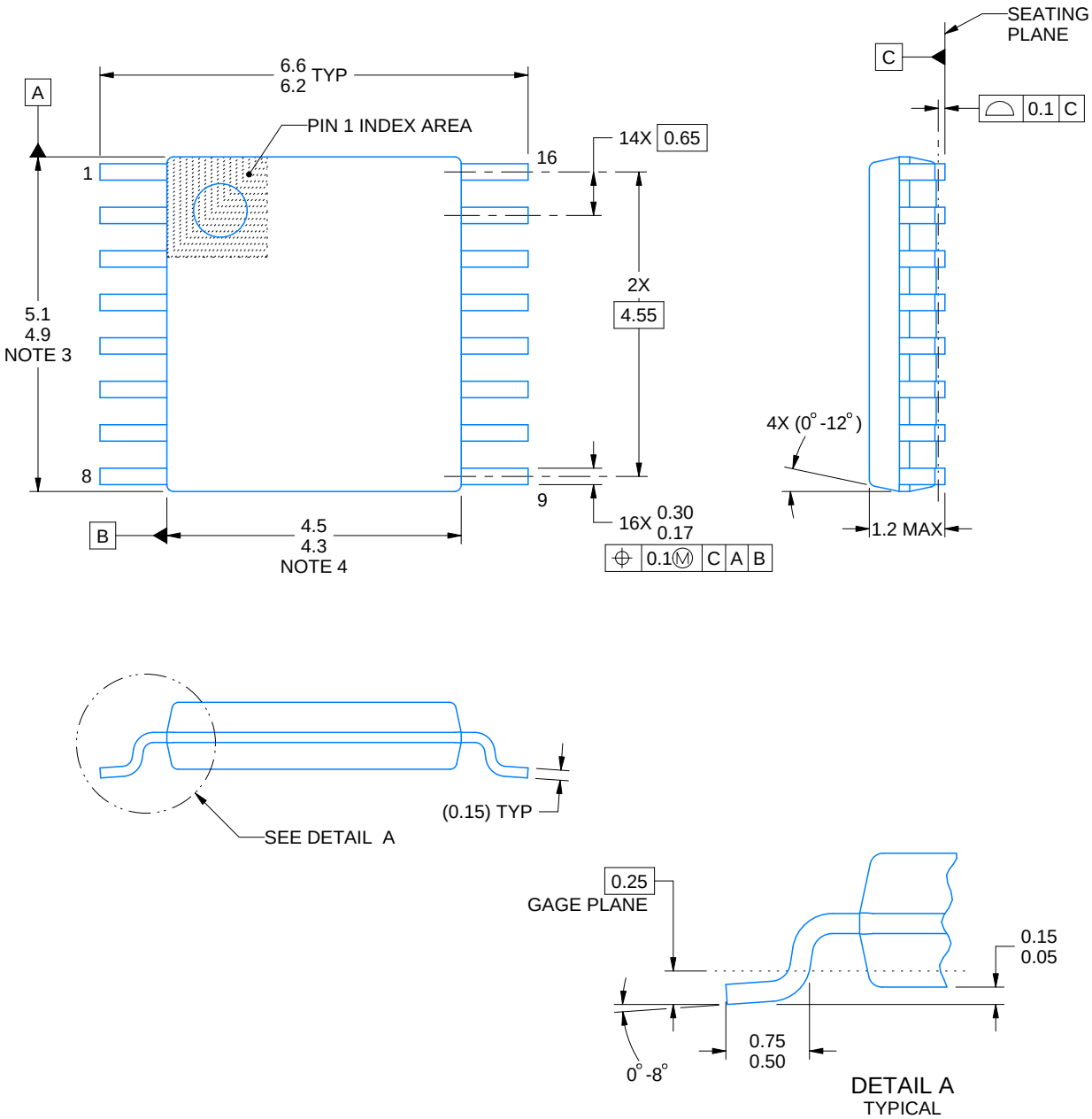
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| TSC2046EIPW | PW | TSSOP | 16 | 90 | 530 | 10.2 | 3600 | 3.5 |
| TSC2046EIPW.B | PW | TSSOP | 16 | 90 | 530 | 10.2 | 3600 | 3.5 |
| TSC2046EIPWG4 | PW | TSSOP | 16 | 90 | 530 | 10.2 | 3600 | 3.5 |

# PACKAGE OUTLINE

## PW0016A

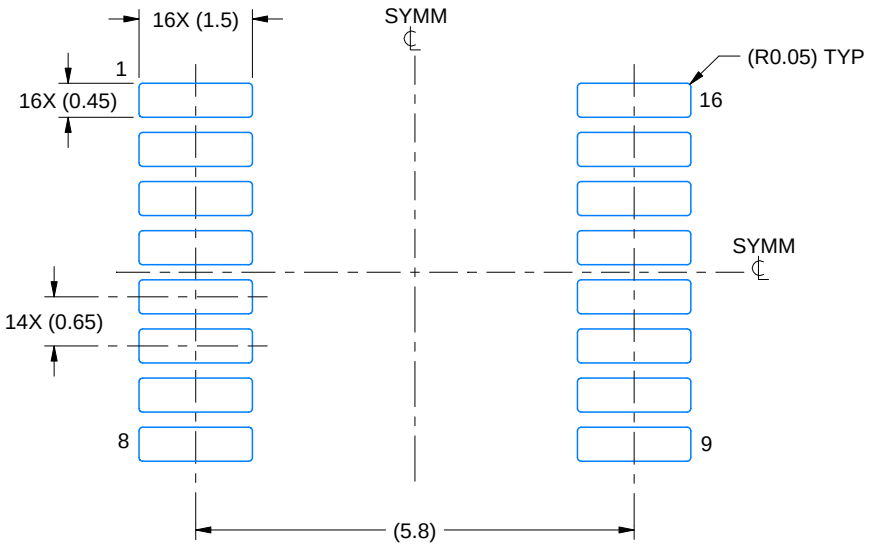
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

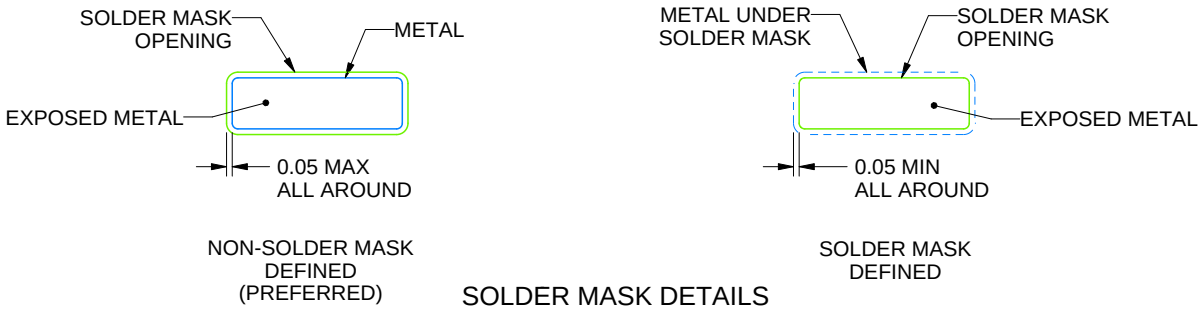



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

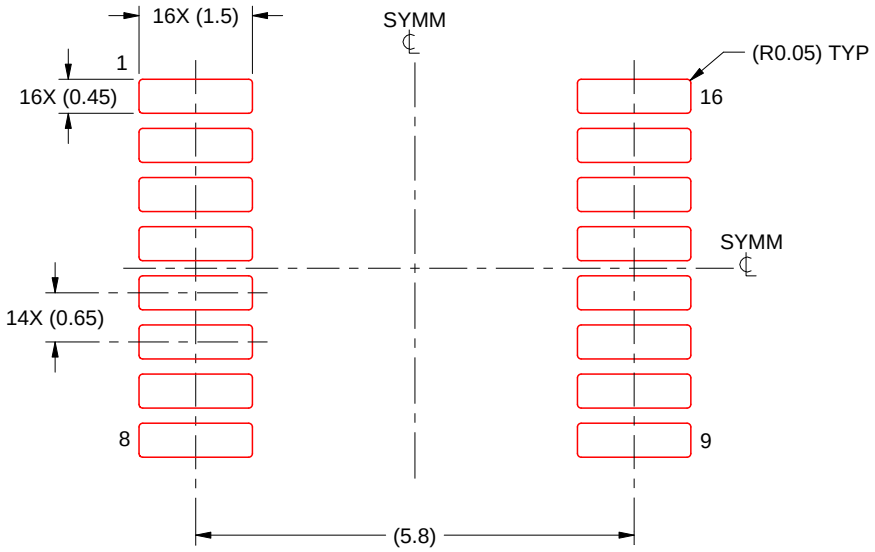



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

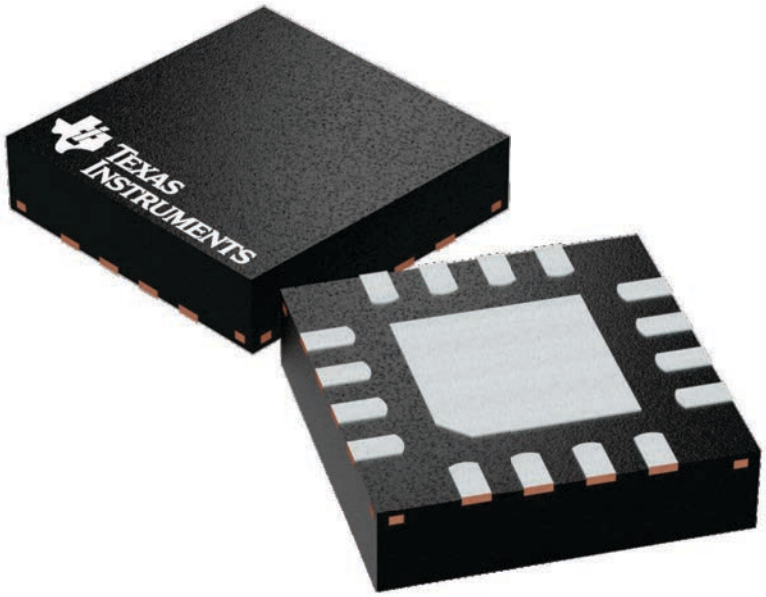
# GENERIC PACKAGE VIEW

## RGV 16

## VQFN - 1 mm max height

**4 x 4, 0.65 mm pitch**

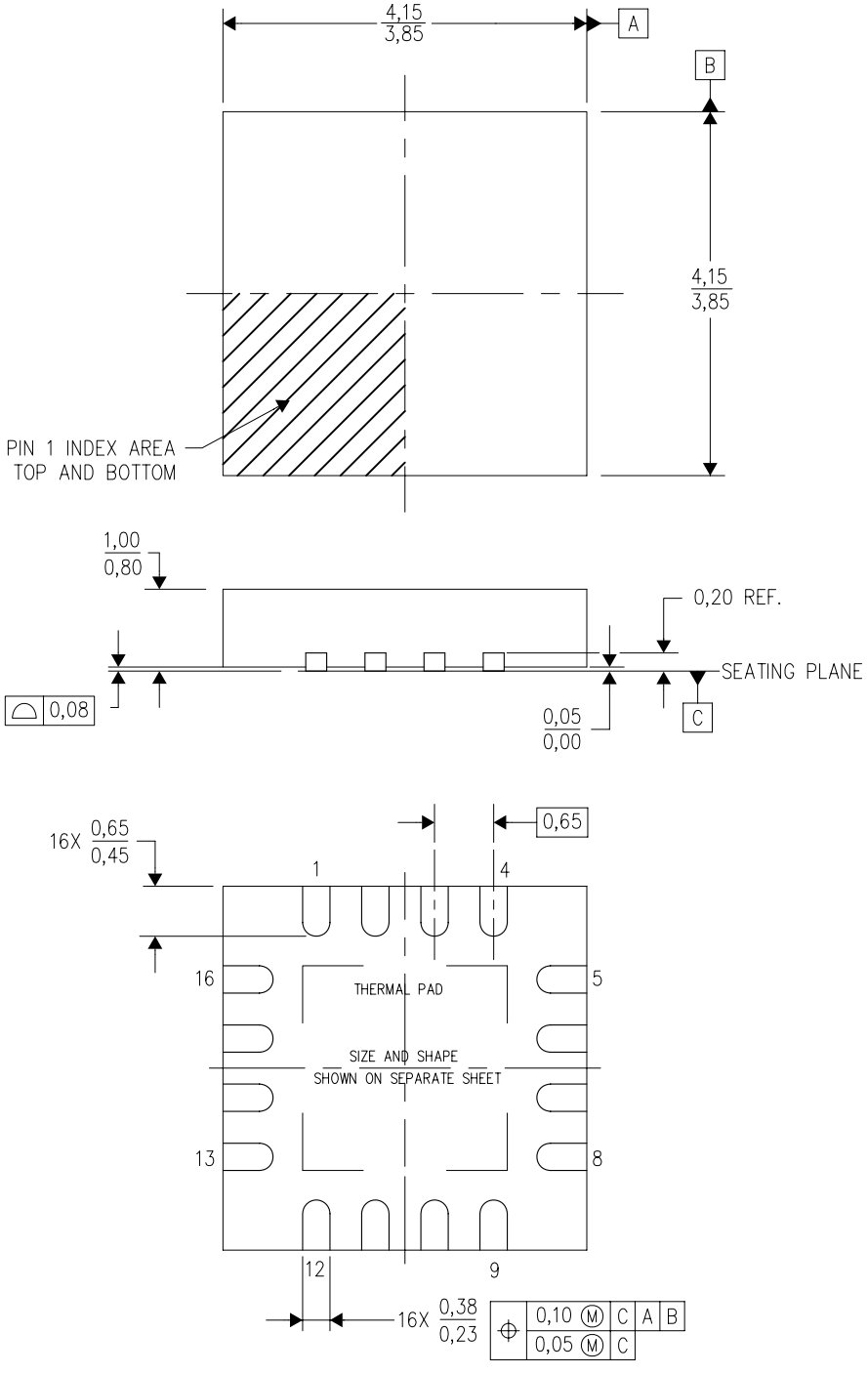
PLASTIC QUAD FLATPACK - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224748/A

RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

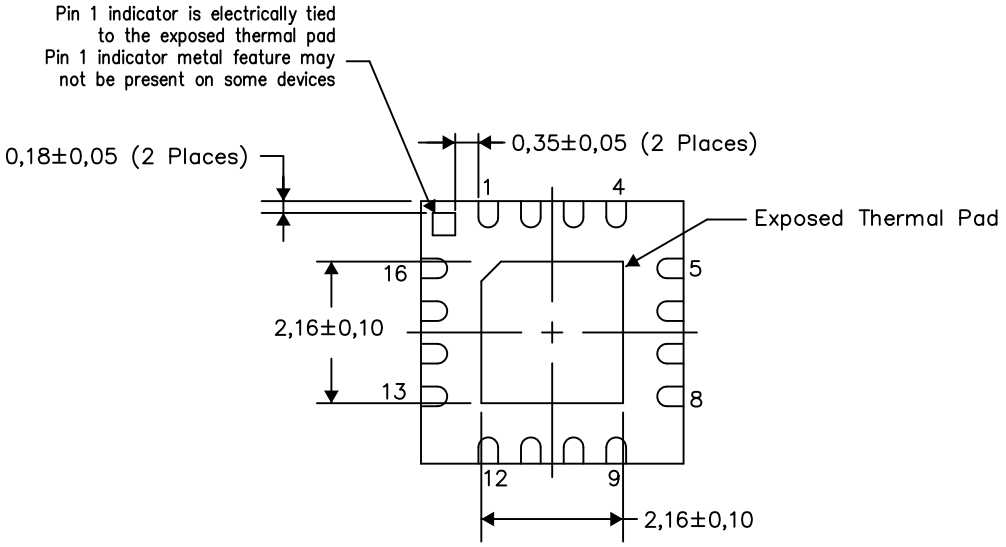
RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



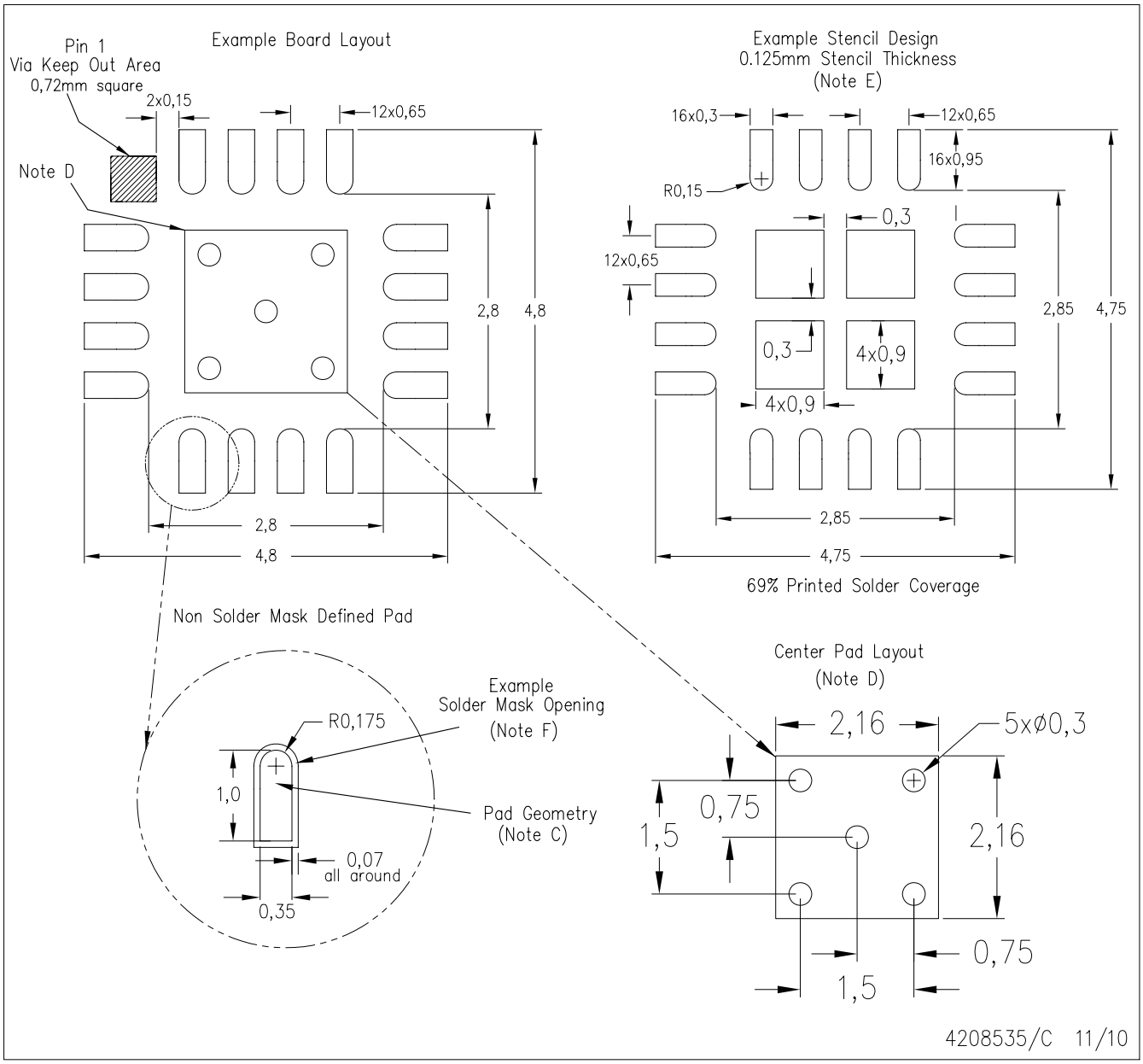

Bottom View

Exposed Thermal Pad Dimensions

4206351–2/L 05/13

NOTE: All linear dimensions are in millimeters

RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025