TEXAS INSTRUMENTS
UCC27323, UCC27324, UCC27325, UCC37323, UCC37324, UCC37325
ZHCSIU2K – JUNE 2001 – REVISED NOVEMBER 2023

UCCx732x 双路 4A 峰值高速低侧电源 MOSFET 驱动器

1 特性

- Bi-CMOS 输出架构
- 可在米勒平坦区提供 ±4A 驱动电流
- 即使在低电源电压下也能实现恒流
- 并联输出以获得更高的驱动电流
- 采用 MSOP-PowerPAD™ 封装
- 与电源电压无关的 TTL/CMOS 输入
- 业界通用引脚排列

2 应用

- 开关电源供电
- 直流/直流转换器
- 太阳能逆变器、电机控制、不间断电源 (UPS)

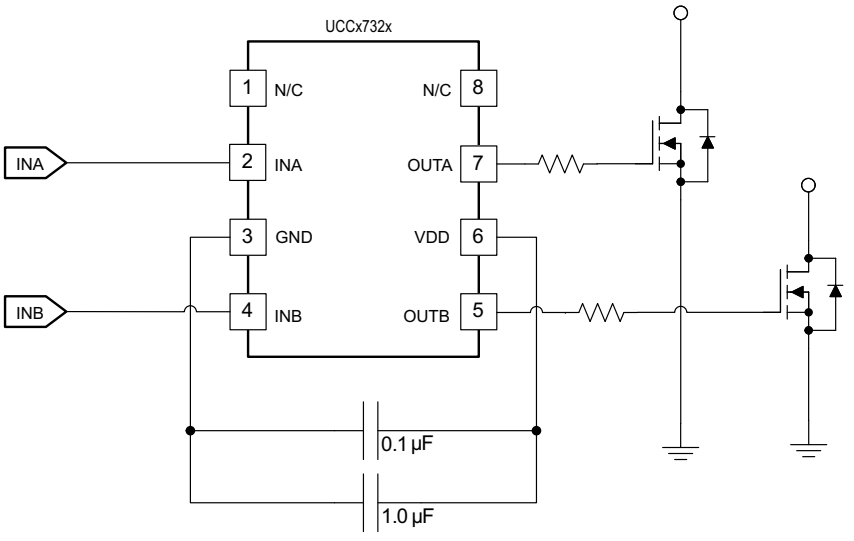
3 说明

UCC2732x 和 UCC3732x 系列高速双路 MOSFET 驱动器提供 4A 峰值拉电流和 4A 峰值灌电流，以在米勒平坦区域提供最需要的高效 MOSFET 驱动。独特的双极和 MOSFET 混合输出级并联，可在低电源电压下实现高效的拉电流和灌电流。提供了 3 个标准逻辑选项的组合 - 双路反相、双路同相、一路反相和一路同相。输入阈值基于 TTL 和 CMOS，和电源电压无关，并具有能提供极佳防噪性能的宽输入迟滞。UCC2732x 和 UCC3732x 系列提供标准 SOIC-8 (D) 以及热增强型 8 引脚 PowerPAD MSOP 封装 (DGN)，大大降低了热阻以改善长期可靠性。

器件信息

器件(1)	关键规格	封装
UCCx732x	-40C <= 温度 <= 125C 4.5V <= V_{DD} <= 15V 20ns/15ns - 1.8nF 负载时的上升/下降时间 35ns/25ns 上升/下降传播延迟	SOIC (8)：4.90mm × 3.91mm
		MSOP-PowerPAD (8)：3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



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简化版应用示意图

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Table of Contents

1 特性 1
2 应用 1
3 说明 1
4 Device Comparison Table 3
5 Pin Configuration and Functions 4
6 Specifications 5
6.1 Absolute Maximum Ratings 5
6.2 ESD Ratings 5
6.3 Recommended Operating Conditions 5
6.4 Thermal Information 5
6.5 Electrical Characteristics 7
6.6 Switching Characteristics 7
6.7 Typical Characteristics 9
7 Detailed Description 10
7.1 Overview 10
7.2 Functional Block Diagram 10
7.3 Feature Description 10
7.4 Device Functional Modes 11
8 Application and Implementation 12
8.1 Application Information 12
8.2 Typical Application 13
9 Power Supply Recommendations 17
10 Layout 18
10.1 Layout Guidelines 18
10.2 Layout Example 18
10.3 Thermal Considerations 19
11 Device and Documentation Support 20
11.1 Device Support 20
11.2 Documentation Support 20
11.3 接收文档更新通知 20
11.4 支持资源 20
11.5 Trademarks 20
11.6 静电放电警告 20
11.7 术语表 20
12 Revision History 21
13 Mechanical, Packaging, and Orderable Information 21

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4 Device Comparison Table

OUTPUT CONFIGURATION	TEMPERATURE RANGE $T_A = T_J$	PACKAGED DEVICES(1)		
		SOIC-8 (D)	MSOP-8 PowerPAD (DGN) (2)	PDIP-8 (P)
Dual inverting	–40°C to +125°C	UCC27323D	UCC27323DGN	UCC27323P
	0°C to +70°C	UCC37323D	UCC37323DGN	UCC37323P
Dual noninverting	–40°C to +125°C	UCC27324D	UCC27324DGN	UCC27324P
	0°C to +70°C	UCC37324D	UCC37324DGN	UCC37324P
One inverting, one noninverting	–40°C to +125°C	UCC27325D	UCC27325DGN	UCC27325P
	0°C to +70°C	UCC37325D	UCC37325DGN	UCC37325P

(1) D (SOIC-8) and DGN (PowerPAD-MSOP) packages are available taped and reeled. Add R suffix to device type (for example UCC27323DR, UCC27324DGNR) to order quantities of 2,500 devices per reel for D or 1,000 devices per reel for DGN package.
(2) The PowerPAD is not directly connected to any leads of the package. However, the PowerPAD is electrically and thermally connected to the substrate which is the ground of the device.

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5 Pin Configuration and Functions

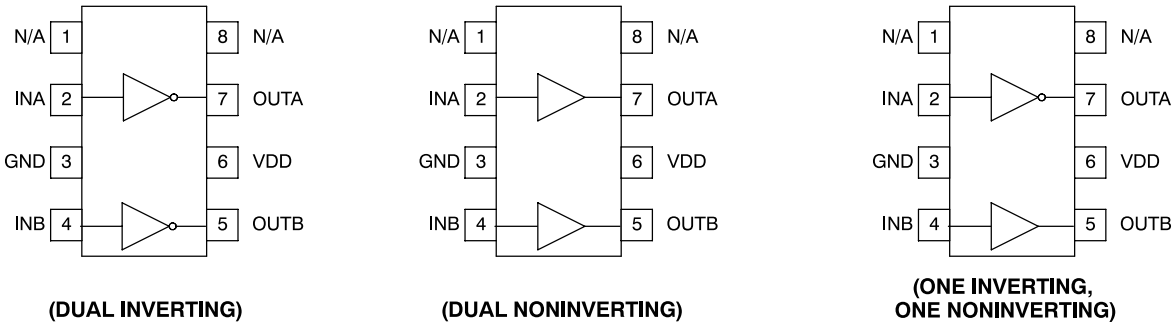


图 5-1. D, DGN Package 8-Pin SOIC, MSOP With PowerPAD Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	3	—	**Common ground**: This ground should be connected very closely to the source of the power MOSFET which the driver is driving.
INA	2	I	**Input A**: Input signal of the A driver which has logic compatible threshold and hysteresis. If not used, this input must be tied to either VDD or GND; it must not be left floating.
INB	4	I	**Input B**: Input signal of the A driver which has logic compatible threshold and hysteresis. If not used, this input must be tied to either VDD or GND; it must not be left floating.
N/C	1	—	**No Internal Connection**
N/C	8	—	**No Internal Connection**
OUTA	7	O	**Driver output A**: The output stage is capable of providing 4-A drive current to the gate of a power MOSFET.
OUTB	5	O	**Driver output B**: The output stage is capable of providing 4-A drive current to the gate of a power MOSFET.
VDD	6	I	**Supply**: Supply voltage and the power input connection for this device.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
	Analog input voltage (INA, INB)		– 0.3 to V_{DD} + 0.3 V	not to exceed 16	V
	Output body diode DC current (OUTA, OUTB)			0.2	A
I_{OUT_DC}	Output current (OUTA, OUTB)	DC		0.2	
I_{OUT_PULSED}		Pulsed (0.5 µs)		4.5	
	Output voltage (OUTA, OUTB)			16	V
V_{DD}	Supply voltage		– 0.3	16	V
T_J	Junction operating temperature		– 55	150	°C
T_{stg}	Storage temperature		– 65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Supply voltage		4.5		15	V
	Input voltage		0		15	V
	Operating junction temperature	UCC2732x	– 40		125	°C
		UCC3732x	0		70	°C

6.4 Thermal Information

THERMAL METRIC(1)		UCCx732x			UNIT
		D (SOIC)	DGN (MSOP With PowerPAD)	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.3	56.6	55.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.2	52.8	45.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.3	32.6	32.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.2	1.8	23	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46.8	32.3	32.5	°C/W

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THERMAL METRIC[1]		UCCx732x			UNIT
		D (SOIC)	DGN (MSOP With PowerPAD)	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	5.9	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

V_{DD} = 4.5 to 15 V, T_A = T_J (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT (INA, INB)							
V_{IN_H}	Logic 1 input threshold			1.6	2.2	2.5	V
V_{IN_L}	Logic 0 input threshold			0.8	1.2	1.5	V
	Input current		0 V ≤ V_{IN} ≤ V_{DD}	–10		10	µA
OUTPUT (OUTA, OUTB)							
	Output current		V_{DD} = 14 V(1)		4		A
R_{OH}	Output resistance high		I_{OUT} = –10 mA, (2)		0.6	1.5	Ω
R_{OL}	Output resistance low		I_{OUT} = 10 mA, (2)		0.4	1	Ω
OVERALL							
I_{DD}	Static Operating Current	UCCx7323	INA = 0 V, INB = 0 V		300	450	µA
			INA = 0 V, INB = HIGH		300	450	
			INA = HIGH, INB = 0 V		300	450	
			INA = HIGH, INB = HIGH		300	450	
		UCCx7324	INA = 0 V, INB = 0 V		2	50	
			INA = 0 V, INB = HIGH		300	450	
			INA = HIGH, INB = 0 V		300	450	
			INA = HIGH, INB = HIGH		600	750	
		UCCx7325	INA = 0 V, INB = 0 V		150	300	
			INA = 0 V, INB = HIGH		450	600	
			INA = HIGH, INB = 0 V		150	300	
			INA = HIGH, INB = HIGH		450	600	

(1) Parameter not tested in production
(2) Output pullup resistance is a DC measurement that measures resistance of PMOS structure only, not N-channel structure.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_R	Rise time (OUTA, OUTB)	C_{LOAD} = 1.8 nF, see 图 6-1		20	40	ns
T_F	Fall time (OUTA, OUTB)	C_{LOAD} = 1.8 nF, see 图 6-1		15	40	ns
T_{D1}	Delay, IN rising (IN to OUT)	C_{LOAD} = 1.8 nF, see 图 6-1		25	40	ns
T_{D2}	Delay, IN falling (IN to OUT)	C_{LOAD} = 1.8 nF, see 图 6-1		35	35	ns

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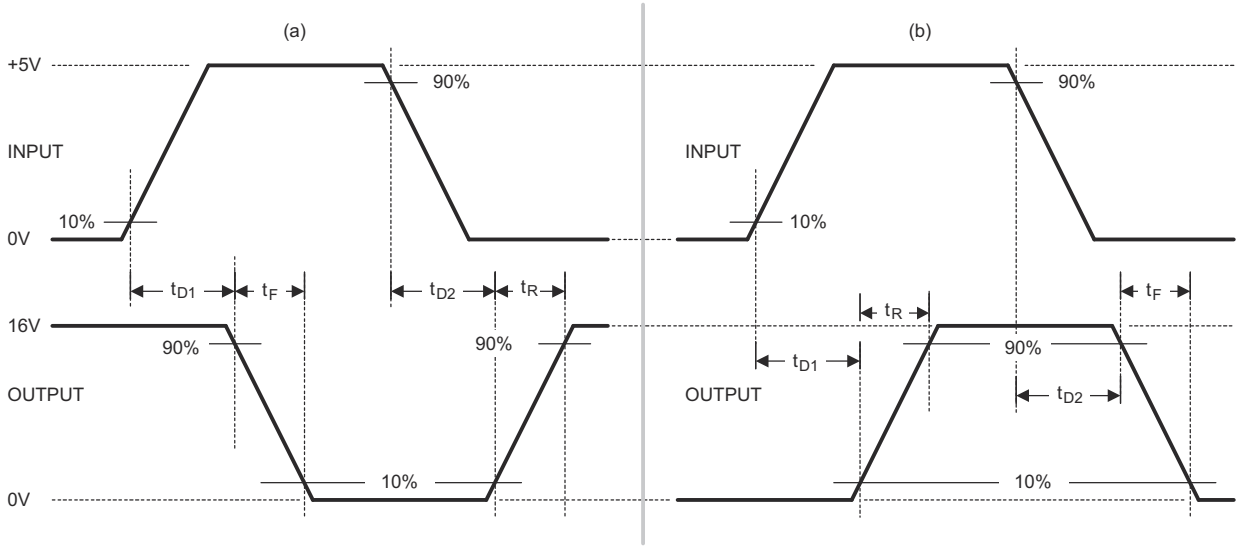


图 6-1. Switching Waveforms for (a) Inverting Driver and (b) Noninverting Driver

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6.7 Typical Characteristics

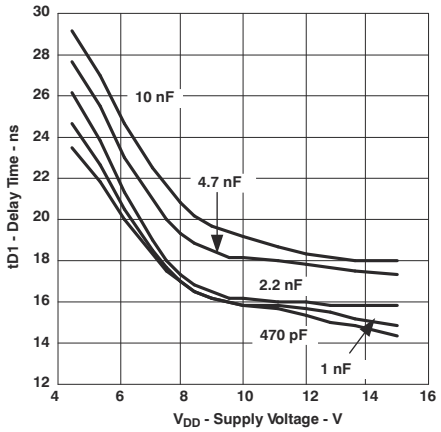


图 6-2. Delay Time (t_{D1}) vs Supply Voltage

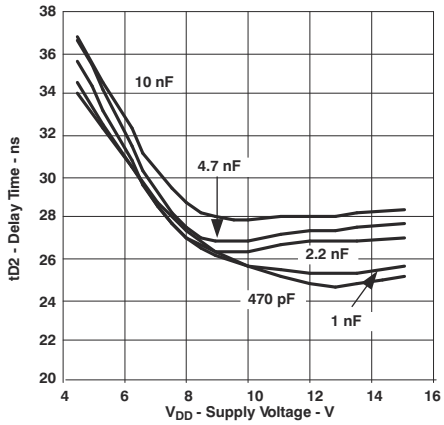


图 6-3. Delay Time (t_{D2}) vs Supply Voltage

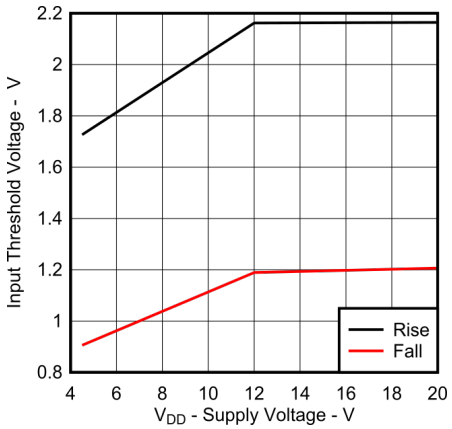


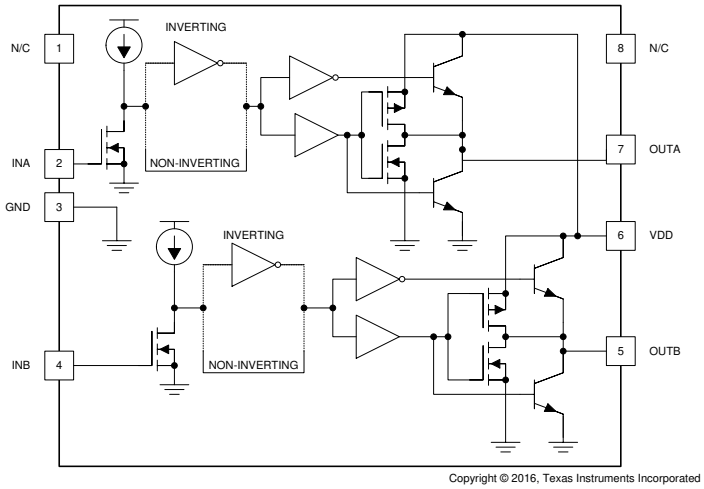
图 6-4. Input Threshold vs Supply Voltage

7 Detailed Description

7.1 Overview

The UCC2732x and UCC3732x family of high-speed dual MOSFET drivers can deliver large peak currents into capacitive loads. Three standard logic options are offered – dual-inverting, dual-noninverting and one-inverting and one-noninverting driver. Using a design that inherently minimizes shoot-through current, these drivers deliver 4A of current where it is needed most at the Miller plateau region during the MOSFET switching transition. A unique Bipolar and MOSFET hybrid output stage in parallel also allows efficient current sourcing and sinking at low supply voltages.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Input Stage

The input thresholds have a 3.3-V logic sensitivity over the full range of V_{DD} voltage; yet it is equally compatible with 0 V to V_{DD} signals.

The inputs of UCC2732x and UCC3732x family of drivers are designed to withstand 500-mA reverse current without either damage to the IC for logic upset. The input stage of each driver must be driven by a signal with a short rise or fall time. This condition is satisfied in typical power-supply applications, where the input signals are provided by a PWM controller or logic gates with fast transition times (<200 ns). The input stages to the drivers function as a digital gate, and are not intended for applications where a slow-changing input voltage is used to generate a switching output when the logic threshold of the input section is reached. While this may not be harmful to the driver, the output of the driver may switch repeatedly at a high frequency.

Users should not attempt to shape the input signals to the driver in an attempt to slow down (or delay) the signal at the output. If limited rise or fall times to the power device is desired, an external resistance can be added between the output of the driver and the load device, which is generally a power MOSFET gate. The external resistor may also help remove power dissipation from the device package, as discussed in (see *节 10.3*).

Importantly, input signal of the two channels, INA and INB, which has logic compatible threshold and hysteresis. If not used, INA and INB must be tied to either VDD or GND; it must not be left floating.

7.3.2 Output Stage

Inverting outputs of the UCCx7323 and OUTA of the UCCx7325 are intended to drive external P-channel MOSFETs. Noninverting outputs of the UCCx7324 and OUTB of the UCCx7325 are intended to drive external N-Channel MOSFETs.

Each output stage is capable of supplying ±4-A peak current pulses and swings to both VDD and GND. The pullup and pulldown circuits of the driver are constructed of bipolar and MOSFET transistors in parallel. The

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peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{DS(on)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor. Each output stage also provides a very low impedance to overshoot and undershoot due to the body diode of the external MOSFET.

This means that in many cases, external-Schottky-clamp diodes are not required. The UCCx732x family delivers 4 A of gate drive where it is most needed during the MOSFET switching transition – at the Miller plateau region – providing improved efficiency gains. A unique Bipolar and MOSFET hybrid output stage in parallel also allows efficient current sourcing at low supply voltages.

7.4 Device Functional Modes

With VDD power supply in the range of 4.5 V to 15 V, the output stage is dependent on the states of the HI and LI pins. 表 7-1 shows the UCCx732x truth table.

表 7-1. Input and Output Table

INPUTS (VIN_L, VIN_H)		UCC37323x		UCC37324x		UCC37325x	
INA	INB	OUTA	OUTB	OUTA	OUTB	OUTA	OUTB
L	L	H	H	L	L	H	L
L	H	H	L	L	H	H	H
H	L	L	H	H	L	L	L
H	H	L	L	H	H	L	H

Importantly, if INA and INB are not used, they must be tied to either VDD or GND; it must not be left floating.

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8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

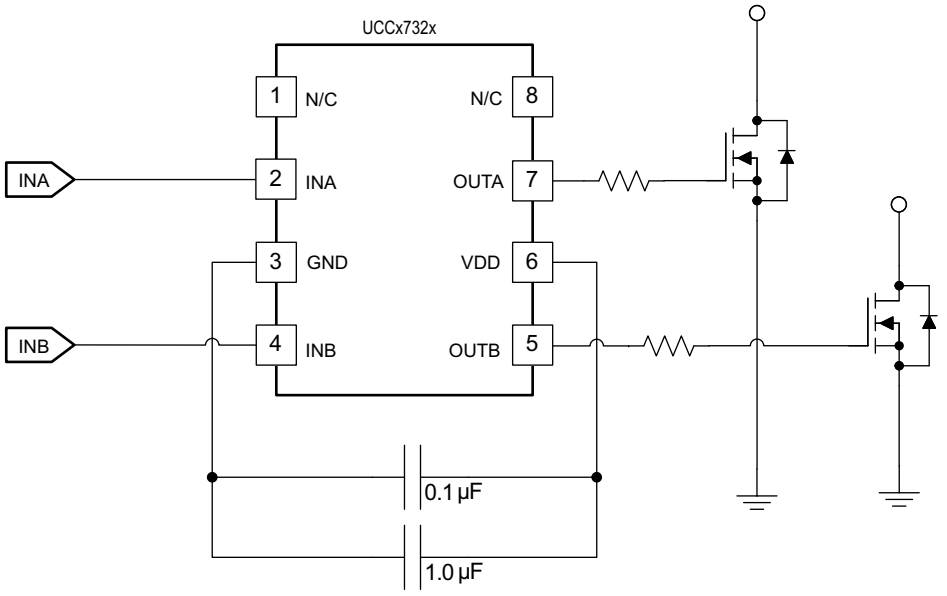
8.1 Application Information

High-frequency power supplies often require high-speed, high-current drivers such as the UCCx732x family. A leading application is the needed to provide a high-power buffer stage between the PWM output of the control IC and the gates of the primary power MOSFET or IGBT switching devices. In other cases, the driver IC is used to drive the power-device gates through a drive transformer. Synchronous rectification supplies are also needed to simultaneously drive multiple devices which presents an extremely large load to the control circuitry.

Driver ICs are used when having the primary PWM regulator IC directly drive the switching devices for one or more reasons is not feasible. The PWMIC does not have the brute drive capability required for the intended switching MOSFET, limiting the switching performance in the application. In other cases there may be a desire to minimize the effect of high-frequency switching noise by placing the high current driver physically close to the load. Also, newer ICs that target the highest operating frequencies do not incorporate onboard gate drivers at all. Their PWM outputs are only intended to drive the high impedance input to a driver such as the UCCx732x. Finally, the control IC is under thermal stress due to power dissipation, and an external driver helps by moving the heat from the controller to an external package.

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8.2 Typical Application



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图 8-1. UCCx732x Driving Two Independent MOSFETs

8.2.1 Design Requirements

To select proper device from UCCx732x family, TI recommends first checking the appropriate logic for the outputs. UCCx7323 has dual inverting outputs; UCCx7324 has dual noninverting outputs; UCCx7325 have inverting channel A and noninverting channel B. Moreover, some design considerations must be evaluated first in order to make the most appropriate selection. Among these considerations are VDD, drive current, and power dissipation.

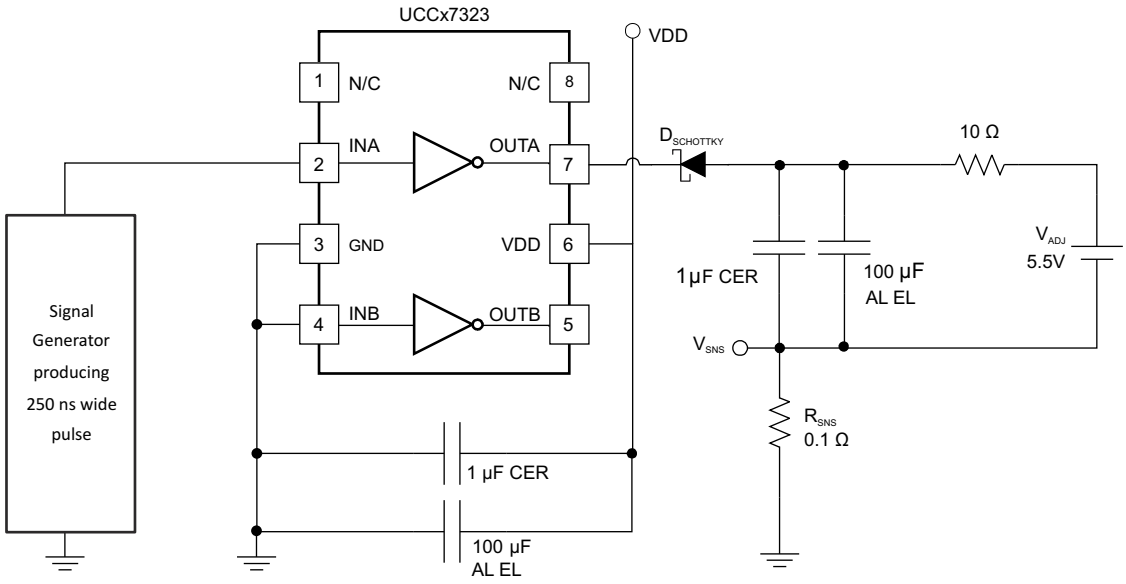
8.2.2 Detailed Design Procedure

8.2.2.1 Source/Sink Capabilities During Miller Plateau

Large power MOSFETs present a large load to the control circuitry. Proper drive is required for efficient, reliable operation. The UCCx732x drivers have been optimized to provide maximum drive to a power MOSFET during the Miller plateau region of the switching transition. This interval occurs while the drain voltage is swinging between the voltage levels dictated by the power topology, requiring the charging/discharging of the drain-gate capacitance with current supplied or removed by the driver device [1].

Two circuits are used to test the current capabilities of the UCCx732x driver. In each case external circuitry is added to clamp the output near 5 V while the IC is sinking or sourcing current. An input pulse of 250 ns is applied at a frequency of 1 kHz in the proper polarity for the respective test. In each test there is a transient period where the current peaked up and then settled down to a steady-state value. The noted current measurements are made at a time of 200 ns after the input pulse is applied, after the initial transient. [1]

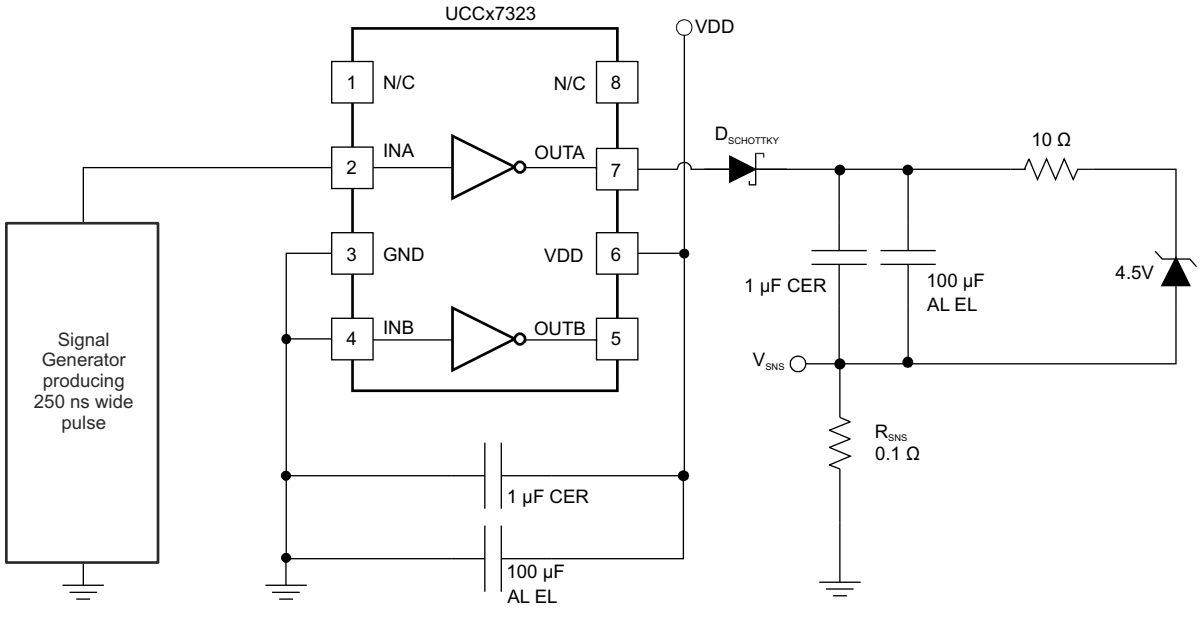
The first circuit in 图 8-2 is used to verify the current sink capability when the output of the driver is clamped around 5 V, a typical value of gate-source voltage during the Miller plateau region. The UCCx7323 is found to sink 4.5 A at VDD = 15 V and 4.28 A at VDD = 12 V.



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图 8-2. Current Sink Capability Test

The circuit shown in 图 8-3 is used to test the current source capability with the output clamped to around 5 V with a string of Zener diodes. The UCCx7323 is found to source 4.8 A at VDD = 15 V and 3.7 A at VDD = 12 V.



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图 8-3. Current Source Capability Test

8.2.2.2 Parallel Outputs

The A and B drivers may be combined into a single driver by connecting the INA/INB inputs together as close to the IC as possible, and the OUTA/OUTB outputs ties together if the external gate drive resistor is not used. In some cases where the external gate drive resistor is used, Ti recommends that the resistor can be equally split in OUTA and OUTB respectively to reduce the parasitic inductance induce unbalance between two channels, as show in 图 8-4.

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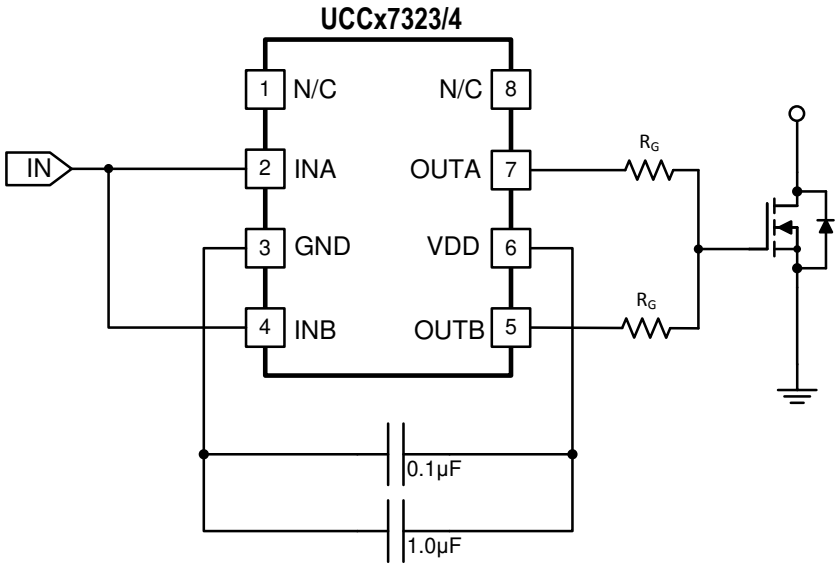


图 8-4. Parallel Operation of UCCx7323 and UCCx7324

Important consideration about paralleling two channels for UCCx7323/4 include: 1) INA and INB should be shorted in PCB layout as close to the device as possible, as well as for OUTA and OUTB, in which condition PCB layout parasitic mismatching between two channels could be minimized. 2) INA/B input slope signal should be fast enough to avoid mismatched V_{IN_H}/V_{IN_L}, t_{d1}/t_{d2} between channel-A and channel-B. TI recommends having input signal slope faster than 20 V/us.

8.2.2.3 VDD

Although quiescent VDD current is very low, total supply current will be higher, depending on OUTA and OUTB current and the programmed oscillator frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_g), average OUT current can be calculated using 方程式 1.

$$I_{OUT} = Q_g \times f \tag{1}$$

where

- f is frequency

For the best high-speed circuit performance, two VDD bypass capacitors are recommended to prevent noise problems. The use of surface mount components is highly recommended. A 0.1-µF ceramic capacitor should be located closest to the VDD to ground connection. In addition, a larger capacitor (such as 1 µF and above) with relatively low ESR should be connected in parallel, to help deliver the high current peaks to the load. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels in the driver application.

8.2.2.4 Driver Current and Power Requirements

The UCCx732x family of drivers is capable of delivering 4 A of current to a MOSFET gate for a period of tens of nanoseconds. High peak current is required to turn the device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device. A MOSFET is used in this discussion because it is the most common type of switching device used in high-frequency power conversion equipment.

Reference [1] and reference [2] discuss the current required to drive a power MOSFET and other capacitive-input switching devices. Reference [2] includes information on the previous generation of bipolar IC gate drivers.

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When a driver IC is tested with a discrete, capacitive load, it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by 方程式 2.

$$E = ½CV^2 \quad (2)$$

where

- C is the load capacitor
- V is the bias voltage feeding the driver

There is an equal amount of energy transferred to ground when the capacitor is discharged. This leads to a power loss given by 方程式 3.

$$P = CV^2 \times f \quad (3)$$

where

- f is the switching frequency

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged. An actual example using the conditions of the previous gate drive waveform should help clarify this.

With V_{DD} = 12 V, C_{LOAD} = 10 nF, and f = 300 kHz, the power loss can be calculated as 方程式 4.

$$P = 10\ nF \times (12\ V)^2 \times (300\ kHz) = 0.432\ W \quad (4)$$

With a 12-V supply, this equates to a current of (see 方程式 5):

$$I = P/V = 0.432\ W / 12\ V = 36\ mA \quad (5)$$

The actual current measured from the supply was 0.037 A, and is very close to the predicted value. But, the I_{DD} current that is due to the IC internal consumption should be considered. With no load the IC current draw is 0.0027 A. Under this condition the output rise and fall times are faster than with a load. This could lead to an almost insignificant, yet measurable current due to cross-conduction in the output stages of the driver. However, these small current differences are buried in the high frequency switching spikes, and are beyond the measurement capabilities of a basic lab setup. The measured current with 10-nF load is reasonably close to that expected.

The switching load presented by a power MOSFET can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain of the device between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence $Q_g = C_{eff} \times V$ to provide 方程式 6 for power:

$$P = C \times V^2 \times f = V \times Q_g \times f \quad (6)$$

方程式 6 allows a power designer to calculate the bias power required to drive a specific MOSFET gate at a specific bias voltage and a specific switching frequency.

8.2.3 Application Curves

图 8-5 shows the circuit performance achievable with a single driver (half of the 8-pin IC) driving a 10-nF load. The input pulse width (not shown) is set to 300 ns to show both transitions in the output waveform. Note the

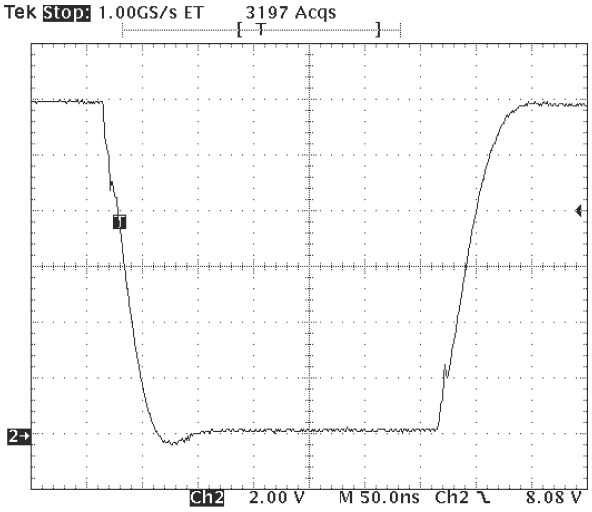
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linear rise and fall edges of the switching waveforms which is due to the constant output current characteristic of the driver as opposed to the resistive output impedance of traditional MOSFET-based gate drivers.

Sink and source currents of the driver are dependent upon the VDD value and the output capacitive load. The larger the VDD value, the higher the current capability; also, the larger the capacitive load, the higher the current sink and source capability.

Trace resistance and inductance, including wires and cables for testing, slows down the rise and fall times of the outputs; thus reducing the current capabilities of the driver.

To achieve higher current results, reduce resistance and inductance on the board as much as possible and increase the capacitive load value in order to swamp out the effect of inductance values.



C_L = 10 nF, C_L = 10 nF, VDD = 12 V

图 8-5. Rising and Falling Time of UCCx732x

9 Power Supply Recommendations

The recommended bias supply voltage range for UCCx732x is from 4.5 V to 15 V. The upper end of this range is driven by the 16 V absolute maximum voltage rating of the VDD. TI recommends keeping proper margin to allow for transient voltage spikes.

A local bypass capacitor must be placed between the VDD and GND pins. And this capacitor must be placed as close to the device as possible. A low ESR, ceramic surface mount capacitor is recommended. TI recommends using 2 capacitors across VDD and GND: a 100-nF ceramic surface-mount capacitor for high frequency filtering placed very close to VDD and GND pin, and another surface-mount capacitor, 220 nF to
10 µF, for IC bias requirements.

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10 Layout

10.1 Layout Guidelines

Optimum performance of high and low-side gate drivers cannot be achieved without taking due considerations during circuit board layout. The following points are emphasized:

1) Low ESR/ESL capacitors must be connected close to the IC between VDD and GND pins to support high peak currents drawn from VDD during the turn-on of the external MOSFETs.

2) Grounding considerations:

- The first priority in designing grounding connections is to confine the high peak currents that charge and discharge the MOSFET gates to a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminals of the MOSFETs. The gate driver must be placed as close as possible to the MOSFETs.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver is connected to the other circuit nodes such as source of power MOSFET and ground of PWM controller at one, single point. The connected paths must be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.

3) In noisy environments, tying inputs of an unused channel of the UCC2742x device to VDD or GND using short traces in order to ensure that the output is enabled and to prevent noise from causing malfunction in the output may be necessary.

4) Separate power traces and signal traces, such as output and input signals.

10.2 Layout Example

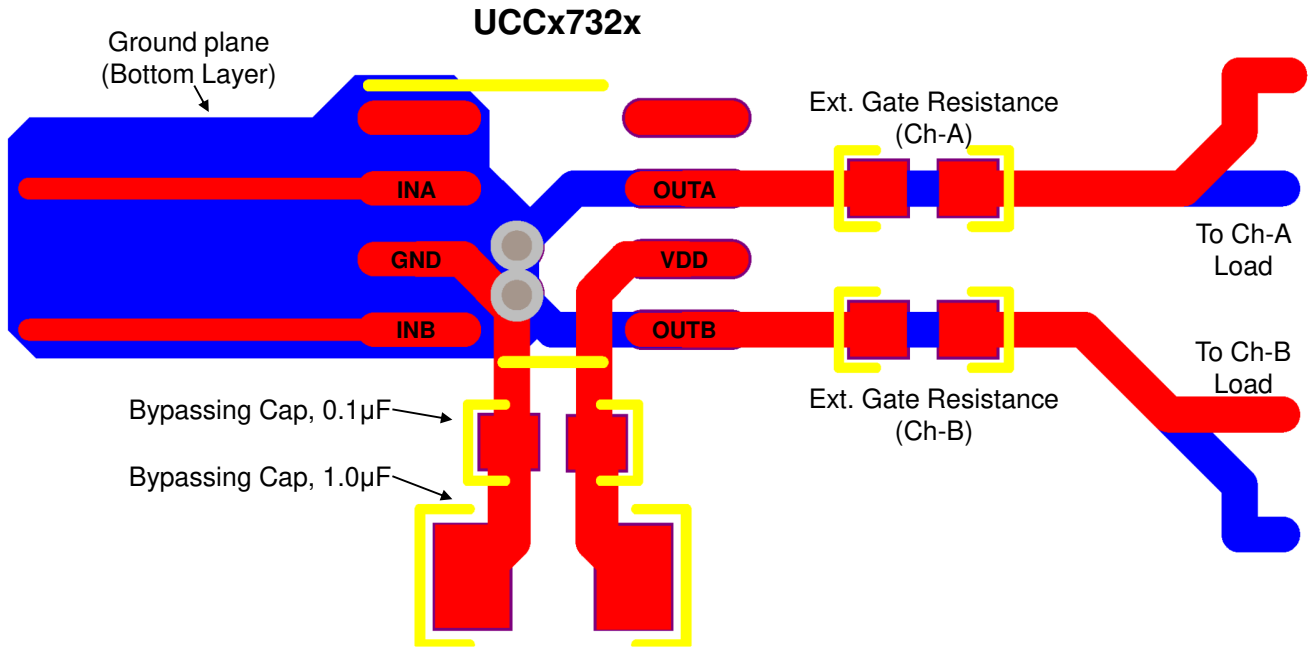


图 10-1. Recommended PCB Layout for UCCx732x

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10.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the IC package. In order for a power driver to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCCx732x family of drivers is available in three different packages to cover a range of application requirements.

The MSOP PowerPAD-8 (DGN) package significantly relieves this concern by offering an effective means of removing the heat from the semiconductor junction. As illustrated in reference [3], the PowerPAD packages offer a lead-frame die pad that is exposed at the base of the package. This pad is soldered to the copper on the PC board directly underneath the IC package, reducing the θ_{JC} down to 4.7°C/W. Data is presented in reference [3] to show that the power dissipation can be quadrupled in the PowerPAD configuration when compared to the standard packages. The PC board must be designed with thermal lands and thermal vias to complete the heat removal subsystem, as summarized in reference [4]. This design allows a significant improvement in heat sinking over that which is available in the D or P packages, and is shown to more than double the power capability of the D and P packages.

备注

The PowerPAD is not directly connected to any leads of the package. However, the PowerPad is electrically and thermally connected to the substrate which is the ground of the device.

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11 Device and Documentation Support

11.1 Device Support

11.1.1 第三方产品免责声明

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11.2 Documentation Support

11.2.1 Related Documentation

See the following for related documentation:

1. Power Supply Seminar SEM-1400 Topic 2, *Design And Application Guide For High Speed MOSFET Gate Drive Circuits* (SLUP133)
2. *Practical Considerations in High Performance MOSFET, IGBT and MCT Gate Drive Circuits* (SLUA105)
3. *PowerPad Thermally Enhanced Package* (SLMA002)
4. *PowerPAD Made Easy* (SLMA004)

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

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静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

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12 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision J (September 2018) to Revision K (November 2023)	Page
• Changed ESD HBM value from 4000 V to 2000 V in ESD Ratings	5
• Changed input threshold voltage values, deleted V_{OH} output high level and V_{OL} output low level, changed output resistance high and output resistance low values in Electrical Characteristics	7
• Changed 图 6-4	9

Changes from Revision I (July 2016) to Revision J (September 2018)	Page
• Changed NC description from "No connection: must be grounded” to “No Internal Connection"	4

Changes from Revision H (May 2013) to Revision I (July 2016)	Page
• 新增了 *ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实现* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分	1
• Deleted Power Dissipation rows from *Absolute Maximum Ratings*	5

Changes from Revision G (March 2010) to Revision H (May 2013)	Page
• Changed $D_{SCHOTTKY}$ diode direction and voltage of zener diode from 5.5 to 4.5 V in 图 8-3	13
• Added three paragraphs after first paragraph of *Operational Waveforms and Circuit Layout* section before 图 8-5	16

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC27323D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	27323
UCC27323DGN	Obsolete	Production	HVSSOP (DGN) | 8	-	-	Call TI	Call TI	-40 to 125	27323
UCC27323DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27323
UCC27323DGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27323
UCC27323DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27323
UCC27323DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27323
UCC27323P	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	UCC27323P
UCC27323P.A	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	UCC27323P
UCC27324D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	27324
UCC27324DGN	Obsolete	Production	HVSSOP (DGN) | 8	-	-	Call TI	Call TI	-40 to 125	27324
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UCC27324DGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27324
UCC27324DGNRG4	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27324
UCC27324DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27324
UCC27324DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27324
UCC27324DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27324
UCC27324P	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	UCC27324P
UCC27324P.A	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	UCC27324P
UCC27324PE4	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	UCC27324P
UCC27325D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	27325
UCC27325DGN	Obsolete	Production	HVSSOP (DGN) | 8	-	-	Call TI	Call TI	-40 to 125	27325
UCC27325DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27325
UCC27325DGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27325
UCC27325DGNRG4	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27325
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UCC27325DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27325
UCC27325DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27325
UCC27325DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27325
UCC27325DRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27325

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
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UCC27325P.A	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	UCC27325P
UCC27325PE4	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	UCC27325P
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UCC37323DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	37323
UCC37323DGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	37323
UCC37323DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	37323
UCC37323DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	37323
UCC37323P	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UCC37323P
UCC37323P.A	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UCC37323P
UCC37324D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	37324
UCC37324DGN	Obsolete	Production	HVSSOP (DGN) | 8	-	-	Call TI	Call TI	0 to 70	37324
UCC37324DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	37324
UCC37324DGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	37324
UCC37324DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	37324
UCC37324DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	37324
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UCC37324P.A	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UCC37324P
UCC37324PE4	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UCC37324P
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UCC37325DGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	37325
UCC37325DGNRG4	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	37325
UCC37325DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	37325
UCC37325DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	37325
UCC37325P	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UCC37325P
UCC37325P.A	NRND	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UCC37325P

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF UCC27324 :

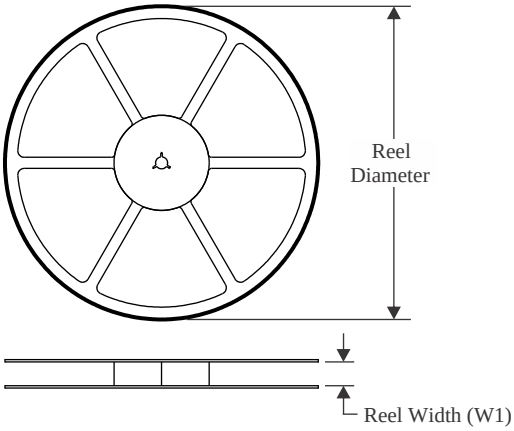
- Automotive : UCC27324-Q1

NOTE: Qualified Version Definitions:

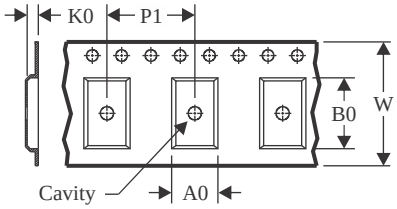
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

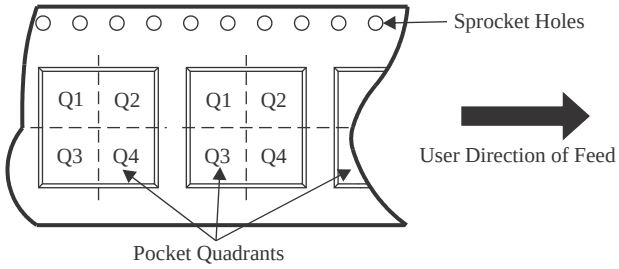


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

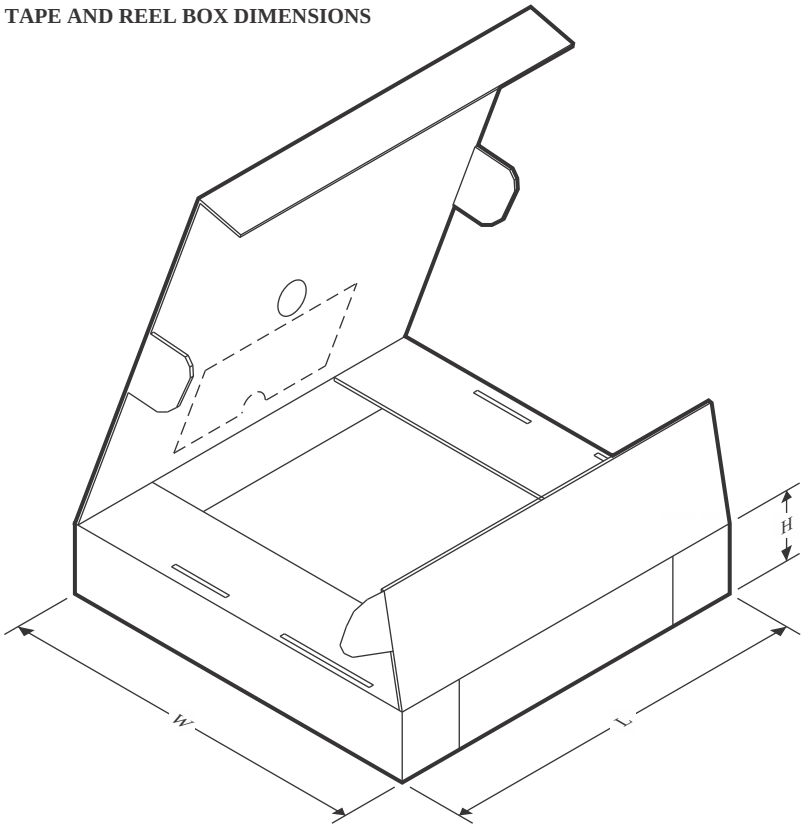


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27323DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27323DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27324DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27324DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27324DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27324DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27325DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27325DGNRG4	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27325DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27325DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC37323DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC37323DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC37323DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC37324DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC37324DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC37324DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC37325DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC37325DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC37325DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

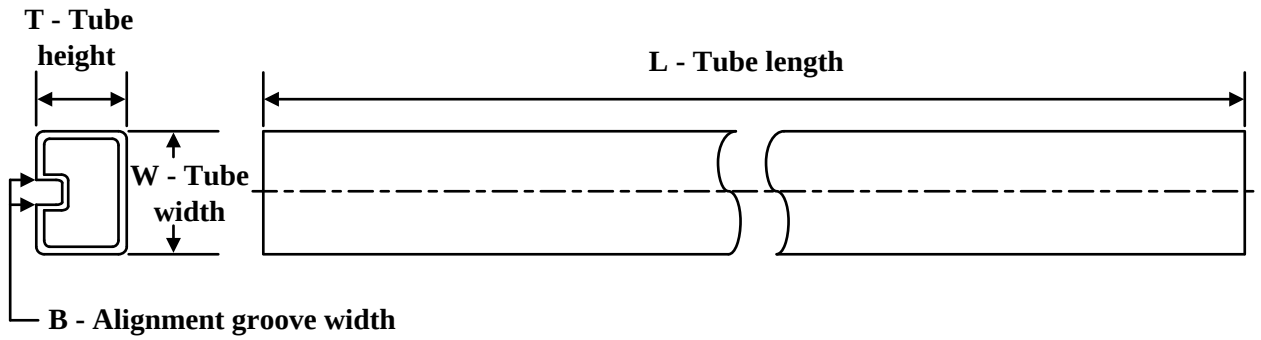


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27323DGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
UCC27323DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC27324DGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
UCC27324DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC27324DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC27324DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC27325DGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
UCC27325DGNRG4	HVSSOP	DGN	8	2500	353.0	353.0	32.0
UCC27325DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC27325DRG4	SOIC	D	8	2500	353.0	353.0	32.0
UCC37323DGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
UCC37323DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC37323DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC37324DGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
UCC37324DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC37324DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC37325DGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
UCC37325DR	SOIC	D	8	2500	340.5	338.1	20.6

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC37325DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC27323P	P	PDIP	8	50	506	13.97	11230	4.32
UCC27323P.A	P	PDIP	8	50	506	13.97	11230	4.32
UCC27324P	P	PDIP	8	50	506	13.97	11230	4.32
UCC27324P.A	P	PDIP	8	50	506	13.97	11230	4.32
UCC27324PE4	P	PDIP	8	50	506	13.97	11230	4.32
UCC27325P	P	PDIP	8	50	506	13.97	11230	4.32
UCC27325P.A	P	PDIP	8	50	506	13.97	11230	4.32
UCC27325PE4	P	PDIP	8	50	506	13.97	11230	4.32
UCC37323P	P	PDIP	8	50	506	13.97	11230	4.32
UCC37323P.A	P	PDIP	8	50	506	13.97	11230	4.32
UCC37324P	P	PDIP	8	50	506	13.97	11230	4.32
UCC37324P.A	P	PDIP	8	50	506	13.97	11230	4.32
UCC37324PE4	P	PDIP	8	50	506	13.97	11230	4.32
UCC37325P	P	PDIP	8	50	506	13.97	11230	4.32
UCC37325P.A	P	PDIP	8	50	506	13.97	11230	4.32

GENERIC PACKAGE VIEW

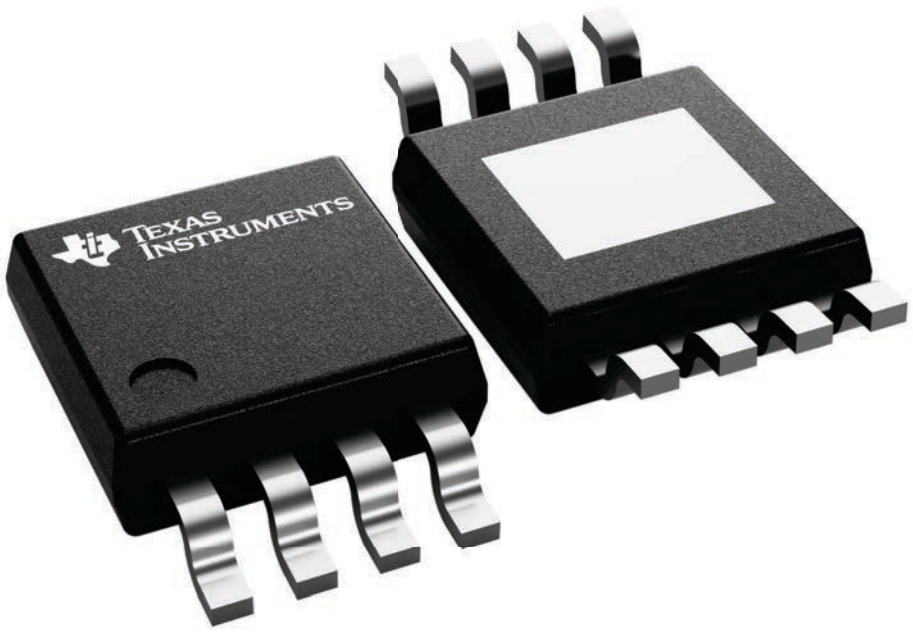
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

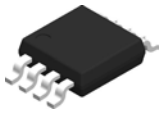
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B

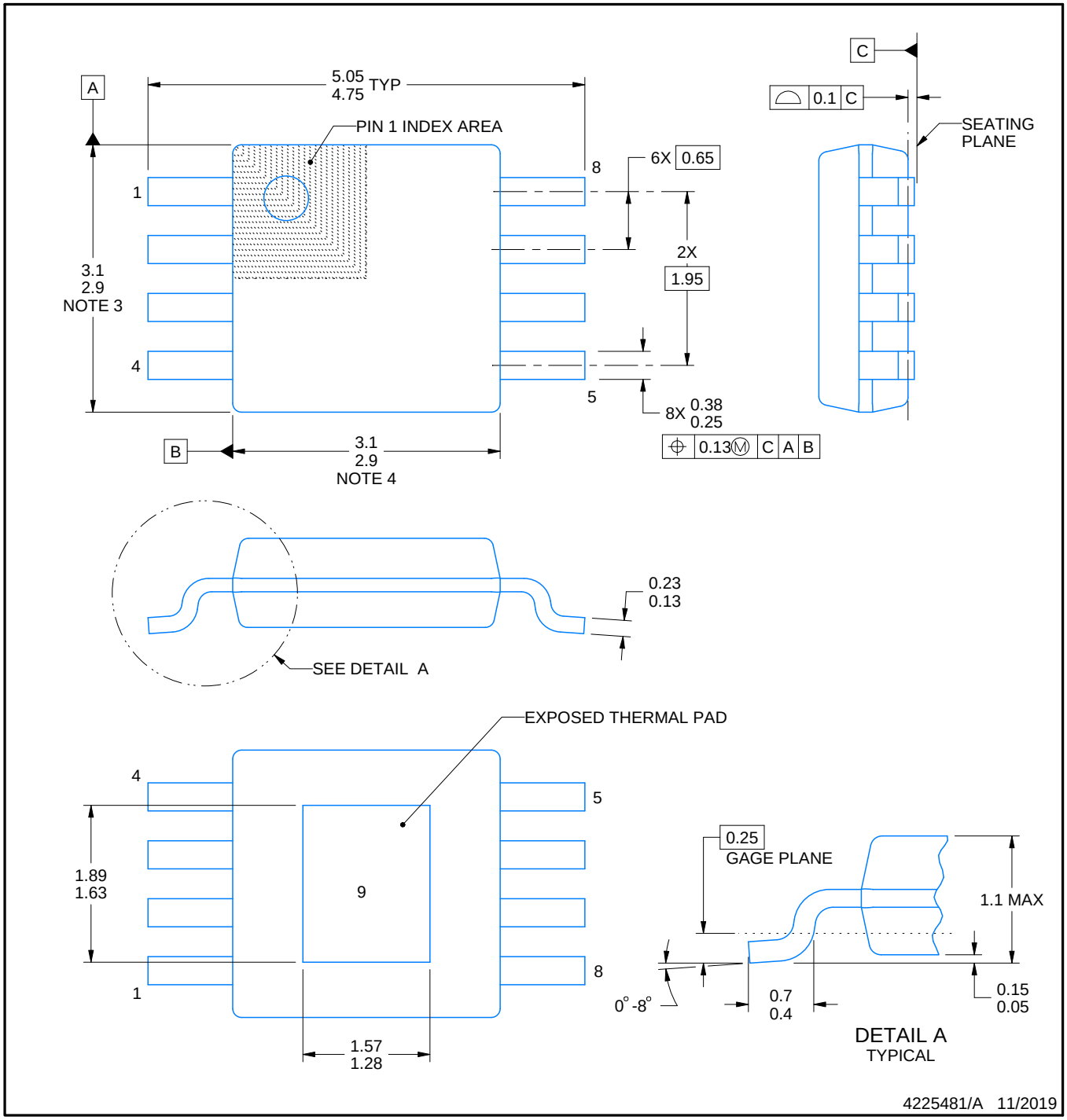
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

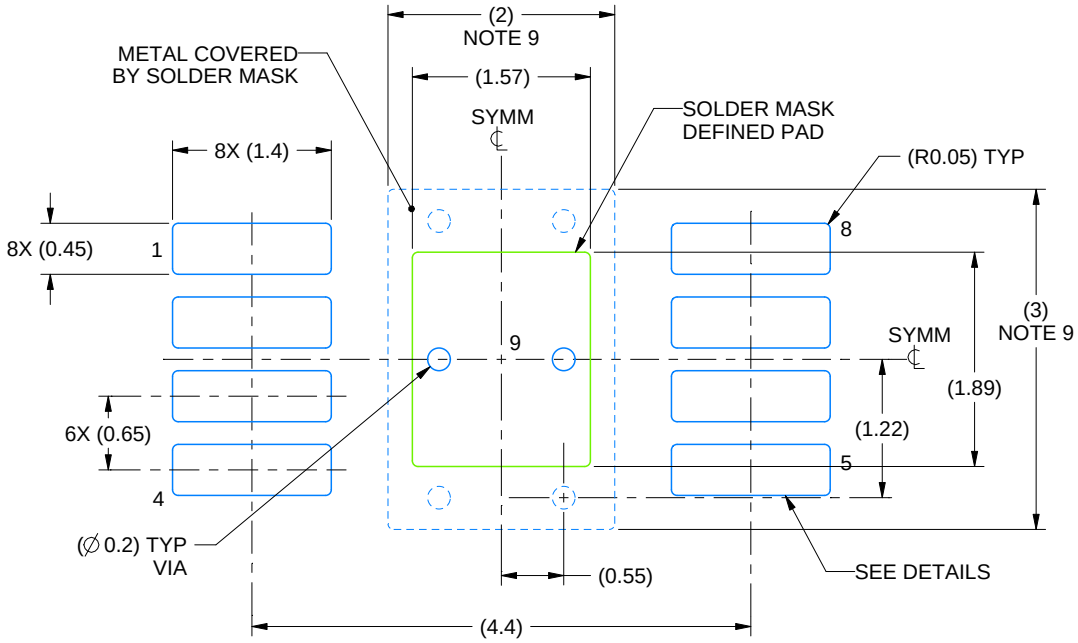
SMALL OUTLINE PACKAGE



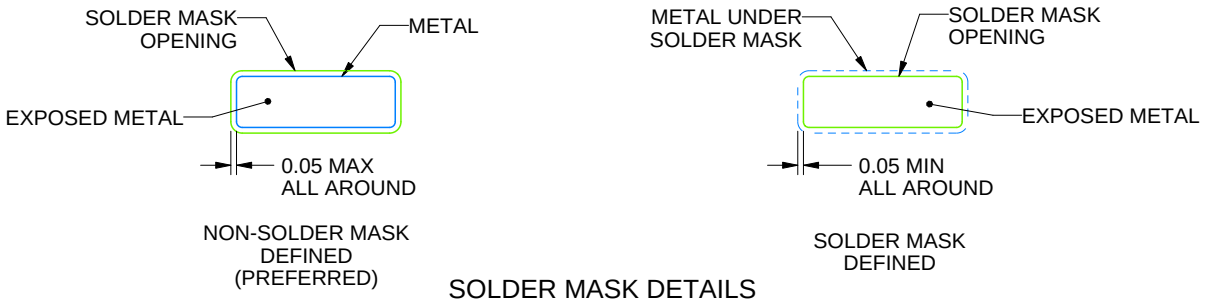
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

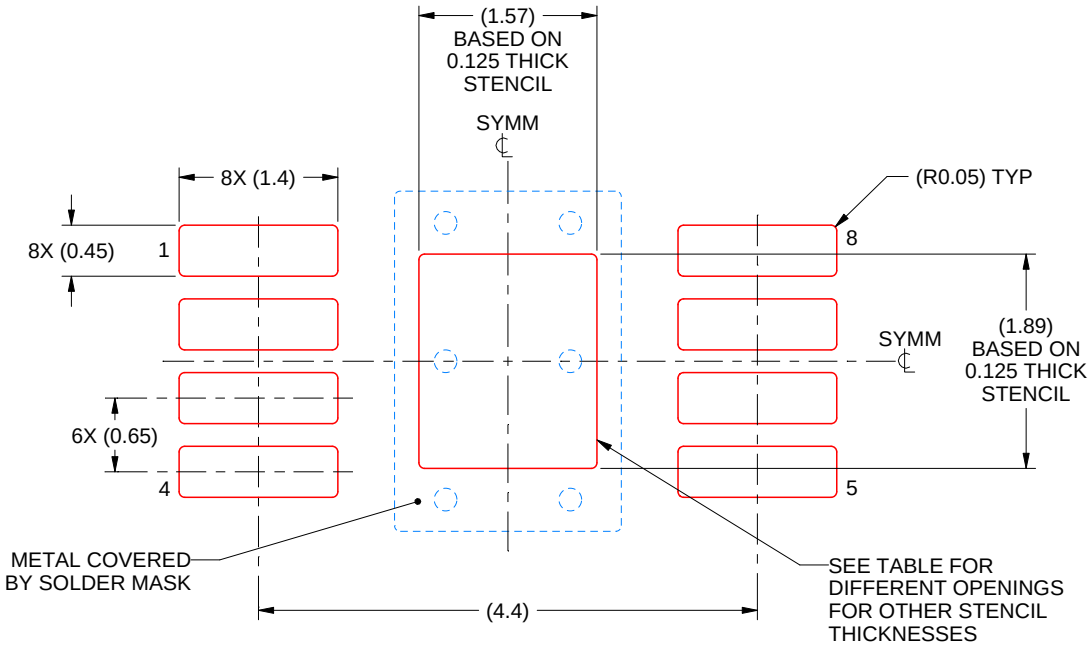


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

NOTES: (continued)

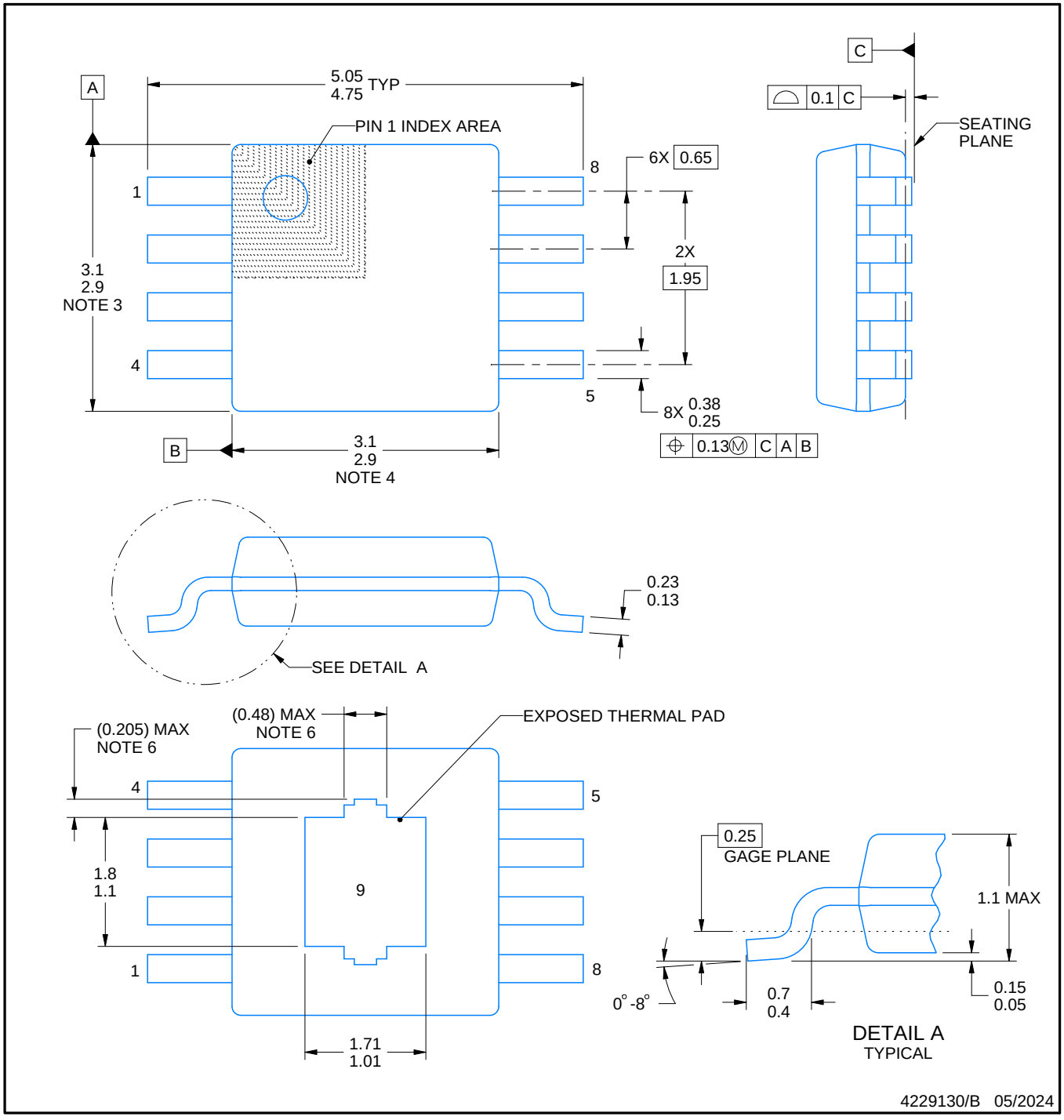
10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGN0008H

PowerPAD™ VSSOP - 1.1 mm max height

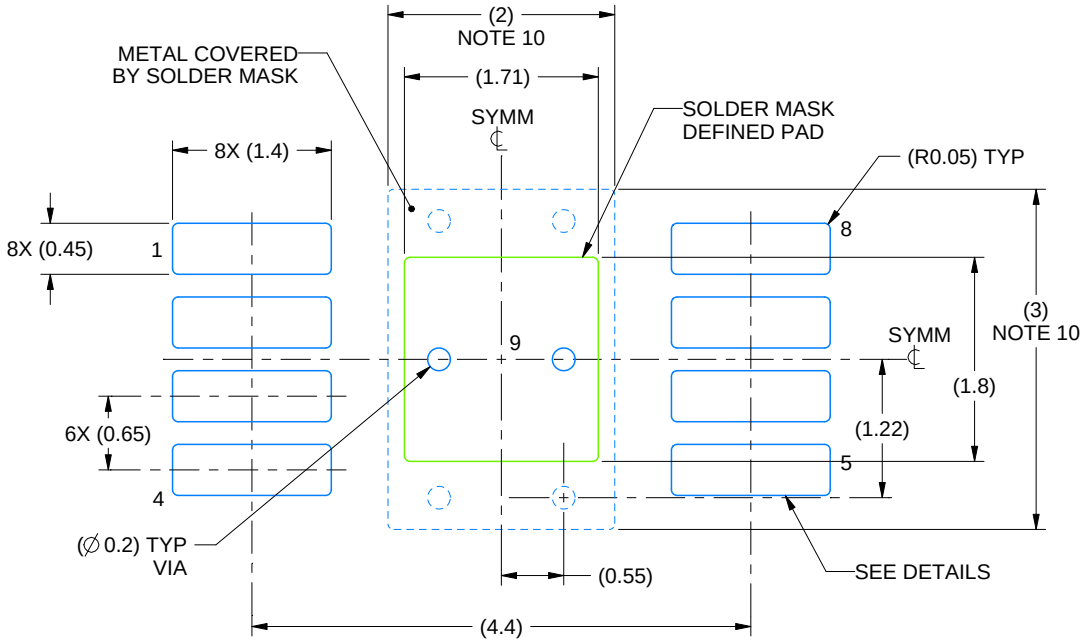
SMALL OUTLINE PACKAGE



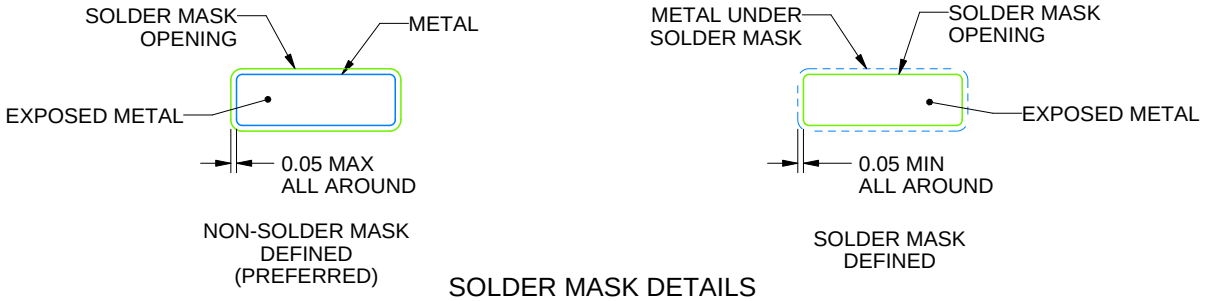
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

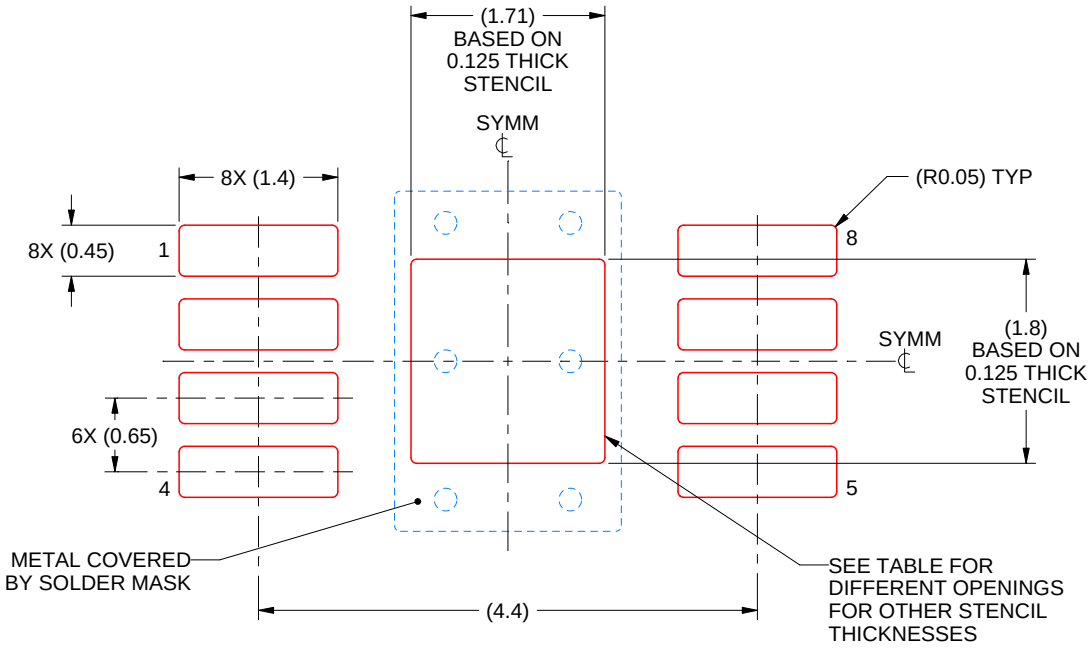


SOLDER MASK DETAILS

4229130/B 05/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



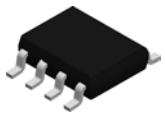
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.91 X 2.01
0.125	1.71 X 1.80 (SHOWN)
0.15	1.56 X 1.64
0.175	1.45 X 1.52

4229130/B 05/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

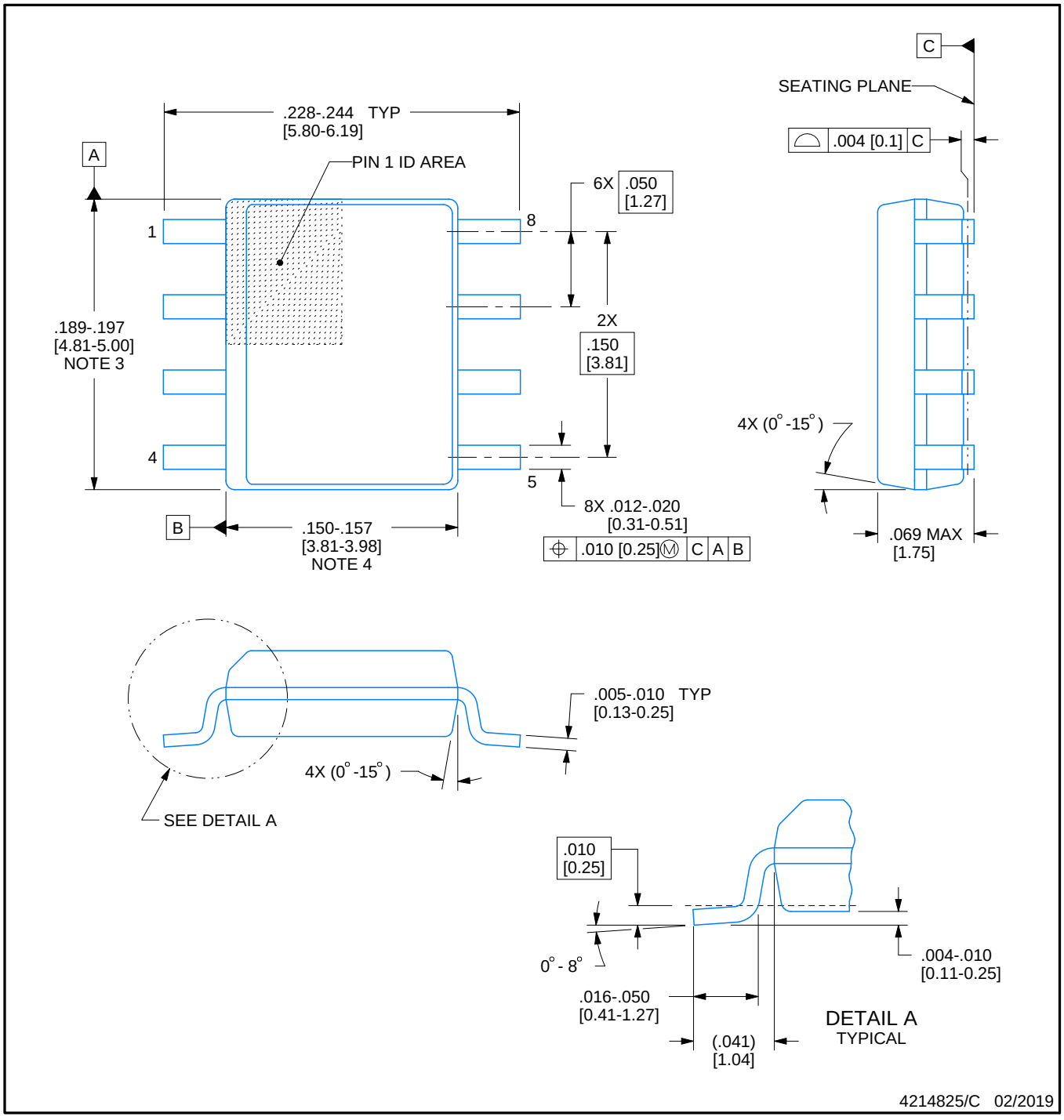


PACKAGE OUTLINE

D0008A

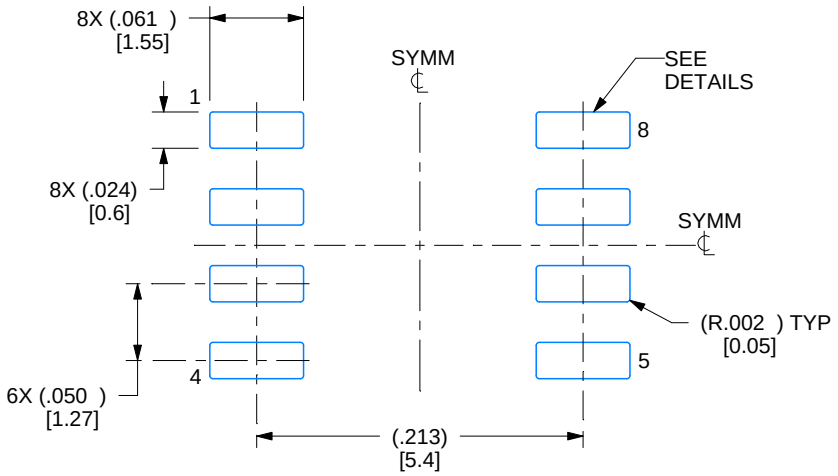
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

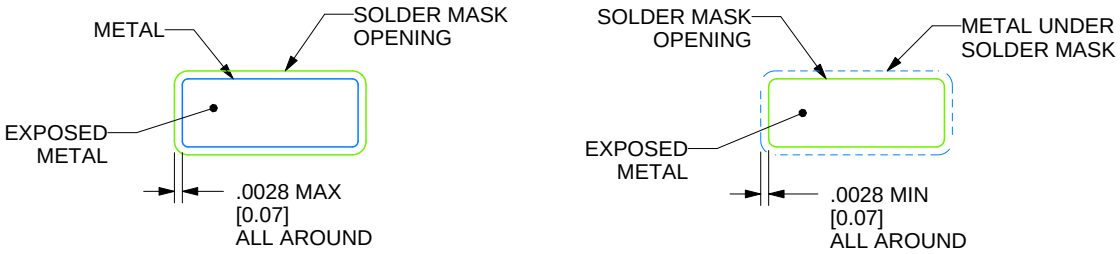


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

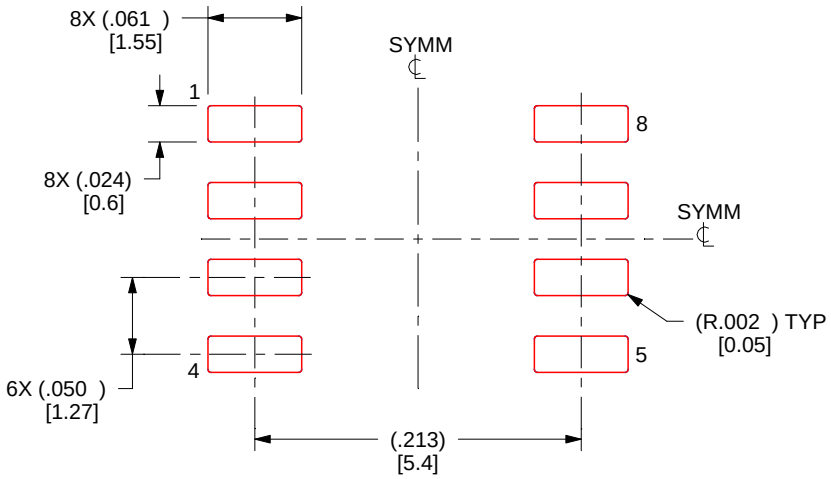
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



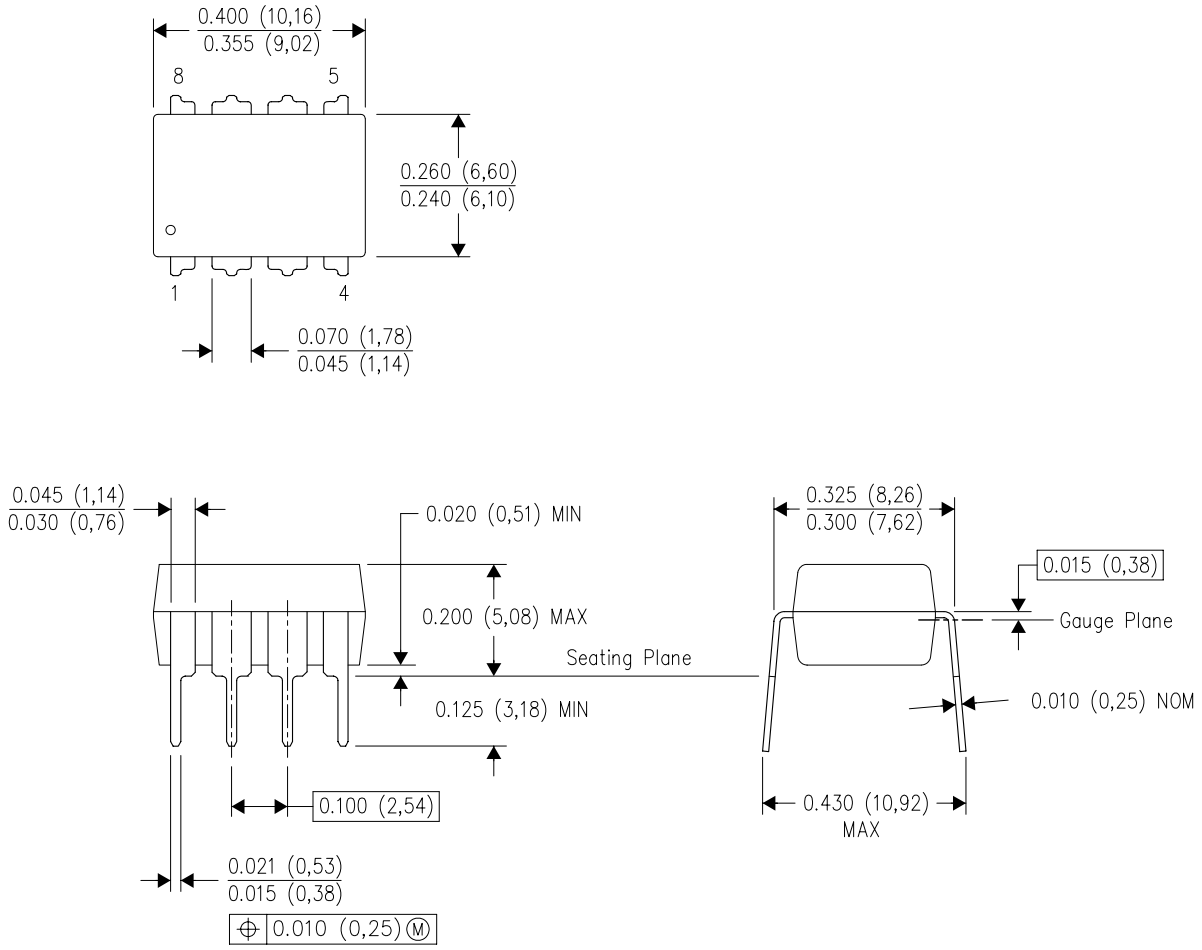
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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