### 特性

- 低电源电压范围：1.8V 至 3.6V
- 超低功耗
  - 运行模式：230 μA（在1 MHz 频率下），2.2 V
  - 待机模式：0.5μA
  - 关断模式（RAM 保持）：0.1μA
- 5 种节能模式
- 可在不到 1μs 的时间里超快速地从待机模式唤醒
- 16 位 RISC 架构，62.5ns 指令周期
- 基本时钟模块配置
  - 高达16 MHz 的内部频率，具有4 种校准频率
  - 内部超低功耗低频 (LF) 振荡器
  - 32-kHz 晶体
  - 外部数字时钟信号源
- 具有 3 个捕获/比较寄存器的两个 16 位 Timer_A
- 最多 24 个支持触感的 I/O 引脚

- 通用串行通信接口 (USCI)
  - 增强型 UART 可支持自动波特率检测 (LIN)
  - IrDA 编码器和解码器
  - 同步 SPI
  - I^C™
- 带内部基准、采样与保持及自动扫描功能的 10 位 200-ksp/s 模数 (A/D) 转换器（见 表 1）
- 欠压检测器
- 串行板上编程，无需从外部进行电压编程，利用安全熔丝实现可编程代码保护
- 具有两线制 JTA（SBW）接口的片载仿真逻辑电路
- 系列成员汇总于 表 1
- 封装选项
  - TSSOP：20 引脚，28 引脚
  - PDIP：20 引脚
  - QFN：32 引脚
- 如需了解完整的模块说明，请查阅 MSP430x2xx 系列用户指南（文献编号 SLAU144）

### 说明

德州仪器 (TI) MSP430 系列超低功耗微控制器包含多种器件，它们具有面向各种应用的不同外设集。这种架构与 5 种低功耗模式相组合，专为在便携式测量应用中延长电池的使用寿命而进行了优化。该器件具有一个强大的 16 位 RISC CPU、16 位寄存器和有助于获得最大编译效率的常数发生器。数字控制振荡器 (DCO) 可在不到 1μs 的时间里完成从低功耗模式至运行模式的唤醒。

MSP430G2x03 和 MSP430G2x33 系列是超低功耗混合信号微控制器，具有内置的 16 位计时器、最多 24 个支持触摸感测的 I/O 引脚、以及采用通用串行通信接口的内置通信能力。此外，MSP430G2x33 系列成员还具有一个 10 位 A/D 转换器。有关配置的详情请见 表 1。

典型应用包括低成本传感器系统，此类系统负责捕获模拟信号、将之转换为数字值、随后对数据进行处理以进行显示或传送至主机系统。

⚠️ 请务必注意，本数据表中可能包含产品可用性、标准保修、以及在关键应用的使用声明等信息。

PRODUCTION DATA:

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English Data Sheet: SLAS734D
表1. 提供的选项(1)(2)

<table>
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<tr>
<th>器件</th>
<th>BSL</th>
<th>EEM</th>
<th>闪存 (KB)</th>
<th>RAM (B)</th>
<th>Timer_A</th>
<th>10 通道</th>
<th>USCI A0/B0</th>
<th>时钟</th>
<th>I/O</th>
<th>封装类型</th>
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(1) 有关最新的封装和订购信息，请参阅本文档结尾的“封装选项附录”，或访问 TI 网站：www.ti.com。
(2) 封装图样、散热数据和符号可登录 www.ti.com/packaging 获取。
表 1. 提供的选项(1)(2) (接下页)

<table>
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<th>器件</th>
<th>BSL</th>
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<th>闪存 (KB)</th>
<th>RAM (B)</th>
<th>Timer_A</th>
<th>ADC</th>
<th>USCI A0/B0</th>
<th>时钟</th>
<th>I/O</th>
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(1) 提供的选项(1)(2) (接下页)
Device Pinout, MSP430G2x03 and MSP430G2x33, 20-Pin Devices, TSSOP and PDIP

NOTE: ADC10 is available on MSP430G2x33 devices only.

NOTE: The pulldown resistors of port P3 should be enabled by setting P3REN.x = 1.

Device Pinout, MSP430G2x03 and MSP430G2x33, 28-Pin Devices, TSSOP

NOTE: ADC10 is available on MSP430G2x33 devices only.
NOTE: ADC10 is available on MSP430G2x33 devices only.
NOTE: Port P3 is available on 28-pin and 32-pin devices only.

NOTE: Port P3 is available on 28-pin and 32-pin devices only.
<table>
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<tr>
<th>Terminal</th>
<th>Terminal No.</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>P1.0/</td>
<td>PW20, N20</td>
<td>General-purpose digital I/O pin</td>
</tr>
<tr>
<td>TAOCLK/</td>
<td>PW28</td>
<td>Timer0_A, clock signal TACLK input</td>
</tr>
<tr>
<td>ACLK/</td>
<td>RHB32</td>
<td>ACLK signal output</td>
</tr>
<tr>
<td>A0</td>
<td></td>
<td>ADC10 analog input A0&lt;sup&gt;(1)&lt;/sup&gt;</td>
</tr>
<tr>
<td>P1.1/</td>
<td>PW28</td>
<td>General-purpose digital I/O pin</td>
</tr>
<tr>
<td>TA0.0/</td>
<td>PW28</td>
<td>Timer0_A, capture: CCI0A input, compare: Out0 output / BSL transmit</td>
</tr>
<tr>
<td>UCA0RXD/</td>
<td>RHB32</td>
<td>USCI_A0 receive data input in UART mode</td>
</tr>
<tr>
<td>UCA0SOMI/</td>
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<td>USCI_A0 slave data out/master in SPI mode</td>
</tr>
<tr>
<td>A1</td>
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<td>ADC10 analog input A1&lt;sup&gt;(1)&lt;/sup&gt;</td>
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<td>P1.1/</td>
<td>PW28</td>
<td>General-purpose digital I/O pin</td>
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<td>TA0.1/</td>
<td>PW28</td>
<td>Timer0_A, capture: CCI1A input, compare: Out1 output</td>
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<td>UCA0TXD/</td>
<td>RHB32</td>
<td>USCI_A0 transmit data output in UART mode</td>
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<td>UCA0SIMO/</td>
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<td>USCI_A0 slave data in/master out in SPI mode</td>
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<td>ADC10 analog input A2&lt;sup&gt;(1)&lt;/sup&gt;</td>
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<td>P1.3/</td>
<td>PW28</td>
<td>General-purpose digital I/O pin</td>
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<td>ADC10CLK/</td>
<td>PW28</td>
<td>ADC10, conversion clock output&lt;sup&gt;(1)&lt;/sup&gt;</td>
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<td>A3/</td>
<td>PW28</td>
<td>ADC10 analog input A3&lt;sup&gt;(1)&lt;/sup&gt;</td>
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<td>VREF+/VREF-</td>
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<td>ADC10 negative reference voltage&lt;sup&gt;(1)&lt;/sup&gt;</td>
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<td>P1.4/</td>
<td>PW28</td>
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<td>SMCLK/</td>
<td>PW28</td>
<td>SMCLK signal output</td>
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<td>UCB0STE/</td>
<td>PW28</td>
<td>USCI_B0 slave transmit enable</td>
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<tr>
<td>UCA0CLK/</td>
<td>PW28</td>
<td>USCI_A0 clock input/output</td>
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<td>PW28</td>
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<td>VREF+/VREF+</td>
<td>PW28</td>
<td>ADC10 positive reference voltage&lt;sup&gt;(1)&lt;/sup&gt;</td>
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<td>TCK</td>
<td>PW28</td>
<td>JTAG test clock, input terminal for device programming and test</td>
</tr>
<tr>
<td>P1.5/</td>
<td>PW28</td>
<td>General-purpose digital I/O pin</td>
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<td>TA0.0/</td>
<td>PW28</td>
<td>Timer0_A, compare: Out0 output / BSL receive</td>
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<tr>
<td>UCB0CLK/</td>
<td>PW28</td>
<td>USCI_B0 clock input/output</td>
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<td>UCA0STE/</td>
<td>PW28</td>
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<td>JTAG test mode select, input terminal for device programming and test</td>
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<td>PW28</td>
<td>Timer0_A, compare: Out1 output</td>
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<td>A6/</td>
<td>PW28</td>
<td>ADC10 analog input A6&lt;sup&gt;(1)&lt;/sup&gt;</td>
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<td>USCI_B0 slave out/master in SPI mode,</td>
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<td>UCB0SCL/</td>
<td>PW28</td>
<td>USCI_B0 SCL I2C clock in I2C mode</td>
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<td>TDI/TCLK</td>
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<td>JTAG test data input or test clock input during programming and test</td>
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<td>P1.7/</td>
<td>PW28</td>
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<td>UCB0SIMO/</td>
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<td>PW28</td>
<td>JTAG test data output terminal or test data input during programming and test&lt;sup&gt;(2)&lt;/sup&gt;</td>
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<sup>(1)</sup> MSP430G2x33 devices only  
<sup>(2)</sup> TDO or TDI is selected via JTAG instruction.
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<td>XIN/TA0.1</td>
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<td>Input terminal of crystal oscillator General-purpose digital I/O pin Timer0_A, compare: Out1 output</td>
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<tr>
<td>P3.4/TA0.0</td>
<td>-, 15, 14</td>
<td>I/O</td>
<td>General-purpose digital I/O pin Timer0_A, compare: Out0 output</td>
</tr>
<tr>
<td>P3.5/TA0.1</td>
<td>-, 19, 18</td>
<td>I/O</td>
<td>General-purpose digital I/O pin Timer0_A, compare: Out1 output</td>
</tr>
<tr>
<td>P3.6/TA0.2</td>
<td>-, 20, 19</td>
<td>I/O</td>
<td>General-purpose digital I/O pin Timer0_A, compare: Out2 output</td>
</tr>
<tr>
<td>P3.7/TA1CLK</td>
<td>-, 21, 20</td>
<td>I/O</td>
<td>General-purpose digital I/O pin Timer1_A, clock signal TACLK input</td>
</tr>
<tr>
<td>RST/NMI/SBWTDOI</td>
<td>16, 24, 23</td>
<td></td>
<td>Reset Nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test</td>
</tr>
<tr>
<td>TEST/SBWTCK</td>
<td>17, 25, 24</td>
<td></td>
<td>Selects test mode for JTAG pins on Port 1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test</td>
</tr>
<tr>
<td>AVCC</td>
<td>NA</td>
<td>NA</td>
<td>Analog supply voltage</td>
</tr>
<tr>
<td>DVCC</td>
<td>1</td>
<td>1</td>
<td>Digital supply voltage</td>
</tr>
<tr>
<td>DVSS</td>
<td>20</td>
<td>28</td>
<td>Ground reference</td>
</tr>
<tr>
<td>NC</td>
<td>NA</td>
<td>NA</td>
<td>Not connected</td>
</tr>
</tbody>
</table>

(3) If XOUT/P2.7 is used as an input, excess current will flow until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.
### Table 2. Terminal Functions (continued)

<table>
<thead>
<tr>
<th>TERMINAL NAME</th>
<th>PW20, N20</th>
<th>PW28</th>
<th>RHB32</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>QFN Pad</td>
<td>NA</td>
<td>NA</td>
<td>Pad</td>
<td>QFN package pad connection to VSS recommended.</td>
</tr>
</tbody>
</table>
CPU
The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

Instruction Set
The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 3 shows examples of the three types of instruction formats; Table 4 shows the address modes.

### Table 3. Instruction Word Formats

<table>
<thead>
<tr>
<th>INSTRUCTION FORMAT</th>
<th>EXAMPLE</th>
<th>OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dual operands, source-destination</td>
<td>ADD R4,R5</td>
<td>R4 + R5 --&gt; R5</td>
</tr>
<tr>
<td>Single operands, destination only</td>
<td>CALL R8</td>
<td>PC --&gt;(TOS), R8--PC</td>
</tr>
<tr>
<td>Relative jump, un/conditional</td>
<td>JNE</td>
<td>Jump-on-equal bit = 0</td>
</tr>
</tbody>
</table>

### Table 4. Address Mode Descriptions

<table>
<thead>
<tr>
<th>ADDRESS MODE</th>
<th>S</th>
<th>D</th>
<th>SYNTAX</th>
<th>EXAMPLE</th>
<th>OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register</td>
<td>✓</td>
<td>✓</td>
<td>MOV Rs,Rd</td>
<td>MOV R10,R11</td>
<td>R10 --&gt; R11</td>
</tr>
<tr>
<td>Indexed</td>
<td>✓</td>
<td>✓</td>
<td>MOV X(Rn),Y(Rm)</td>
<td>MOV 2(R5),6(R6)</td>
<td>M(2+R5) --&gt; M(6+R6)</td>
</tr>
<tr>
<td>Symbolic (PC relative)</td>
<td>✓</td>
<td>✓</td>
<td>MOV EDE,TONI</td>
<td>M(EDE) --&gt; M(TONI)</td>
<td></td>
</tr>
<tr>
<td>Absolute</td>
<td>✓</td>
<td>✓</td>
<td>MOV &amp;MEM,&amp;TCDAT</td>
<td>M(MEM) --&gt; M(TCDAT)</td>
<td></td>
</tr>
<tr>
<td>Indirect</td>
<td>✓</td>
<td>✓</td>
<td>MOV @Rn,Y(Rm)</td>
<td>MOV @R10,Tab(R6)</td>
<td>M(R10) --&gt; M(Tab+R6)</td>
</tr>
<tr>
<td>Indirect autoincrement</td>
<td>✓</td>
<td></td>
<td>MOV @Rn+,Rm</td>
<td>MOV @R10+,.R11</td>
<td>M(R10) --&gt; R11</td>
</tr>
<tr>
<td>Immediate</td>
<td>✓</td>
<td></td>
<td>MOV #X,TONI</td>
<td>MOV #45,TONI</td>
<td>#45 --&gt; M(TONI)</td>
</tr>
</tbody>
</table>

(1) S = source, D = destination
Operating Modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

• Active mode (AM)
  – All clocks are active
• Low-power mode 0 (LPM0)
  – CPU is disabled
  – ACLK and SMCLK remain active, MCLK is disabled
• Low-power mode 1 (LPM1)
  – CPU is disabled
  – ACLK and SMCLK remain active, MCLK is disabled
  – DCO’s dc generator is disabled if DCO not used in active mode
• Low-power mode 2 (LPM2)
  – CPU is disabled
  – MCLK and SMCLK are disabled
  – DCO’s dc generator remains enabled
  – ACLK remains active
• Low-power mode 3 (LPM3)
  – CPU is disabled
  – MCLK and SMCLK are disabled
  – DCO’s dc generator is disabled
  – ACLK remains active
• Low-power mode 4 (LPM4)
  – CPU is disabled
  – ACLK is disabled
  – MCLK and SMCLK are disabled
  – DCO’s dc generator is disabled
  – Crystal oscillator is stopped
## Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (for example, flash is not programmed), the CPU goes into LPM4 immediately after power-up.

### Table 5. Interrupt Sources, Flags, and Vectors

<table>
<thead>
<tr>
<th>INTERRUPT SOURCE</th>
<th>INTERRUPT FLAG</th>
<th>SYSTEM INTERRUPT</th>
<th>ADDRESS</th>
<th>PRIORITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power-Up</td>
<td>PORIFG</td>
<td>Reset</td>
<td>0FFFEh</td>
<td>31, highest</td>
</tr>
<tr>
<td>External Reset</td>
<td>RSTIFG</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Watchdog Timer+</td>
<td>WDTIFG</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Flash key violation</td>
<td>KEVF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PC out-of-range(1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NMI</td>
<td>NMIFG</td>
<td>(non)-maskable</td>
<td>0FFCh</td>
<td>30</td>
</tr>
<tr>
<td>Oscillator fault</td>
<td>OFIG</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Flash memory access violation</td>
<td>ACCVIFG(2)(3)</td>
<td>(non)-maskable</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Timer1_A3</td>
<td>TACCR0 CCIFG(4)</td>
<td>maskable</td>
<td>0FFFFAh</td>
<td>29</td>
</tr>
<tr>
<td>Timer1_A3</td>
<td>TACCR2 TACCR1 CCIFG, TAIFG(2)(4)</td>
<td>maskable</td>
<td>0FFFF8h</td>
<td>28</td>
</tr>
<tr>
<td>Watchdog Timer+</td>
<td>WDTIFG</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Timer0_A3</td>
<td>TACCR0 CCIFG(4)</td>
<td>maskable</td>
<td>0FFFF2h</td>
<td>25</td>
</tr>
<tr>
<td>Timer0_A3</td>
<td>TACCR2 TACCR1 CCIFG, TAIFG(5)(4)</td>
<td>maskable</td>
<td>0FFFF0h</td>
<td>24</td>
</tr>
<tr>
<td>USCI_A0/USCI_B0 receive</td>
<td>UCA0RXIFG, UCB0RXIFG(2)(5)</td>
<td>maskable</td>
<td>0FFE8h</td>
<td>23</td>
</tr>
<tr>
<td>USCI_B0 I2C status</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>USCI_B0/I2C transmit</td>
<td>UCA0TXIFG, UCB0TXIFG(2)(6)</td>
<td>maskable</td>
<td>0FFECh</td>
<td>22</td>
</tr>
<tr>
<td>USCI_B0/I2C receive/transmit</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADC10 (MSP430G2x33 only)</td>
<td>ADC10IFG(4)</td>
<td>maskable</td>
<td>0FFE4h</td>
<td>21</td>
</tr>
<tr>
<td>I/O Port P2 (up to eight flags)</td>
<td>P2IFG.0 to P2IFG.7(2)(4)</td>
<td>maskable</td>
<td>0FFE6h</td>
<td>19</td>
</tr>
<tr>
<td>I/O Port P1 (up to eight flags)</td>
<td>P1IFG.0 to P1IFG.7(2)(4)</td>
<td>maskable</td>
<td>0FFE4h</td>
<td>18</td>
</tr>
<tr>
<td>See (7)</td>
<td></td>
<td></td>
<td>0FFE2h</td>
<td>17</td>
</tr>
<tr>
<td>See (8)</td>
<td></td>
<td></td>
<td>0FFE0h</td>
<td>16</td>
</tr>
<tr>
<td>See (7)</td>
<td></td>
<td></td>
<td>0FFDEh</td>
<td>15</td>
</tr>
<tr>
<td>See (8)</td>
<td></td>
<td></td>
<td>0FFDEh to 0FFC0h</td>
<td>14 to 0, lowest</td>
</tr>
</tbody>
</table>

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.
(2) Multiple source flags
(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.
(4) Interrupt flags are located in the module.
(5) In SPI mode: UCB0RXIFG. In I2C mode: UCALIFG, UCNACKIFG, ICSTTIFG, UCSTIFG.
(6) In UART/SPI mode: UCB0TXIFG. In I2C mode: UCB0RXIFG, UCB0TXIFG.
(7) This location is used as bootstrap loader security key (BSLSKEY). A 0xAA55 at this location disables the BSL completely. A zero (0h) disables the erasure of the flash if an invalid password is supplied.
(8) The interrupt vectors at addresses 0FFDEh to 0FFC0h are not used in this device and can be used for regular program code if necessary.
Special Function Registers (SFRs)

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

Legend
- **rw**: Bit can be read and written.
- **rw-0,1**: Bit can be read and written. It is reset or set by PUC.
- **rw-(0,1)**: Bit can be read and written. It is reset or set by POR.
- SFR bit is not present in device.

### Table 6. Interrupt Enable Register 1 and 2

<table>
<thead>
<tr>
<th>Address</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ACCVIE</td>
<td>NMIIE</td>
<td>OFIE</td>
</tr>
<tr>
<td></td>
<td>rw-0</td>
<td>rw-0</td>
<td>rw-0</td>
<td>rw-0</td>
<td>rw-0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **WDTIE**: Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.
- **OFIE**: Oscillator fault interrupt enable
- **NMIIE**: (Non)maskable interrupt enable
- **ACCVIE**: Flash access violation interrupt enable

### Table 7. Interrupt Flag Register 1 and 2

<table>
<thead>
<tr>
<th>Address</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>02h</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>NMIIFG</td>
<td>RSTIFG</td>
<td>PORIFG</td>
</tr>
<tr>
<td></td>
<td>rw-0</td>
<td>rw-(0)</td>
<td>rw-(1)</td>
<td>rw-1</td>
<td>rw-(0)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **WDTIFG**: Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on VCC power-on or a reset condition at the RST/NMI pin in reset mode.
- **OFIFG**: Flag set on oscillator fault.
- **PORIFG**: Power-On Reset interrupt flag. Set on VCC power-up.
- **RSTIFG**: External reset interrupt flag. Set on a reset condition at RST/NMI pin in reset mode. Reset on VCC power-up.
- **NMIIFG**: Set via RST/NMI pin

### Table 8. Interrupt Flag Register 3

<table>
<thead>
<tr>
<th>Address</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>03h</td>
<td>UCB0TXIFG</td>
<td>UCB0RXIFG</td>
<td>UCA0TXIFG</td>
<td>UCA0RXIFG</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>rw-1</td>
<td>rw-0</td>
<td>rw-1</td>
<td>rw-0</td>
<td>rw-0</td>
<td>rw-0</td>
<td>rw-0</td>
<td>rw-0</td>
</tr>
</tbody>
</table>

- **UCB0RXIFG**: USCI_B0 receive interrupt flag
- **UCB0TXIFG**: USCI_B0 transmit interrupt flag
- **UCA0RXIFG**: USCI_A0 receive interrupt flag
- **UCA0TXIFG**: USCI_A0 transmit interrupt flag
- **UCB0RXIFG**: USCI_B0 transmit interrupt flag
- **UCB0TXIFG**: USCI_B0 transmit interrupt flag
Memory Organization

Table 8. Memory Organization

<table>
<thead>
<tr>
<th></th>
<th>MSP430G2233</th>
<th>MSP430G2233</th>
<th>MSP430G2433</th>
<th>MSP430G2433</th>
<th>MSP430G2533</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory</td>
<td>Size</td>
<td>2kB</td>
<td>4kB</td>
<td>8kB</td>
<td>16kB</td>
</tr>
<tr>
<td>Main: interrupt vector</td>
<td>Flash</td>
<td>0xFFFF to 0xFFC0</td>
<td>0xFFFF to 0xFFC0</td>
<td>0xFFFF to 0xFFC0</td>
<td>0xFFFF to 0xFFC0</td>
</tr>
<tr>
<td>Main: code memory</td>
<td>Flash</td>
<td>0xFFFF to 0xF800</td>
<td>0xFFFF to 0xF000</td>
<td>0xFFFF to 0xE000</td>
<td>0xFFFF to 0xC000</td>
</tr>
<tr>
<td>Information memory</td>
<td>Size</td>
<td>256 Byte</td>
<td>256 Byte</td>
<td>256 Byte</td>
<td>256 Byte</td>
</tr>
<tr>
<td></td>
<td>Flash</td>
<td>010FFh to 01000h</td>
<td>010FFh to 01000h</td>
<td>010FFh to 01000h</td>
<td>010FFh to 01000h</td>
</tr>
<tr>
<td>RAM</td>
<td>Size</td>
<td>256 Byte</td>
<td>256 Byte</td>
<td>512 Byte</td>
<td>512 Byte</td>
</tr>
<tr>
<td></td>
<td>Flash</td>
<td>0x02FF to 0x0200</td>
<td>0x02FF to 0x0200</td>
<td>0x03FF to 0x0200</td>
<td>0x03FF to 0x0200</td>
</tr>
<tr>
<td>Peripherals</td>
<td>16-bit</td>
<td>01FFh to 0100h</td>
<td>01FFh to 0100h</td>
<td>01FFh to 0100h</td>
<td>01FFh to 0100h</td>
</tr>
<tr>
<td></td>
<td>8-bit</td>
<td>0FFh to 010h</td>
<td>0FFh to 010h</td>
<td>0FFh to 010h</td>
<td>0FFh to 010h</td>
</tr>
<tr>
<td></td>
<td>8-bit SFR</td>
<td>0Fh to 00h</td>
<td>0Fh to 00h</td>
<td>0Fh to 00h</td>
<td>0Fh to 00h</td>
</tr>
</tbody>
</table>

Bootstrap Loader (BSL)

The MSP430 BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the MSP430 Programming Via the Bootstrap Loader User's Guide (SLAU319).

Table 9. BSL Function Pins

<table>
<thead>
<tr>
<th>BSL FUNCTION</th>
<th>20-PIN PW PACKAGE 20-PIN N PACKAGE</th>
<th>28-PIN PACKAGE PW</th>
<th>32-PIN PACKAGE RHB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data transmit</td>
<td>3 - P1.1</td>
<td>3 - P1.1</td>
<td>1 - P1.1</td>
</tr>
<tr>
<td>Data receive</td>
<td>7 - P1.5</td>
<td>7 - P1.5</td>
<td>5 - P1.5</td>
</tr>
</tbody>
</table>

Flash Memory

The flash memory can be programmed via the Spy-Bi-Wire/JTAG port or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually or as a group with segments 0 to n. Segments A to D are also called information memory.
- Segment A contains calibration data. After reset segment A is protected against programming and erasing. It can be unlocked but care should be taken not to erase this segment if the device-specific calibration data is required.
Peripherals
Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the MSP430x2xx Family User’s Guide (SLAU144).

Oscillator and System Clock
The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator and an internal digitally controlled oscillator (DCO). The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 µs. The basic clock module provides the following clock signals:
- Auxiliary clock (ACLK), sourced either from a 32768-Hz watch crystal or the internal LF oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

The DCO settings to calibrate the DCO output frequency are stored in the information memory segment A.

Calibration Data Stored in Information Memory Segment A
Calibration data is stored for both the DCO and for ADC10 organized in a tag-length-value structure.

<table>
<thead>
<tr>
<th>NAME</th>
<th>ADDRESS</th>
<th>VALUE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>TAG_DCO_30</td>
<td>0x10F6</td>
<td>0x01</td>
<td>DCO frequency calibration at V&lt;sub&gt;CC&lt;/sub&gt; = 3 V and T&lt;sub&gt;A&lt;/sub&gt; = 30°C at calibration</td>
</tr>
<tr>
<td>TAG_ADC10_1</td>
<td>0x10DA</td>
<td>0x10</td>
<td>ADC10_1 calibration tag</td>
</tr>
<tr>
<td>TAG_EMPTY</td>
<td>-</td>
<td>0xFE</td>
<td>Identifier for empty memory areas</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>LABEL</th>
<th>ADDRESS OFFSET</th>
<th>SIZE</th>
<th>CONDITION AT CALIBRATION / DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAL_ADC_25T85</td>
<td>0x0010</td>
<td>word</td>
<td>INCHx = 0x1010, REF2_5 = 1, T&lt;sub&gt;A&lt;/sub&gt; = 85°C</td>
</tr>
<tr>
<td>CAL_ADC_25T30</td>
<td>0x000E</td>
<td>word</td>
<td>INCHx = 0x1010, REF2_5 = 1, T&lt;sub&gt;A&lt;/sub&gt; = 30°C</td>
</tr>
<tr>
<td>CAL_ADC_25VREF_FACTOR</td>
<td>0x000C</td>
<td>word</td>
<td>REF2_5 = 1, T&lt;sub&gt;A&lt;/sub&gt; = 30°C, I&lt;sub&gt;VREF+&lt;/sub&gt; = 1 mA</td>
</tr>
<tr>
<td>CAL_ADC_15T85</td>
<td>0x000A</td>
<td>word</td>
<td>INCHx = 0x1010, REF2_5 = 0, T&lt;sub&gt;A&lt;/sub&gt; = 85°C</td>
</tr>
<tr>
<td>CAL_ADC_15T30</td>
<td>0x0008</td>
<td>word</td>
<td>INCHx = 0x1010, REF2_5 = 0, T&lt;sub&gt;A&lt;/sub&gt; = 30°C</td>
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<tr>
<td>CAL_ADC_15VREF_FACTOR</td>
<td>0x0006</td>
<td>word</td>
<td>REF2_5 = 0, T&lt;sub&gt;A&lt;/sub&gt; = 30°C, I&lt;sub&gt;VREF+&lt;/sub&gt; = 0.5 mA</td>
</tr>
<tr>
<td>CAL_ADC_OFFSET</td>
<td>0x0004</td>
<td>word</td>
<td>External VREF = 1.5 V, f&lt;sub&gt;ADC10CLK&lt;/sub&gt; = 5 MHz</td>
</tr>
<tr>
<td>CAL_ADC_GAIN_FACTOR</td>
<td>0x0002</td>
<td>word</td>
<td>External VREF = 1.5 V, f&lt;sub&gt;ADC10CLK&lt;/sub&gt; = 5 MHz</td>
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<td>CAL_Bc1_1MHZ</td>
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<tr>
<td>CAL_DCO_1MHZ</td>
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<td>byte</td>
<td>-</td>
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<td>CAL_Bc1_8MHZ</td>
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<td>byte</td>
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<td>CAL_Bc1_12MHZ</td>
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<tr>
<td>CAL_Bc1_16MHZ</td>
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<td>-</td>
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<tr>
<td>CAL_DCO_16MHZ</td>
<td>0x0002</td>
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<td>-</td>
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</tbody>
</table>

Brownout
The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.
Digital I/O
Up to three 8-bit I/O ports are implemented:
• All individual I/O bits are independently programmable.
• Any combination of input, output, and interrupt condition (port P1 and port P2 only) is possible.
• Edge-selectable interrupt input capability for all bits of port P1 and port P2 (if available).
• Read/write access to port-control registers is supported by all instructions.
• Each I/O has an individually programmable pullup/pulldown resistor.
• Each I/O has an individually programmable pin oscillator enable bit to enable low-cost touch sensing.

WDT+ Watchdog Timer
The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

Timer_A3 (TA0, TA1)
Timer0_A3 and Timer1_A3 are 16-bit timers/counters with three capture/compare registers. Timer_A3 can support multiple capture/compare, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

<table>
<thead>
<tr>
<th>INPUT PIN NUMBER</th>
<th>DEVICE INPUT SIGNAL</th>
<th>MODULE BLOCK</th>
<th>MODULE OUTPUT SIGNAL</th>
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<tbody>
<tr>
<td>PW20, N20</td>
<td>PW28</td>
<td>RHB32</td>
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<tr>
<td>P1.0-2</td>
<td>P1.0-2</td>
<td>P1.0-31</td>
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<td>SMCLK</td>
<td></td>
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</tr>
<tr>
<td>PinOsc</td>
<td>PinOsc</td>
<td>PinOsc</td>
<td>TACLK</td>
</tr>
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<td>P1.1-3</td>
<td>P1.1-3</td>
<td>P1.1-1</td>
<td>TA0.0</td>
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<td>VCC</td>
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<td>P3.0-7</td>
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<td>PinOsc</td>
<td>PinOsc</td>
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Table 12. Timer0_A3 Signal Connections

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<th>MODULE BLOCK</th>
<th>MODULE OUTPUT SIGNAL</th>
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<tr>
<td>PW20, N20</td>
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<td>RHB32</td>
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<td>P1.0-2</td>
<td>P1.0-2</td>
<td>P1.0-31</td>
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<td>PinOsc</td>
<td>PinOsc</td>
<td>PinOsc</td>
<td>TACLK</td>
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<td>PinOsc</td>
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<tr>
<th>OUTPUT PIN NUMBER</th>
<th>INPUT PIN NUMBER</th>
<th>DEVICE INPUT SIGNAL</th>
<th>MODULE BLOCK</th>
<th>MODULE OUTPUT SIGNAL</th>
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<tr>
<td>PW20, N20</td>
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### Table 13. Timer1_A3 Signal Connections

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<th>MODULE INPUT NAME</th>
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<th>OUTPUT PIN NUMBER</th>
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<td>PW20, N20, RHB32</td>
<td>PW28</td>
<td>P2.0-8</td>
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<td>P3.3-14</td>
<td>P3.3-13</td>
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</table>

### Universal Serial Communications Interface (USCI)

The USCI module is used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3 or 4 pin) and I2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection (LIN), and IrDA. Not all packages support the USCI functionality.

USCI_A0 provides support for SPI (3 or 4 pin), UART, enhanced UART, and IrDA.

USCI_B0 provides support for SPI (3 or 4 pin) and I2C.

### ADC10 (MSP430G2x33 Only)

The ADC10 module supports fast 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator, and data transfer controller (DTC) for automatic conversion result handling, allowing ADC samples to be converted and stored without any CPU intervention.
## Peripheral File Map

### Table 14. Peripherals With Word Access

<table>
<thead>
<tr>
<th>MODULE</th>
<th>REGISTER DESCRIPTION</th>
<th>REGISTER NAME</th>
<th>OFFSET</th>
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<tbody>
<tr>
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<td>ADC data transfer start address</td>
<td>ADC10SA</td>
<td>1BCh</td>
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<td>ADC memory</td>
<td>ADC10MEM</td>
<td>1B4h</td>
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<tr>
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<td>ADC control register 1</td>
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<td>ADC control register 0</td>
<td>ADC10CTL0</td>
<td>1B0h</td>
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<tr>
<td>Timer1_A3</td>
<td>Capture/compare register</td>
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<td>Capture/compare register</td>
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<td>Capture/compare register</td>
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<td>Timer_A register</td>
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<td>Capture/compare control</td>
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<td>0186h</td>
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<td>Capture/compare control</td>
<td>TACCTL1</td>
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<td>Capture/compare control</td>
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<td>011Eh</td>
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<td>Capture/compare register</td>
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<td>Capture/compare register</td>
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<td>Timer_A register</td>
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<td>Capture/compare control</td>
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<td>Watchdog Timer+</td>
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### Table 15. Peripherals With Byte Access

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<td>UCB0RXBUF</td>
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<td>06Ch</td>
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<td>UCB0BR1</td>
<td>06Bh</td>
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<tr>
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<td>USCI_B0 bit rate control 0</td>
<td>UCB0BR0</td>
<td>06Ah</td>
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<td>USCI_B0 control 0</td>
<td>UCB0CTL0</td>
<td>068h</td>
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<td>UCB0SA</td>
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<td>USCI_B0 I2C own address</td>
<td>UCB0OA</td>
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<td>USCI_A0 auto baud rate control</td>
<td>UCA0ABCTL</td>
<td>05Dh</td>
</tr>
<tr>
<td>ADC10</td>
<td>ADC analog enable 0</td>
<td>ADC10AE0</td>
<td>04Ah</td>
</tr>
<tr>
<td></td>
<td>(MSP430G2x33 devices only)</td>
<td>ADC10AE1</td>
<td>04Bh</td>
</tr>
<tr>
<td></td>
<td>ADC data transfer control register 1</td>
<td>ADC10DTC1</td>
<td>049h</td>
</tr>
<tr>
<td></td>
<td>ADC data transfer control register 0</td>
<td>ADC10DTC0</td>
<td>048h</td>
</tr>
<tr>
<td>Basic Clock System+</td>
<td>Basic clock system control 3</td>
<td>BCSCCTL3</td>
<td>053h</td>
</tr>
<tr>
<td></td>
<td>Basic clock system control 2</td>
<td>BCSCCTL2</td>
<td>058h</td>
</tr>
<tr>
<td></td>
<td>Basic clock system control 1</td>
<td>BCSCCTL1</td>
<td>057h</td>
</tr>
<tr>
<td></td>
<td>DCO clock frequency control</td>
<td>DCOCCTL</td>
<td>056h</td>
</tr>
<tr>
<td>Port P3</td>
<td>Port P3 selection 2, pin</td>
<td>P3SEL2</td>
<td>043h</td>
</tr>
<tr>
<td></td>
<td>(28-pin PW and 32-pin RHB only)</td>
<td>Port P3 resistor enable</td>
<td>P3REN</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Port P3 selection</td>
<td>P3SEL</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Port P3 direction</td>
<td>P3DIR</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Port P3 output</td>
<td>P3OUT</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Port P3 input</td>
<td>P3IN</td>
</tr>
<tr>
<td>Port P2</td>
<td>Port P2 selection 2</td>
<td>P2SEL2</td>
<td>042h</td>
</tr>
<tr>
<td></td>
<td>Port P2 resistor enable</td>
<td>P2REN</td>
<td>02Fh</td>
</tr>
<tr>
<td></td>
<td>Port P2 selection</td>
<td>P2SEL</td>
<td>02Eh</td>
</tr>
<tr>
<td></td>
<td>Port P2 interrupt enable</td>
<td>P2IE</td>
<td>02Dh</td>
</tr>
<tr>
<td></td>
<td>Port P2 interrupt edge select</td>
<td>P2IES</td>
<td>02Ch</td>
</tr>
<tr>
<td></td>
<td>Port P2 interrupt flag</td>
<td>P2IFG</td>
<td>02Bh</td>
</tr>
<tr>
<td></td>
<td>Port P2 direction</td>
<td>P2DIR</td>
<td>02Ah</td>
</tr>
<tr>
<td></td>
<td>Port P2 output</td>
<td>P2OUT</td>
<td>029h</td>
</tr>
<tr>
<td></td>
<td>Port P2 input</td>
<td>P2IN</td>
<td>028h</td>
</tr>
<tr>
<td>Port P1</td>
<td>Port P1 selection 2</td>
<td>P1SEL2</td>
<td>041h</td>
</tr>
<tr>
<td></td>
<td>Port P1 resistor enable</td>
<td>P1REN</td>
<td>027h</td>
</tr>
<tr>
<td></td>
<td>Port P1 selection</td>
<td>P1SEL</td>
<td>026h</td>
</tr>
<tr>
<td></td>
<td>Port P1 interrupt enable</td>
<td>P1IE</td>
<td>025h</td>
</tr>
<tr>
<td></td>
<td>Port P1 interrupt edge select</td>
<td>P1IES</td>
<td>024h</td>
</tr>
<tr>
<td></td>
<td>Port P1 interrupt flag</td>
<td>P1IFG</td>
<td>023h</td>
</tr>
<tr>
<td></td>
<td>Port P1 direction</td>
<td>P1DIR</td>
<td>022h</td>
</tr>
<tr>
<td></td>
<td>Port P1 output</td>
<td>P1OUT</td>
<td>021h</td>
</tr>
<tr>
<td></td>
<td>Port P1 input</td>
<td>P1IN</td>
<td>020h</td>
</tr>
<tr>
<td>Special Function</td>
<td>SFR interrupt flag 2</td>
<td>IFG2</td>
<td>003h</td>
</tr>
<tr>
<td></td>
<td>SFR interrupt flag 1</td>
<td>IFG1</td>
<td>002h</td>
</tr>
<tr>
<td></td>
<td>SFR interrupt enable 2</td>
<td>IE2</td>
<td>001h</td>
</tr>
<tr>
<td></td>
<td>SFR interrupt enable 1</td>
<td>IE1</td>
<td>000h</td>
</tr>
</tbody>
</table>
Absolute Maximum Ratings\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage applied at (V_{CC}) to (V_{SS})</td>
<td>-0.3 V to 4.1 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage applied to any pin (^{(2)})</td>
<td>-0.3 V to (V_{CC} + 0.3) V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Diode current at any device pin</td>
<td>(\pm 2) mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage temperature range, (T_{stg}) (^{(3)})</td>
<td>Unprogrammed device: -55°C to 150°C</td>
<td>Programmed device: -55°C to 150°C</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(^{(2)}\) All voltages referenced to \(V_{SS}\). The JTAG fuse-blow voltage, \(V_{FB}\), is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.

\(^{(3)}\) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{CC})</td>
<td>Supply voltage</td>
<td>During program execution</td>
<td>1.8</td>
<td>3.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>During flash programming/erase</td>
<td>2.2</td>
<td>3.6</td>
</tr>
<tr>
<td>(V_{SS})</td>
<td>Supply voltage</td>
<td></td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>(T_A)</td>
<td>Operating free-air temperature</td>
<td>I version</td>
<td>-40</td>
<td>85</td>
</tr>
<tr>
<td></td>
<td></td>
<td>T version</td>
<td>-40</td>
<td>105</td>
</tr>
<tr>
<td>(f_{SYSTEM})</td>
<td>Processor frequency (maximum MCLK frequency using the USART module) (^{(1)}) (^{(2)})</td>
<td>(V_{CC} = 1.8) V, Duty cycle = 50% ± 10%</td>
<td>dc</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_{CC} = 2.7) V, Duty cycle = 50% ± 10%</td>
<td>dc</td>
<td>12</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_{CC} = 3.3) V, Duty cycle = 50% ± 10%</td>
<td>dc</td>
<td>16</td>
</tr>
</tbody>
</table>

\(^{(1)}\) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.

\(^{(2)}\) Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.

Figure 1. Safe Operating Area
Electrical Characteristics

Active Mode Supply Current Into V\textsubscript{CC} Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)\(^{(1)}\)(\(2\))

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>T\textsubscript{A}</th>
<th>V\textsubscript{CC}</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>I\textsubscript{AM,1MHz}</td>
<td>Active mode (AM) current at 1 MHz</td>
<td></td>
<td></td>
<td>2.2 V</td>
<td>230</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>f\textsubscript{DCO} = f\textsubscript{MCLK} = f\textsubscript{SMCLK} = 1 MHz,</td>
<td></td>
<td></td>
<td>3 V</td>
<td>330</td>
<td>420</td>
<td></td>
</tr>
<tr>
<td></td>
<td>f\textsubscript{ACLK} = 0 Hz,</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Program executes in flash,</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>BCSCT1L = CALBC1_1MHZ,</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>DCOCTL = CALDCO_1MHZ,</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>CPUOFF = 0, SCG0 = 0, SCG1 = 0,</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>OSCOFF = 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) All inputs are tied to 0 V or to V\textsubscript{CC}. Outputs do not source or sink any current.

\(^{(2)}\) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

Typical Characteristics, Active Mode Supply Current (Into V\textsubscript{CC})

![Figure 2. Active Mode Current vs V\textsubscript{CC}, T\textsubscript{A} = 25°C](image)

![Figure 3. Active Mode Current vs DCO Frequency](image)
### Low-Power Mode Supply Currents (Into \( V_{CC} \)) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)\(^{(1)}\) \(^{(2)}\)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>( T_A )</th>
<th>( V_{CC} )</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{LPM0,1MHz} ) Low-power mode 0 (LPM0) current(^{(5)})</td>
<td>( f_{MCLK} = 0 \text{ MHz}, ) ( f_{SMCLK} = f_{DCO} = 1 \text{ MHz}, ) ( f_{ACLK} = 32768 \text{ Hz}, ) ( BCSCTL1 = \text{CALBC1}_1\text{MHz}, ) ( DCOCTL = \text{CALDCO}_1\text{MHz}, ) ( CPUOFF = 1, ) ( SCG0 = 0, ) ( SCG1 = 0, ) ( OSCOFF = 0 )</td>
<td>25°C</td>
<td>2.2 V</td>
<td>56</td>
<td></td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{LPM2} ) Low-power mode 2 (LPM2) current(^{(4)})</td>
<td>( f_{MCLK} = f_{SMCLK} = 0 \text{ MHz}, ) ( f_{DCO} = 1 \text{ MHz}, ) ( f_{ACLK} = 32768 \text{ Hz}, ) ( BCSCTL1 = \text{CALBC1}_1\text{MHz}, ) ( DCOCTL = \text{CALDCO}_1\text{MHz}, ) ( CPUOFF = 1, ) ( SCG0 = 0, ) ( SCG1 = 1, ) ( OSCOFF = 0 )</td>
<td>25°C</td>
<td>2.2 V</td>
<td>22</td>
<td></td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{LPM3,LFX1} ) Low-power mode 3 (LPM3) current(^{(4)})</td>
<td>( f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 \text{ MHz}, ) ( f_{ACLK} = 32768 \text{ Hz}, ) ( CPUOFF = 1, ) ( SCG0 = 1, ) ( SCG1 = 1, ) ( OSCOFF = 0 )</td>
<td>25°C</td>
<td>2.2 V</td>
<td>0.7</td>
<td>1.5</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{LPM3,VLO} ) Low-power mode 3 current, (LPM3)(^{(4)})</td>
<td>( f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 \text{ MHz}, ) ( f_{ACLK} = 0 \text{ Hz}, ) ( CPUOFF = 1, ) ( SCG0 = 1, ) ( SCG1 = 1, ) ( OSCOFF = 0 )</td>
<td>25°C</td>
<td>2.2 V</td>
<td>0.5</td>
<td>0.7</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{LPM4} ) Low-power mode 4 (LPM4) current(^{(5)})</td>
<td>( f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 \text{ MHz}, ) ( f_{ACLK} = 0 \text{ Hz}, ) ( CPUOFF = 1, ) ( SCG0 = 1, ) ( SCG1 = 1, ) ( OSCOFF = 1 )</td>
<td>25°C</td>
<td>2.2 V</td>
<td>0.1</td>
<td>0.5</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>85°C</td>
<td>2.2 V</td>
<td>0.8</td>
<td>1.7</td>
<td></td>
<td>( \mu A )</td>
</tr>
</tbody>
</table>

\(^{(1)}\) All inputs are tied to 0 V or to \( V_{CC} \). Outputs do not source or sink any current.

\(^{(2)}\) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

\(^{(3)}\) Current for brownout and WDT clocked by SMCLK included.

\(^{(4)}\) Current for brownout and WDT clocked by ACLK included.

\(^{(5)}\) Current for brownout included.

### Typical Characteristics, Low-Power Mode Supply Currents

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
### Schmitt-Trigger Inputs, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>V\textsubscript{CC}</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V\textsubscript{IT+}</td>
<td>Positive-going input threshold voltage</td>
<td>0.45 V\textsubscript{CC}</td>
<td>0.75 V\textsubscript{CC}</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3 V</td>
<td>1.35</td>
<td>2.25</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V\textsubscript{IT−}</td>
<td>Negative-going input threshold voltage</td>
<td>0.25 V\textsubscript{CC}</td>
<td>0.55 V\textsubscript{CC}</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3 V</td>
<td>0.75</td>
<td>1.65</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V\textsubscript{hys}</td>
<td>Input voltage hysteresis (V\textsubscript{IT+} – V\textsubscript{IT−})</td>
<td>3 V</td>
<td></td>
<td></td>
<td>0.3</td>
<td>1</td>
</tr>
<tr>
<td>R\textsubscript{Pull}</td>
<td>Pullup/pulldown resistor</td>
<td>For pullup: ( V\text{IN} = V\text{SS} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>For pulldown: ( V\text{IN} = V\text{CC} )</td>
<td>3 V</td>
<td>20</td>
<td>35</td>
<td>50</td>
<td>kΩ</td>
</tr>
<tr>
<td>C\textsubscript{I}</td>
<td>Input capacitance</td>
<td>( V\text{IN} = V\text{SS} ) or ( V\text{CC} )</td>
<td>5</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

### Leakage Current, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>V\textsubscript{CC}</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>I\textsubscript{lkg}(Px,y)</td>
<td>High-impedance leakage current</td>
<td>(1) (2)</td>
<td>3 V</td>
<td>±50</td>
<td>nA</td>
</tr>
</tbody>
</table>

(1) The leakage current is measured with \( V\text{SS} \) or \( V\text{CC} \) applied to the corresponding pin(s), unless otherwise noted.

(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

### Outputs, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>V\textsubscript{CC}</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V\textsubscript{OH}</td>
<td>High-level output voltage</td>
<td>( I\text{(OHmax)} = –6 \text{mA} \textsuperscript{(1)} )</td>
<td>3 V</td>
<td>( V\text{CC} – 0.3 )</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V\textsubscript{OL}</td>
<td>Low-level output voltage</td>
<td>( I\text{(OLmax)} = 6 \text{mA} \textsuperscript{(1)} )</td>
<td>3 V</td>
<td>( V\text{SS} + 0.3 )</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

(1) The maximum total current, \( I\text{(OHmax)} \) and \( I\text{(OLmax)} \), for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

### Output Frequency, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>V\textsubscript{CC}</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>f\textsubscript{Px,y}</td>
<td>Port output frequency (with load)</td>
<td>( P_{x,y}, C_L = 20 \text{pF}, R_L = 1 \text{kΩ} \textsuperscript{(1)} ) (2)</td>
<td>3 V</td>
<td>12</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>f\textsubscript{Port_CLK}</td>
<td>Clock output frequency</td>
<td>( P_{x,y}, C_L = 20 \text{pF} \textsuperscript{(2)} )</td>
<td>3 V</td>
<td>16</td>
<td></td>
<td>MHz</td>
</tr>
</tbody>
</table>

(1) A resistive divider with two 0.5-kΩ resistors between \( V\text{CC} \) and \( V\text{SS} \) is used as load. The output is connected to the center tap of the divider.

(2) The output voltage reaches at least 10% and 90% \( V\text{CC} \) at the specified toggle frequency.
Typical Characteristics, Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TYPICAL LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

TYPICAL HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

Figure 6.

Figure 7.

Figure 8.

Figure 9.
Pin-Oscillator Frequency – Ports Px
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>VCC</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(f_{oP1.x})</td>
<td>Port output oscillation frequency</td>
<td>3 V</td>
<td>1400</td>
<td>900</td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>(f_{oP2.x})</td>
<td>Port output oscillation frequency</td>
<td>3 V</td>
<td>1800</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>(f_{oP2.6/7})</td>
<td>Port output oscillation frequency</td>
<td>3 V</td>
<td>700</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>(f_{oP3.x})</td>
<td>Port output oscillation frequency</td>
<td>3 V</td>
<td>1800</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
</tbody>
</table>

(1) A resistive divider with two 0.5-k\(\Omega\) resistors between \(V_{CC}\) and \(V_{SS}\) is used as load. The output is connected to the center tap of the divider.

(2) The output voltage reaches at least 10% and 90% \(V_{CC}\) at the specified toggle frequency.

### Typical Characteristics, Pin-Oscillator Frequency

**TYPICAL OSCILLATING FREQUENCY vs LOAD CAPACITANCE**

- \(V_{CC} = 3.0\) V
- \(V_{CC} = 2.2\) V

![Graph](image)

A. One output active at a time.

**Figure 10.**

**Figure 11.**
POR/Brownout Reset (BOR)\(^{(1)}\)
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>( V_{CC} )</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CC(start)} )</td>
<td>See Figure 12</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V(B_{IT-}) )</td>
<td>See Figure 12 through Figure 14</td>
<td>( dV_{CC}/dt \leq 3 \text{ V/s} )</td>
<td>( 0.7 \times V_{(B_{IT-})} )</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{hys(B_{IT-})} )</td>
<td>See Figure 12</td>
<td>( dV_{CC}/dt \leq 3 \text{ V/s} )</td>
<td>1.35</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( t_d(BOR) )</td>
<td>See Figure 12</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>( 140 \text{ mV} )</td>
</tr>
<tr>
<td>( t_{(reset)} )</td>
<td>Pulse length needed at RST/NMI pin to accepted reset internally</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>( 2000 \text{ µs} )</td>
</tr>
</tbody>
</table>

(1) The current consumption of the brownout module is already included in the \( I_{CC} \) current consumption data. The voltage level \( V_{(B_{IT-})} + V_{hys(B_{IT-})} \) is \( \leq 1.8 \text{ V} \).

![Figure 12. POR/Brownout Reset (BOR) vs Supply Voltage](image-url)
Typical Characteristics, POR/Brownout Reset (BOR)

Figure 13. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

Figure 14. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal
Main DCO Characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter $S_{DCO}$.
- Modulation control bits MODx select how often $f_{DCO(RSEL,DCO+1)}$ is used within the period of 32 DCCLK cycles. The frequency $f_{DCO(RSEL,DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO+1)} + f_{DCO(RSEL,DCO)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$V_{CC}$</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{DCO(0,0)}$</td>
<td>DCO frequency (0, 0)</td>
<td>RSELx = 0, DCOx = 0, MODx = 0</td>
<td>3 V</td>
<td>0.06</td>
<td>0.14</td>
<td>MHz</td>
</tr>
<tr>
<td>$f_{DCO(0,3)}$</td>
<td>DCO frequency (0, 3)</td>
<td>RSELx = 0, DCOx = 3, MODx = 0</td>
<td>3 V</td>
<td>0.07</td>
<td>0.17</td>
<td>MHz</td>
</tr>
<tr>
<td>$f_{DCO(1,3)}$</td>
<td>DCO frequency (1, 3)</td>
<td>RSELx = 1, DCOx = 3, MODx = 0</td>
<td>3 V</td>
<td>0.15</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>$f_{DCO(2,3)}$</td>
<td>DCO frequency (2, 3)</td>
<td>RSELx = 2, DCOx = 3, MODx = 0</td>
<td>3 V</td>
<td>0.21</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>$f_{DCO(4,3)}$</td>
<td>DCO frequency (4, 3)</td>
<td>RSELx = 4, DCOx = 3, MODx = 0</td>
<td>3 V</td>
<td>0.41</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>$f_{DCO(5,3)}$</td>
<td>DCO frequency (5, 3)</td>
<td>RSELx = 5, DCOx = 3, MODx = 0</td>
<td>3 V</td>
<td>0.58</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>$f_{DCO(6,3)}$</td>
<td>DCO frequency (6, 3)</td>
<td>RSELx = 6, DCOx = 3, MODx = 0</td>
<td>3 V</td>
<td>0.54</td>
<td>1.06</td>
<td>MHz</td>
</tr>
<tr>
<td>$f_{DCO(7,3)}$</td>
<td>DCO frequency (7, 3)</td>
<td>RSELx = 7, DCOx = 3, MODx = 0</td>
<td>3 V</td>
<td>0.80</td>
<td>1.50</td>
<td>MHz</td>
</tr>
<tr>
<td>$f_{DCO(8,3)}$</td>
<td>DCO frequency (8, 3)</td>
<td>RSELx = 8, DCOx = 3, MODx = 0</td>
<td>3 V</td>
<td>1.6</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>$f_{DCO(9,3)}$</td>
<td>DCO frequency (9, 3)</td>
<td>RSELx = 9, DCOx = 3, MODx = 0</td>
<td>3 V</td>
<td>2.3</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>$f_{DCO(10,3)}$</td>
<td>DCO frequency (10, 3)</td>
<td>RSELx = 10, DCOx = 3, MODx = 0</td>
<td>3 V</td>
<td>3.4</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>$f_{DCO(11,3)}$</td>
<td>DCO frequency (11, 3)</td>
<td>RSELx = 11, DCOx = 3, MODx = 0</td>
<td>3 V</td>
<td>4.25</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>$f_{DCO(12,3)}$</td>
<td>DCO frequency (12, 3)</td>
<td>RSELx = 12, DCOx = 3, MODx = 0</td>
<td>3 V</td>
<td>4.30</td>
<td>7.30</td>
<td>MHz</td>
</tr>
<tr>
<td>$f_{DCO(13,3)}$</td>
<td>DCO frequency (13, 3)</td>
<td>RSELx = 13, DCOx = 3, MODx = 0</td>
<td>3 V</td>
<td>6.00</td>
<td>9.60</td>
<td>MHz</td>
</tr>
<tr>
<td>$f_{DCO(14,3)}$</td>
<td>DCO frequency (14, 3)</td>
<td>RSELx = 14, DCOx = 3, MODx = 0</td>
<td>3 V</td>
<td>8.60</td>
<td>13.9</td>
<td>MHz</td>
</tr>
<tr>
<td>$f_{DCO(15,3)}$</td>
<td>DCO frequency (15, 3)</td>
<td>RSELx = 15, DCOx = 3, MODx = 0</td>
<td>3 V</td>
<td>12.0</td>
<td>18.5</td>
<td>MHz</td>
</tr>
<tr>
<td>$f_{DCO(15,7)}$</td>
<td>DCO frequency (15, 7)</td>
<td>RSELx = 15, DCOx = 7, MODx = 0</td>
<td>3 V</td>
<td>16.0</td>
<td>26.0</td>
<td>MHz</td>
</tr>
<tr>
<td>$S_{RSEL}$</td>
<td>Frequency step between range RSEL and RSEL+1</td>
<td>$S_{RSEL} = f_{DCO(RSEL+1,DCO)} / f_{DCO(RSEL,DCO)}$</td>
<td>3 V</td>
<td>1.35</td>
<td>ratio</td>
<td></td>
</tr>
<tr>
<td>$S_{DCO}$</td>
<td>Frequency step between tap DCO and DCO+1</td>
<td>$S_{DCO} = f_{DCO(DCO+1,DCO)} / f_{DCO(RSEL,DCO)}$</td>
<td>3 V</td>
<td>1.08</td>
<td>ratio</td>
<td></td>
</tr>
<tr>
<td>Duty cycle</td>
<td>Measured at SMCLK output</td>
<td>3 V</td>
<td>50</td>
<td>%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Calibrated DCO Frequencies, Tolerance
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th><strong>T&lt;sub&gt;A&lt;/sub&gt;</strong></th>
<th><strong>V&lt;sub&gt;CC&lt;/sub&gt;</strong></th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-MHz tolerance over temperature</td>
<td>BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V</td>
<td>0°C to 85°C</td>
<td>3 V</td>
<td>-3</td>
<td>±0.5</td>
<td>+3</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>30°C</td>
<td>1.8 V to 3.6 V</td>
<td>-3</td>
<td>±2</td>
<td>+3</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-40°C to 85°C</td>
<td>1.8 V to 3.6 V</td>
<td>-6</td>
<td>±3</td>
<td>+6</td>
<td>%</td>
</tr>
<tr>
<td>8-MHz tolerance over temperature</td>
<td>BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V</td>
<td>0°C to 85°C</td>
<td>3 V</td>
<td>-3</td>
<td>±0.5</td>
<td>+3</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>30°C</td>
<td>2.2 V to 3.6 V</td>
<td>-3</td>
<td>±2</td>
<td>+3</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-40°C to 85°C</td>
<td>2.2 V to 3.6 V</td>
<td>-6</td>
<td>±3</td>
<td>+6</td>
<td>%</td>
</tr>
<tr>
<td>12-MHz tolerance over temperature</td>
<td>BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V</td>
<td>0°C to 85°C</td>
<td>3 V</td>
<td>-3</td>
<td>±0.5</td>
<td>+3</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>30°C</td>
<td>2.7 V to 3.6 V</td>
<td>-3</td>
<td>±2</td>
<td>+3</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-40°C to 85°C</td>
<td>2.7 V to 3.6 V</td>
<td>-6</td>
<td>±3</td>
<td>+6</td>
<td>%</td>
</tr>
<tr>
<td>16-MHz tolerance over temperature</td>
<td>BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V</td>
<td>0°C to 85°C</td>
<td>3 V</td>
<td>-3</td>
<td>±0.5</td>
<td>+3</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>30°C</td>
<td>3.3 V to 3.6 V</td>
<td>-3</td>
<td>±2</td>
<td>+3</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-40°C to 85°C</td>
<td>3.3 V to 3.6 V</td>
<td>-6</td>
<td>±3</td>
<td>+6</td>
<td>%</td>
</tr>
</tbody>
</table>

(1) This is the frequency change from the measured frequency at 30°C over temperature.
Wake-Up From Lower-Power Modes (LPM3/4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$V_{CC}$</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{DCO,LPM3/4}$</td>
<td>DCO clock wake-up time from LPM3/4&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>3 V</td>
<td>1.5</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$t_{CPU,LPM3/4}$</td>
<td>CPU wake-up time from LPM3/4&lt;sup&gt;(2)&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) The DCO clock wake-up time is measured from the edge of an external wake-up signal (e.g., port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).

(2) Parameter applicable only if DCOCLK is used for MCLK.

Typical Characteristics, DCO Clock Wake-Up Time From LPM3/4

![Figure 15. DCO Wake-Up Time From LPM3 vs DCO Frequency](image_url)
Crystal Oscillator, XT1, Low-Frequency Mode\(^{(1)}\)
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>(V_{CC})</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(f_{LFXT1,LF})</td>
<td>LFXT1 oscillator crystal frequency, LF mode 0, 1</td>
<td>XTS = 0, LFXT1Sx = 0 or 1</td>
<td>1.8 V to 3.6 V</td>
<td>32768</td>
<td>Hz</td>
<td></td>
</tr>
<tr>
<td>(f_{LFXT1,LF,logic})</td>
<td>LFXT1 oscillator logic level square wave input frequency, LF mode</td>
<td>XTS = 0, XCAPx = 0, LFXT1Sx = 3</td>
<td>1.8 V to 3.6 V</td>
<td>10000 50000</td>
<td>Hz</td>
<td></td>
</tr>
<tr>
<td>(OA_{LF})</td>
<td>Oscillation allowance for LF crystals</td>
<td>XTS = 0, LFXT1Sx = 0, (f_{LFXT1,LF} = 32768) Hz, (C_{L,eff} = 6) pF</td>
<td>500</td>
<td>k\Omega</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(C_{L,eff})</td>
<td>Integrated effective load capacitance, LF mode(^{(2)})</td>
<td>XTS = 0, XCAPx = 0</td>
<td>1</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>XTS = 0, XCAPx = 1</td>
<td>5.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>XTS = 0, XCAPx = 2</td>
<td>8.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>XTS = 0, XCAPx = 3</td>
<td>11</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Duty cycle</td>
<td>LF mode</td>
<td>XTS = 0, Measured at P2.0/ACLK, (f_{LFXT1,LF} = 32768) Hz</td>
<td>2.2 V</td>
<td>30 50 70</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>(f_{Fault,LF})</td>
<td>Oscillator fault frequency, LF mode(^{(3)})</td>
<td>XTS = 0, XCAPx = 0, LFXT1Sx = 3(^{(4)})</td>
<td>2.2 V</td>
<td>10 10000</td>
<td>Hz</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
(a) Keep the trace between the device and the crystal as short as possible.
(b) Design a good ground plane around the oscillator pins.
(c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
(d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
(e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
(f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
(g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

\(^{(2)}\) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

\(^{(3)}\) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.

\(^{(4)}\) Measured with logic-level input frequency but also applies to operation with crystals.

Internal Very-Low-Power Low-Frequency Oscillator (VLO)
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>(T_{A})</th>
<th>(V_{CC})</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(f_{VLO})</td>
<td>VLO frequency</td>
<td>-40°C to 85°C</td>
<td>3 V</td>
<td>4 12 20</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>(df_{VLO}/dT)</td>
<td>VLO frequency temperature drift</td>
<td>-40°C to 85°C</td>
<td>3 V</td>
<td>0.5</td>
<td>%°C</td>
<td></td>
</tr>
<tr>
<td>(df_{VLO}/dV_{CC})</td>
<td>VLO frequency supply voltage drift</td>
<td>25°C</td>
<td>1.8 V to 3.6 V</td>
<td>4</td>
<td>%/V</td>
<td></td>
</tr>
</tbody>
</table>

Timer_A
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>(V_{CC})</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(f_{TA})</td>
<td>Timer_A input clock frequency</td>
<td>SMCLK, duty cycle = 50% ± 10%</td>
<td>(I_{\text{SYSTEM}})</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(\tau_{TA,\text{cap}})</td>
<td>Timer_A capture timing</td>
<td>TA0, TA1</td>
<td>3 V</td>
<td>20</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>
USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$V_{CC}$</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{USCI}$</td>
<td>USCI input clock frequency</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>SMCLK, duty cycle = 50% ± 10%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>$f_{max,BITCLK}$</td>
<td>Maximum BITCLK clock frequency (equals baudrate in MBaud)(^{(1)})</td>
<td>3 V</td>
<td>2</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>$t_{\tau}$</td>
<td>UART receive deglitch time(^{(2)})</td>
<td>3 V</td>
<td>50</td>
<td>100</td>
<td>600</td>
<td>ns</td>
</tr>
</tbody>
</table>

\(^{(1)}\) The DCO wake-up time must be considered in LPM3/4 for baud rates above 1 MHz.
\(^{(2)}\) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their width should exceed the maximum specification of the deglitch time.

USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 16 and Figure 17)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$V_{CC}$</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{USCI}$</td>
<td>USCI input clock frequency</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>SMCLK, duty cycle = 50% ± 10%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>$t_{SU,MI}$</td>
<td>SOMI input data setup time</td>
<td>3 V</td>
<td>75</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{HD,MI}$</td>
<td>SOMI input data hold time</td>
<td>3 V</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{VALID,MO}$</td>
<td>SIMO output data valid time</td>
<td>UCLK edge to SIMO valid, $C_L = 20 , \text{pF}$</td>
<td>3 V</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

\(^{(1)}\) The DCO wake-up time must be considered in LPM3/4 for baud rates above 1 MHz.

Figure 16. SPI Master Mode, CKPH = 0

Figure 17. SPI Master Mode, CKPH = 1
USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 18 and Figure 19)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>V&lt;sub&gt;CC&lt;/sub&gt;</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>t&lt;sub&gt;STE,LEAD&lt;/sub&gt;</td>
<td>STE lead time, STE low to clock</td>
<td>3 V</td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;STE,LAG&lt;/sub&gt;</td>
<td>STE lag time, Last clock to STE high</td>
<td>3 V</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;STE,ACC&lt;/sub&gt;</td>
<td>STE access time, STE low to SOMI data out</td>
<td>3 V</td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;STE,DIS&lt;/sub&gt;</td>
<td>STE disable time, STE high to SOMI high impedance</td>
<td>3 V</td>
<td>50</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;SU,SI&lt;/sub&gt;</td>
<td>SIMO input data setup time</td>
<td>3 V</td>
<td>15</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;HD,SI&lt;/sub&gt;</td>
<td>SIMO input data hold time</td>
<td>3 V</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;VALID,SO&lt;/sub&gt;</td>
<td>SOMI output data valid time</td>
<td>UCLK edge to SOMI valid, C&lt;sub&gt;L&lt;/sub&gt; = 20 pF</td>
<td>3 V</td>
<td>50</td>
<td>75</td>
<td>ns</td>
</tr>
</tbody>
</table>

Figure 18. SPI Slave Mode, CKPH = 0

Figure 19. SPI Slave Mode, CKPH = 1
USCI (I2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 20)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>( V_{CC} )</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{USCI} )</td>
<td>USCI input clock frequency</td>
<td>SMCLK, duty cycle = 50% ± 10%</td>
<td></td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>( f_{SCL} )</td>
<td>SCL clock frequency</td>
<td>3 V</td>
<td>0</td>
<td>400</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>( t_{HD,STA} )</td>
<td>Hold time (repeated) START</td>
<td>( f_{SCL} \leq 100 \text{ kHz} )</td>
<td>3 V</td>
<td>4.0</td>
<td>0.6</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( f_{SCL} &gt; 100 \text{ kHz} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{SU,STA} )</td>
<td>Setup time for a repeated START</td>
<td>( f_{SCL} \leq 100 \text{ kHz} )</td>
<td>3 V</td>
<td>4.7</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( f_{SCL} &gt; 100 \text{ kHz} )</td>
<td></td>
<td>0.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{HD,DAT} )</td>
<td>Data hold time</td>
<td>3 V</td>
<td>0</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{SU,DAT} )</td>
<td>Data setup time</td>
<td>3 V</td>
<td>250</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{SU,STO} )</td>
<td>Setup time for STOP</td>
<td>3 V</td>
<td>4.0</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>( t_{SP} )</td>
<td>Pulse width of spikes suppressed</td>
<td>3 V</td>
<td>50</td>
<td>100</td>
<td>600</td>
<td>ns</td>
</tr>
</tbody>
</table>

Figure 20. I2C Mode Timing
10-Bit ADC, Power Supply and Input Range Conditions (MSP430G2x33 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>T&lt;sub&gt;A&lt;/sub&gt;</th>
<th>V&lt;sub&gt;CC&lt;/sub&gt;</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>Analog supply voltage</td>
<td>V&lt;sub&gt;SS&lt;/sub&gt; = 0 V</td>
<td>2.2</td>
<td>3.6</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;Ax&lt;/sub&gt;</td>
<td>Analog input voltage (2)</td>
<td>All Ax terminals, Analog inputs selected in ADC10AE register</td>
<td>3 V</td>
<td>0</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;ADC10&lt;/sub&gt;</td>
<td>ADC10 supply current (3)</td>
<td>f&lt;sub&gt;ADC10CLK&lt;/sub&gt; = 5.0 MHz, ADC10ON = 1, REFON = 0, ADC10SHT0 = 1, ADC10SHT1 = 0, ADC10DIV = 0</td>
<td>25°C</td>
<td>3 V</td>
<td>0.6</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;REF+&lt;/sub&gt;</td>
<td>Reference supply current, reference buffer disabled (4)</td>
<td>f&lt;sub&gt;ADC10CLK&lt;/sub&gt; = 5.0 MHz, ADC10ON = 0, REF2_5V = 0, REFON = 1, REFOUT = 0</td>
<td>25°C</td>
<td>3 V</td>
<td>0.25</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;REFB,0&lt;/sub&gt;</td>
<td>Reference buffer supply current with ADC10SR = 0 (4)</td>
<td>f&lt;sub&gt;ADC10CLK&lt;/sub&gt; = 5.0 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 0</td>
<td>25°C</td>
<td>3 V</td>
<td>1.1</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;REFB,1&lt;/sub&gt;</td>
<td>Reference buffer supply current with ADC10SR = 1 (4)</td>
<td>f&lt;sub&gt;ADC10CLK&lt;/sub&gt; = 5.0 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 1</td>
<td>25°C</td>
<td>3 V</td>
<td>0.5</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>C&lt;sub&gt;i&lt;/sub&gt;</td>
<td>Input capacitance</td>
<td>Only one terminal Ax can be selected at one time</td>
<td>25°C</td>
<td>3 V</td>
<td>27</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>R&lt;sub&gt;i&lt;/sub&gt;</td>
<td>Input MUX ON resistance</td>
<td>0 V ≤ V&lt;sub&gt;Ax&lt;/sub&gt; ≤ V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>25°C</td>
<td>3 V</td>
<td>1000</td>
<td>Ω</td>
<td></td>
</tr>
</tbody>
</table>

(1) The leakage current is defined in the leakage current table with Px.y/Ax parameter.
(2) The analog input voltage range must be within the selected reference voltage range V<sub>R+</sub> to V<sub>R−</sub> for valid conversion results.
(3) The internal reference supply current is not included in current consumption parameter I<sub>ADC10</sub>.
(4) The internal reference current is supplied via terminal V<sub>CC</sub>. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables the built-in reference to settle before starting an A/D conversion.
## 10-Bit ADC, Built-In Voltage Reference (MSP430G2x33 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>Vcc</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CC,REF^+} ) Positive built-in reference analog supply voltage range</td>
<td>( I_{VREF^+} \leq 1 \text{ mA}, \text{REF2}<em>5\text{V} = 0 ) ( I</em>{VREF^+} \leq 1 \text{ mA}, \text{REF2}_5\text{V} = 1 )</td>
<td>2.2</td>
<td>2.9</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{REF^+} ) Positive built-in reference voltage</td>
<td>( I_{VREF^+} \leq I_{VREF^+}\text{max}, \text{REF2}<em>5\text{V} = 0 ) ( I</em>{VREF^+} \leq I_{VREF^+}\text{max}, \text{REF2}_5\text{V} = 1 )</td>
<td>3 V</td>
<td>1.41</td>
<td>1.5</td>
<td>1.59</td>
<td>V</td>
</tr>
<tr>
<td>( I_{LD,VREF^+} ) Maximum VREF+ load current</td>
<td>( I_{VREF^+} \leq \text{const} \text{with } 0 \text{ mA} \leq I_{VREF^+} \leq 1 \text{ mA} )</td>
<td>3 V</td>
<td>±2</td>
<td></td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td>( V_{REF^+} \text{ load regulation } )</td>
<td>( I_{VREF^+} = 500 \mu A \pm 100 \mu A ), ( V_{Ax} \neq 0.75 \text{ V} ), ( \text{REF2}_5\text{V} = 0 )</td>
<td>3 V</td>
<td></td>
<td>±2</td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td>( V_{REF^+} \text{ load regulation response time } )</td>
<td>( I_{VREF^+} = 500 \mu A \pm 100 \mu A ), ( V_{Ax} \neq 1.25 \text{ V} ), ( \text{REF2}_5\text{V} = 1 )</td>
<td>3 V</td>
<td></td>
<td>±2</td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td>( C_{VREF^+} ) Maximum capacitance at pin VREF+</td>
<td>( I_{VREF^+} \leq \pm 1 \text{ mA} ), ( \text{REFON} = 1 ), ( \text{REFOUT} = 1 )</td>
<td>3 V</td>
<td>100</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( T_{C_{REF^+}} ) Temperature coefficient</td>
<td>( I_{VREF^+} = \text{const} \text{ with } 0 \text{ mA} \leq I_{VREF^+} \leq 1 \text{ mA} )</td>
<td>3 V</td>
<td>±100</td>
<td>ppm/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{REFON} ) Settling time of internal reference voltage to 99.9% VREF</td>
<td>( I_{VREF^+} = 0.5 \text{ mA} ), ( \text{REF2}_5\text{V} = 0 ), ( \text{REFON} = 0 \rightarrow 1 )</td>
<td>3.6 V</td>
<td>30</td>
<td>µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{REFBURST} ) Settling time of reference buffer to 99.9% VREF</td>
<td>( I_{VREF^+} = 0.5 \text{ mA} ), ( \text{REF2}_5\text{V} = 1 ), ( \text{REFON} = 1 ), ( \text{REFBURST} = 1 ), ( \text{ADC10SR} = 0 )</td>
<td>3 V</td>
<td>2</td>
<td>µs</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
# 10-Bit ADC, External Reference

**(MSP430G2x33 Only)**

Over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>( V_{CC} )</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{EREF}^+ )</td>
<td>Positive external reference input voltage range</td>
<td>( V_{EREF}^+ &gt; V_{EREF}^-, ) ( SREF1 = 1, SREF0 = 0 )</td>
<td>1.4</td>
<td>( V_{CC} )</td>
<td>3</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{EREF}^- \leq V_{EREF}^+ \leq V_{CC} - 0.15 ) V, ( SREF1 = 1, SREF0 = 1 )</td>
<td>1.4</td>
<td>3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{EREF}^- )</td>
<td>Negative external reference input voltage range</td>
<td>( V_{EREF}^+ &gt; V_{EREF}^- )</td>
<td>0</td>
<td>1.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( \Delta V_{EREF} )</td>
<td>Differential external reference input voltage range, ( \Delta V_{EREF} = V_{EREF}^+ - V_{EREF}^- )</td>
<td>( V_{EREF}^+ &gt; V_{EREF}^- )</td>
<td>1.4</td>
<td>( V_{CC} )</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_{V_{EREF}^+} )</td>
<td>Static input current into ( V_{EREF}^+ )</td>
<td>( 0 \leq V_{EREF}^+ \leq V_{CC} - 0.15 ) V, ( SREF1 = 1, SREF0 = 0 )</td>
<td>3 V</td>
<td>±1</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( 0 \leq V_{EREF}^- \leq V_{CC} - 0.15 \leq 3 ) V, ( SREF1 = 1, SREF0 = 1 )</td>
<td>3 V</td>
<td>0</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>( I_{V_{EREF}^-} )</td>
<td>Static input current into ( V_{EREF}^- )</td>
<td>( 0 \leq V_{EREF}^- \leq V_{CC} )</td>
<td>3 V</td>
<td>±1</td>
<td>( \mu A )</td>
<td></td>
</tr>
</tbody>
</table>

(1) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, \( C_I \), is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.

(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.

(3) Under this condition the external reference is internally buffered. The reference buffer is active and requires the reference buffer supply current \( I_{REFB} \). The current consumption can be limited to the sample and conversion period with \( \text{REBURST} = 1 \).

(4) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.

(5) The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

# 10-Bit ADC, Timing Parameters

**(MSP430G2x33 Only)**

Over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>( V_{CC} )</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{ADC10CLK} )</td>
<td>ADC10 input clock frequency</td>
<td>For specified performance of ADC10 linearity parameters</td>
<td>3 V</td>
<td>0.45</td>
<td>6.3</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( ADC10SR = 0 )</td>
<td></td>
<td>0.45</td>
<td>1.5</td>
<td>MHz</td>
</tr>
<tr>
<td>( f_{ADC10OSC} )</td>
<td>ADC10 built-in oscillator frequency</td>
<td>( ADC10DIVx = 0, ADC10SSEx = 0, f_{ADC10CLK} = f_{ADC10OSC} )</td>
<td>3 V</td>
<td>3.7</td>
<td>6.3</td>
<td>MHz</td>
</tr>
<tr>
<td>( f_{CONVERT} )</td>
<td>Conversion time</td>
<td>ADC10 built-in oscillator, ( ADC10SSEx = 0, f_{ADC10CLK} = f_{ADC10OSC} )</td>
<td>3 V</td>
<td>2.06</td>
<td>3.51</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( f_{ADC10ON} )</td>
<td>Turn-on settling time of the ADC</td>
<td>From ACLK, MCLK, or SMCLK: ( ADC10SSEx \neq 0 )</td>
<td></td>
<td>13 \times \frac{1}{f_{ADC10DIV}} \times \frac{1}{f_{ADC10CLK}}</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) The condition is that the error in a conversion started after \( f_{ADC10ON} \) is less than ±0.5 LSB. The reference and input signal are already settled.

# 10-Bit ADC, Linearity Parameters

**(MSP430G2x33 Only)**

Over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>( V_{CC} )</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( E_I )</td>
<td>Integral linearity error</td>
<td>3 V</td>
<td>±1</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( E_D )</td>
<td>Differential linearity error</td>
<td>3 V</td>
<td>±1</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( E_O )</td>
<td>Offset error</td>
<td>Source impedance ( R_S &lt; 100 ) Ω</td>
<td>3 V</td>
<td>±1</td>
<td>LSB</td>
<td></td>
</tr>
<tr>
<td>( E_G )</td>
<td>Gain error</td>
<td>3 V</td>
<td>±1.1</td>
<td>±2</td>
<td>LSB</td>
<td></td>
</tr>
<tr>
<td>( E_T )</td>
<td>Total unadjusted error</td>
<td>3 V</td>
<td>±2</td>
<td>±5</td>
<td>LSB</td>
<td></td>
</tr>
</tbody>
</table>
10-Bit ADC, Temperature Sensor and Built-In $V_{\text{MID}}$ (MSP430G2x33 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$V_{\text{CC}}$</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{\text{SENSOR}}$</td>
<td>Temperature sensor supply current $^{(1)}$</td>
<td>$\text{REFON} = 0$, $\text{INCH} = 0\text{Ah}$, $T_A = 25^\circ\text{C}$</td>
<td>3 V</td>
<td>60</td>
<td></td>
<td>$\mu\text{A}$</td>
</tr>
<tr>
<td>$T_{\text{SENSOR}}$</td>
<td>Sample time required if channel 10 is selected $^{(3)}$</td>
<td>$\text{ADC10ON} = 1$, $\text{INCH} = 0\text{Ah}$, Error of conversion result $\leq 1$ LSB</td>
<td>3 V</td>
<td>30</td>
<td></td>
<td>$\mu\text{s}$</td>
</tr>
<tr>
<td>$I_{\text{VMID}}$</td>
<td>Current into divider at channel 11</td>
<td>$\text{ADC10ON} = 1$, $\text{INCH} = 0\text{Bh}$</td>
<td>3 V</td>
<td></td>
<td></td>
<td>$\mu\text{A}$</td>
</tr>
<tr>
<td>$V_{\text{MID}}$</td>
<td>$V_{\text{CC}}$ divider at channel 11</td>
<td>$\text{ADC10ON} = 1$, $\text{INCH} = 0\text{Bh}$, $V_{\text{MID}} = 0.5 \times V_{\text{CC}}$</td>
<td>3 V</td>
<td>1.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{\text{VMID(sample)}}$</td>
<td>Sample time required if channel 11 is selected $^{(5)}$</td>
<td>$\text{ADC10ON} = 1$, $\text{INCH} = 0\text{Bh}$, Error of conversion result $\leq 1$ LSB</td>
<td>3 V</td>
<td>1220</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

$^{(1)}$ The sensor current $I_{\text{SENSOR}}$ is consumed if ($\text{ADC10ON} = 1$ and $\text{REFON} = 1$) or ($\text{ADC10ON} = 1$ and $\text{INCH} = 0\text{Ah}$ and sample signal is high). When $\text{REFON} = 1$, $I_{\text{SENSOR}}$ is included in $I_{\text{REF+}}$. When $\text{REFON} = 0$, $I_{\text{SENSOR}}$ applies during conversion of the temperature sensor input ($\text{INCH} = 0\text{Ah}$).

$^{(2)}$ The following formula can be used to calculate the temperature sensor output voltage:

$$V_{\text{Sensor,typ}} = T_{\text{Sensor}}(273 + T_{[\circ\text{C}]} + V_{\text{Offset,sensor}}) \text{[mV]} \text{ or } V_{\text{Sensor,typ}} = T_{[\circ\text{C}]} + V_{\text{Sensor}}(T_{[\circ\text{C}]} = 0) \text{[mV]}$$

$^{(3)}$ The typical equivalent impedance of the sensor is 51 $\Omega$. The sample time required includes the sensor-on time $t_{\text{SENSOR(on)}}$.

$^{(4)}$ No additional current is needed. The $V_{\text{MID}}$ is used during sampling.

$^{(5)}$ The on-time $t_{\text{VMID(on)}}$ is included in the sampling time $t_{\text{VMID(sample)}}$; no additional on time is needed.

Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$V_{\text{CC}}$</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{CC(PGM/ERASE)}}$</td>
<td>Program and erase supply voltage</td>
<td>2.2</td>
<td>3.6</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f_{\text{FTG}}$</td>
<td>Flash timing generator frequency</td>
<td>257</td>
<td>476</td>
<td>kHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{\text{PGM}}$</td>
<td>Supply current from $V_{\text{CC}}$ during program</td>
<td>2.2 $V/3.6 V$</td>
<td>1</td>
<td>5</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{\text{ERASE}}$</td>
<td>Supply current from $V_{\text{CC}}$ during erase</td>
<td>2.2 $V/3.6 V$</td>
<td>1</td>
<td>7</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$t_{\text{CPT}}$</td>
<td>Cumulative program time $^{(1)}$</td>
<td>2.2 $V/3.6 V$</td>
<td>10</td>
<td></td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>$t_{\text{CMErase}}$</td>
<td>Cumulative mass erase time</td>
<td>2.2 $V/3.6 V$</td>
<td>20</td>
<td></td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>$t_{\text{Retention}}$</td>
<td>Data retention duration</td>
<td>$T_J = 25^\circ\text{C}$</td>
<td>100</td>
<td></td>
<td>years</td>
<td>cycles</td>
</tr>
<tr>
<td>$t_{\text{Word}}$</td>
<td>Word or byte program time $^{(2)}$</td>
<td>30</td>
<td>25</td>
<td>$f_{\text{FTG}}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{\text{Block, 0}}$</td>
<td>Block program time for first byte or word $^{(2)}$</td>
<td>18</td>
<td>6</td>
<td>$f_{\text{FTG}}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{\text{Block, 1-63}}$</td>
<td>Block program time for each additional byte or word $^{(2)}$</td>
<td>1</td>
<td>8</td>
<td>$f_{\text{FTG}}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{\text{Block, End}}$</td>
<td>Block program end-sequence wait time $^{(2)}$</td>
<td>6</td>
<td>$f_{\text{FTG}}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{\text{Mass Erase}}$</td>
<td>Mass erase time</td>
<td>10593</td>
<td>$f_{\text{FTG}}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{\text{Seg Erase}}$</td>
<td>Segment erase time $^{(2)}$</td>
<td>4819</td>
<td>$f_{\text{FTG}}$</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

$^{(1)}$ The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.

$^{(2)}$ These values are hardwired into the Flash Controller's state machine ($f_{\text{FTG}} = 1/f_{\text{FTG}}$).
RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{RAMh}}$</td>
<td>RAM retention supply voltage (1)</td>
<td>CPU halted</td>
<td>1.6</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) This parameter defines the minimum supply voltage $V_{CC}$ when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$V_{CC}$</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{\text{SBW}}$</td>
<td>Spy-Bi-Wire input frequency</td>
<td>2.2 V</td>
<td>0</td>
<td>20</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>$t_{\text{SBW,Low}}$</td>
<td>Spy-Bi-Wire low clock pulse length</td>
<td>2.2 V</td>
<td>0.025</td>
<td>15</td>
<td>$\mu$s</td>
<td></td>
</tr>
<tr>
<td>$t_{\text{SBW,En}}$</td>
<td>Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge(1))</td>
<td>2.2 V</td>
<td>1</td>
<td>$\mu$s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{\text{SBW,Ret}}$</td>
<td>Spy-Bi-Wire return to normal operation time</td>
<td>2.2 V</td>
<td>15</td>
<td>100</td>
<td>$\mu$s</td>
<td></td>
</tr>
<tr>
<td>$f_{\text{TCK}}$</td>
<td>TCK input frequency(2)</td>
<td>2.2 V</td>
<td>0</td>
<td>5</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>$R_{\text{Internal}}$</td>
<td>Internal pulldown resistance on TEST</td>
<td>2.2 V</td>
<td>25</td>
<td>60</td>
<td>90 kΩ</td>
<td></td>
</tr>
</tbody>
</table>

(1) Tools accessing the Spy-Bi-Wire interface need to wait for the maximum $t_{\text{SBW,En}}$ time after pulling the TEST/SBWCLK pin high before applying the first SBWCLK clock edge.
(2) $f_{\text{TCK}}$ may be restricted to meet the timing requirements of the module selected.

JTAG Fuse (1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{CC(FB)}}$</td>
<td>Supply voltage during fuse-blow condition</td>
<td>$T_A = 25^\circ$C</td>
<td>2.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{FB}}$</td>
<td>Voltage level on TEST for fuse blow</td>
<td>6</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>$I_{\text{FB}}$</td>
<td>Supply current into TEST during fuse blow</td>
<td>100</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$t_{\text{FB}}$</td>
<td>Time to blow fuse</td>
<td>1</td>
<td>ms</td>
<td></td>
</tr>
</tbody>
</table>

(1) Once the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, and emulation feature is possible, and JTAG is switched to bypass mode.
PORT SCHEMATICS

Port P1 Pin Schematic: P1.0 to P1.2, Input/Output With Schmitt Trigger

* Note: MSP430G2x33 devices only. MSP430G2x03 devices have no ADC10.
Table 16. Port P1 (P1.0 to P1.2) Pin Functions

<table>
<thead>
<tr>
<th>PIN NAME (P1.x)</th>
<th>x</th>
<th>FUNCTION</th>
<th>CONTROL BITS / SIGNALS(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>P1DIR.x</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P1.0/ TA0CLK/</td>
<td>0</td>
<td>P1.x (I/O)</td>
<td>I: 0; O: 1</td>
</tr>
<tr>
<td>ACLK/ A0(2)/</td>
<td></td>
<td>TA0.TACLK</td>
<td>0</td>
</tr>
<tr>
<td>Pin Osc</td>
<td></td>
<td>ACLK</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A0</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Capacitive sensing</td>
<td>X</td>
</tr>
<tr>
<td>P1.1/ TA0.0/</td>
<td>1</td>
<td>P1.x (I/O)</td>
<td>I: 0; O: 1</td>
</tr>
<tr>
<td>UCA0RXD/ UCA0SOMI/ A1(2)/</td>
<td>1</td>
<td>TA0.0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TA0.CC10A</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>UCA0RXD from USCI</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>UCA0SOMI from USCI</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A1</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Capacitive sensing</td>
<td>X</td>
</tr>
<tr>
<td>P1.2/ TA0.1/</td>
<td>2</td>
<td>P1.x (I/O)</td>
<td>I: 0; O: 1</td>
</tr>
<tr>
<td>UCA0TXD/ UCA0SIMO/ A2(2)/</td>
<td>2</td>
<td>TA0.1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TA0.CC11A</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>UCA0TXD from USCI</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>UCA0SIMO from USCI</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A2</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Capacitive sensing</td>
<td>X</td>
</tr>
</tbody>
</table>

(1) X = don’t care
(2) MSP430G2x33 devices only
Port P1 Pin Schematic: P1.3, Input/Output With Schmitt Trigger

* Note: MSP430G2x33 devices only. MSP430G2x03 devices have no ADC10.
Table 17. Port P1 (P1.3) Pin Functions

<table>
<thead>
<tr>
<th>PIN NAME (P1.x)</th>
<th>x</th>
<th>FUNCTION</th>
<th>CONTROL BITS / SIGNALS(1)</th>
<th>ADC10AE.x (INCH.x = 1)(2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1.3/ADC10CLK(2)/A3(2)/VREF-(2)/VEREF-(2)/Pin Osc</td>
<td>3</td>
<td>P1.x (I/O)</td>
<td>P1DIR.x  P1SEL.x  P1SEL2.x</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ADC10CLK</td>
<td>1  1  0  0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A3</td>
<td>X  X  X  1 (y = 3)</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VREF-</td>
<td>X  X  X  1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VREF-</td>
<td>X  X  X  1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pin Osc</td>
<td>X  0  1  0</td>
<td>0</td>
</tr>
</tbody>
</table>

(1) X = don’t care
(2) MSP430G2x33 devices only
Port P1 Pin Schematic: P1.4, Input/Output With Schmitt Trigger

* Note: MSP430G2x33 devices only. MSP430G2x03 devices have no ADC10.
## Table 18. Port P1 (P1.4) Pin Functions

<table>
<thead>
<tr>
<th>PIN NAME  (P1.x)</th>
<th>x</th>
<th>FUNCTION</th>
<th>CONTROL BITS / SIGNALS&lt;sup&gt;(1)&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1.4/SMCLK/UCB0STE/UCA0CLK/VREF+/A4/TCK/Pin Osc</td>
<td>4</td>
<td>P1.x (I/O)</td>
<td>P1DIR.x  P1SEL.x P1SEL2.x ADC10AE.x (INCH.x = 1)&lt;sup&gt;(2)&lt;/sup&gt; JTAG Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SMCLK</td>
<td>1 0 0 0 0 0 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>UCB0STE</td>
<td>1 1 1 0 0 0 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>UCA0CLK</td>
<td>1 1 1 0 0 0 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VREF+</td>
<td>X X X 1 0 0 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VREF+</td>
<td>X X X 1 0 0 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VREF+</td>
<td>X X X 1 0 0 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A4</td>
<td>X X X 1 (y = 4) 0 0 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TCK</td>
<td>X X X 0 1 0 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Capacitive sensing</td>
<td>X 0 1 0 0 0 0</td>
</tr>
</tbody>
</table>

<sup>(1)</sup> X = don’t care
<sup>(2)</sup> MSP430G2x33 devices only
Port P1 Pin Schematic: P1.5 to P1.7, Input/Output With Schmitt Trigger

* Note: MSP430G2x33 devices only. MSP430G2x03 devices have no ADC10.
### Table 19. Port P1 (P1.5 to P1.7) Pin Functions

<table>
<thead>
<tr>
<th>PIN NAME (P1.x)</th>
<th>x</th>
<th>FUNCTION</th>
<th>CONTROL BITS / SIGNALS&lt;sup&gt;(1)&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1.5/TA0.0/UCB0CLK/UCA0STEE/A5&lt;sup&gt;(2)&lt;/sup&gt;/TMS/Pin Osc</td>
<td>5</td>
<td>P1.x (I/O)</td>
<td>P1DIR.x</td>
</tr>
<tr>
<td>TA0.0</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>UCB0CLK</td>
<td></td>
<td>UCB0CLK</td>
<td>1</td>
</tr>
<tr>
<td>UCA0STEE</td>
<td></td>
<td>UCA0STEE</td>
<td>1</td>
</tr>
<tr>
<td>A5</td>
<td></td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>TMS</td>
<td></td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Pin Osc</td>
<td></td>
<td>Capacitive sensing</td>
<td>X</td>
</tr>
<tr>
<td>P1.6/TA0.1/UCB0SOMI/UCB0SCL/A6&lt;sup&gt;(2)&lt;/sup&gt;/TDI/TCLK/Pin Osc</td>
<td>6</td>
<td>P1.x (I/O)</td>
<td>P1DIR.x</td>
</tr>
<tr>
<td>TA0.1</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>UCB0SOMI</td>
<td></td>
<td>UCB0SOMI</td>
<td>1</td>
</tr>
<tr>
<td>UCB0SCL</td>
<td></td>
<td>UCB0SCL</td>
<td>1</td>
</tr>
<tr>
<td>A6</td>
<td></td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>TDI/TCLK</td>
<td></td>
<td>TDI/TCLK</td>
<td>X</td>
</tr>
<tr>
<td>Pin Osc</td>
<td></td>
<td>Capacitive sensing</td>
<td>X</td>
</tr>
<tr>
<td>P1.7/UCB0SIMO/UCB0SDA/A7&lt;sup&gt;(2)&lt;/sup&gt;/TDI/TDI/Pin Osc</td>
<td>7</td>
<td>P1.x (I/O)</td>
<td>P1DIR.x</td>
</tr>
<tr>
<td>UCB0SIMO</td>
<td></td>
<td>UCB0SIMO</td>
<td>1</td>
</tr>
<tr>
<td>UCB0SDA</td>
<td></td>
<td>UCB0SDA</td>
<td>1</td>
</tr>
<tr>
<td>A7</td>
<td></td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>TDO/TDI</td>
<td></td>
<td>TDO/TDI</td>
<td>X</td>
</tr>
<tr>
<td>Pin Osc</td>
<td></td>
<td>Capacitive sensing</td>
<td>X</td>
</tr>
</tbody>
</table>

<sup>(1)</sup> X = don't care  
<sup>(2)</sup> MSP430G2x33 devices only
Port P2 Pin Schematic: P2.0 to P2.5, Input/Output With Schmitt Trigger
<table>
<thead>
<tr>
<th>PIN NAME (P2.x)</th>
<th>x</th>
<th>FUNCTION</th>
<th>CONTROL BITS / SIGNALS&lt;sup&gt;(1)&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>P2.0/ TA1.0/ Pin Osc</td>
<td>0</td>
<td>P2.x (I/O)</td>
<td>I: 0; O: 1</td>
</tr>
<tr>
<td>Timer1_A3.CCIOA</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Timer1_A3.TA0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Capacitive sensing</td>
<td>X</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>P2.1/ TA1.1/ Pin Osc</td>
<td>1</td>
<td>P2.x (I/O)</td>
<td>I: 0; O: 1</td>
</tr>
<tr>
<td>Timer1_A3.CCIA</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Timer1_A3.TA1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Capacitive sensing</td>
<td>X</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Pin Osc</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
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<sup>(1)</sup> X = don't care
Port P2 Pin Schematic: P2.6, Input/Output With Schmitt Trigger
## Table 21. Port P2 (P2.6) Pin Functions

<table>
<thead>
<tr>
<th>PIN NAME (P2.x)</th>
<th>x</th>
<th>FUNCTION</th>
<th>CONTROL BITS / SIGNALS&lt;sup&gt;(1)&lt;/sup&gt;</th>
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(1) X = don't care
Table 22. Port P2 (P2.7) Pin Functions

<table>
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<th>PIN NAME (P2.x)</th>
<th>x</th>
<th>FUNCTION</th>
<th>CONTROL BITS / SIGNALS(^{(1)})</th>
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</thead>
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<td>P2DIR.x</td>
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<tr>
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<td>X</td>
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\(^{(1)}\) X = don't care
Port P3 Pin Schematic: P3.0 to P3.7, Input/Output With Schmitt Trigger (RHB Package Only)
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<th>FUNCTION</th>
<th>CONTROL BITS / SIGNALS(1)</th>
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</thead>
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<td>P3.x (I/O)</td>
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<td>1</td>
</tr>
<tr>
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<td>P3.x (I/O)</td>
<td>P3DIR.x</td>
</tr>
<tr>
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<tr>
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</tr>
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<td>P3.x (I/O)</td>
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<td>1</td>
</tr>
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<td>P3DIR.x</td>
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</tr>
<tr>
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<td>1</td>
</tr>
<tr>
<td>P3.4/TA0.0/Pin Osc</td>
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<td>P3.x (I/O)</td>
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<tr>
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</tr>
<tr>
<td>P3.5/TA0.1/Pin Osc</td>
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<td>P3.x (I/O)</td>
<td>P3DIR.x</td>
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<td>0</td>
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<tr>
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<td>P3DIR.x</td>
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(1) X = don't care
## REVISION HISTORY

<table>
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<tr>
<th>REVISION</th>
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<tr>
<td>SLAS734</td>
<td>Production Data release</td>
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| SLAS734A  | Corrections to Control Bits / Signals column in Table 18  
Corrections to Pin Name and Function columns in Table 23 |
| SLAS734B  | Changed Storage temperature range limit in Absolute Maximum Ratings  
Added BSL functions to P1.1 and P1.5 in Table 2  
Port P1 Pin Schematic, corrected pin name |
| SLAS734C  | Changed $T_{\text{stg}}$, Programmed device, to $-55°C$ to $150°C$ in Absolute Maximum Ratings.  
Changed TAG_ADC10_1 value to 0x10 in Table 10. |
| SLAS734D  | Added AVCC (RHB package only, pin 29) to Table 2 Terminal Functions.  
Correct typo in P3.7/TA1CLK description in Table 2.  
Corrected pin number for PW28 Input and Output columns in Table 13.  
Changed all port schematics (added buffer after PxOUT,y mux) in Port Schematics. |
<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead finish/ Ball material</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
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<tbody>
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<td>PDIP</td>
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<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>M430G2203</td>
<td>Samples</td>
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<td>MSP430G2203IPW20</td>
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<td>TSSOP</td>
<td>PW</td>
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<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>430G2203</td>
<td>Samples</td>
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<td>Samples</td>
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<td>-40 to 85</td>
<td>M430G2233</td>
<td>Samples</td>
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<td>Op Temp (°C)</td>
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<td>Samples</td>
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(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
 OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤1000ppm threshold. Antimony trioxide based flame retardants must also meet the ≤1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
### TAPE AND REEL INFORMATION

#### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

#### REEL DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Q1**: Pocket Quadrants
- **Q2**: Sprocket Holes
- **Q3**: User Direction of Feed

*All dimensions are nominal*

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**PACKAGE MATERIALS INFORMATION**

www.ti.com

**TUBE**

- **T** - Tube height
- **W** - Tube width
- **B** - Alignment groove width

*All dimensions are nominal*

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PLASTIC DUAL-IN-LINE PACKAGE

PINS **

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MS–001 VARIATION

|        | AA | BB | AC | AD |

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.
NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side.

E. Falls within JEDEC MO-153
NOTE:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Publication IPC-7351 is recommended for alternate design.  
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.  
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
Example Board Layout

Based on a stencil thickness of .127mm (.005 inch).

Example Non Soldermask Defined Pad

Example Solder Mask Opening (See Note E)

Pad Geometry

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.
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