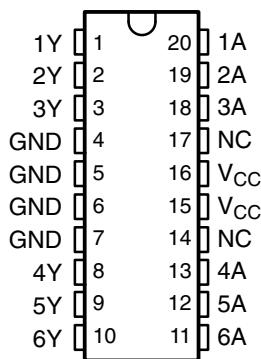


- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V<sub>CC</sub> and GND Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, and Standard Plastic 300-mil DIPs (N)

DB, DW, OR N PACKAGE  
(TOP VIEW)

NC – No internal connection

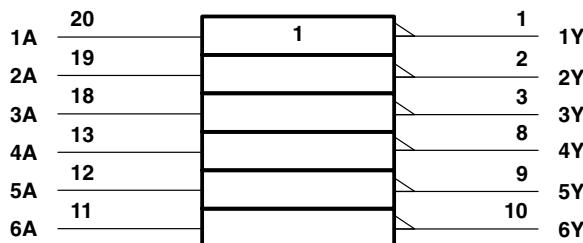
## description

This device contains six independent inverters. It performs the Boolean function  $Y = \bar{A}$ .

The 74AC11004 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic symbol<sup>†</sup>

<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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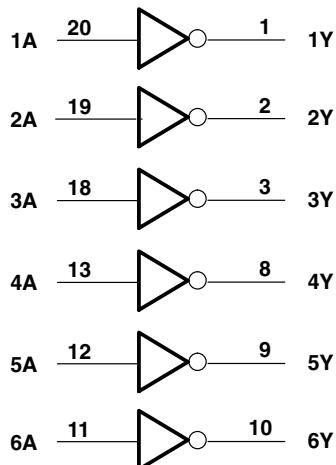
**TEXAS  
INSTRUMENTS**

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# 74AC11004 HEX INVERTER

SCAS033B – JANUARY 1988 – REVISED APRIL 1996

## logic diagram (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V	
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V	
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V	
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA	
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 50$ mA	
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 50$ mA	
Continuous current through $V_{CC}$ or GND .....	$\pm 100$ mA	
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DW package .....	1.6 W	
	DB package .....	0.6 W
	N package .....	1.3 W
Storage temperature range, $T_{Stg}$ .....	-65°C to 150°C	

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

**recommended operating conditions**

			MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage		3	5	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 3\text{ V}$	2.1			V
		$V_{CC} = 4.5\text{ V}$	3.15			
		$V_{CC} = 5.5\text{ V}$	3.85			
$V_{IL}$	Low-level input voltage	$V_{CC} = 3\text{ V}$		0.9		V
		$V_{CC} = 4.5\text{ V}$		1.35		
		$V_{CC} = 5.5\text{ V}$		1.65		
$V_I$	Input voltage		0	$V_{CC}$		V
$V_O$	Output voltage		0	$V_{CC}$		V
$I_{OH}$	High-level output current	$V_{CC} = 3\text{ V}$		-4		mA
		$V_{CC} = 4.5\text{ V}$		-24		
		$V_{CC} = 5.5\text{ V}$		-24		
$I_{OL}$	Low-level output current	$V_{CC} = 3\text{ V}$		12		mA
		$V_{CC} = 4.5\text{ V}$		24		
		$V_{CC} = 5.5\text{ V}$		24		
$\Delta t/\Delta V$	Input transition rise or fall rate		0	10	ns/V	
$T_A$	Operating free-air temperature		-40	85	$^{\circ}\text{C}$	

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^{\circ}\text{C}$			UNIT
			MIN	TYP	MAX	
$V_{OH}$	$I_{OH} = -50\text{ }\mu\text{A}$	3 V	2.9		2.9	V
		4.5 V	4.4		4.4	
		5.5 V	5.4		5.4	
	$I_{OH} = -4\text{ mA}$	3 V	2.58		2.48	
		4.5 V	3.94		3.8	
	$I_{OH} = -24\text{ mA}$	5.5 V	4.94		4.8	
		5.5 V			3.85	
	$I_{OL} = 50\text{ }\mu\text{A}$	3 V		0.1	0.1	
		4.5 V		0.1	0.1	
		5.5 V		0.1	0.1	
	$I_{OL} = 12\text{ mA}$	3 V		0.36	0.44	
		4.5 V		0.36	0.44	
	$I_{OL} = 24\text{ mA}$	5.5 V		0.36	0.44	
		5.5 V			1.65	
$I_I$	$V_I = V_{CC}$ or GND	5.5 V		$\pm 0.1$	$\pm 1$	$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		4	40	$\mu\text{A}$
$C_i$	$V_I = V_{CC}$ or GND	5 V		3.5		$\text{pF}$

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

# 74AC11004 HEX INVERTER

SCAS033B – JANUARY 1988 – REVISED APRIL 1996

**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$t_{PLH}$	A	Y	1.5	6.1	9	1.5	10	ns
			1.5	5.2	7.4	1.5	8.2	

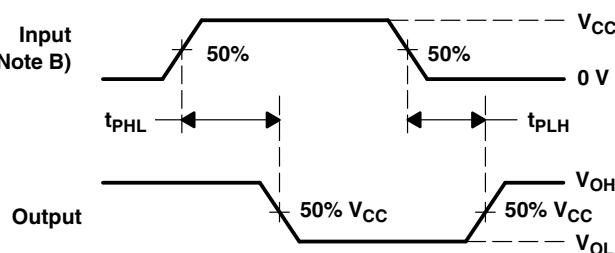
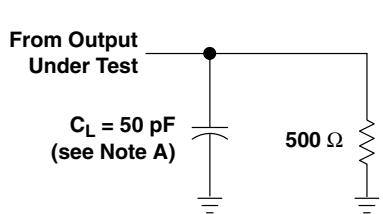
**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$t_{PLH}$	A	Y	1.5	4.2	6.3	1.5	7.1	ns
			1.5	3.8	5.5	1.5	6	

**operating characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance per inverter	$C_L = 50 \text{ pF}$ , $f = 1 \text{ MHz}$	29	pF

## PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Input pulses are supplied by generators having the following characteristics: PRR  $\leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74AC11004DW	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	-40 to 85	AC11004
74AC11004DWR	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC11004
74AC11004DWR.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC11004
74AC11004N	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	74AC11004N
74AC11004N.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	74AC11004N

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

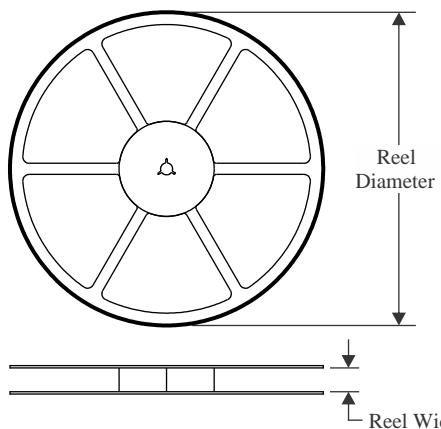
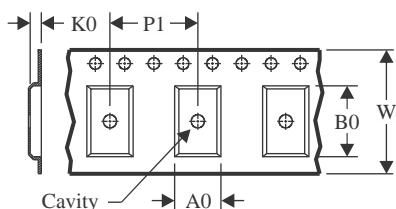
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

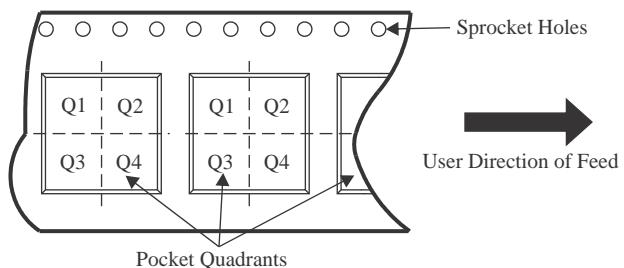
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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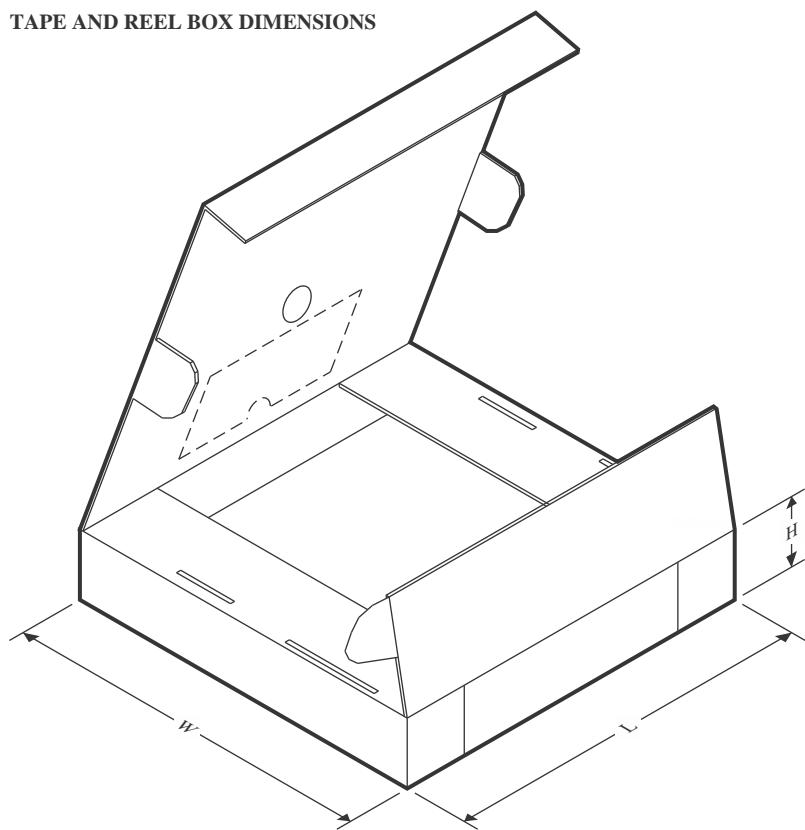
**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


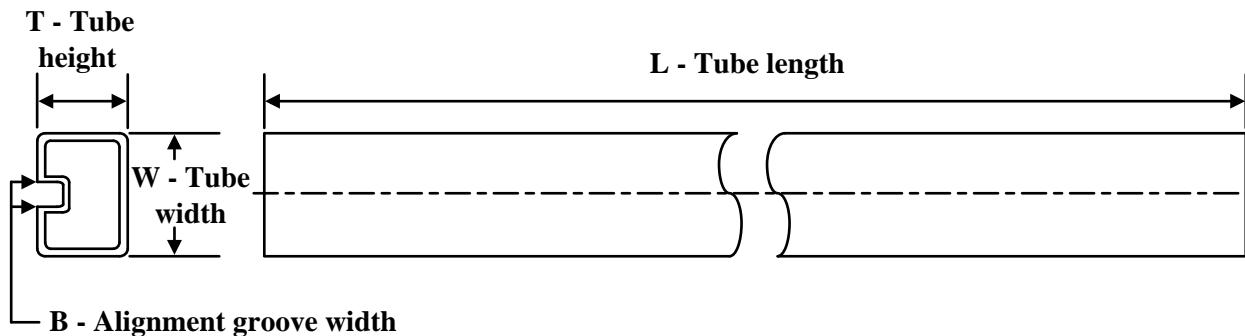
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AC11004DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AC11004DWR	SOIC	DW	20	2000	356.0	356.0	45.0

**TUBE**


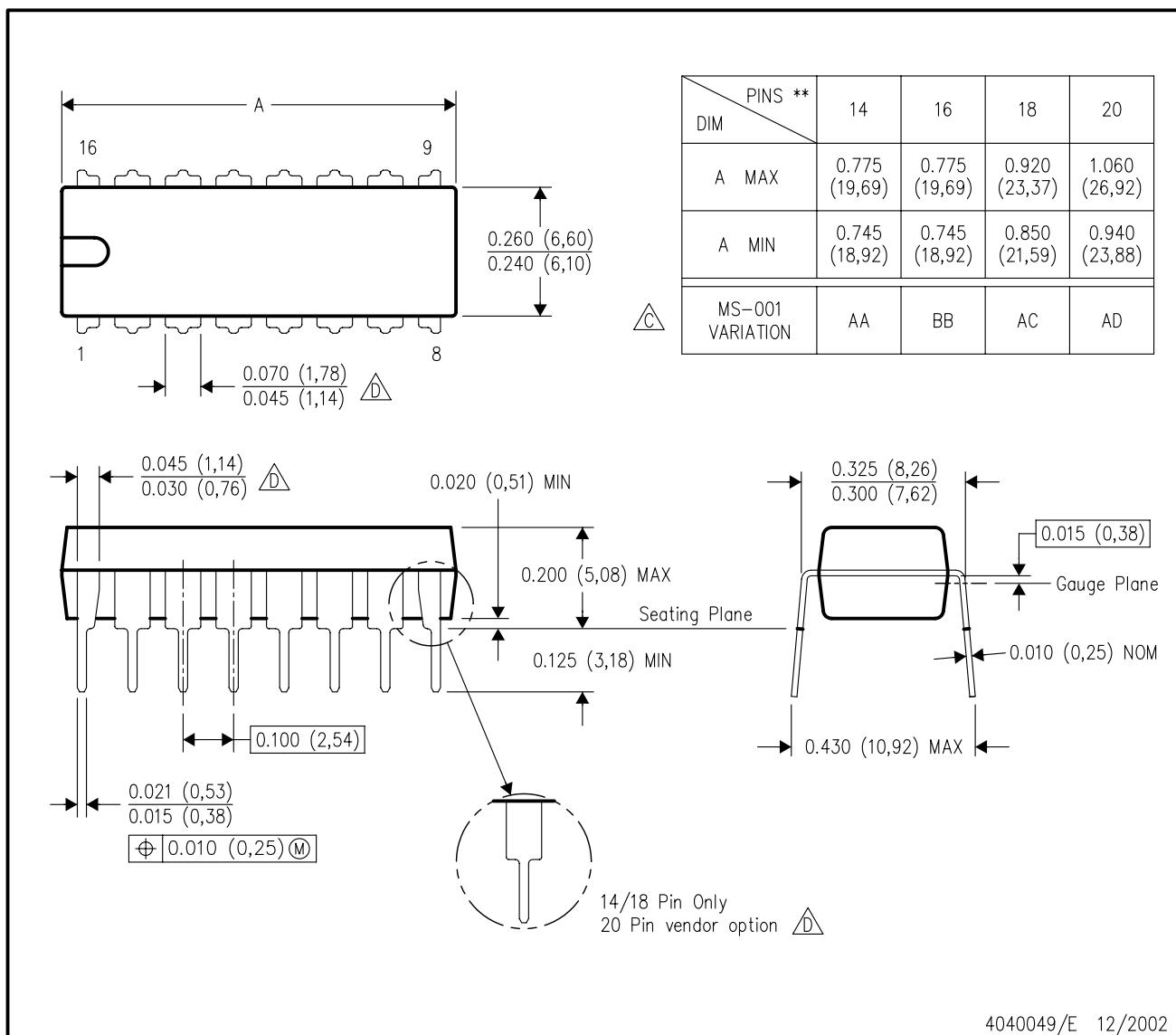
\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T ( $\mu$ m)	B (mm)
74AC11004N	N	PDIP	20	20	506	13.97	11230	4.32
74AC11004N.A	N	PDIP	20	20	506	13.97	11230	4.32

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



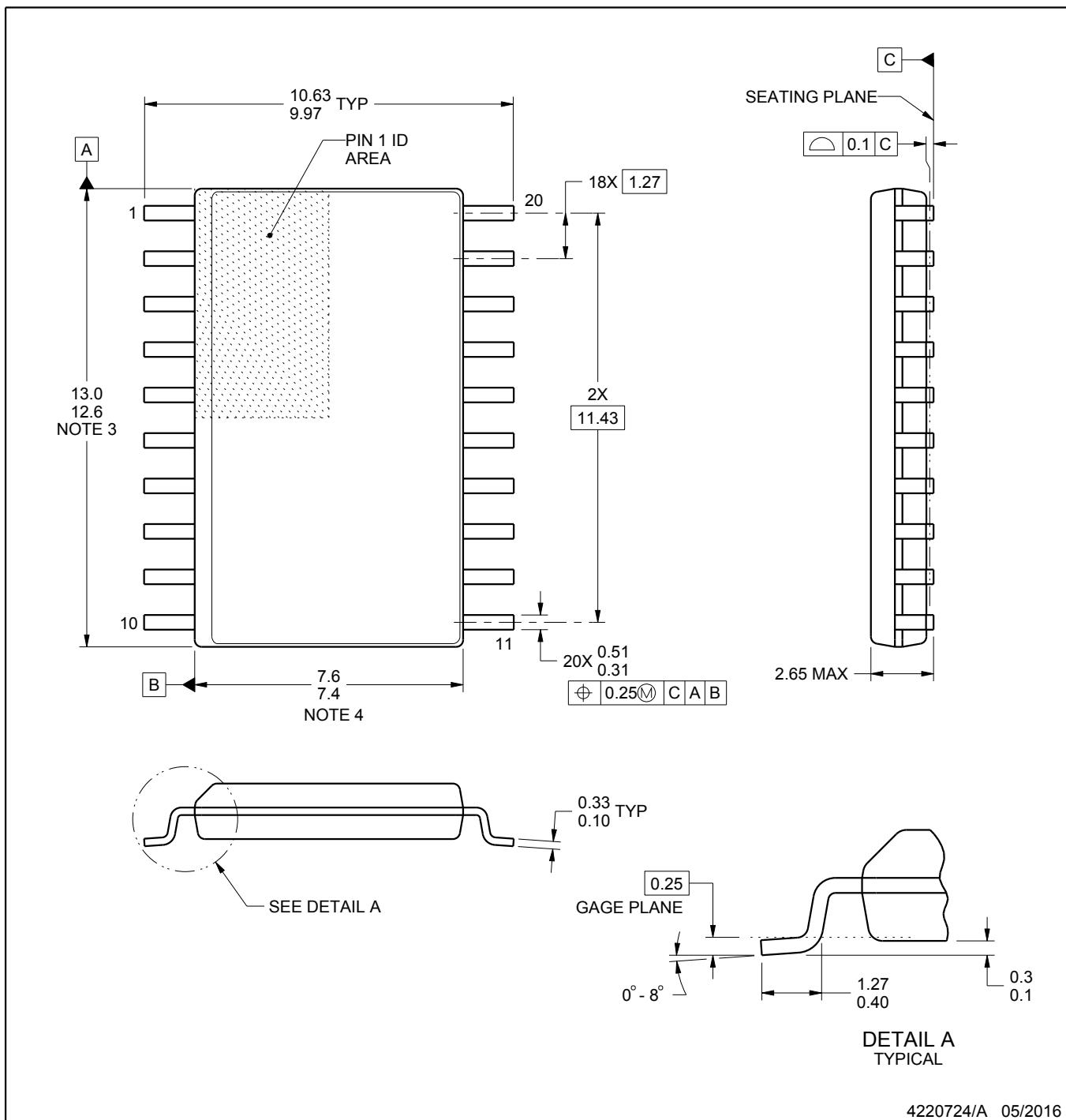


## PACKAGE OUTLINE

**DW0020A**

## **SOIC - 2.65 mm max height**

SOIC



## NOTES:

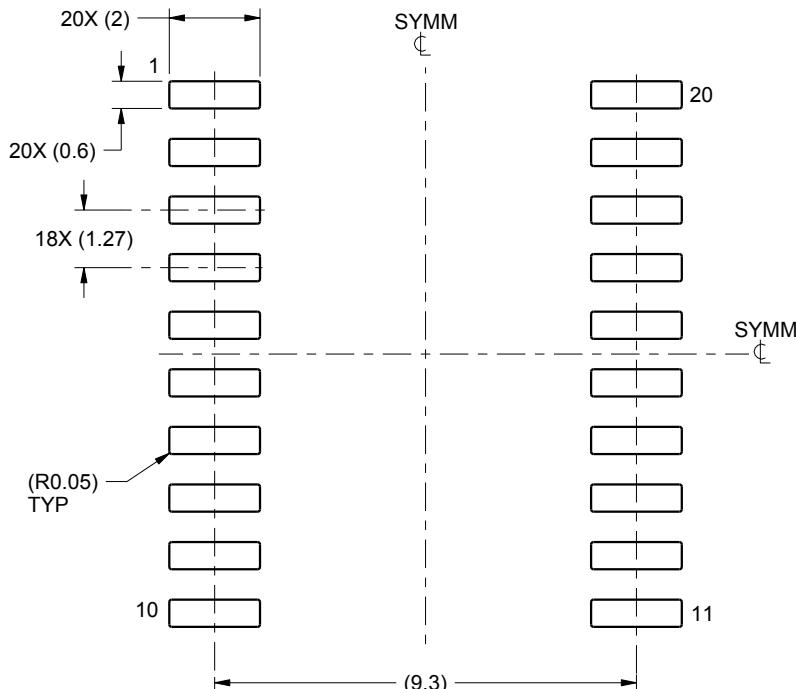
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

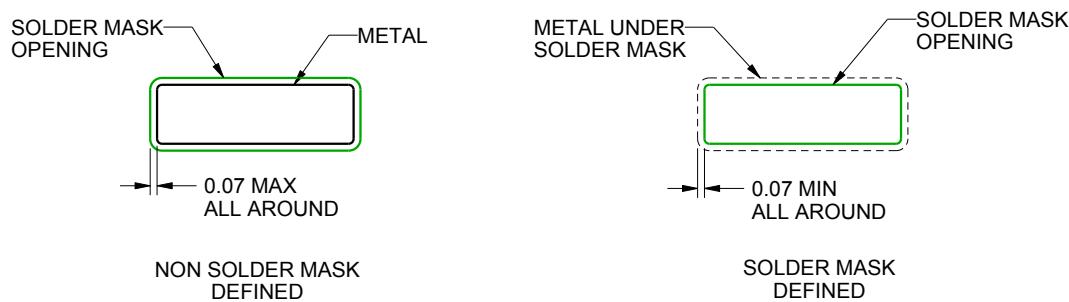
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

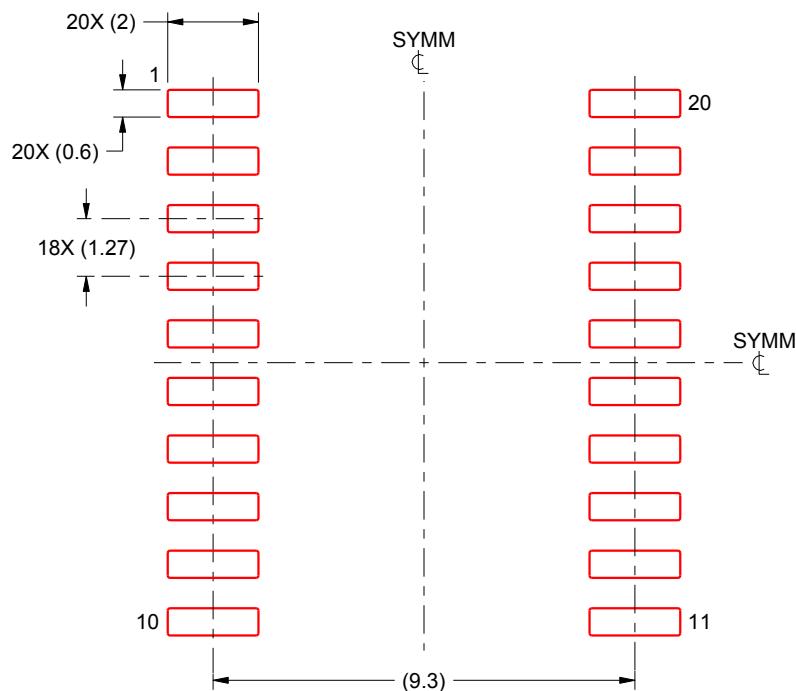
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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