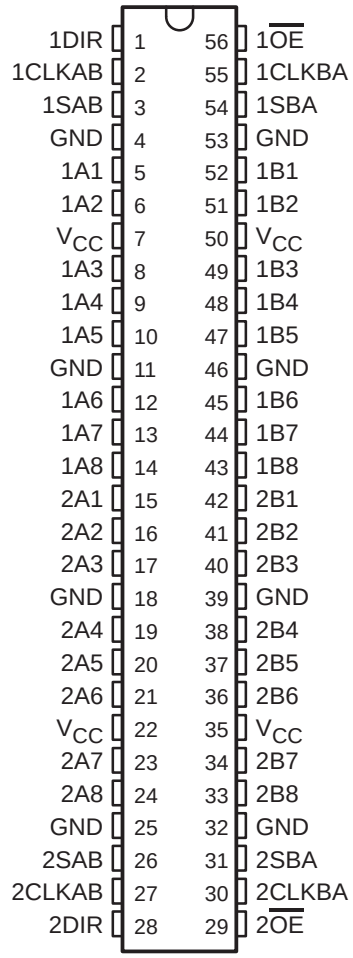
- **Members of the Texas Instruments *Widebus*™ Family**
- **Inputs Are TTL-Voltage Compatible**
- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings**

54ACT16646 . . . WD PACKAGE
74ACT16646 . . . DL PACKAGE
(TOP VIEW)



description

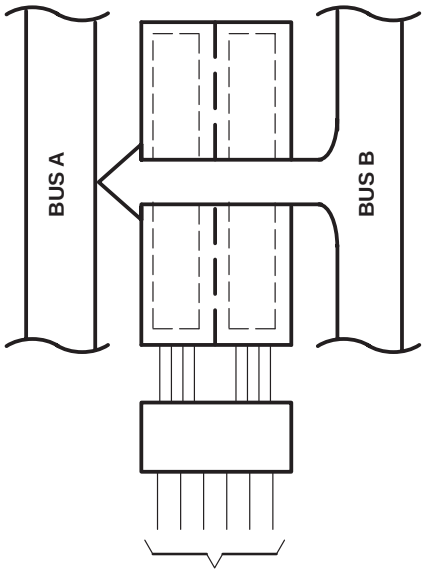
The ’ACT16646 are 16-bit bus transceivers consisting of D-type flip-flops and control circuitry with 3-state outputs arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The devices can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the bus transceivers and registers.

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. DIR determines which bus receives data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

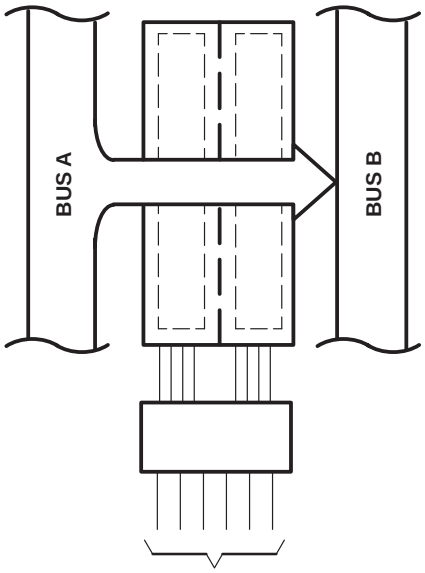
The 74ACT16646 is packaged in TI’s shrink small-outline package, which provides twice the functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16646 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT16646 is characterized for operation from –40°C to 85°C.



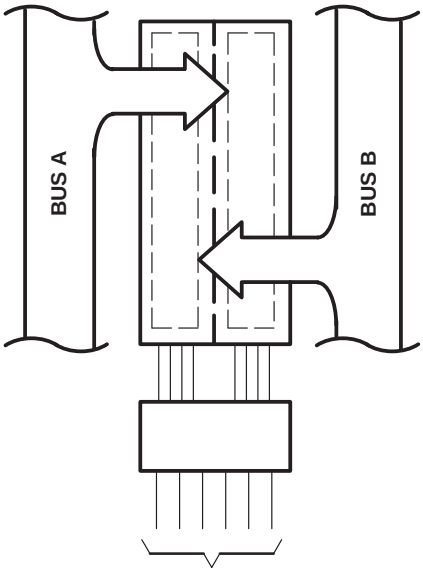
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



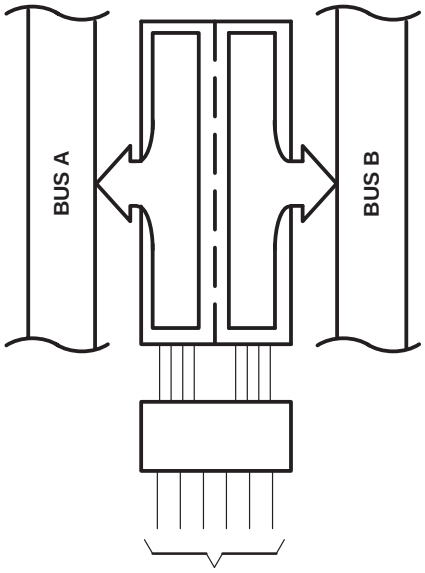
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA
TO A AND/OR B

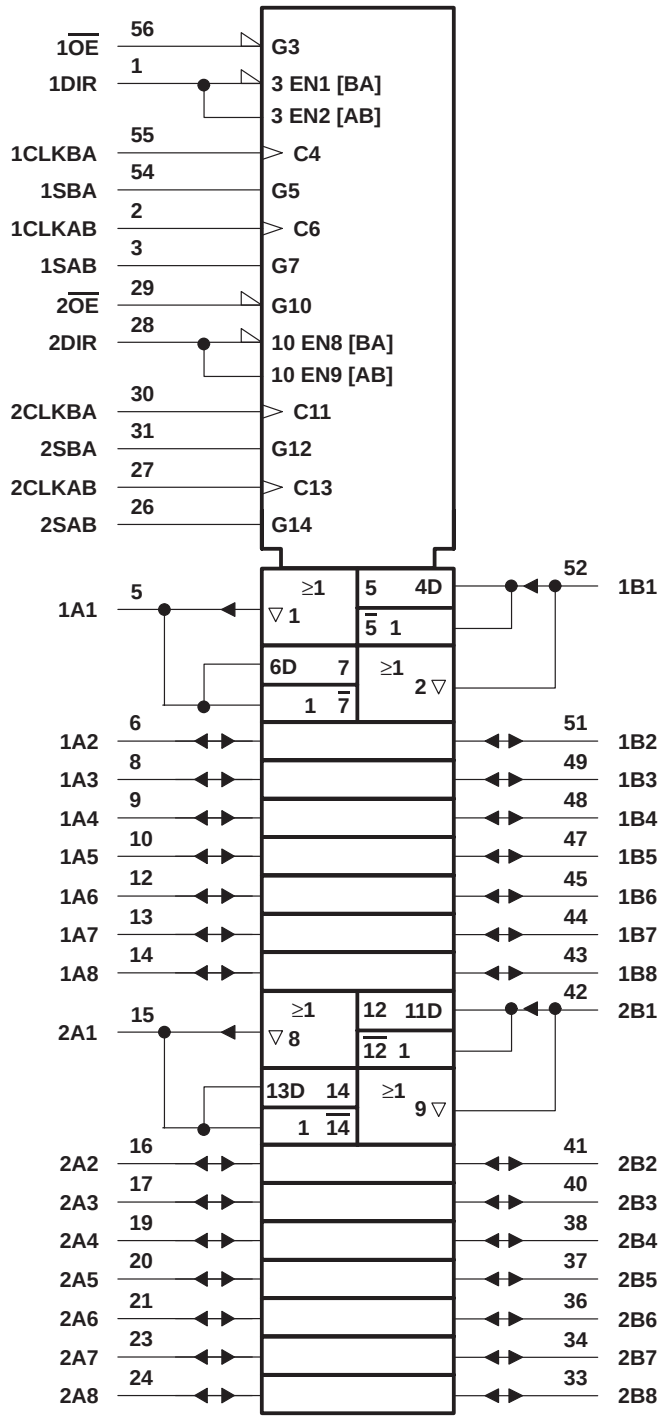
Figure 1. Bus-Management Functions

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
X	X	↑	X	X	X	Input	Unspecified	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B Bus
L	H	H or L	X	H	X	Input	Output	Stored A data to bus

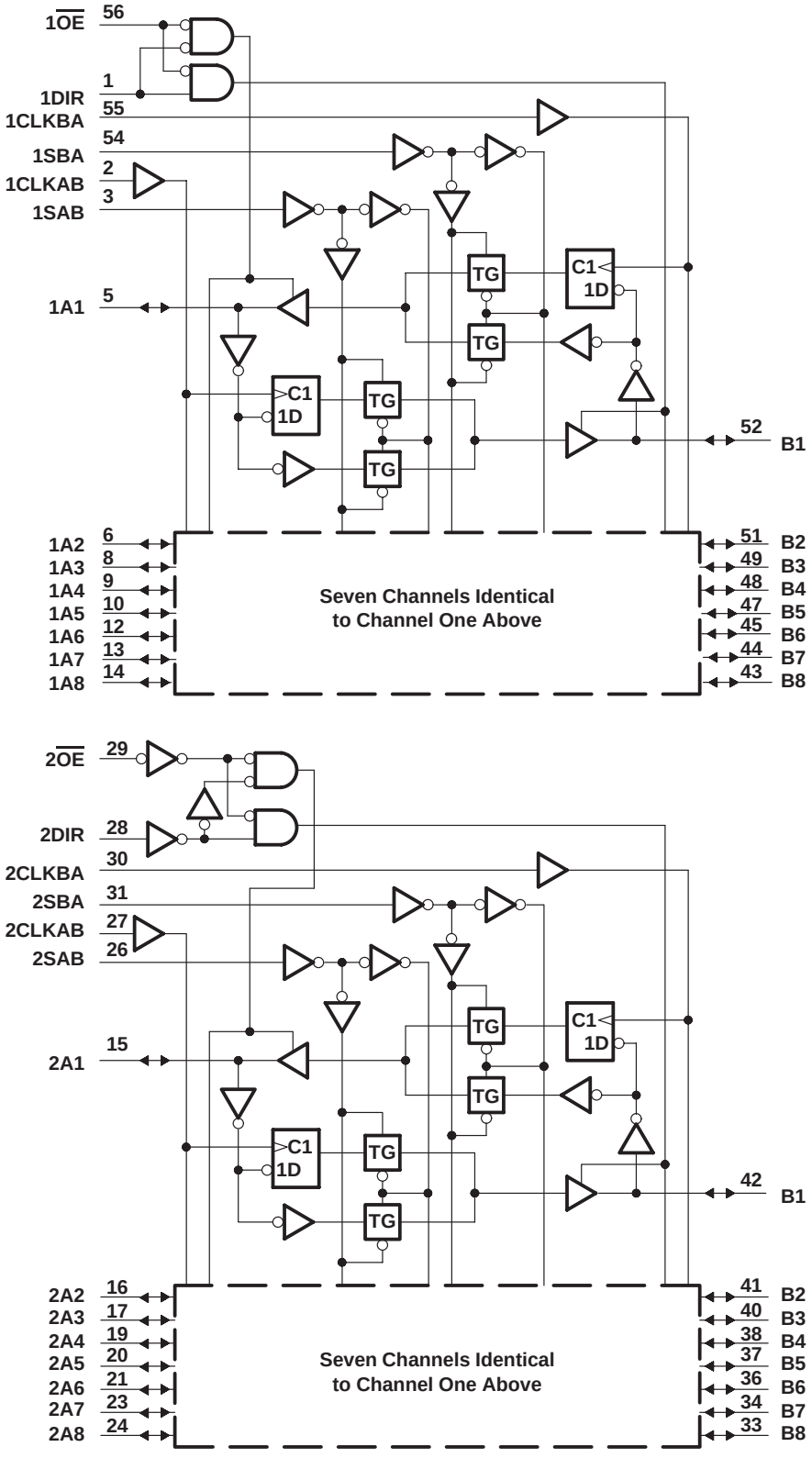
† The data-output functions may be enabled or disabled by various signals at $\overline{OE}$ or DIR. Data-input functions are always enabled, i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±400 mA
Maximum package power dissipation at T_A = 55°C (in still air) (see Note 2): DL package . . . . . 1.4 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

		54ACT16646		74ACT16646		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage (see Note 4)	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTES: 3. Unused inputs must be held high or low to prevent them from floating.
4. All V_{CC} and GND pins must be connected to the proper voltage power supply.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT16646		74ACT16646		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 μA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I_{OH} = –24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = –50 mA†	5.5 V				3.85				
		I_{OH} = –75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
I_{OZ}	A or B ports‡	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}§		One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4						pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, (unless otherwise noted) (see Figure 2)

			T_A = 25°C		54ACT16646		74ACT16646		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	90	0	90	0	90	MHz
t_w	Pulse duration, CLKAB or CLKBA high or low		5.5		5.5		5.5		ns
t_{su}	Setup time, A before CLKAB↑ or B before CLKBA↑	Data high	4		4		4		ns
		Data low	6		6		6		
t_h	Hold time, A before CLKAB↑ or B before CLKBA↑		1.5		1.5		1.5		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, (unless otherwise noted) (see Figure 2)

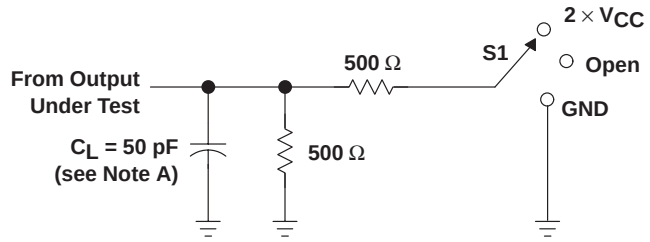
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT16646		74ACT16646		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			90			90		90		MHz
t_{PLH}	A or B	B or A	3.9	7.5	9.4	3.9	11.5	3.9	10.6	ns
t_{PHL}			3.4	7.6	10.6	3.4	12.2	3.4	11.4	
t_{PZH}	$\overline{OE}$	A or B	3.2	7.7	10.8	3.2	12.9	3.2	11.9	ns
t_{PZL}			4.2	9	12.2	4.2	14.6	4.2	13.5	
t_{PHZ}	$\overline{OE}$	A or B	5.3	7.7	9.6	5.3	10.4	5.3	10.2	ns
t_{PLZL}			4.9	7.3	9.2	4.9	10.3	4.9	9.9	
t_{PLH}	CLKBA or CLKAB	A or B	4.9	8.9	11.1	4.9	13.1	4.9	12.2	ns
t_{PHL}			5.1	9	11	5.1	13.1	5.1	12.3	
t_{PLH}	SAB or SBA† (with A or B high)	A or B	5.2	10.3	13.8	5.2	17.2	5.2	15.6	ns
t_{PHL}			4.9	8.2	10.6	4.9	12.5	4.9	11.7	
t_{PLH}	SBA or SAB† (with A or B high)	A or B	4.3	7.8	9.9	4.3	12.1	4.3	11.1	ns
t_{PHL}			5.9	11.2	14.9	5.9	18.2	5.9	16.7	
t_{PZH}	DIR	A or B	4.5	9.5	13.6	4.5	16.2	4.5	15.2	ns
t_{PZL}			4.3	9.2	11.8	4.3	14.2	4.3	13.1	
t_{PHZ}	DIR	A or B	4.5	7.9	10.2	4.5	11.2	4.5	10.8	ns
t_{PLZ}			4.4	7.5	9.8	4.4	10.8	4.4	10.4	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

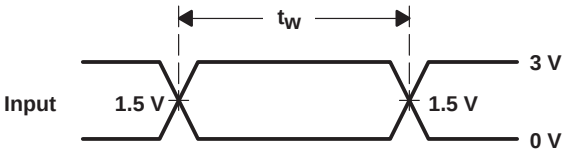
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	58	pF
		Outputs disabled		13	

PARAMETER MEASUREMENT INFORMATION

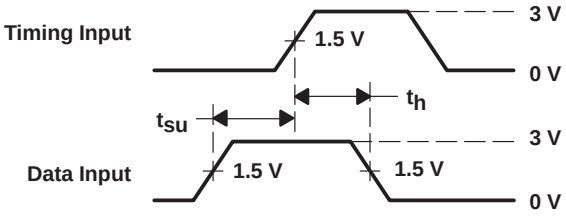


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

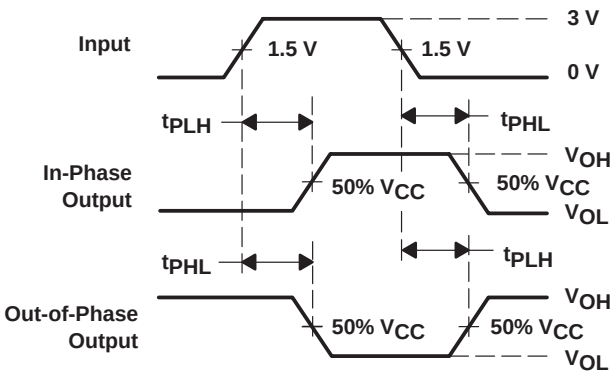
LOAD CIRCUIT



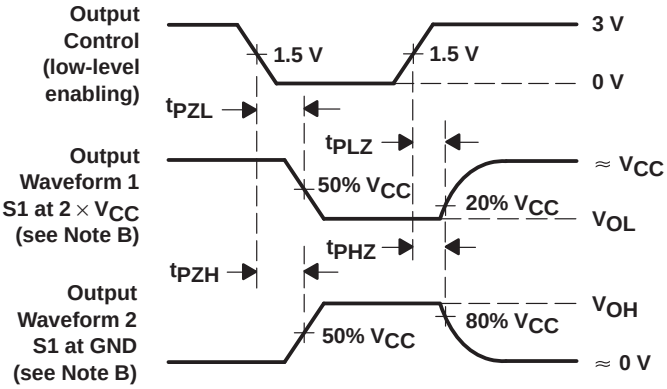
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74ACT16646DL	Obsolete	Production	SSOP (DL) | 56	-	-	Call TI	Call TI	-40 to 85	ACT16646
74ACT16646DLR	Active	Production	SSOP (DL) | 56	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16646
74ACT16646DLR.A	Active	Production	SSOP (DL) | 56	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16646

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

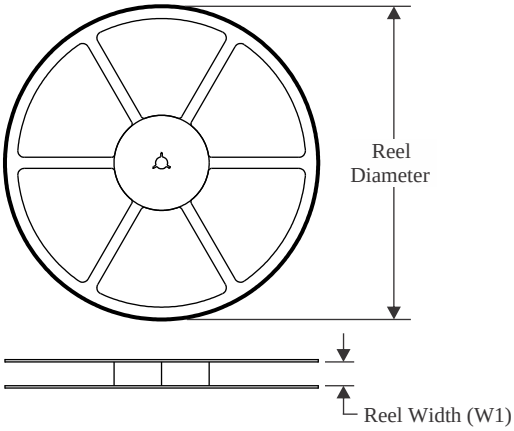
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

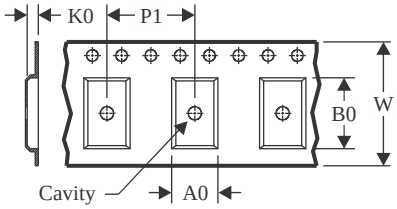
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

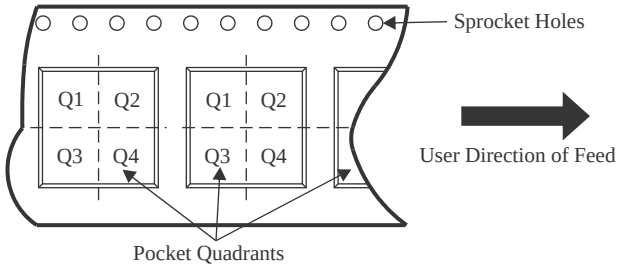


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

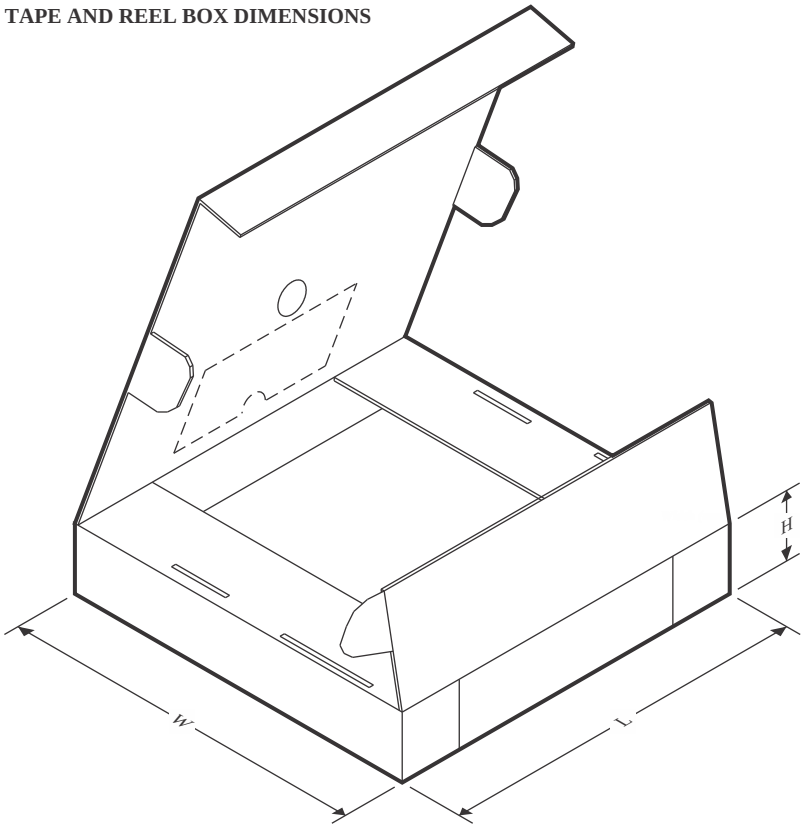
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ACT16646DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

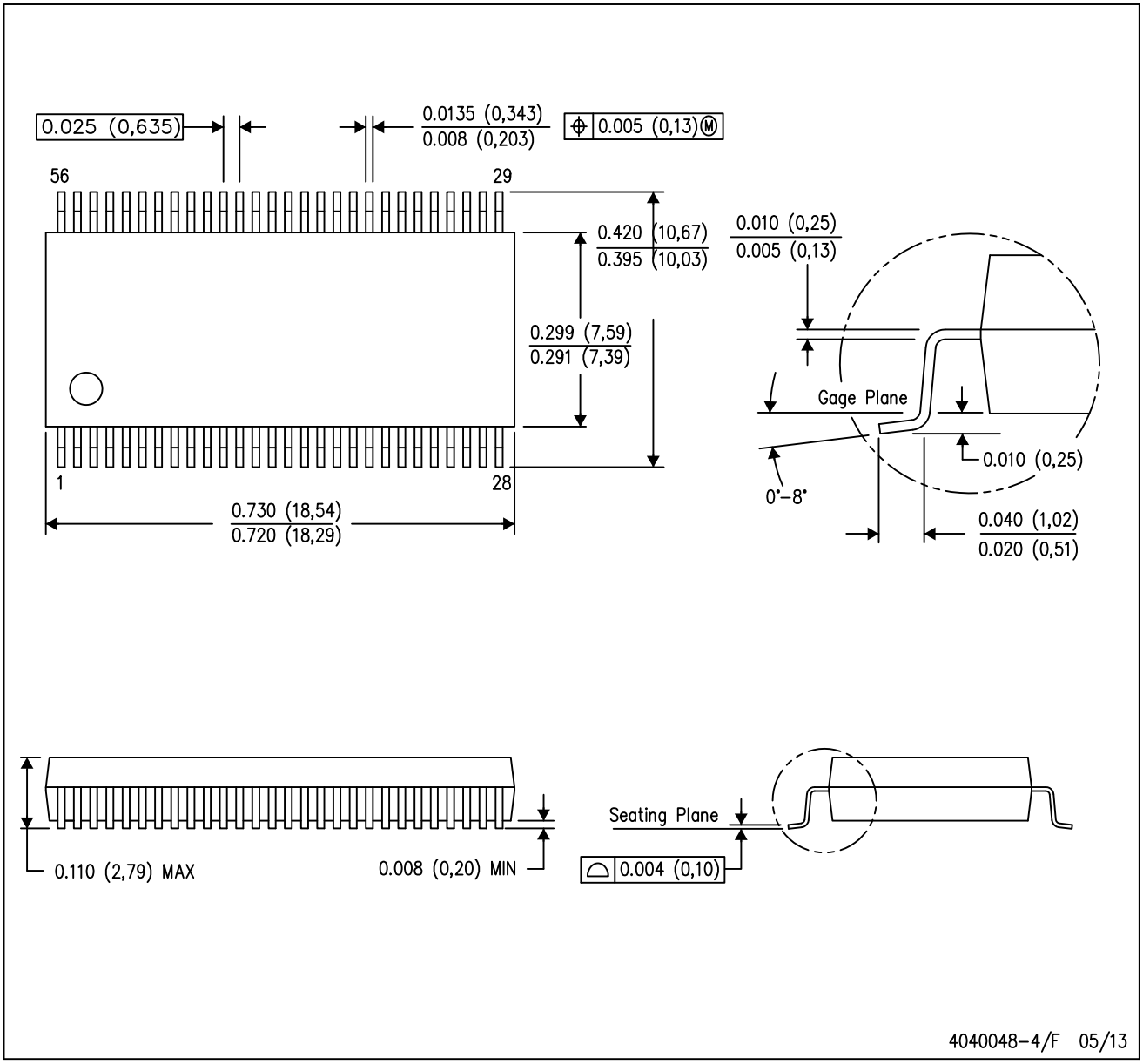
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ACT16646DLR	SSOP	DL	56	1000	356.0	356.0	53.0

DL (R–PDSO–G56) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

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