DAC8775 四通道、16 位可编程电流输出和电压输出具有自适应电源管理功能的数模转换器

1 特性

- 输出电流：
  - 0mA 至 24mA；3.5mA 至 23.5mA；0mA 至 20mA；4mA 至 20mA；±24mA
- 输出电压（超出/不超出范围的 20%）：
  - 0V 至 5V；0V 至 10V；±5V；±10V
  - 0V 至 6V；0V 至 12V；±6V；±12V
- 自适应电源管理
- 电压范围较宽的单电源（12V 至 36V）引脚
- ±0.1% 满量程范围 (FSR) 总未调节误差 (TUE)
- 微分非线性 (DNL)：±1 最低有效位 (LSB) 最大值
- 5V 内部基准（10ppm/°C 最大值）
- 5V 内部数字电源输出
- CRC/帧错误检查，看门狗定时器
- 保障系统可靠性的过热报警、开路/短路保护
- 报警条件下的安全操作
- 自动学习负载检测
- 宽温度范围：-40°C 至 +125°C

2 应用范围

- 4mA 至 20mA 电流环路
- 模拟输出模块
- 可编程逻辑控制器 (PLC)
- 楼宇自动化
- 传感器发送器
- 过程控制

3 说明

DAC8775是一款四通道、精密全集成 16 位、数模转换器 (DAC)，具有自适应电源管理功能，设计用于满足工业控制 应用的各项要求。自适应电源管理电路在使能后能够最大程度降低芯片功耗。通过编程设定为电流输出后，电流输出驱动器的电源电压根据电流输出引脚处电压的连续反馈，通过集成降压/升压转换器在 4.5V 至 32V 范围内进行调节。通过编程设定为电压输出后，该电路为电压输出级 (±15V) 生成可编程电源电压。DAC8775 还包括一个 LDO，用于从单电源引脚生成数字电源 (5V)。

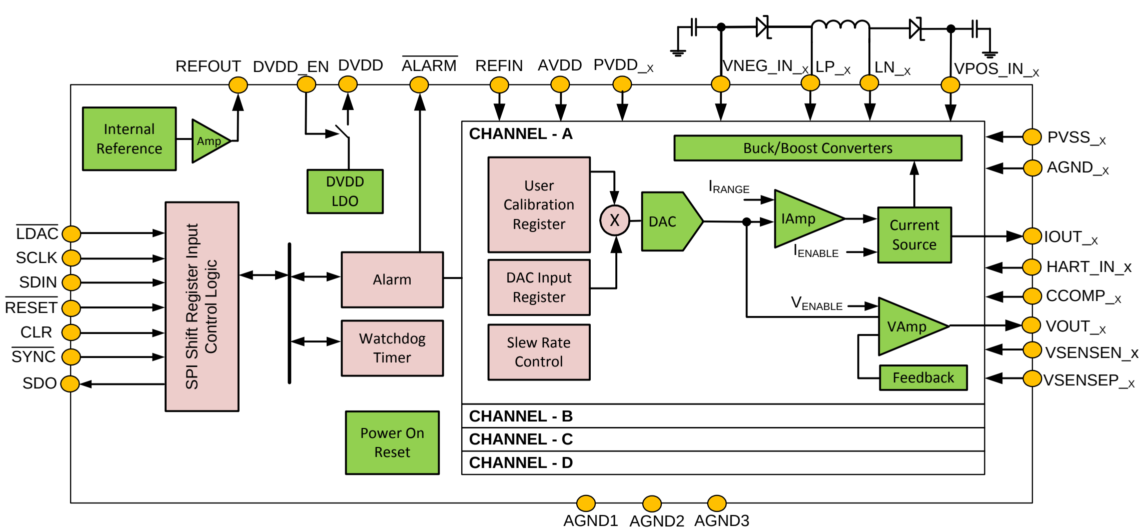
DAC8775 还实现了一种高速可寻址远程传感器 (HART) 信号接口，支持在电流输出中叠加外部 HART 信号。电流输出 DAC 转换率由寄存器通过编程设定。在禁用降压/升压转换器时，该器件可将集成降压/升压转换器或外部电源作为 +12V 至 +36V 单一外部电源供电运行。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DAC8775	VQFN (72)	10.00mm x 10.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

框图



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4 修订历史记录

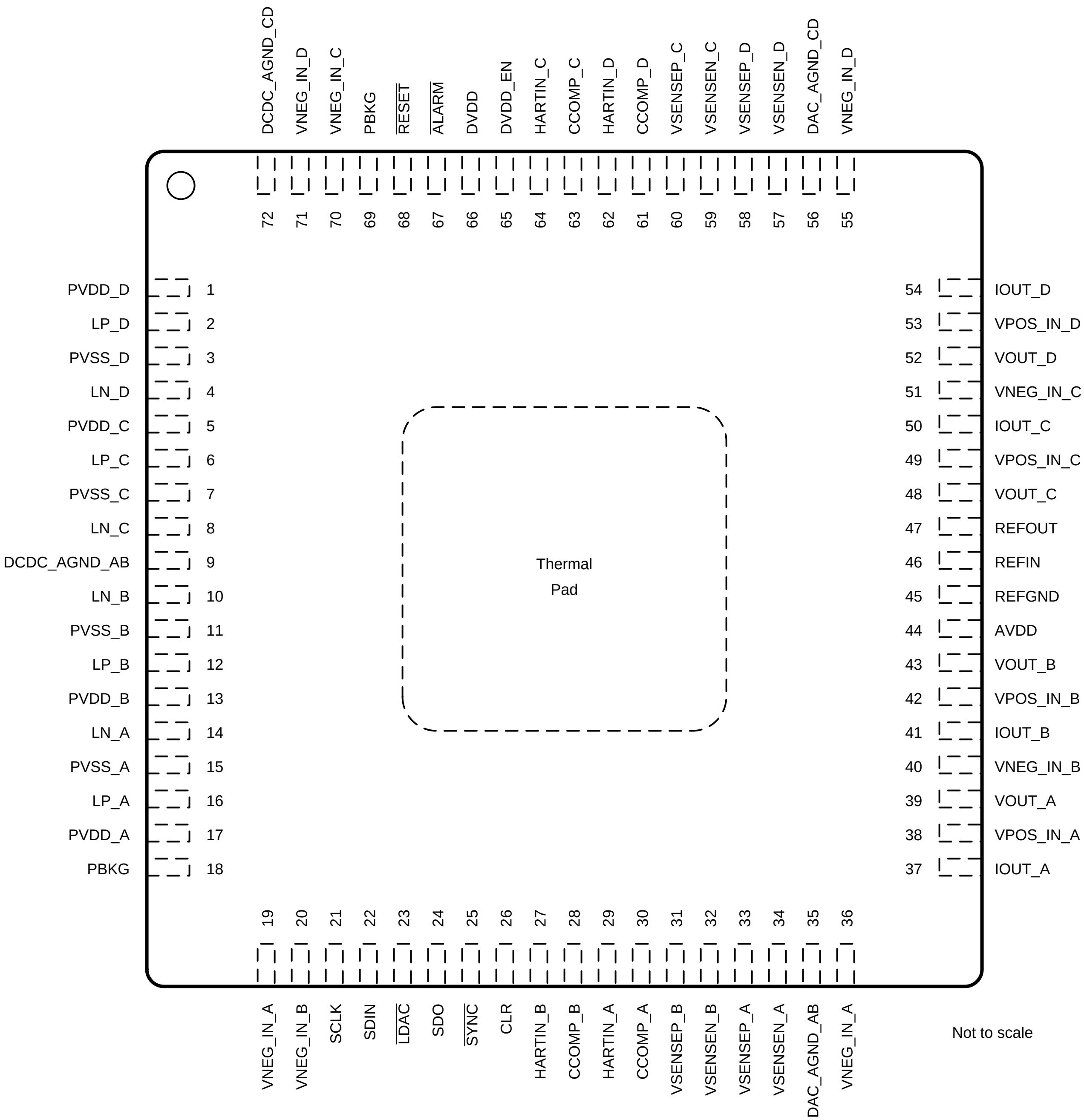
日期	修订版本	注释
2017 年2 月	*	最初发布版本。

5 Device Comparison Table

PRODUCT	RESOLUTION	DIFFERENTIAL NONLINEARITY (LSB)
DAC8775	16	±1

6 Pin Configuration and Functions

RWF Package
72-Pin VQFN
Top View



(1) Thermal pad should be connected to ground.

Pin Functions

PIN		DESCRIPTION
NAME	NO.	
PVDD_D	1	Buck-Boost Converter power switch supply D
LP_D	2	External Inductor terminal - positive D
PVSS_D	3	Ground for Buck-Boost converter switches D
LN_D	4	External Inductor terminal - negative D
PVDD_C	5	Buck-Boost Converter power switch supply C
LP_C	6	External Inductor terminal - positive C
PVSS_C	7	Ground for Buck-Boost converter switches C
LN_C	8	External Inductor terminal - negative C
DCDC_AGND_AB	9	Analog GND Buck-Boost converter Channels A and B
LN_B	10	External Inductor terminal - negative B
PVSS_B	11	Ground for Buck-Boost converter switches B
LP_B	12	External Inductor terminal - positive B
PVDD_B	13	Buck-Boost Converter power switch supply B
LN_A	14	External Inductor terminal - negative A
PVSS_A	15	Ground for Buck-Boost converter switches A
LP_A	16	External Inductor terminal - positive A
PVDD_A	17	Buck-Boost Converter power switch supply A
PBKG	18	Chip substrate, connect to 0 V
VNEG_IN_A	19	Negative power supply for VOUT_A and IOUT_A
VNEG_IN_B	20	Negative power supply for VOUT_B and IOUT_A
SCLK	21	Serial clock input of serial peripheral interface (SPI™). Data can be transferred at rates up to 25 MHz. Schmitt-Trigger logic input.
SDIN	22	Serial data input. Data are clocked into the 24-bit input shift register on the falling edge of the serial clock input. Schmitt-Trigger logic input.
$\overline{\text{LDAC}}$	23	Load DAC latch control input. A logic low on this pin loads the input shift register data into the DAC register and updates the DAC output.
SDO	24	Serial data output. Data are valid on the falling edge of SCLK.
$\overline{\text{SYNC}}$	25	SPI bus chip select input (active low). Data bits are not clocked into the serial shift register unless SYNC is low. When SYNC is high, SDO is in high-impedance status.
CLR	26	Level Triggered clear pin (Active High). Clears all DAC channel to zero code or mid code (see DAC clear section)
HARTIN_B	27	Input pin for HART modulation. for IOUT_B
CCOMP_B	28	External compensation capacitor connection pin for VOUT_B . Addition of the external capacitor improves the stability with high capacitive loads at the VOUT_B pin by reducing the bandwidth of the output amplifier at the expense of increased settling time.
HARTIN_A	29	Input pin for HART modulation. for IOUT_A
CCOMP_A	30	External compensation capacitor connection pin for VOUT_A . Addition of the external capacitor improves the stability with high capacitive loads at the VOUT_A pin by reducing the bandwidth of the output amplifier at the expense of increased settling time.
VSENSEP_B	31	Sense output pin for the positive voltage output (channel B) load connection.
VSENSEN_B	32	Sense output pin for the negative voltage output (channel B) load connection.
VSENSEP_A	33	Sense output pin for the positive voltage output (channel A) load connection.
VSENSEN_A	34	Sense output pin for the negative voltage output (channel A) load connection.
DAC_AGND_AB	35	Analog GND DAC Channels A and B
VNEG_IN_A	36	Negative power supply for VOUT_A and IOUT_A
IOUT_A	37	Current Output Pin (Channel A)
VPOS_IN_A	38	Positive power supply for VOUT_A and IOUT_A
VOUT_A	39	Voltage Output Pin (Channel A)
VNEG_IN_B	40	Negative power supply for VOUT_B and IOUT_B

Pin Functions (continued)

PIN		DESCRIPTION
NAME	NO.	
IOUT_B	41	Current Output Pin (Channel B)
VPOS_IN_B	42	Positive power supply for VOUT_B and IOUT_B
VOUT_B	43	Voltage Output Pin (Channel B)
AVDD	44	Power supply for all analog circuitry of the device except buck-boost converters and output amplifiers
REFGND	45	Reference ground
REFIN	46	Reference input
REFOUT	47	Internal reference output. Connects to REFIN when using internal reference.
VOUT_C	48	Voltage Output Pin (Channel C)
VPOS_IN_C	49	Positive power supply for VOUT_C and IOUT_C
IOUT_C	50	Current Output Pin (Channel C)
VNEG_IN_C	51	Negative power supply for VOUT_C and IOUT_C
VOUT_D	52	Voltage Output Pin (Channel D)
VPOS_IN_D	53	Positive power supply for VOUT_D and IOUT_D
IOUT_D	54	Current Output Pin (Channel D)
VNEG_IN_D	55	Negative power supply for VOUT_D and IOUT_D
DAC_AGND_CD	56	Analog GND DAC Channels C and D
VSENSEN_D	57	Sense output pin for the negative voltage output (channel D) load connection.
VSENSEP_D	58	Sense output pin for the positive voltage output (channel D) load connection.
VSENSEN_C	59	Sense output pin for the negative voltage output (channel C) load connection.
VSENSEP_C	60	Sense output pin for the positive voltage output (channel C) load connection.
CCOMP_D	61	External compensation capacitor connection pin for VOUT_D . Addition of the external capacitor improves the stability with high capacitive loads at the VOUT_D pin by reducing the bandwidth of the output amplifier at the expense of increased settling time.
HARTIN_D	62	Input pin for HART modulation. for IOUT_D
CCOMP_C	63	External compensation capacitor connection pin for VOUT_C . Addition of the external capacitor improves the stability with high capacitive loads at the VOUT_C pin by reducing the bandwidth of the output amplifier at the expense of increased settling time.
HARTIN_C	64	Input pin for HART modulation. for IOUT_C
DVDD_EN	65	Internal power-supply enable pin. Connect this pin to PBKG to disable the internal DVDD, or leave this pin unconnected to enable the internal DVDD. When this pin is connected to PBKG, an external supply must be connected to the DVDD pin.
DVDD	66	Digital Supply pin (Input/Output) Internal DVDD enabled when DVDD_EN is floating, External DVDD must be supplied when DVDD_EN is connected to PBKG
$\overline{\text{ALARM}}$	67	ALARM pin. Open drain output. External pull-up resistor required (10 kΩ). The pin goes low (active) when the $\overline{\text{ALARM}}$ condition is detected on any of the outputs (OUT_A through OUT_D) (open circuit, over temperature, watchdog timeout, and others).
$\overline{\text{RESET}}$	68	Reset input (active low). Logic low on this pin causes the device to perform a reset. A hardware reset must be issued using this pin after power up.
PBKG	69	Chip substrate, connect to 0 V
VNEG_IN_C	70	Negative power supply for VOUT_C
VNEG_IN_D	71	Negative power supply for VOUT_D
DCDC_AGND_CD	72	Analog GND Buck-Boost converter Channels C and D

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Input voltage	PVDD_x/AVDD to PBKG	-0.3	40	V
	PVSS_x/REFGND/DCDC_AGND_x/DAC_AGND_x to PBKG	-0.3	0.3	
	VPOS_IN_x to VNEG_IN_x	-0.3	40	
	VPOS_IN_x to PBKG	-0.3	33	
	VNEG_IN_x to PBKG	-20	0.3	
	VSENSEN_x to PBKG	VNEG_IN_x	VPOS_IN_x	
	VSENSEP_x to PBKG	VNEG_IN_x	VPOS_IN_x	
	DVDD to PBKG	-0.3	6	
	REFOUT/REFIN to PBKG	-0.3	6	
	Digital input voltage to PBKG	-0.3	DVDD+0.3	
Output voltage	VOUT_x to PBKG	VNEG_IN_x	VPOS_IN_x	V
	IOUT_x to PBKG	VNEG_IN_x	VPOS_IN_x	
	SDO, ALARM to PBKG	-0.3	DVDD+0.3	
Input current	Current into any digital input pin	-10	10	mA
Power dissipation			$(T_{Jmax} – T_A)/\theta_{JA}$	W
Operating junction temperature, T_J		-40	150	°C
Junction temperature range, T_{Jmax}			150	
Storage temperature, T_{stg}		-65	150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
POWER SUPPLY					
PVDD_x/AVDD_x to PBKG/PVSS_x[1]	Positive supply voltage to ground range	12		36	V
VPOS_IN_x to PBKG[1]	Positive supply voltage to ground range	12		33	V
VNEG_IN_x to PBKG[1]	Negative supply voltage to substrate for current output mode	-18		0	V
	Negative supply voltage to substrate for voltage output mode	-18		-5	V
VPOS_IN_x to VNEG_IN_x[1]		12		36	V
VSENSEN_x to PBKG	The minimum headroom spec for voltage output stage must be met	-7		7	V

(1) The minimum headroom spec for voltage output stage and the compliance voltage for current output stage should be met. When Buck-Boost converter is enabled VPOS_IN_x/VNEG_IN_x are generated internally to meet headroom and compliance specs. When Buck-Boost converter is disabled VPOS_IN_x, AVDD, and PVDD must be tied together.

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
DVDD to PBKG	Digital supply voltage to substrate	2.7		5.5	V
DIGITAL INPUTS					
V_{IH}	Input high voltage	2			V
V_{IL}	Input low voltage			0.6	V
REFERENCE INPUT					
REFIN to PBKG	Reference input to substrate	4.95		5.05	V
TEMPERATURE RANGE					
T_A	Operating temperature	-40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		DAC8775 RWF (VQFN) 72 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	21.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	3.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	1.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	1.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

AVDD/PVDD_x/VPOS_IN_x = +15 V, VNEG_IN_x = -15 V, VSENSEN_x = PBKG = PVSS_x = 0 V, External DVDD = 2.7 V. VOUT : R_L = 1 kΩ, C_L = 200 pF, IOUT : R_L = 250 Ω; all specifications -40℃ to +125℃, unless otherwise noted. REFIN= +5 V external;, Buck-Boost Converter disabled unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT OUTPUT						
IOUT	Output Current Ranges		0		24	mA
			0		20	mA
			3.5		23.5	mA
			-24		24	mA
			4		20	mA
Accuracy						
	Resolution		16			Bits
INL	Relative Accuracy(1)	All ranges except bipolar range	-12		12	LSB
		Bipolar range only	-16		16	LSB
DNL	Differential Nonlinearity(1)	Ensured monotonic	-1		1	LSB
TUE	Total Unadjusted Error(1)	-40℃ to +125℃	-0.14		0.14	%FSR
		-40℃ to +125℃, 4 to 20 mA	-0.4		0.4	%FSR
		T_A = +25℃, 4 to 20 mA	-0.2		0.2	%FSR
		T_A = +25℃	-0.12		0.12	%FSR
OE	Offset Error(1)	-40℃ to +125℃	-0.1		0.1	%FSR
		T_A = +25℃	-0.05		0.05	%FSR
OE-TC	Offset Error Temperature Coefficient	-40℃ to +125℃		4		ppm FSR/ºC

(1) For current output all ranges except ±24 mA, low code of 256d and a high code of 65535d are used, for ±24 mA range low code of 0d and a high code of 65535d. For voltage output, low code of 256d and a high code of 65535d are used

Electrical Characteristics (continued)

AVDD/PVDD_x/VPOS_IN_x = +15 V, VNEG_IN_x = -15 V, VSENSEN_x = PBKG = PVSS_x = 0 V, External DVDD = 2.7 V. VOUT : R_L = 1 kΩ, C_L = 200 pF, IOUT : R_L = 250 Ω; all specifications -40℃ to +125℃, unless otherwise noted. REFIN= +5 V external;, Buck-Boost Converter disabled unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ZCE	Zero Code Error	-40℃ to +125℃, 0x0000h into DAC	-15		15	uA
		-40℃ to +125℃, 0x0000h into DAC, 4 to 20 mA	-18		18	uA
		T_A = 25℃, 0x0000h into DAC		1.2		m%FSR
		T_A = 25℃, 0x0000h into DAC, 4 to 20 mA		1.8		m%FSR
ZCE-TC	Zero Code Error Temperature Coefficient	0x0000h into DAC, -40℃ to +125℃		4		ppm/ºC
GE	Gain Error(2)	-40℃ to +125℃	-0.125		0.125	%FSR
		-40℃ to +125℃, 4 to 20 mA	-0.25		0.25	%FSR
		T_A = +25℃, 4 to 20 mA	-0.2		0.2	%FSR
		T_A = +25°C	-0.12		0.12	%FSR
GE-TC	Gain Error Temperature Coefficient	-40℃ to +125℃		3		ppm FSR/ºC
PFSE	Positive Full Scale Error	0xFFFFh into DAC, -40℃ to +125℃	-0.125		0.125	%FSR
		0xFFFFh into DAC, -40℃ to +125℃, 4 to 20 mA	-0.25		0.25	%FSR
		0xFFFFh into DAC, T_A = 25℃		0.016		%FSR
		0xFFFFh into DAC, T_A = 25℃, 4 to 20 mA		0.024		%FSR
NFSE	Negative Full Scale Error	0x0000h into DAC, Bipolar range only, -40℃ to +125℃	-0.125		0.125	%FSR
		0x0000h into DAC, Bipolar range only, T_A = 25℃		0.02		%FSR
PFSE-TC	Positive Full Scale Error Temperature Coefficient			5		ppm FSR/ºC
NFSE-TC	Negative Full Scale Error Temperature Coefficient	Bipolar range only		5		ppm FSR/ºC
BPZE	Bipolar Zero Error	Bipolar range only, 0x8000h into DAC -40℃ to +125℃	-0.05		0.05	%FSR
		Bipolar range only, 0x8000h into DAC, T_A = +25°C	-0.02		0.02	%FSR
BPZE-TC	Bipolar Zero Error Temperature Coefficient	0x8000h into DAC,-40℃ to +125℃		4		ppm/ºC
VCL	Compliance Voltage	Output = 24 mA			VPOS_IN_x-3	V
		Output = ±24 mA	|VNEG_IN_x|+3		VPOS_IN_x-3	V
R_L	Resistive Load	All except ±24 mA range			1.2	KΩ
		±24 mA range			0.625	KΩ
DC-PSRR	DC Power Supply Rejection Ratio	Code = 0x8000, 20 mA range		0.1		µA/V
Z_O	Output Impedance	Code = 0x8000		10		MΩ
IOLEAK	Output Current Leakage	Iout is disabled or in power-down		1		nA
HART INTERFACE						
VHART-IN	HART Input		400	500	600	mVpp
	Corresponding Output	HART In = 500 mVpp 1.2 KHz		1		mApp

(2) No load, DVDD supply ramps up before VPOS_IN_x,and VNEG_IN_x, ramp rate of VPOS_IN_x,and VNEG_IN_x limited to 18 V/msec

Electrical Characteristics (continued)

AVDD/PVDD_x/VPOS_IN_x = +15 V, VNEG_IN_x = -15 V, VSENSEN_x = PBKG = PVSS_x = 0 V, External DVDD = 2.7 V. VOUT : R_L = 1 kΩ, C_L = 200 pF, IOUT : R_L = 250 Ω; all specifications -40℃ to +125℃, unless otherwise noted. REFIN= +5 V external;, Buck-Boost Converter disabled unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE OUTPUT						
VOUT	Voltage Output Ranges (normal mode)		0		5	V
			0		10	V
			-5		5	V
			-10		10	V
	Voltage Output Ranges (Overrange mode)		0		6	V
			0		12	V
			-6		6	V
			-12		12	V
Accuracy						
	Resolution		16			Bits
INL	Relative Accuracy, INL(1)		-12		12	LSB
DNL	Differential Nonlinearity, DNL(1)	Ensured monotonic	-1		1	LSB
TUE	Total Unadjusted Error, TUE(1)	-40℃ to +125℃, VOUT unloaded	-0.1	±0.05	0.1	%FSR
		T_A = +25°C, VOUT unloaded	-0.075		0.075	%FSR
ZCE	Zero Code Error(3)	Unipolar ranges only, VOUT unloaded, -40℃ to +125℃	-2.5		2.5	mV
		Unipolar ranges only, VOUT unloaded, T_A = 25℃		0.14		mV
ZCE-TC	Zero Code Error Temperature Coefficient	Unipolar ranges only, -40℃ to +125℃		2		ppm FSR/ºC
BPZE	Bipolar Zero Error	Bipolar range only, 0x8000h into DAC -40℃ to +125℃, VOUT unloaded	-0.03		0.03	%FSR
		Bipolar range only, 0x8000h into DAC, T_A = +25°C, VOUT unloaded	-0.025		0.025	%FSR
BPZE-TC	Bipolar Zero Error Temperature Coefficient	Bipolar range only, 0x8000h into DAC, -40℃ to +125℃, VOUT unloaded		1		ppm FSR/ºC
GE	Gain Error(1)	-40℃ to +125℃, VOUT unloaded	-0.1		0.1	%FSR
		T_A = +25°C, VOUT unloaded	-0.07		0.07	%FSR
GE-TC	Gain Error Temperature Coefficient	-40℃ to +125℃		3		ppm FSR/ºC
PFSE	Positive Full Scale Error	0xFFFFh into DAC, -40℃ to +125℃, VOUT unloaded	-0.1		0.1	%FSR
		0xFFFFh into DAC, T_A = 25℃, VOUT unloaded		0.03		%FSR
NFSE	Negative Full Scale Error(3)	Bipolar ranges only, 0x0000h into DAC, -40℃ to +125℃, VOUT unloaded	-0.06		0.06	%FSR
		Bipolar ranges only, 0x0000h into DAC, T_A = 25℃, VOUT unloaded		0.002		%FSR
PFSE-TC	Positive Full Scale Error Temperature Coefficient	VOUT unloaded, -40℃ to +125℃		2		ppm FSR/ºC
NFSE-TC	Negative Full Scale Error Temperature Coefficient	VOUT unloaded, -40℃ to +125℃		2		ppm FSR/ºC
	Headroom	Output unloaded, VPOS_IN_x with respect to VOUT_x, 0xFFFFh into DAC, No load	0.5			V
		Output unloaded, VPOS_IN_x with respect to VOUT_x, 0xFFFFh into DAC, 1 kΩ load	3			V

(3) DAC code at 0d, this error includes offset error of the DAC since the DAC is linear between 0d to 65535d

Electrical Characteristics (continued)

AVDD/PVDD_x/VPOS_IN_x = +15 V, VNEG_IN_x = -15 V, VSENSEN_x = PBKG = PVSS_x = 0 V, External DVDD = 2.7 V. VOUT : R_L = 1 kΩ, C_L = 200 pF, IOUT : R_L = 250 Ω; all specifications -40℃ to +125℃, unless otherwise noted. REFIN= +5 V external;, Buck-Boost Converter disabled unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Footroom	Bipolar, ranges only, VNEG_IN_x with respect to VOUT_x, 0x0000h into DAC	3			V
		Unipolar ranges only, VNEG_IN_x with respect to VOUT_x, 0x0000h into DAC	5			V
	Short-Circuit Current	SCLIM[1:0] = "00" (see register map)	17		23	mA
		SCLIM[1:0] = "01" (see register map)	8		11	mA
		SCLIM[1:0] = "10" (see register map)	22		28	mA
		SCLIM[1:0] = "11" (see register map)	26		34	mA
R_L	Load		1			kΩ
C_L	Capacitive Load Stability	R_L = Open			20	nF
		R_L = 1 kΩ			20	nF
		R_L = 1 kΩ with External compensation capacitor (150 pF) connected			1	µF
Z_O	DC Output Impedance	Voltage output enabled, VOUT = Mid Scale, UP10V range		0.01		Ω
		Voltage output disabled (POC = '1')		50		MΩ
		Voltage output disabled (POC = '0')		30		kΩ
ILEAK	Output Leakage (VOUT_x Pin)	Voltage output disabled (POC = '1')		1		nA
DC-PSRR	DC Power Supply Rejection Ratio	No output load		10		µV/V
	VSENSEP Impedance	VOUT enabled Mid-Scale UP10		240		kΩ
	VSENSEN Impedance	VOUT enabled Mid-Scale UP10		120		kΩ
EXTERNAL REFERENCE INPUT						
IREF	External Reference Current	VOUT = Full scale, BP12V range, per channel		0.35		mA
	Reference Input Capacitance			100		pF
INTERNAL REFERENCE OUTPUT						
VREF	Reference Output	T_A = 25°C	4.99		5.01	V
VREF-TC	Reference TC	T_A = -40℃ to +125℃	-13		13	ppm/°C
		T_A = -25℃ to +125℃	-10		10	ppm/°C
TUE	DAC Voltage Output Total Unadjusted Error[(1)]	-40°C to +125°C, VOUT_x unloaded, Internal reference enabled		0.2		%FSR
	DAC Current Output Total Unadjusted Error[(1)]	-40°C to +125°C, Internal reference enabled		0.2		%FSR
		-40°C to +125°C, Internal reference enabled, 4 mA to 20 mA range		0.5		%FSR
	Output Noise (0.1 Hz to 10 Hz)	T_A = 25°C		13		µV p-p
	Noise Spectral Density	At 10 kHz, At 25°C		200		nV/sqrtHz
C_L	Capacitive Load				600	nF
I_L	Load Current			±5		mA
	Short Circuit Current	Ref-Out shorted to PBKG		20		mA
	Load Regulation	Sourcing and Sinking, T_A = +25°C		5		µV/mA
	Line Regulation	T_A = +25°C		2		uV/V
BUCK BOOST CONVERTER						
RON	Switch On Resistanvce	T_A = +25°C		3		Ω
ILEAK	Switch Leakage Current	T_A = +25°C		20		nA
L	Inductor	Between LP_x and LN_x		100		µH

Electrical Characteristics (continued)

AVDD/PVDD_x/VPOS_IN_x = +15 V, VNEG_IN_x = -15 V, VSENSEN_x = PBKG = PVSS_x = 0 V, External DVDD = 2.7 V. VOUT : R_L = 1 kΩ, C_L = 200 pF, IOUT : R_L = 250 Ω; all specifications -40℃ to +125℃, unless otherwise noted. REFIN= +5 V external;, Buck-Boost Converter disabled unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ILMAX	Peak Inductor Current	T_A = +25°C, PVDD = AVDD = 36 V, Buck-Boost Converter enabled			0.5	A
V_O	Output Voltage	VPOS_IN_x minimum		4		V
		VPOS_IN_x maximum		32		V
V_O	Output Voltage	VNEG_IN_x minimum		-18		V
		VNEG_IN_x maximum		-5		V
C_L	Load Capacitor	VPOS_IN_x and VNEG_IN_x	10			µF
	Start Up Time	After enabling VPOS_IN_x and VNEG_IN_x with 10 µF load capacitor on these pins		3		ms
DVDD LDO						
V_O	Output Voltage			5		V
ILOAD	Load Current				10	mA
C_L	Load Capacitor				0.2	nF
THERMAL ALARM						
	Trip Point			150		°C
	Hysteresis			15		°C
DIGITAL INPUTS						
	Hysteresis Voltage			0.4		V
	Input Current		-5		5	µA
	Input Current (DVDD_EN)		-10		10	µA
	Pin Capacitance	Per pin		10		pF
DIGITAL OUTPUTS						
SDO						
V_{OL}	Output Low Voltage	Sinking 200 µA			0.4	V
V_{OH}	Output High Voltage	Sourcing 200 µA	DVDD-0.5			V
ILEAK	High Impedance Leakage		-5		5	µA
	High Impedance Output Capacitance			10		pF
$\overline{\text{ALARM}}$						
V_{OL}	Output Low Voltage	At 2.5 mA		0.4		V
ILEAK	High Impedance Leakage			50		µA
	High Impedance Output Capacitance			10		pF
POWER REQUIREMENTS						
IAVDD+IPVDD	Current Flowing into AVDD and PVDD	All Buck-Boost converter positive output enabled, IOUT_x mode operation, All IOUT channels enabled, 0 mA, PVDD = AVDD = 12 V, Internal reference, VNEG_IN_x = 0 V		5		mA
		All IOUT Active, 0 mA, 0 to 24 mA range, VNEG_IN_x = 0 V		3.5	5	mA
IPVDD_x	Current Flowing into PVDD	Buck-Boost converter enabled, Peak current			0.5	A
		Buck-Boost converter disabled		0.1		mA
IDVDD	Current Flowing into DVDD	All digital pins at DVDD, DVDD = 5.5 V		1.8		mA
IVPOS_IN_x	Current Flowing into VPOS_IN_x	IOUT active, 0 mA, 0 to 24 mA range			1.2	mA
		VOUT active, No load, 0 to 10 V range, Mid scale code			3	mA

Electrical Characteristics (continued)

AVDD/PVDD_x/VPOS_IN_x = +15 V, VNEG_IN_x = -15 V, VSENSEN_x = PBKG = PVSS_x = 0 V, External DVDD = 2.7 V. VOUT : R_L = 1 kΩ, C_L = 200 pF, IOUT : R_L = 250 Ω; all specifications -40℃ to +125℃, unless otherwise noted. REFIN= +5 V external;, Buck-Boost Converter disabled unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IVNEG_IN_x	Current Flowing into VNEG_IN_x	IOUT active, 0 mA, ±24 mA range			1.2	mA
		VOUT active, No load, 0 to 10 V range, Mid scale code			3	mA
PDISS	Power Dissipation (PVDD+AVDD)	All Buck-Boost converter positive output enabled, IOUT_x mode operation, All IOUT channels enabled, Rload = 1 Ω, 24 mA, PVDD = AVDD = 12 V, Internal reference, VNEG_IN_x = 0 V		0.86	1.1	W
IVSENSEP	Current Flowing into VSENSEP	VOUT disabled			40	nA
IVSENSEN	Current Flowing into VSENSEN	VOUT disabled			20	nA
DYNAMIC PERFORMANCE						
Voltage Output						
T_{sett}	Output Voltage Settling Time	0 to10 V, to ±0.03% FSR RL = 1K||CL = 200 pF		15		µs
		0 to 5 V, to ±0.03% FSR RL = 1K||CL = 200 pF		10		µs
		-5 to 5 V, to ±0.03% FSR RL = 1K||CL = 200 pF		15		µs
		-10 to 10 V, to ±0.03% FSR RL = 1K||CL = 200 pF		30		µs
	Output Voltage Ripple	Buck-Boost converter enabled, 50 KHz, 20dB/decade filter on VPOS_IN_x		2		mVpp
SR	Slew Rate	R_L = 1K||CL = 200 pF		1		V/µs
	Power-On Glitch Magnitude (2)			0.1		V
	Power-off Glitch Magnitude (4)			0.8		V
	Channel to Channel DC Crosstalk	Full scale swing on adjacent channel		2		m%FSR
	Code-to-Code Glitch			0.15		µV-sec
	Digital Feedthrough			1		nV-sec
	Output Noise (0.1 Hz to 10 Hz bandwidth)	UP10V, Mid scale		0.1		LSB p-p
	Output Noise (100 kHz bandwidth)	UP10V, Mid scale		200		µVrms
	Output Noise Spectral Density	BP20V Measured at 10 kHz, Mid scale		200		nV/sqrtHz
AC-PSRR	AC Power Supply Rejection Ratio	200 mV 50/60Hz Sine wave superimposed on power supply voltage. (AC analysis)		-75		dB
Current Output						
Tsett	Output Current Settling Time	24 mA Step, to 0.1% FSR, no L		10		µs
		24 mA Step, to 0.1% FSR , L = 1 mH, C_L = 22 nF		50		µs
	Output Current Ripple	Buck-Boost converter enabled, 50 KHz, 20dB/decade filter on VPOS_IN_x		8		µApp
L	Inductive Load (5)				50	mH
AC-PSRR	AC Power Supply Rejection Ratio	200 mV 50/60Hz Sine wave superimposed on power supply voltage.		-75		dB

(4) Vout disabled, no load, ramp rate of VPOS_IN_x,and VNEG_IN_x limited to 18 V/msec
(5) 680 nF is required at IOUT pin for 50 mH pure inductor load.

7.6 Timing Requirements: Write and Readback Mode

At T_A = –40°C to +125°C and DVDD = +2.7 V to +5.5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{SCLK}	Max clock frequency			25	MHz
t_1	SCLK cycle time		40		ns
t_2	SCLK high time		18		ns
t_3	SCLK low time		18		ns
t_4	$\overline{\text{SYNC}}$ falling edge to SCLK falling edge setup time		15		ns
t_5	$24^{th}/32^{nd}$ SCLK falling edge to $\overline{\text{SYNC}}$ rising edge		13		ns
t_6	$\overline{\text{SYNC}}$ high time		40		ns
t_7	Data setup time		8		ns
t_8	Data hold time		5		ns
t_9	$\overline{\text{SYNC}}$ rising edge to $\overline{\text{LDAC}}$ falling edge		33		ns
t_{10}	$\overline{\text{LDAC}}$ pulse width low		10		ns
t_{11}	$\overline{\text{LDAC}}$ falling edge to DAC output response time			50	ns
t_{12}	DAC output settling time		See *Electrical Characteristics*		µs
t_{13}	CLR high time		10		ns
t_{14}	CLR activation time			50	ns
t_{15}	SCLK rising edge to SDO valid			14	ns
t_{16}	$\overline{\text{SYNC}}$ rising edge to DAC output response time			50	ns
t_{17}	$\overline{\text{LDAC}}$ falling edge to $\overline{\text{SYNC}}$ rising edge		100		ns
t_{18}	$\overline{\text{RESET}}$ pulse width		10		ns
t_{19}	$\overline{\text{SYNC}}$ rising edge to CLR falling/rising edge		60		ns

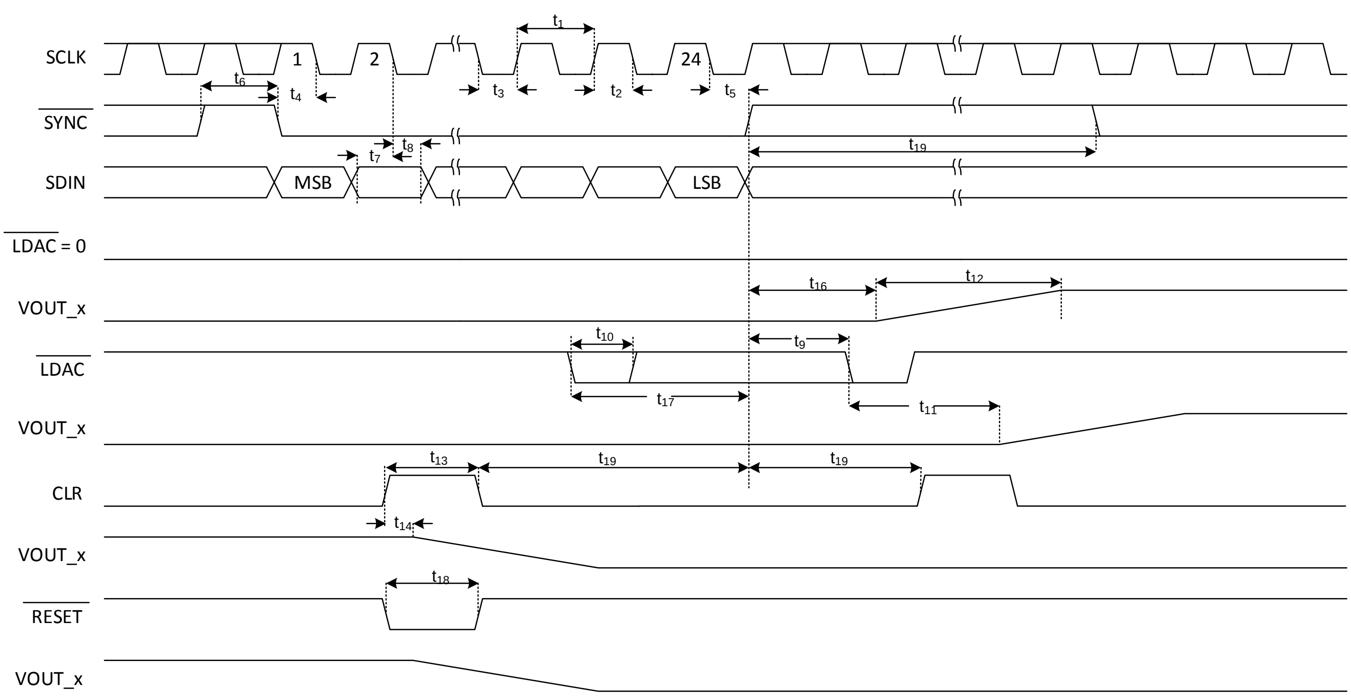


图 1. Write Mode Timing

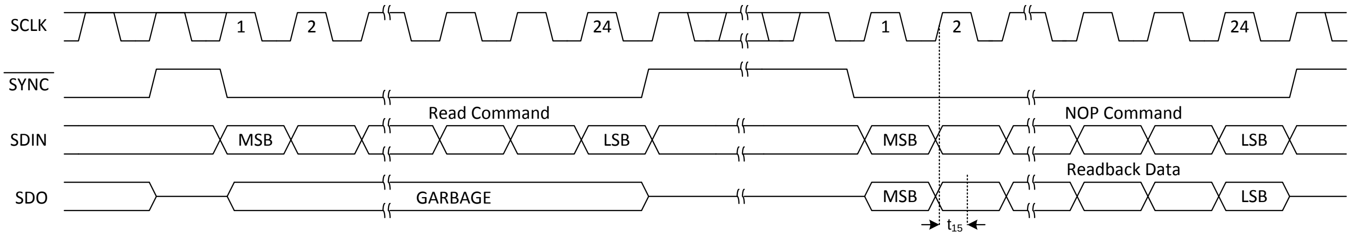


图 2. Readback Mode Timing

7.7 Typical Characteristics

AVDD/PVDD_x/VPOS_IN_x = +15 V, VNEG_IN_x = –15 V, PBKG = PVSS_x = 0 V, External DVDD = 5 V, VOUT disabled, IOUT R_L = 250 Ω, T_A = 25℃, REFIN = +5 V external, Buck-Boost Converter disabled, unless otherwise stated.

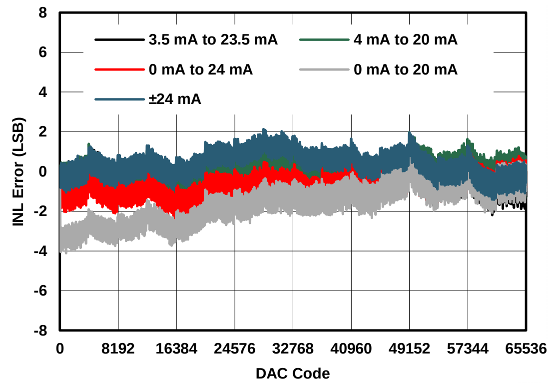


图 3. IOUT Linearity Error vs Digital Input Code

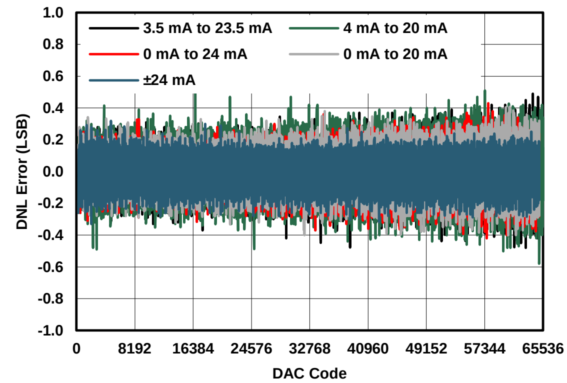


图 4. IOUT Differential Linearity Error vs Digital Input Code

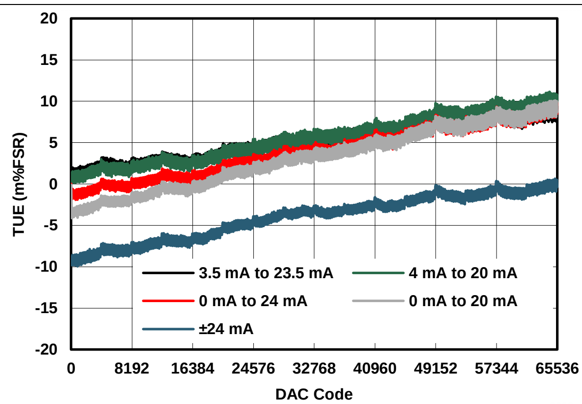


图 5. IOUT Total Unadjusted Error vs Digital Input Code

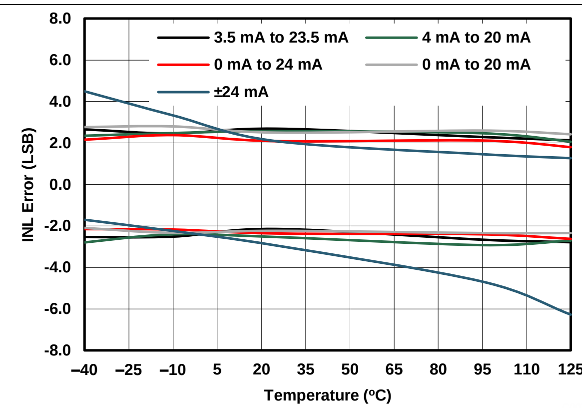


图 6. IOUT Linearity Error vs Temperature

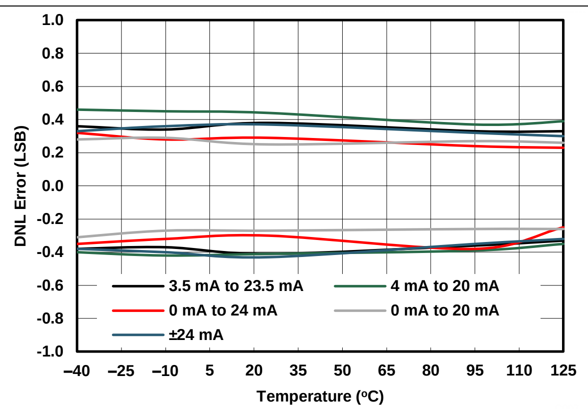


图 7. IOUT Differential Linearity Error vs Temperature

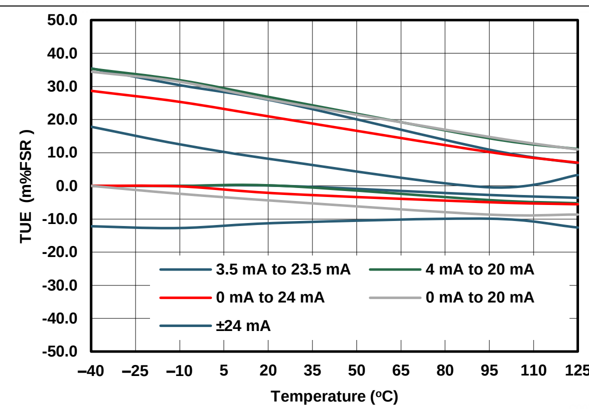


图 8. IOUT Total Unadjusted Error vs Temperature

Typical Characteristics (接下页)

AVDD/PVDD_x/VPOS_IN_x = +15 V, VNEG_IN_x = –15 V, PBKG = PVSS_x = 0 V, External DVDD = 5 V VOUT disabled, IOUT R_L = 250 Ω, T_A = 25℃, REFIN= +5 V external, Buck-Boost Converter disabled, unless otherwise stated.

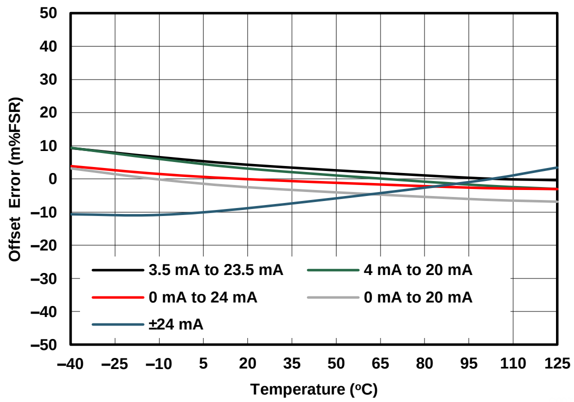


图 9. IOUT Offset Error vs Temperature

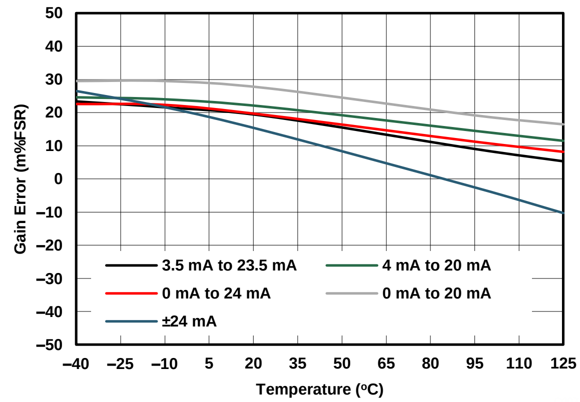


图 10. IOUT Gain Error vs Temperature

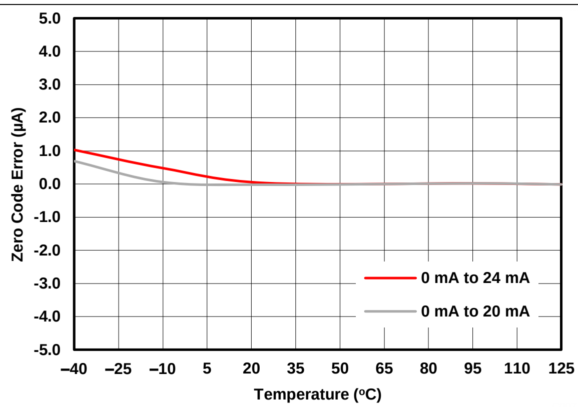


图 11. IOUT Zero Code Error vs Temperature

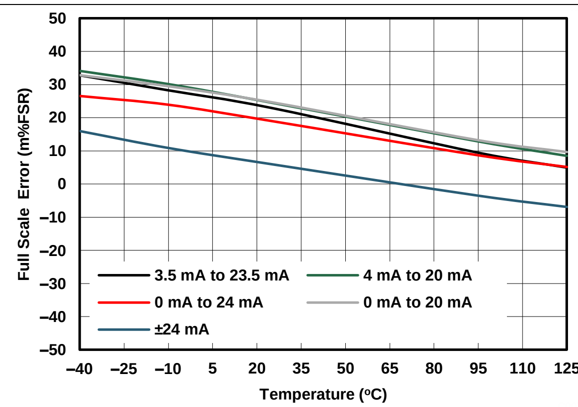


图 12. IOUT Full Scale Error vs Temperature

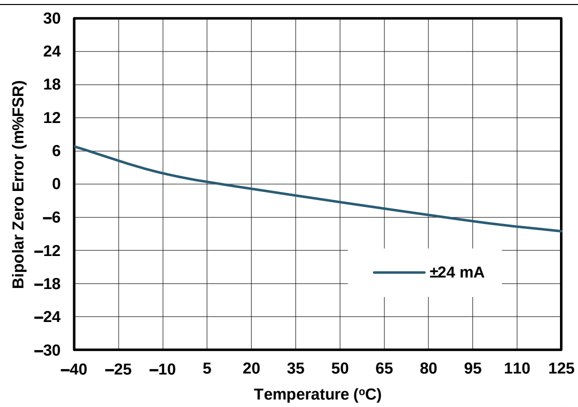


图 13. IOUT Bipolar Zero Error vs Temperature

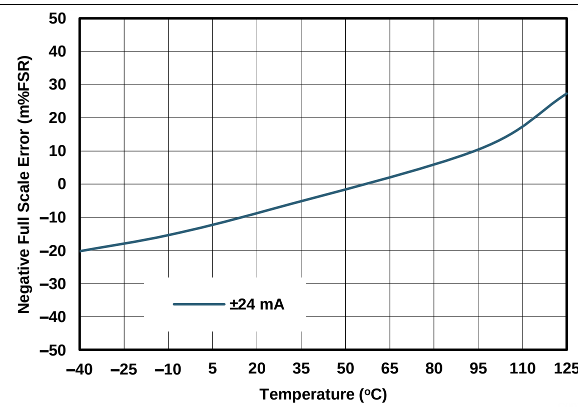


图 14. IOUT Negative Full Scale Error vs Temperature

Typical Characteristics (接下页)

AVDD/PVDD_x = VPOS_IN_x , VNEG_IN_x = PBKG = PVSS_x = 0 V, External DVDD = 5 V VOUT disabled, IOUT R_L = 250 Ω, T_A = 25℃, REFIN = +5 V external, Buck-Boost Converter disabled, unless otherwise stated.

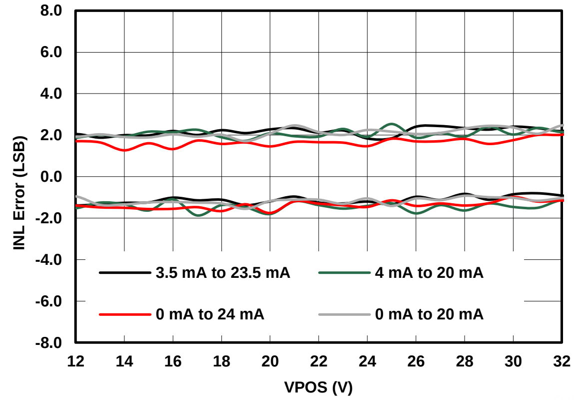


图 15. IOUT Linearity Error vs Power Supplies

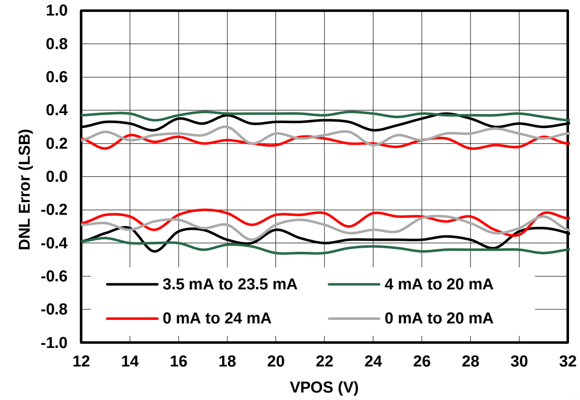
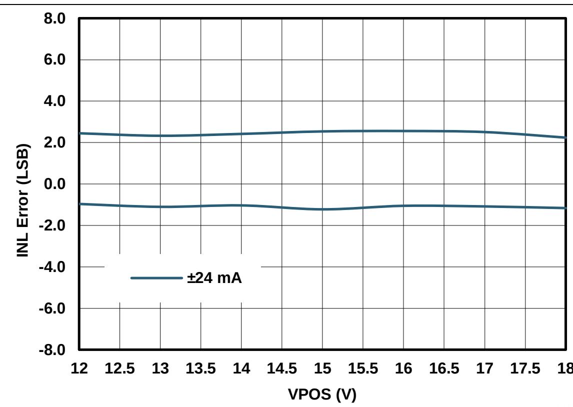
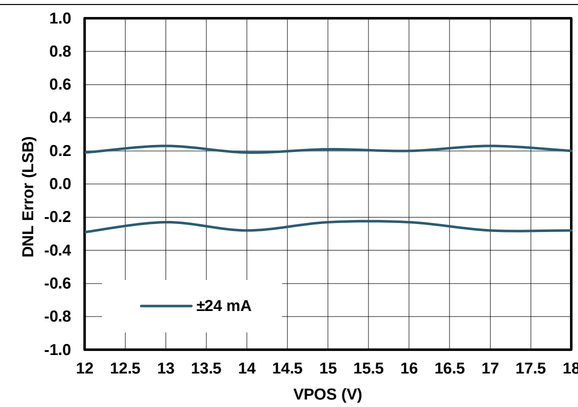


图 16. IOUT Differential Linearity Error vs Power Supplies



|VPOS_IN_x| = |VNEG_IN_x|

图 17. IOUT Linearity Error vs Power Supplies



|VPOS_IN_x| = |VNEG_IN_x|

图 18. IOUT Differential Linearity Error vs Power Supplies

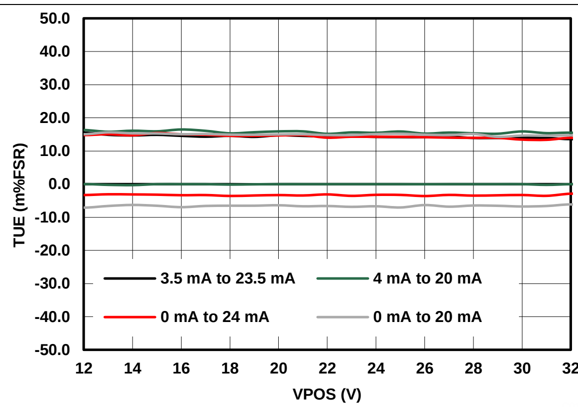
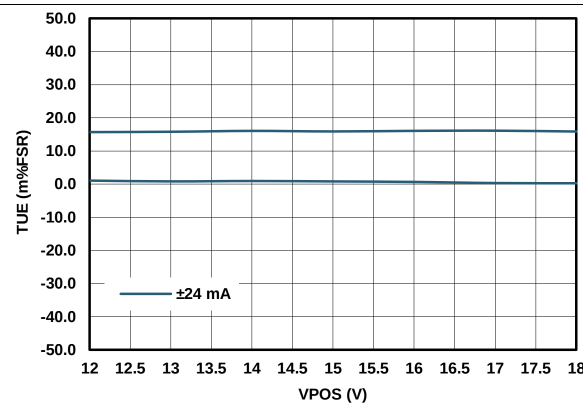


图 19. IOUT Total Unadjusted Error vs Power Supplies

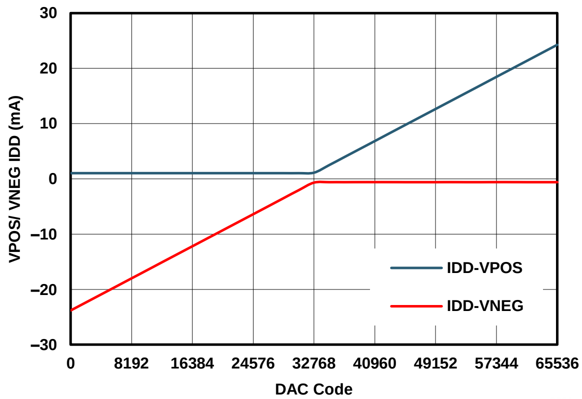


|VPOS_IN_x| = |VNEG_IN_x|

图 20. IOUT Total Unadjusted Error vs Power Supplies

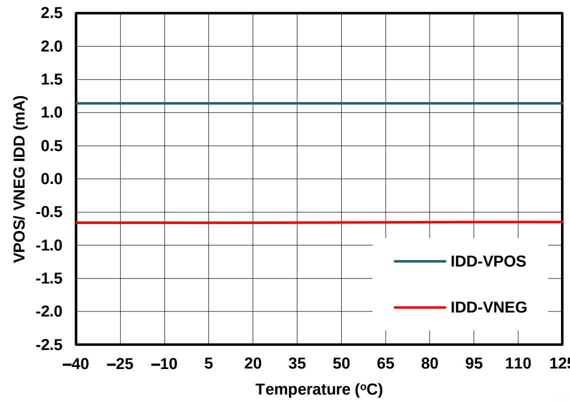
Typical Characteristics (接下页)

AVDD/PVDD_x/VPOS_IN_x = +15 V, VNEG_IN_x = –15 V, PBKG = PVSS_x = 0 V, External DVDD = 5 V VOUT disabled, IOUT R_L = 250 Ω, T_A = 25℃, REFIN = +5 V external, Buck-Boost Converter disabled, unless otherwise stated.



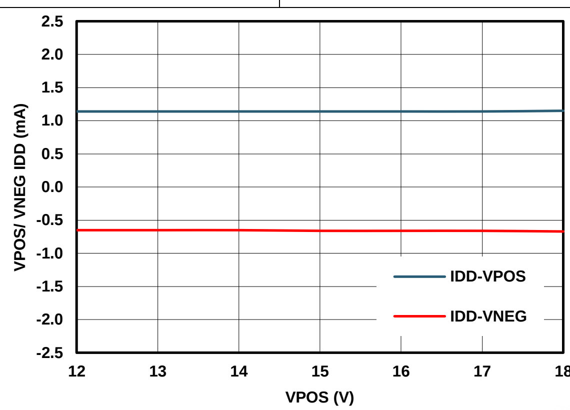
±24 mA Range

图 21. IOUT Power Supply Current vs Digital Input Code



±24 mA Range, Mid Scale Code

图 22. IOUT Power Supply Current vs Temperature

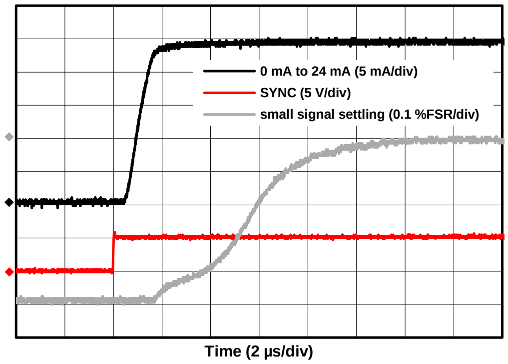


|VPOS_IN_x| = |VNEG_IN_x|, ±24 mA Range, Mid Scale Code

图 23. IOUT Power Supply Current vs Power Supplies Voltages

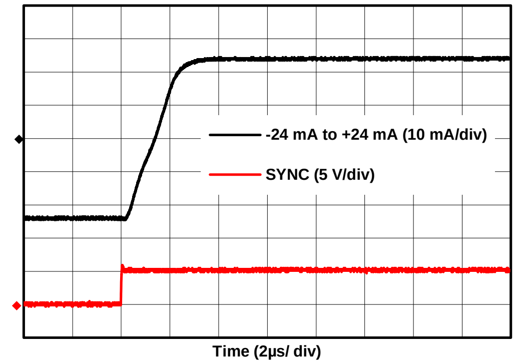
Typical Characteristics (接下页)

AVDD/PVDD_x/VPOS_IN_x = +15 V, VNEG_IN_x = –15 V, PBKG = PVSS_x = 0 V, External DVDD = 5 V VOUT disabled, IOUT R_L = 250 Ω, T_A = 25℃, REFIN = +5 V external, Buck-Boost Converter disabled, unless otherwise stated.



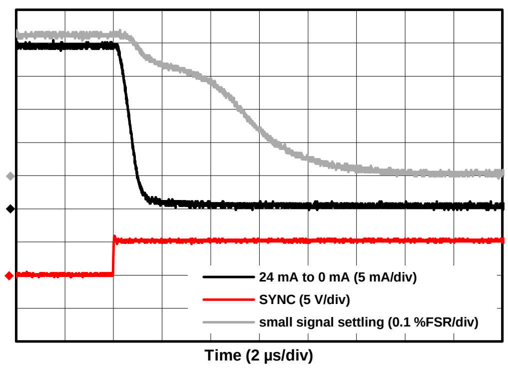
0-24 mA Range

图 24. IOUT Full-Scale Settling Time, Rising Edge



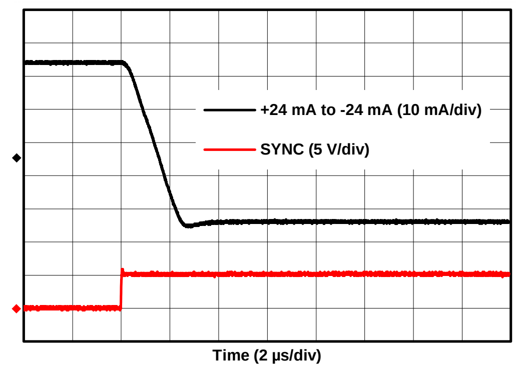
AVDD/PVDD_x/VPOS_IN_x = +18 V, VNEG_IN_x = –18 V, IOUT R_L = 625 Ω

图 25. IOUT Full-Scale Settling Time, Rising Edge



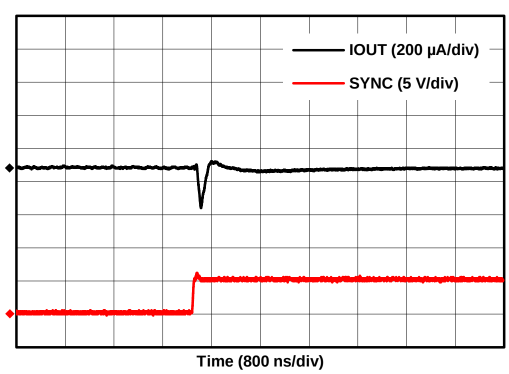
0-24 mA Range

图 26. IOUT Full-Scale Settling Time, Falling Edge



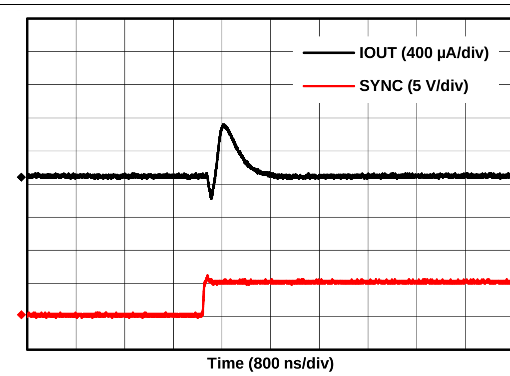
AVDD/PVDD_x/VPOS_IN_x = +18 V, VNEG_IN_x = –18 V, IOUT R_L = 625 Ω

图 27. IOUT Full-Scale Settling Time, Falling Edge



0-24 mA Range, 7FFFh - 8000h

图 28. IOUT Glitch Impulse, Rising Edge, 1LSB Step



0-24 mA Range, 8000h - 7FFFh

图 29. IOUT Glitch Impulse, Falling Edge, 1LSB Step

Typical Characteristics (接下页)

AVDD/PVDD_x/VPOS_IN_x = +15 V, VNEG_IN_x = –15 V, PBKG = PVSS_x = 0 V, External DVDD = 5 V VOUT disabled, IOUT R_L = 250 Ω, T_A = 25℃, REFIN = +5 V external, Buck-Boost Converter disabled, unless otherwise stated.

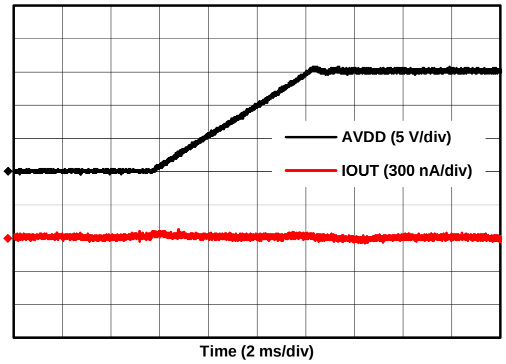
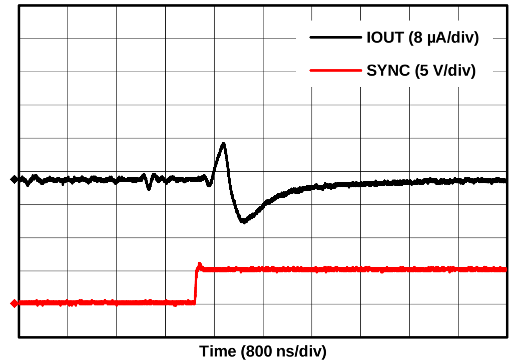
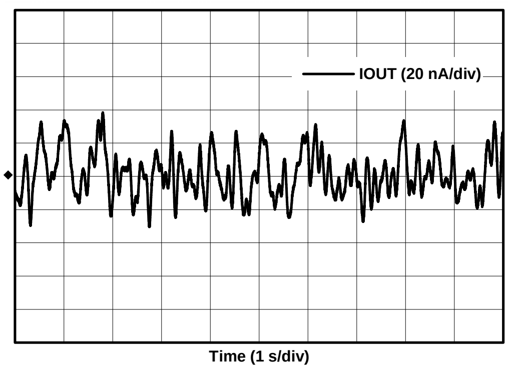


图 30. IOUT Power-On Glitch



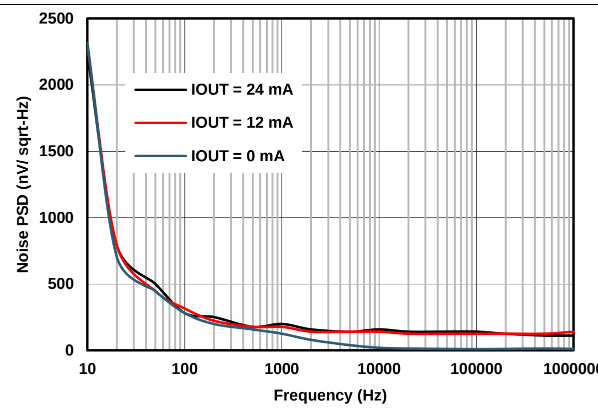
0-24 mA Range

图 31. IOUT Enable Glitch



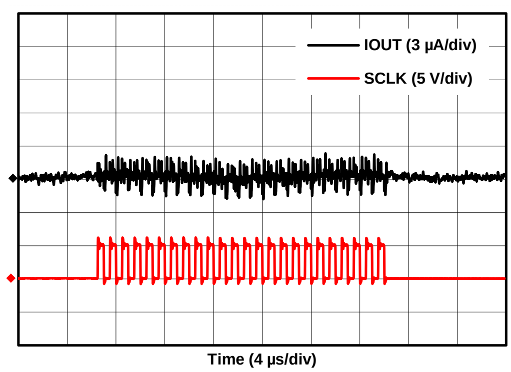
0-24mA Range, Mid Scale Code

图 32. IOUT Noise, 0.1 Hz to 10 Hz



0-24 mA Range

图 33. IOUT Noise Density vs Frequency



0-24 mA Range, Mid Scale Code, SCLK = 1 MHz

图 34. Clock Feedthrough IOUT, 1MHz

Typical Characteristics (接下页)

AVDD/PVDD_x = +15 V, PBKG = PVSS_x = 0 V, External DVDD = 5 V, VOUT disabled, IOUT R_L = 250 Ω, T_A = 25℃, REFIN = +5 V external, Buck-Boost Converter enabled (Full Tracking Mode), unless otherwise stated.

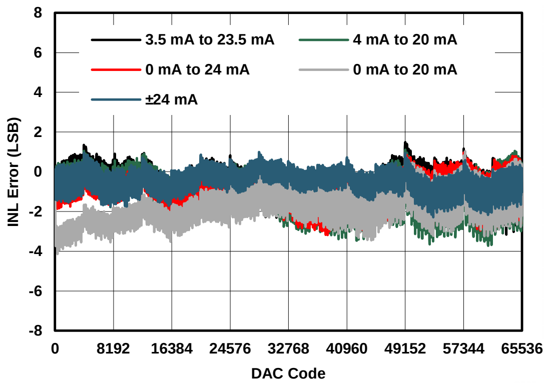


图 35. IOUT Linearity Error vs Digital Input Code

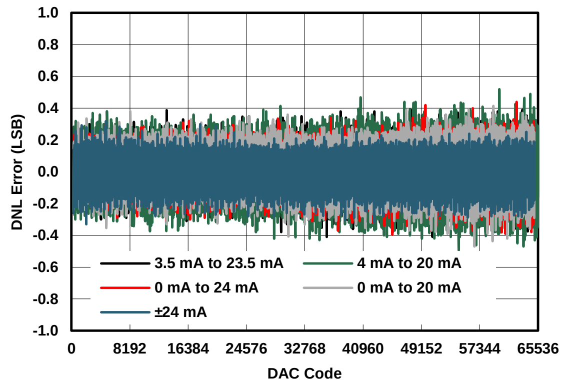


图 36. IOUT Differential Linearity Error vs Digital Input Code

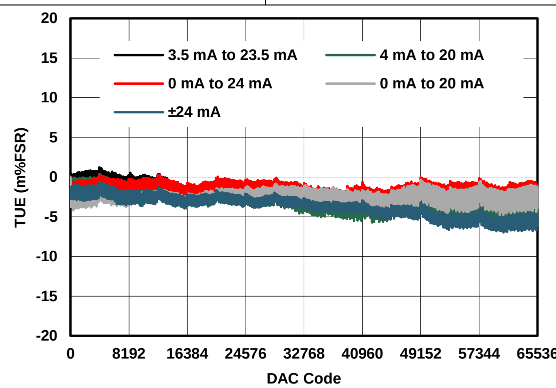
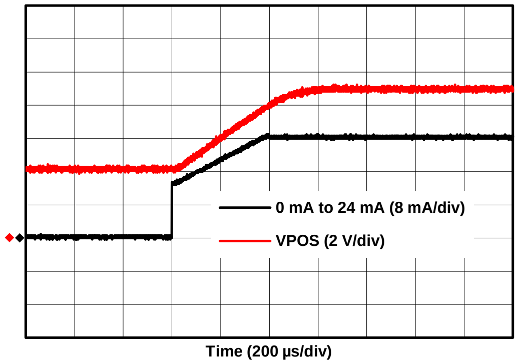


图 37. IOUT Total Unadjusted Error vs Digital Input Code

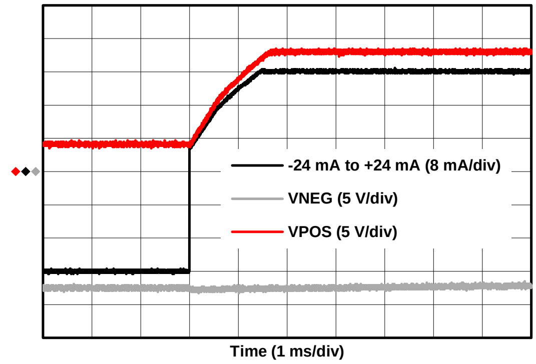
Typical Characteristics (接下页)

AVDD/PVDD_x = +15 V, PBKG = PVSS_x = 0 V, External DVDD = 5 V, VOUT disabled, IOUT R_L = 250 Ω, T_A = 25℃, REFIN = +5 V external, Buck-Boost Converter enabled (Full Tracking Mode), unless otherwise stated.



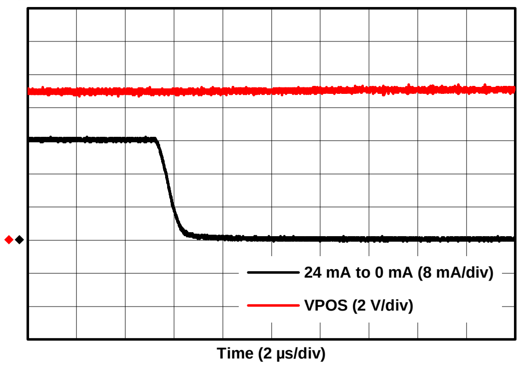
0-24 mA Range

图 38. IOUT Full-Scale Settling Time, Rising Edge



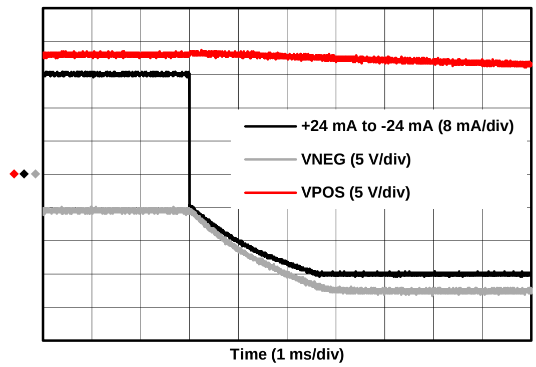
IOUT R_L = 625 Ω

图 39. IOUT Full-Scale Settling Time, Rising Edge



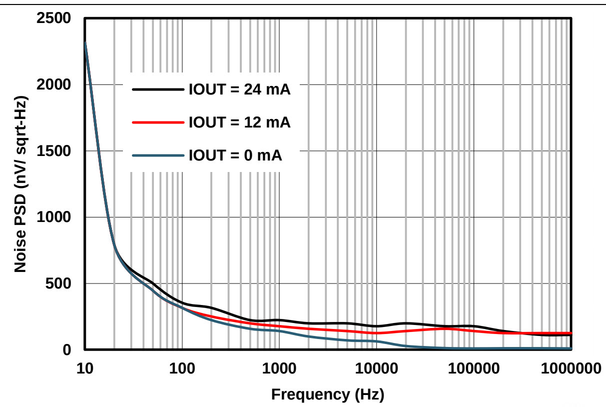
0-24 mA Range

图 40. IOUT Full-Scale Settling Time, Falling Edge



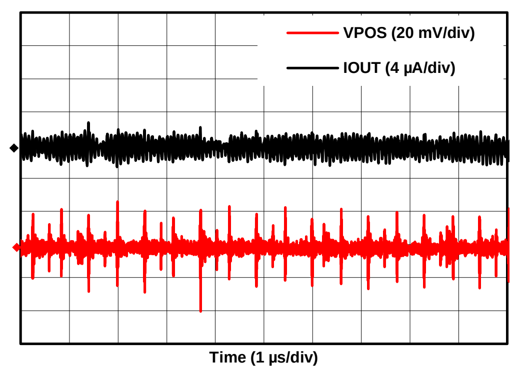
IOUT R_L = 625 Ω

图 41. IOUT Full-Scale Settling Time, Falling Edge



0-24 mA Range

图 42. IOUT Noise Density vs Frequency



0-24 mA Range, Mid Scale Code

图 43. IOUT Ripple

Typical Characteristics (接下页)

AVDD/PVDD_x/VPOS_IN_x = +15 V, VNEG_IN_x = –15 V, VSENSEN_x = PBKG = PVSS_x = 0 V, External DVDD = 5 V. VOUT No load, IOUT disabled; T_A = 25℃, REFIN = +5 V external;, Buck-Boost Converter disabled unless otherwise stated.

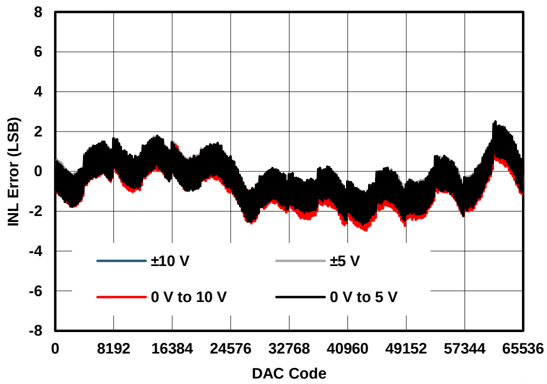


图 44. VOUT Linearity Error vs Digital Input Code

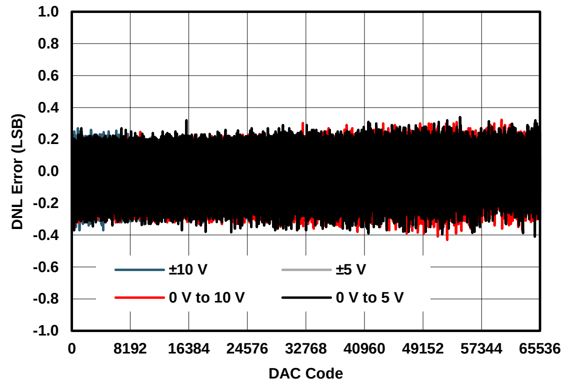


图 45. VOUT Differential Linearity Error vs Digital Input Code

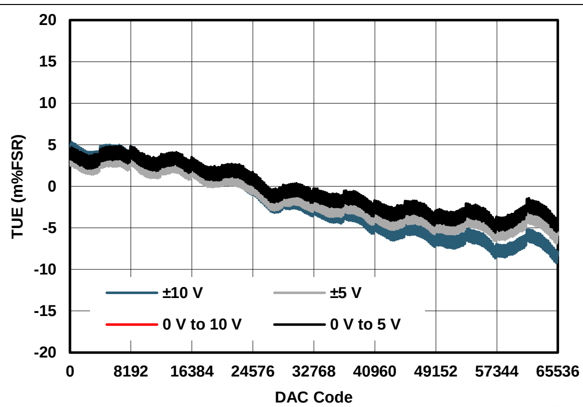


图 46. VOUT Total Unadjusted Error vs Digital Input Code

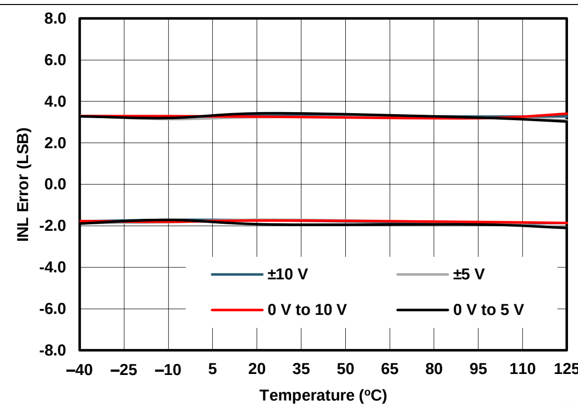


图 47. VOUT Linearity Error vs Temperature

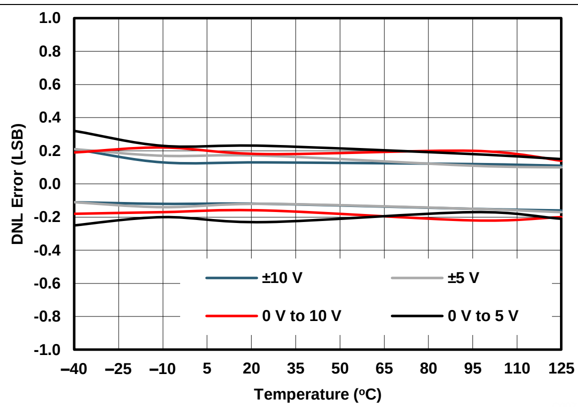


图 48. VOUT Differential Linearity Error vs Temperature

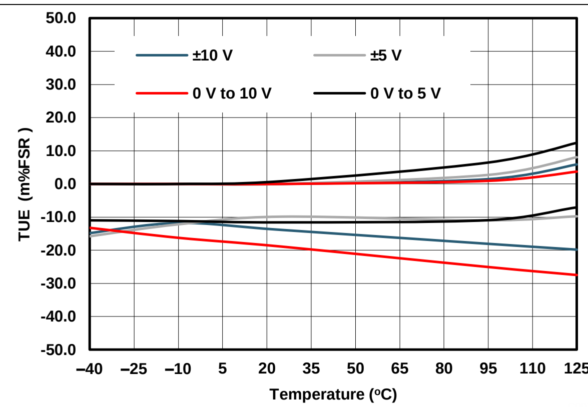


图 49. VOUT Total Unadjusted Error vs Temperature

Typical Characteristics (接下页)

AVDD/PVDD_x/VPOS_IN_x = +15 V, VNEG_IN_x = –15 V, VSENSEN_x = PBKG = PVSS_x = 0 V, External DVDD = 5 V. VOUT No load, IOUT disabled; T_A = 25℃, REFIN = +5 V external; Buck-Boost Converter disabled unless otherwise stated.

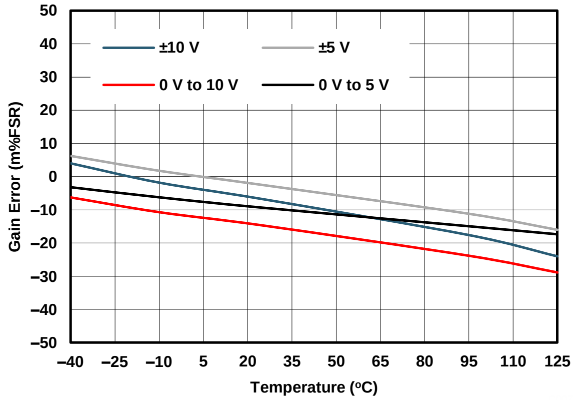


图 50. VOUT Gain Error vs Temperature

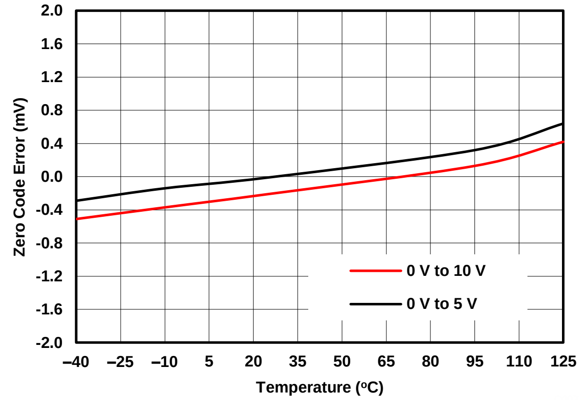


图 51. VOUT Zero Code Error vs Temperature

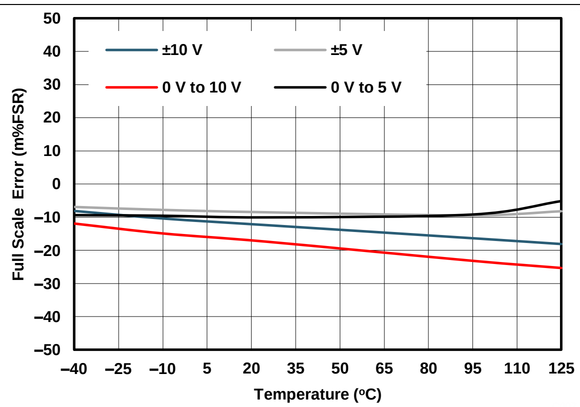


图 52. VOUT Full Scale Error vs Temperature

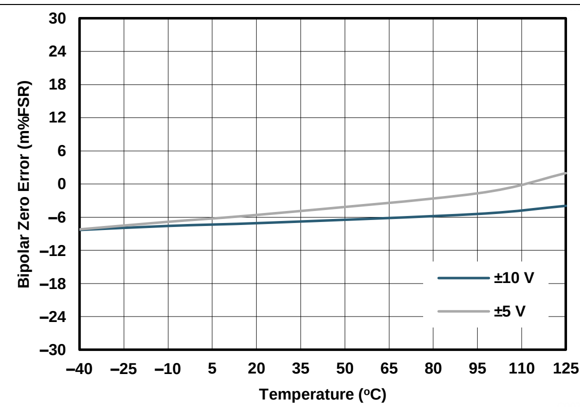


图 53. VOUT Bipolar Zero Error vs Temperature

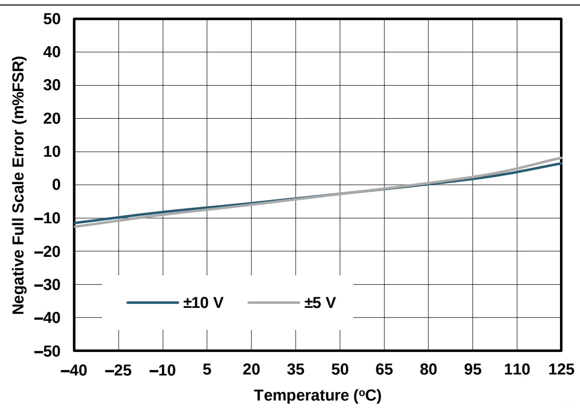
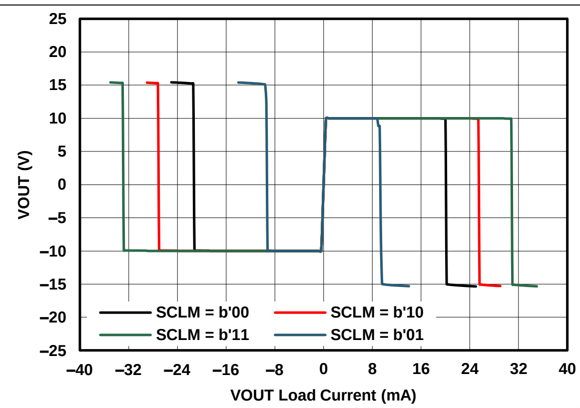


图 54. VOUT Negative Full Scale Error vs Temperature

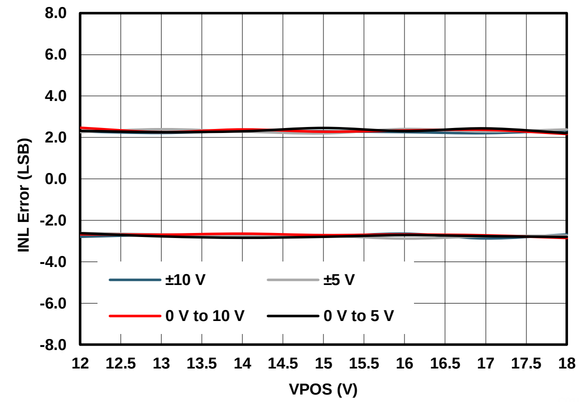


±10-V Range, Full Scale Code for VOUT sourcing & Zero Scale Code for VOUT Sinking

图 55. VOUT Output Voltage vs Load Current

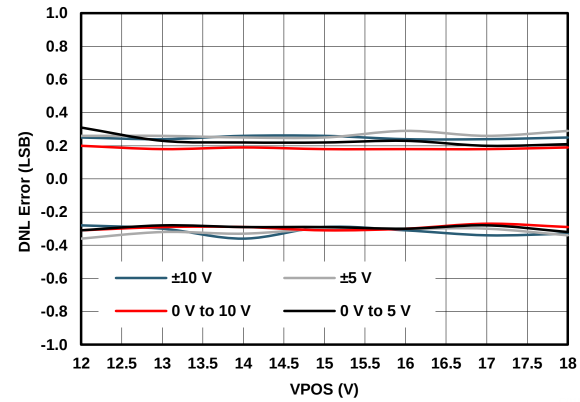
Typical Characteristics (接下页)

AVDD/PVDD_x/VPOS_IN_x = +15 V, VNEG_IN_x = –15 V, VSENSEN_x = PBKG = PVSS_x = 0 V, External DVDD = 5 V. VOUT No load, IOUT disabled; T_A = 25℃, REFIN = +5 V external; Buck-Boost Converter disabled unless otherwise stated.



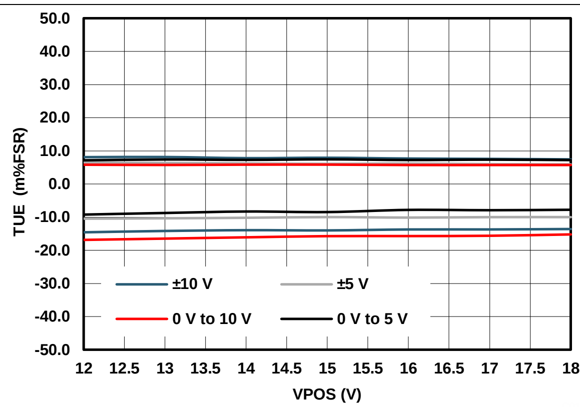
|VPOS_IN_x| = VNEG_IN_x

图 56. VOUT Linearity Error vs Power Supplies



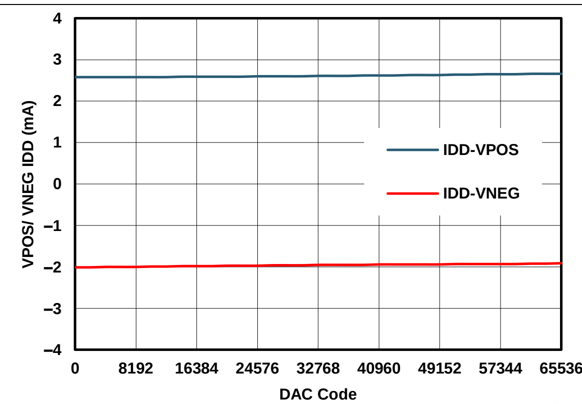
|VPOS_IN_x| = VNEG_IN_x

图 57. VOUT Differential Linearity Error vs Power Supplies



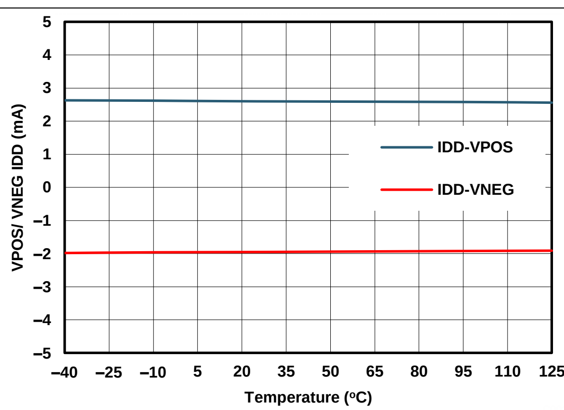
|VPOS_IN_x| = VNEG_IN_x

图 58. VOUT Total Unadjusted Error vs Power Supplies



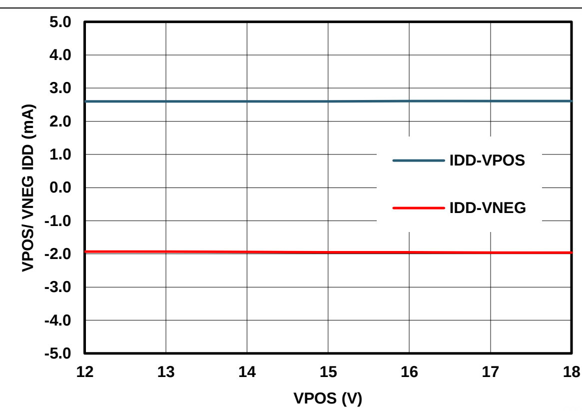
|VPOS_IN_x| = VNEG_IN_x, 10-V Range

图 59. VOUT Power Supply Current vs Digital Input Code



|VPOS_IN_x| = VNEG_IN_x, 10-V Range, Mid Scale Code

图 60. VOUT Power Supply Current vs Temperature

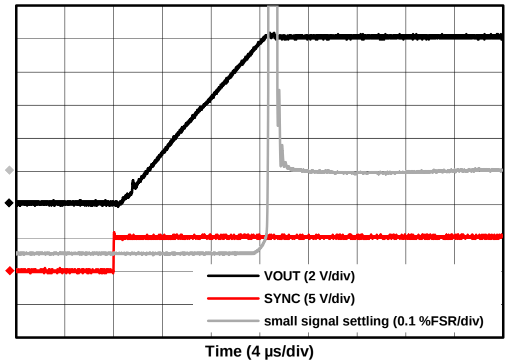


|VPOS_IN_x| = VNEG_IN_x, 10-V Range, Mid Scale Code

图 61. VOUT Power Supply Current vs Power Supplies Voltages

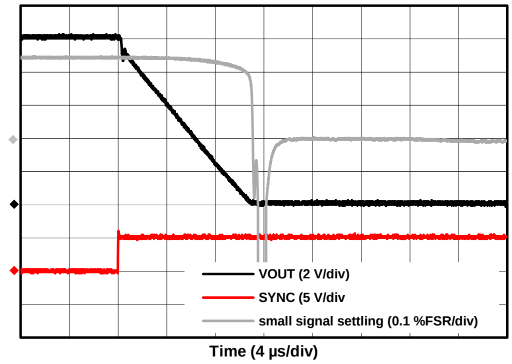
Typical Characteristics (接下页)

AVDD/PVDD_x/VPOS_IN_x = +15 V, VNEG_IN_x = –15 V, VSENSEN_x = PBKG = PVSS_x = 0 V, External DVDD = 5 V. VOUT No load, IOUT disabled; T_A = 25℃, REFIN = +5 V external;, Buck-Boost Converter disabled unless otherwise stated.



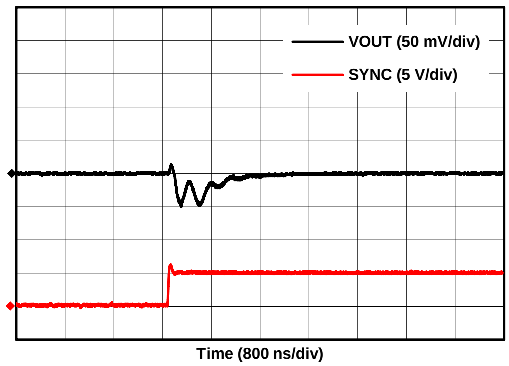
10-V Range, Load 1K//200pF

图 62. VOUT Full-Scale Settling Time, Rising Edge



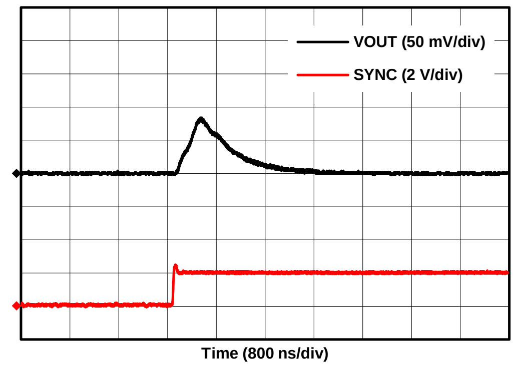
10-V Range, Load 1K//200pF

图 63. VOUT Full-Scale Settling Time, Falling Edge



10-V Range, 7FFFh - 8000h

图 64. VOUT Glitch Impulse, Rising Edge, 1LSB Step



10-V Range, 8000h - 7FFFh

图 65. VOUT Glitch Impulse, Falling Edge, 1LSB Step

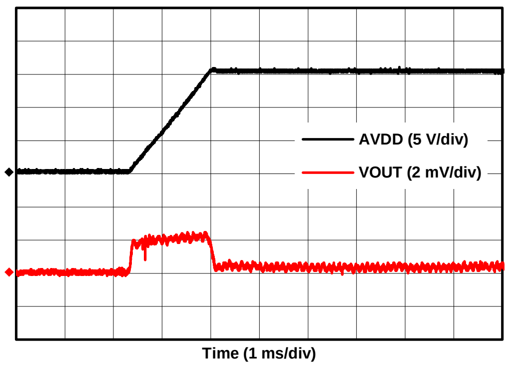
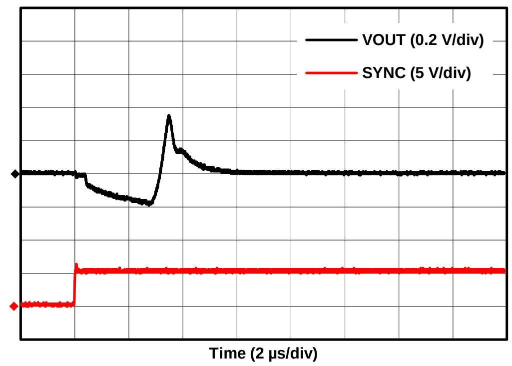


图 66. VOUT Power-On Glitch

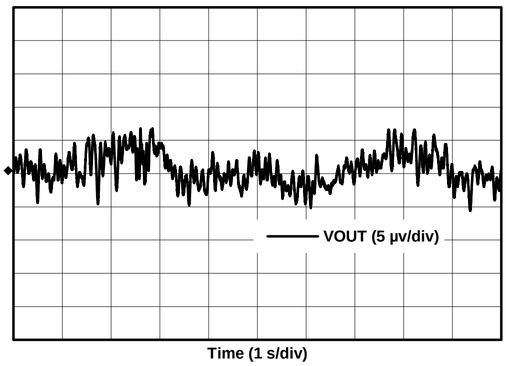


10V Range

图 67. VOUT Enable Glitch

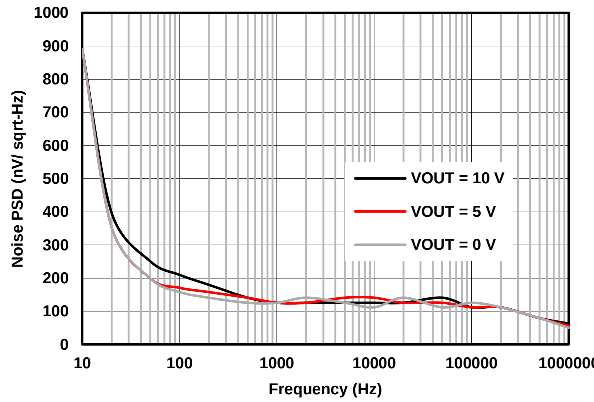
Typical Characteristics (接下页)

AVDD/PVDD_x/VPOS_IN_x = +15 V, VNEG_IN_x = –15 V, VSENSEN_x = PBKG = PVSS_x = 0 V, External DVDD = 5 V. VOUT No load, IOUT disabled; T_A = 25℃, REFIN = +5 V external; Buck-Boost Converter disabled unless otherwise stated.



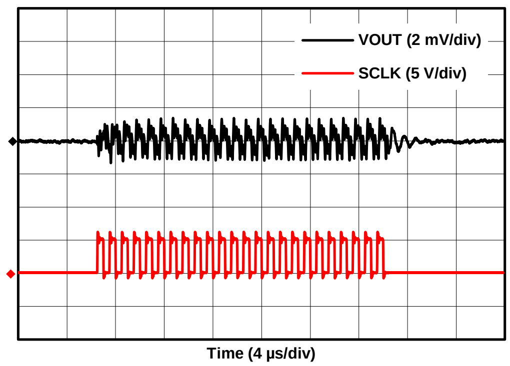
10-V Range, Mid Scale Code

图 68. VOUT Noise, 0.1 Hz to 10 Hz



10-V Range

图 69. VOUT Noise Density vs Frequency



10-V Range, Mid Scale Code, SCLK = 1MHz

图 70. Clock Feedthrough VOUT, 1MHz

Typical Characteristics (接下页)

AVDD/PVDD_x = +15 V, VSENSEN_x = PBKG = PVSS_x = 0 V, External DVDD = 5 V. VOUT No load, IOUT disabled; T_A = 25℃, REFIN = +5 V external; Buck-Boost Converter enabled (Full Tracking Mode), unless otherwise stated.

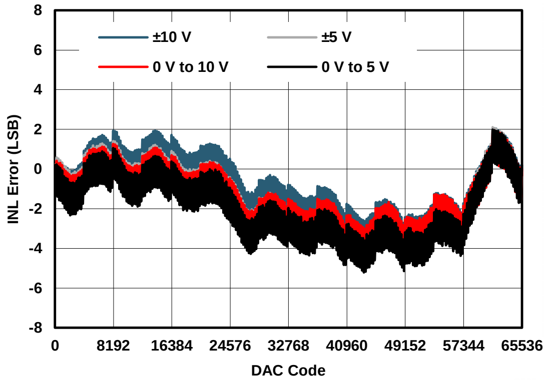


图 71. VOUT Linearity Error vs Digital Input Code

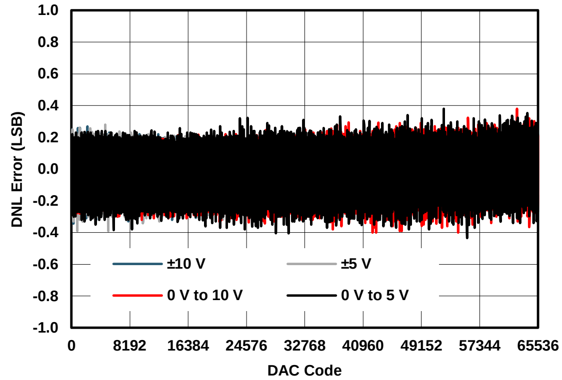


图 72. VOUT Differential Linearity Error vs Digital Input Code

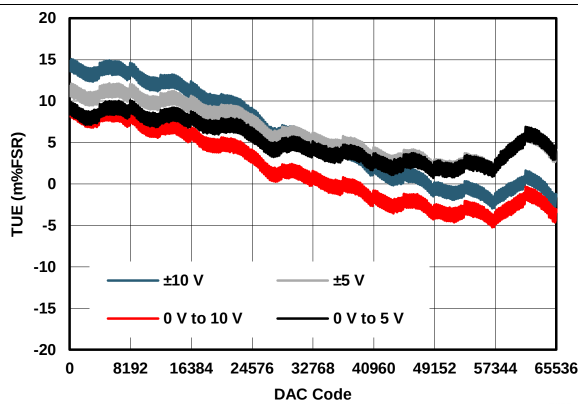
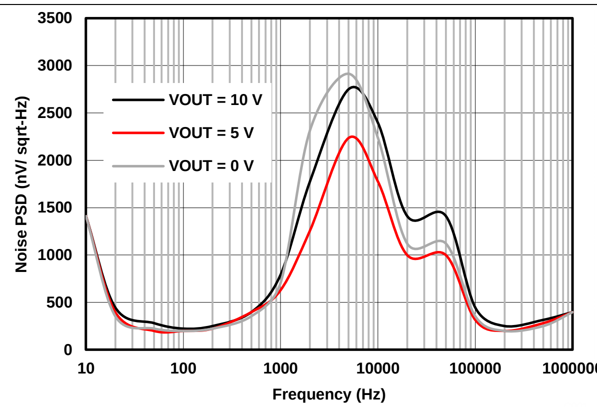
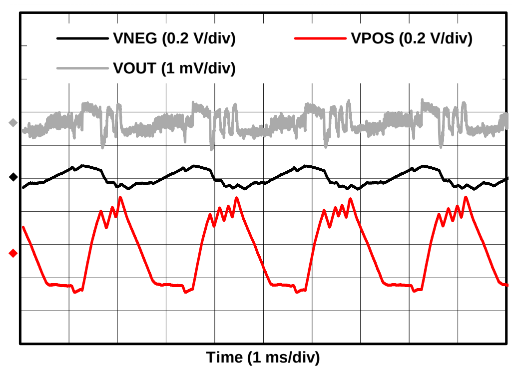


图 73. VOUT Total Unadjusted Error vs Digital Input Code



10-V Range

图 74. VOUT Noise Density vs Frequency

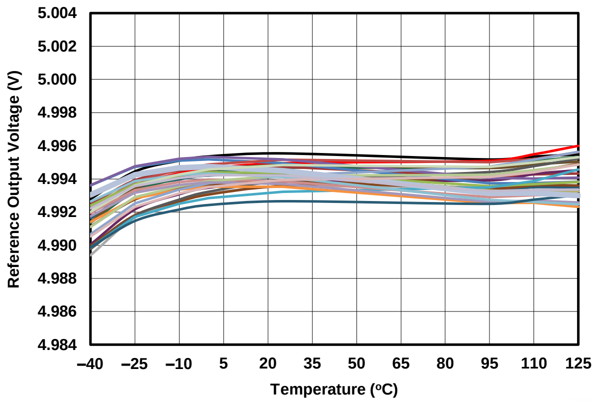


10-V Range, Mid Scale Code

图 75. VOUT Ripple

Typical Characteristics (接下页)

AVDD/PVDD_x/VPOS_IN_x = +15 V, VNEG_IN_x = –15 V, PBKG = PVSS_x = 0 V, External DVDD = 5 V. VOUT disabled, IOUT disabled, T_A = 25℃, Buck-Boost Converter disabled, unless otherwise stated.



30 Units

图 76. Internal Reference Voltage vs Temperature

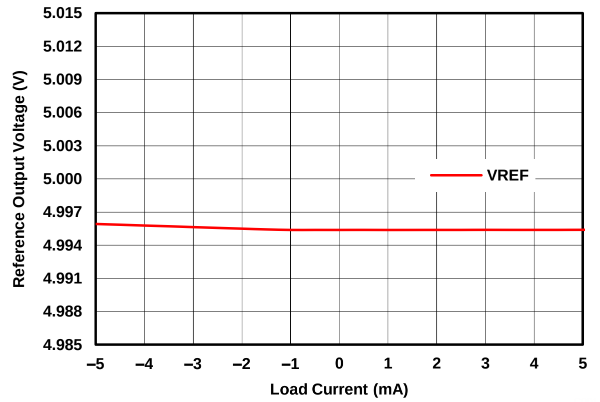


图 77. Internal Reference Voltage vs Load Current

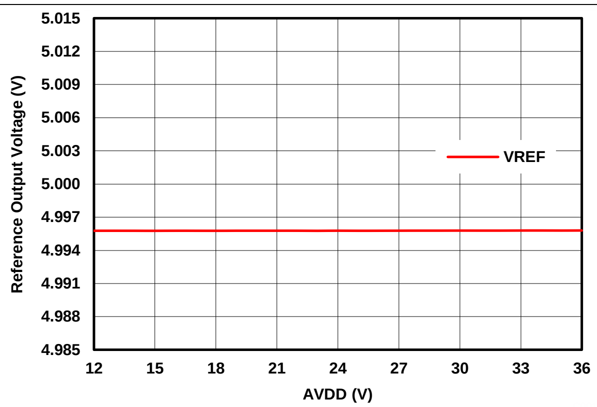


图 78. Internal Reference Voltage vs Power Supply

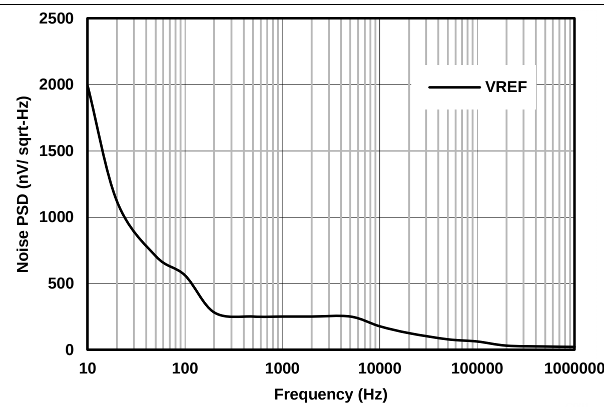


图 79. Internal Reference Noise Density vs Frequency

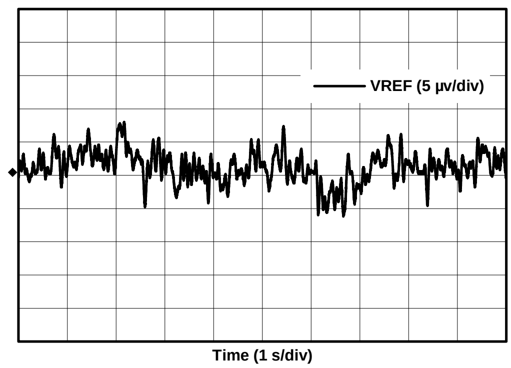
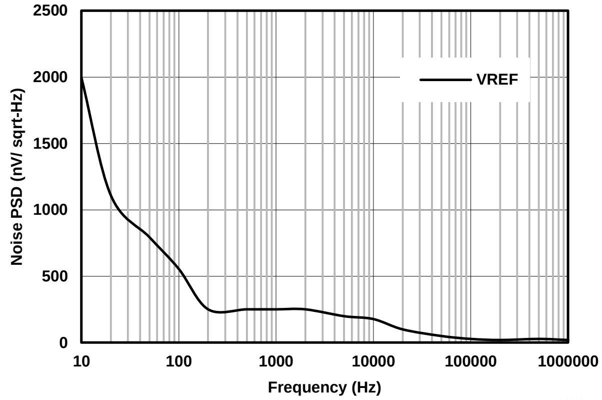


图 80. Internal Reference Noise, 0.1 Hz to 10 Hz

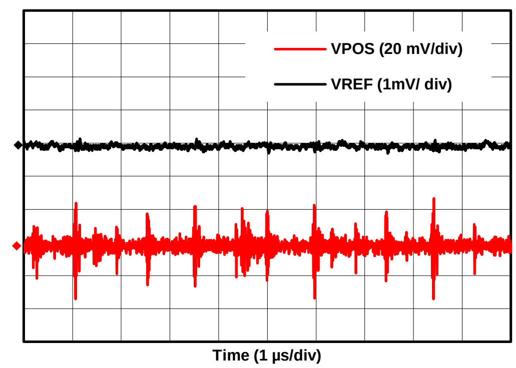
Typical Characteristics (接下页)

AVDD/PVDD_x = +15 V, PBKG = PVSS_x = 0 V, External DVDD = 5 V, VOUT disabled, IOUT R_L = 250Ω, T_A = 25℃, Buck-Boost Converter enabled (Full Tracking Mode), unless otherwise stated.



0-24 mA Range, Full Scale Code on all channels

图 81. Internal Reference Noise Density vs Frequency



0-24 mA Range, Full Scale Code on all channels

图 82. Internal Reference Ripple

Typical Characteristics (接下页)

AVDD/PVDD_x = +15 V, PBKG = PVSS_x = 0 V, External DVDD = 5 V, T_A = 25℃, Buck-Boost Converter enabled (Full Tracking Mode), unless otherwise stated.

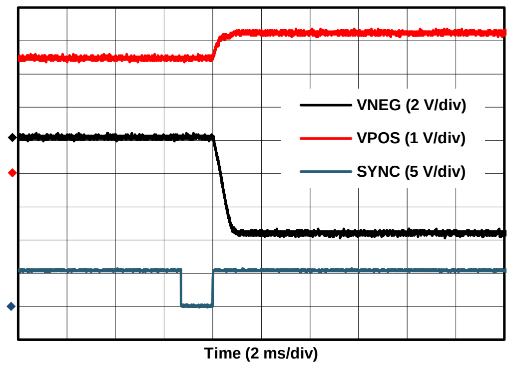


图 83. Buck-Boost Converter Power-On (IOUT Mode)

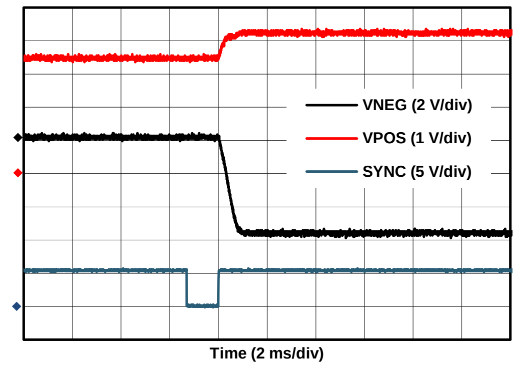
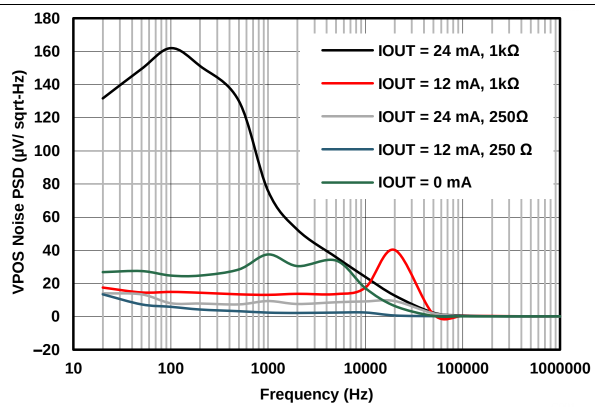
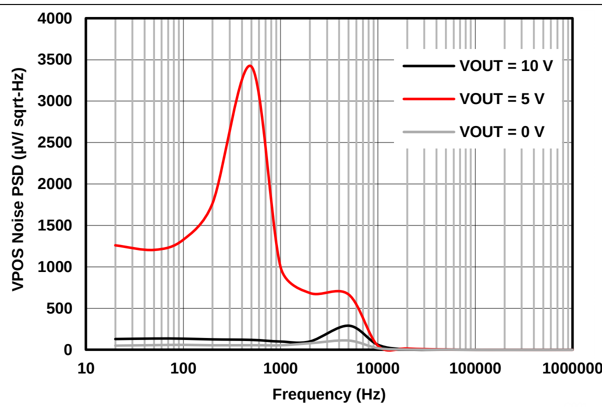


图 84. Buck-Boost Converter Power-On (VOUT Mode)



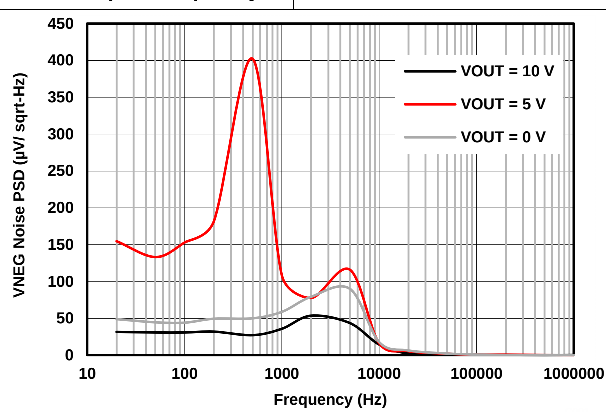
0-24 mA Range, R_L = 250 Ω

图 85. VPOS Noise Density (IOUT Mode) vs Frequency



10-V Range, No Load

图 86. VPOS Noise Density (VOUT Mode) vs Frequency



10-V Range, No Load

图 87. VNEG Noise Density (VOUT Mode) vs Frequency

Typical Characteristics (接下页)

AVDD/PVDD_x = +15 V, VNEG_IN_x = PBKG = PVSS_x = 0 V, External DVDD = 5 V, VOUT disabled, IOUT enabled 0-24 mA Range, T_A = 25℃, REFIN = +5 V external, Buck-Boost Converter VPOS_IN_x enabled (Full Tracking Mode), unless otherwise stated.

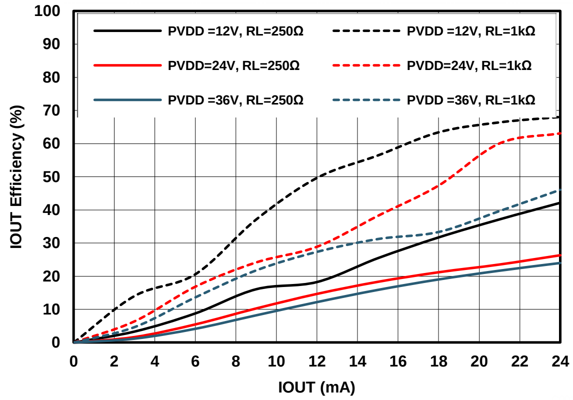


图 88. IOUT Efficiency vs Load Current

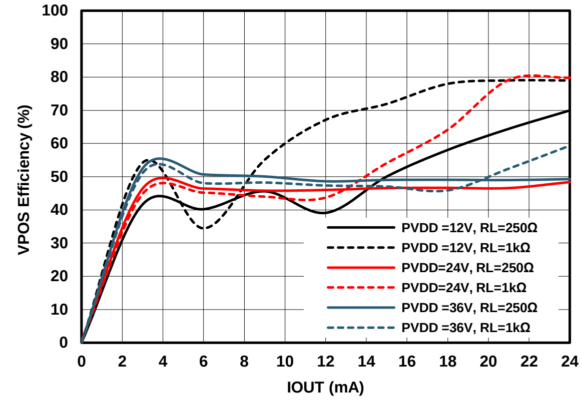
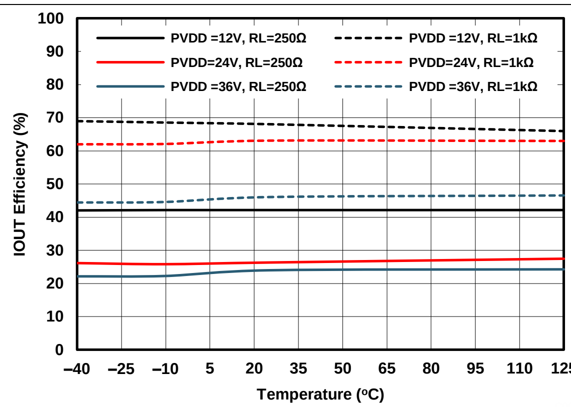
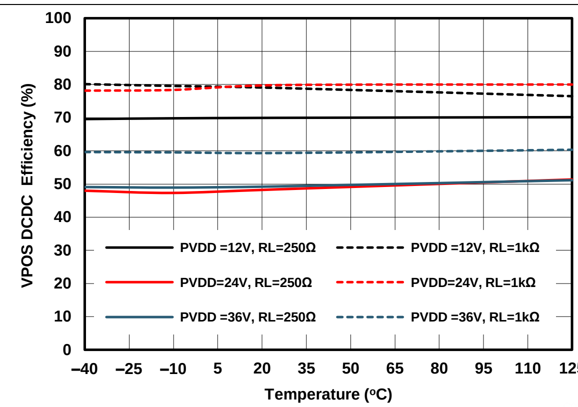


图 89. VPOS Efficiency (IOUT Mode) vs Load Current



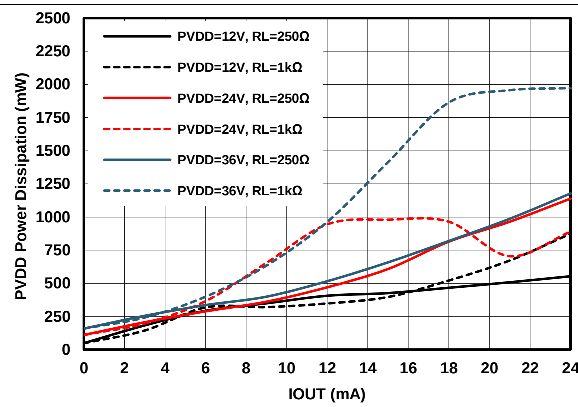
Full Scale Code IOUT = 24 mA

图 90. IOUT Efficiency vs Temperature



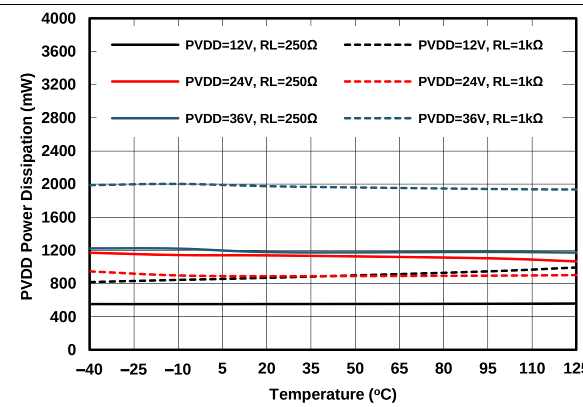
Full Scale Code IOUT = 24 mA

图 91. VPOS Efficiency (IOUT Mode) vs Temperature



Full Scale Code IOUT = 24 mA

图 92. PVDD Power Loss (IOUT Mode) vs Load Current

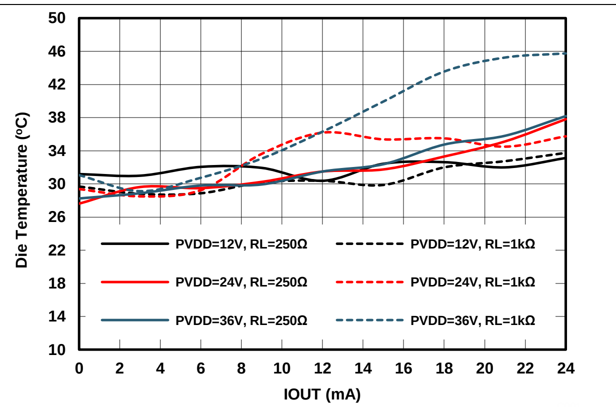


Full Scale Code, 24 mA on all channels

图 93. PVDD Power Loss (IOUT Mode) vs Temperature

Typical Characteristics (接下页)

AVDD/PVDD_x = +15 V, PBKG = PVSS_x = 0 V, External DVDD = 5 V, VOUT enabled, 10-V Range, Load 1K//200pF, IOUT disabled, T_A = 25℃, REFIN = +5 V external, Buck-Boost Converter enabled (Full Tracking Mode), unless otherwise stated.



VOUT disabled, IOUT = 24 mA (all channels), VNEG_IN_x = 0 V

图 94. Intenal Die Temperature (IOUT Mode) vs Load Current

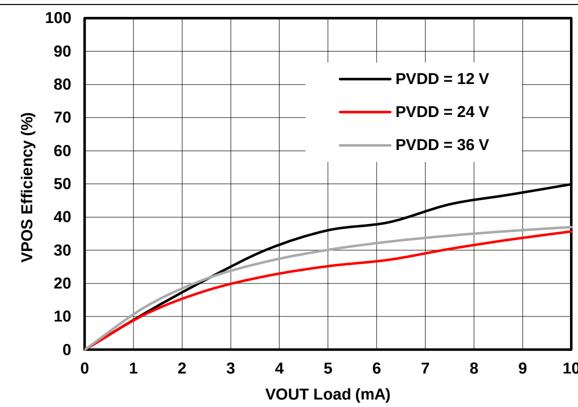
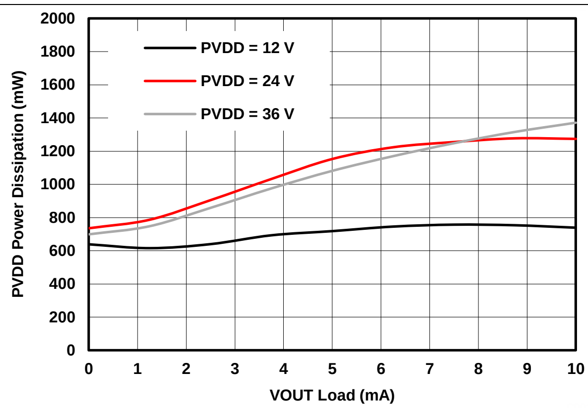
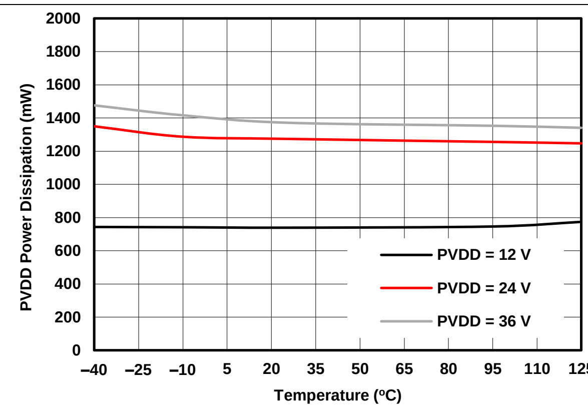


图 95. VPOS Efficiency (VOUT Mode) vs Load Current



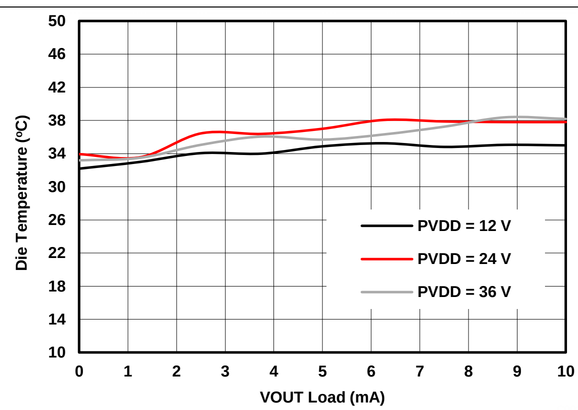
Full Scale Code on all channels

图 96. PVDD Power Loss (VOUT Mode) vs Load Current



Full Scale Code on all channels

图 97. PVDD Power Loss (VOUT Mode) vs Temperature



All channels enabled

图 98. Internal Die Temperature (VOUT Mode) vs Load Current

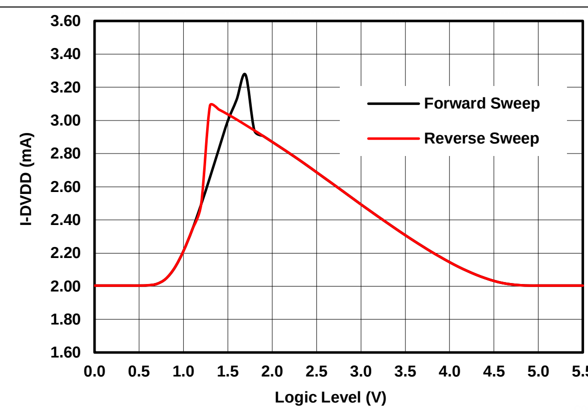


图 99. Power Supply Current (DVDD) vs Input Logic Level

8 Detailed Description

8.1 Overview

Each channel of DAC8775 consists of a resistor-string digital-to-analog converter (DAC) followed by buffer amplifiers. The output of the buffer drives the current output stage and the voltage output amplifier. The resistor-string section is simply a string of resistors, each of value R, from REFIN to PBKG, as the *Functional Block Diagram* illustrates. This type of architecture ensures DAC monotonicity. The 16-bit binary digital code loaded to the DAC register determines at which node on the string the voltage is tapped off before being fed into the output amplifier. The current output stage converts the output from the string to current using a precision current source. The voltage output provides a voltage output to the external load. When the current output stage or the voltage output stage is disabled, the respective output pin is in Hi-Z state. After power-on, both output stages are disabled. Each channel of DAC8775 also contains a Buck-Boost converter which can be used to generate the power supply for the current output stage and voltage output amplifier.

8.2 Functional Block Diagram

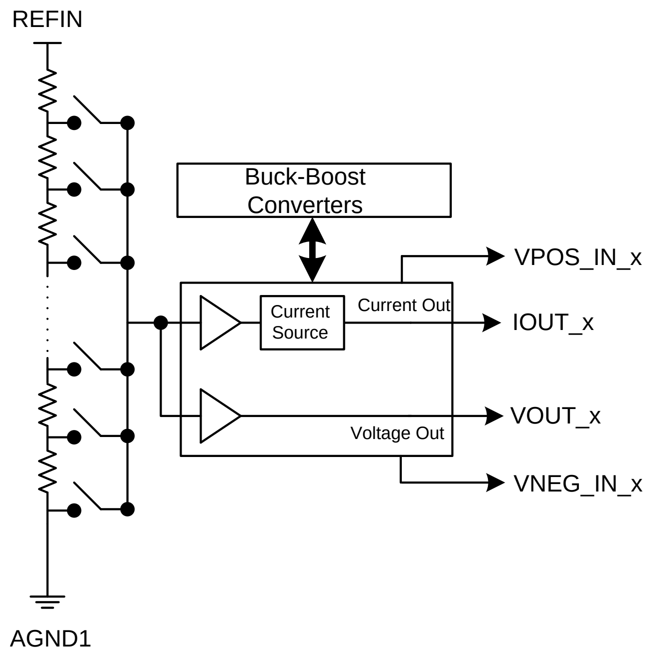


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图 100. General Architecture

8.3 Feature Description

8.3.1 Current Output Stage

Each channel's current output stage consists of a pre-conditioner and a precision current source as shown in 图 101. This stage provides a current output according to the DAC code. The output range can be programmed as 0 mA to 20 mA, 0 mA to 24 mA, 4 mA to 20 mA, 3.5 mA to 23.5 mA, or ±24 mA. In the current output mode, the maximum compliance voltage on pin IOUT_x is between (-|VNEG_IN_x| + 3 V) ≤ |IOUT_x| ≤ (VPOS_IN_x – 3 V). This compliance voltage is automatically maintained when the Buck-Boost converter is used to generate these supplies (see *Buck-Boost Converter* section). However, when using an external supply for VPOS_IN_x pin (Buck-Boost converter disabled), the VPOS_IN_x and VNEG_IN_x supplies should be chosen such that this compliance voltage is maintained.

Feature Description (接下页)

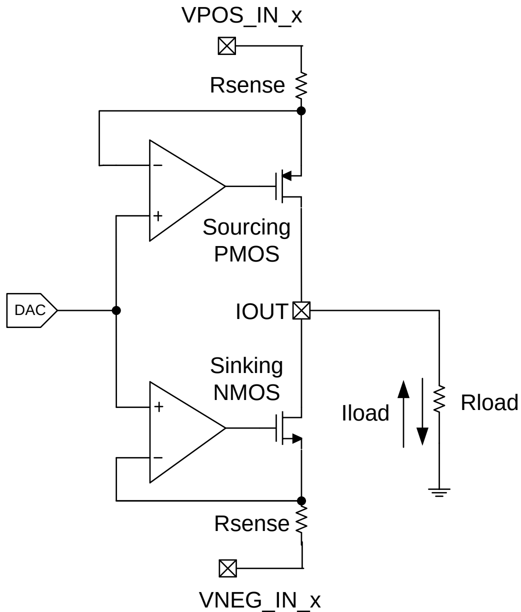

图 101. Current Output

The 16 bit data can be written to DAC8775 using address 0x05 (DAC data registers, see 表 5 and 表 6).

For a 0-mA to 20-mA output range:

$$IOUT\_x = 20\ mA.\left[\frac{CODE}{2^N}\right] \tag{1}$$

For a 0-mA to 24-mA output range:

$$IOUT\_x = 24\ mA.\left[\frac{CODE}{2^N}\right] \tag{2}$$

For a 3.5-mA to 23.5-mA output range:

$$IOUT\_x = 20\ mA.\left[\frac{CODE}{2^N}\right] + 3.5\ mA \tag{3}$$

For a 4-mA to 20-mA output range:

$$IOUT\_x = 16\ mA.\left[\frac{CODE}{2^N}\right] + 4\ mA \tag{4}$$

For a -24-mA to 24-mA output range:

$$IOUT\_x = 48\ mA.\left[\frac{CODE}{2^N}\right] - 24\ mA \tag{5}$$

Where:

- *CODE* is the decimal equivalent of the code loaded to the DAC.
- *N* is the bits of resolution; 16.

Feature Description (接下页)

8.3.2 Voltage Output Stage

The voltage output stage as conceptualized in 图 102 provides the voltage output according to the DAC code and the output range setting. The output range can be programmed as 0 V to +5 V or 0 V to +10 V for unipolar output mode, and ±5 V or ±10 V for bipolar output mode. In addition, an option is available to increase the output voltage range by 20%. The output current drive can be up to 10 mA. The output stage has short-circuit current protection that limits the output current to 16 mA, this limit can be changed to 8 mA, 20 mA or 24mA via writing bits 15 and 14 of address 0x04. This minimum headroom and footroom for the voltage output stage is automatically maintained when the Buck-Boost converter is used to generate these supplies. However, when using an external supply for VPOS_IN_x and VNEG_IN_x pin (Buck-Boost converter disabled) the minimum headroom and footroom as per must be maintained. In this case, the *Recommended Operating Conditions* shows the maximum allowable difference between VPOS_IN_x and VNEG_IN_x.

The voltage output is designed to drive capacitive loads of up to 1 μF. For loads greater than 20 nF, an external compensation capacitor can be connected between CCOMP_x and VOUT_x to keep the output voltage stable at the expense of reduced bandwidth and increased settling time. Note that, a step response (due to input code change) on the voltage output pin loaded with large capacitive load (> 20 nF) will trigger the short circuit limit circuit of the output stage. This will result in setting the short circuit alarm status bits. Therefore, it is recommended to use slew rate control for large step change, when the voltage output pin is loaded with high capacitive loads.

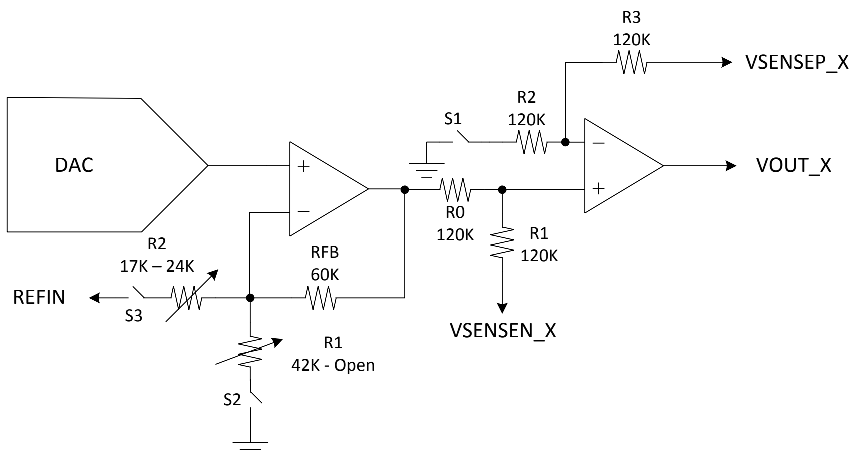

图 102. Voltage Output

The VSENSEP_x pin is provided to enable sensing of the load. Ideally, it is connected to VOUT_x at the terminals. Additionally, it can also be used to connect remotely to points electrically "nearer" to the load. This allows the internal output amplifier to ensure that the correct voltage is applied across the load as long as headroom is available on the power supply. However, if this line is cut, the amplifier loop would be broken. Therefore, an optional resistor can be used between VOUT_x and VSENSEP_x to prevent this.

The VSENSEN_x pin can be used to sense the remote ground and offset the VOUT pin accordingly. The VSENSEN_x pin can sense a maximum of ±7 V difference from the PBKG pin of the DAC8775.

The 16-bit data can be written to DAC8775 as shown in DAC data registers, see 表 5 and 表 6.

For unipolar output mode:

$$\text{VOUT\_x} = \text{VREFIN.GAIN.}\left[\frac{\text{CODE}}{2^N}\right] \tag{6}$$

For bipolar output mode:

$$\text{VOUT\_x} = \text{VREFIN.GAIN.}\left[\frac{\text{CODE}}{2^N}\right] - \frac{\text{GAIN.VREFIN}}{2} \tag{7}$$

Feature Description (接下页)

Where:

- *CODE* is the decimal equivalent of the code loaded to the DAC.
- *N* is the bits of resolution; 16.
- VREFIN is the reference voltage; for internal reference, VREFIN = +5 V.
- *GAIN* is automatically selected for a desired voltage output range as shown in 表 7.

8.3.3 Buck-Boost Converter

The DAC8775 includes a Buck-Boost Converter for each channel to minimize the power dissipation of the chip and provides significant system integration. This Buck-Boost converter is based on a Single Inductor Multiple Output (SIMO) architecture and requires a single inductor (per channel) to simultaneously generate all the analog power supplies required by the chip. The Buck-Boost converters utilize three on-chip switches (shown in 图 103) which are synchronously controlled via current mode control logic. These converters are designed to work in discontinuous conduction mode (DCM) with an external inductor (per channel) of value 100 µH connected between LN_x and LP_x pins (see *Buck-Boost Converter External Component Selection* section). The peak inductor current inductor is limited to a value of 0.5 A internally.

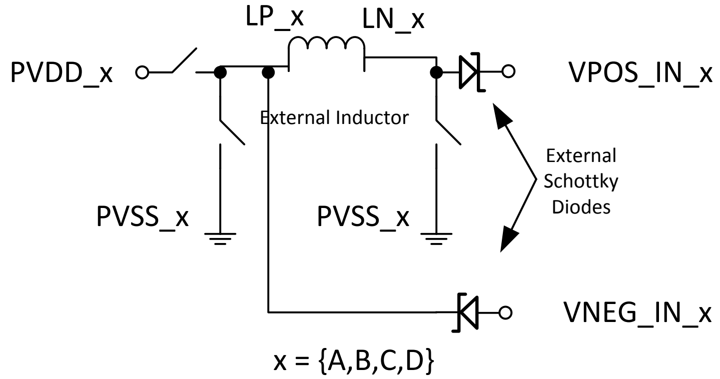

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图 103. Buck-Boost Converter

These Buck-Boost converters employ a variable switching frequency technique. This technique increases the converter efficiency at all loads by automatically reducing the switching frequency at light loads and increasing it at heavy loads. At no load condition, the converter stops switching completely until the load capacitor discharges by a preset voltage. At this point the converter automatically starts switching and recharges the load capacitor(s). In addition to saving power at all loads, this technique ensures low switching noise on the converter outputs at light loads. The minimum load capacitor for these Buck-Boost converters is 10 µF. This capacitor must be connected between the schottky diode(s) and ground (0 V) for each arm of each Buck-Boost converter (A, B, C, D). The Buck-Boost converter, when enabled, generates ripple on the supply pins (VPOS_IN_x and VNEG_IN_x). This ripples is typically attenuated by the power supply rejection ratio of the output amplifiers (IOUT_x or VOUT_x) and appears as noise on the output pin of the amplifiers (IOUT_x and VOUT_x). A larger load capacitor in combination with additional filter (see *Application Information* section) reduces the output ripple at the expense of increasing settling time of the converter output.

The input voltage to the Buck-Boost converters (pin PVDD_x) can vary from +12 V to +36 V. These outputs can be individually enabled or disabled via the user SPI interface (see Commands in 表 5 and 表 6).

8.3.3.1 Buck-Boost Converters Outputs

Each of the four Buck-Boost converters can be used to provide power to the current output stage or the voltage output stage by enabling the respective Buck-Boost converter and connecting the power supplies as shown in 图 104. Additional passive filters can optionally be added between the schottky diode and input supply pins (VPOS_IN_x and VNEG_IN_x) to attenuate the ripple feeding into the VPOS_IN_x and VNEG_IN_x pin.

Feature Description (接下页)

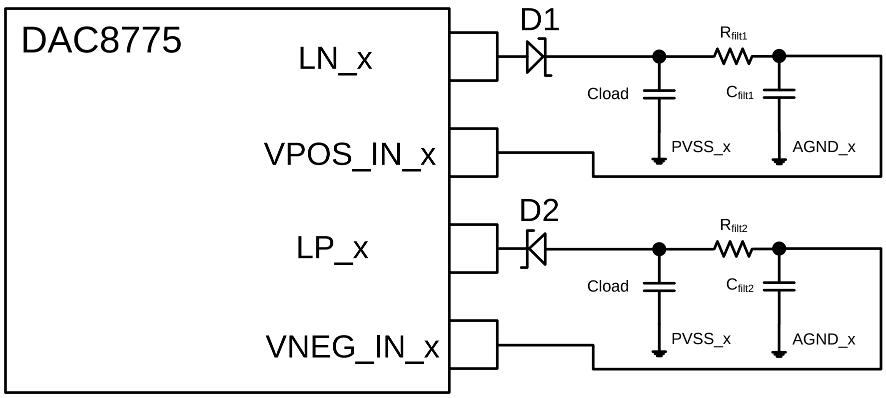


图 104. Buck-Boost Converter Positive and Negative Outputs

8.3.3.2 Selecting and Enabling Buck-Boost Converters

The analog outputs of the Buck-Boost converters can be enabled in two different ways: Current Output Mode or Voltage Output Mode. Any and all combination of the DAC8775 Buck-Boost converters can be selected by writing to address 0x06 (see Table 5). The positive/negative arm of the selected Buck-Boost converter can be enabled via writing to address 0x07 (see Table 6). Note that, VNEG_IN_x is internally shorted to PBKG when the negative arm of Buck-Boost converter is not enabled.

When used in voltage output mode, the Buck-Boost converter generates a constant ±15.0 V for the positive and negative power supplies. Alternatively this constant voltage may be modified by the clamp register setting for each channel.

When used in current output mode the Buck-Boost converter generates the positive and negative power supply based on the RANGE setting, for example the negative power supply is only generated for ±24 mA range.

The minimum voltage that the Buck-Boost converter can generate on the VPOS_IN_x pin in 4.96 V with a typical efficiency of 75% at PVDD_x = 12 V and a load current of 24 mA, thus significantly minimizing power dissipation on chip. The maximum voltage that the Buck-Boost converter can generate on the VPOS_IN_x pin is 32 V. Similarly, the minimum voltage that the Buck-Boost converter can generate on the VNEG_IN_x pin in –18.0 V. The maximum voltage that the Buck-Boost converter can generate on the VNEG_IN_x pin in –5.0 V.

8.3.3.3 Configurable Clamp Feature and Current Output Settling Time

A large signal step on the output pin IOUT_x (for example 0 mA to 24 mA) with a load of 1 KΩ would require that the respective Buck-Boost converter change the output voltage on the VPOS_IN_x pin from 4 V to 27 V. Thus, the current output settling time will be dominated by the settling time of the VPOS_IN_x voltage. A trade off can be made to reduce the settling time at the expense of power saving by increasing the minimum voltage that the respective Buck-Boost converter generates on the positive output.

The DAC8775 implements a configurable clamp feature. This feature allows multiple modes of operation based on CCLP[1:0] and HSCLMP bits (see Table 6).

8.3.3.3.1 Default Mode - CCLP[1:0] = "00" - Current Output Only

This is the default mode of operation, CCLP[1:0] = "00" for Buck-Boost converter is to be in full tracking mode. The minimum voltage generated on VPOS_IN_x in this case is 4 V. The Buck-Boost converter varies the positive and negative outputs adaptively such that the voltage across these outputs and IOUT_x pins is ≤ 3 V. This is accomplished by internally feeding back the voltage across the current output PMOS and NMOS to the respective Buck-Boost converter control circuit. For example, for a load current of 24 mA flowing through a load resistance of 1 KΩ, the generated voltage at the VPOS_IN_x pin will be around 27 V.

Feature Description (接下页)

8.3.3.3.2 Fixed Clamp Mode - CCLP[1:0] = "01" - Current and Voltage Output

In this mode of operation, the user can over-ride the default operation by writing "01" to CCLP[1:0]. The minimum voltage generated on VPOS_IN_x and VNEG_IN_x can be adjusted by writing to PCLMP[3:0] / NCLMP[3:0] (address 0x07). The voltage setting for current output and voltage output are specified in 表 6.

8.3.3.3.3 Auto Learn Mode - CCLP[1:0] = "10" - Current Output Only

In this mode ,the device automatically senses the load on the current output terminal and sets the minimum voltage generated on VPOS_IN_x terminals to a fixed value. The value is calculated such that for any code change, the settling time is dependent only on the DAC settling time. For example, with a load of 250 Ω and a maximum current of 24 mA, the Buck-Boost output voltage is set as 9 - 12 V. This achieves the maximum power saving without sacrificing settling time because the Buck-Boost output is fixed.

In order to ensure the correct operation of auto-learn mode, following steps below must be followed.

1. The device must be enabled in full tracking mode, CCLP[1:0] = "00".
2. Current output is enabled and a code greater then 4000h should be written to the DAC.
3. Write CCLP[1:0] = "10" to enable auto learn mode.

At this point, the clamp register (PCLMP - address 0x07) is populated with the appropriate settings. The clamp status bit CLST (address 0x0B) is set once the clamp register is populated indicating the completion of this process. In this mode the PCLMP bits are read only. Typically, this process of sensing the load is done only once after power up. In order to re initiate this process, the CCLP bits must be rewritten with "10".

8.3.3.3.4 High Side Clamp (HSCLMP)

The default maximum positive voltage that the Buck-Boost converter can generate is 32 V. However, this voltage can be reduced to 26 V by writing '1' to HSCLMP bit (address 0x0E, 表 6). Note that this feature can be enabled or disabled per channel by selecting the corresponding channel (address 0x03, 表 6).

8.3.3.4 Buck-Boost Converters and Open Circuit Current Output

In normal operating condition when current output is loaded with a resistive load, the Buck-Boost converter varies the positive and negative outputs adaptively such that the voltage across these outputs and IOUT_x pins is ≤ 3 V. However, if the current output is in open circuit condition, the Buck-Boost converter output would rail to fixed voltages as described in 表 1.

表 1. Open Circuit IOUT with Buck-Boost Converter

BUCK-BOOST POSITIVE ARM	BUCK-BOOST NEGATIVE ARM	IOUT RANGE	IOUT PIN VOLTAGE	VPOS_IN_x	VNEG_IN_x
Enabled	Enabled	All Ranges	≥ 0 V	20 V	–5 V
Enabled	Enabled	±24 mA only	< 0 V	4 V	–20 V
Enabled	Disabled	All ranges except ±24 mA	≥ 0 V	32 V	0 V

8.3.4 Analog Power Supply

After power up it is required that a hardware reset is issued using the RESET pin.

The DAC8775 is design to operate with a single power supply (12 V to 36 V) using integrated Buck-Boost converter. In this mode, pins PVDD_x and AVDD must be tied together and driven by the same power supply. VPOS_INx and VNEG_IN_x will be enabled as programmed by the device registers. It is recommended that DVDD is applied first to reduce output transients.

The DAC8775 can also be operated without using the integrated Buck-Boost converter. In this mode, pins PVDD_x, AVDD, and VPOS_IN_x must be tied together and driven by the same power supply (12 V to 36 V). In this mode in order to reduce output transients it is recommended that DVDD is applied first, followed by VPOS_IN_x / PVDD_x / AVDD and finally REFIN. Note that in this mode, the minimum required head room and foot room for the output amplifiers must be met.

Recommended Operating Conditions shows the maximum and minimum allowable limits for all the power supplies when DAC8775 is powered using external power supplies.

8.3.5 Digital Power Supply

The digital power supply to DAC8775 can be internally generated or externally supplied. This is determined by the status of DVDD_EN pin.

When the DVDD_EN pin is left floating, the voltage on DVDD pin is generated via an internal LDO. The typical value of the voltage generated on DVDD pin is 5 V. In this mode, the DVDD pin can also be used to power other digital components on the board. The maximum drive capability of this pin is 10mA. Please note that to ensure stability the minimum load capacitance on this pin is limited to 100 pF, where as the maximum load capacitance is limited to 0.1 µF.

When the DVDD_EN pin is tied to 0 V, the internal LDO is disabled and the DVDD pin must be powered via an external digital supply.

8.3.6 Internal Reference

The DAC8775 includes an integrated 5-V reference with an initial accuracy of ±10 mV maximum and a temperature drift coefficient of 10 ppm/°C maximum. A buffered output capable of driving up to 5 mA is available on REFOUT. The internal reference for DAC8775 is disabled by default. To enable the internal reference, REF_EN bit on address 0x02h must be set to '1' (see 表 6).

8.3.7 Power-On-Reset

The DAC8775 contain power on reset circuits which is based on AVDD and DVDD power supplies. After power-on, the power-on-reset circuit ensures that all registers are at their default values (see 表 5). The current, voltage output DACs, and the Buck-Boost converters are disabled. The current output pin is in high impedance state.

The voltage output pin is in a 30kΩ-to-GND state; however, the VSENSEP_x pin is an open circuit. The voltage output pin impedance may be changed to high-impedance by the POC bit setting.

8.3.8 $\overline{\text{ALARM}}$ Pin

The DAC8775 contains an $\overline{\text{ALARM}}$ pin. When one or more of following events occur, the $\overline{\text{ALARM}}$ pin is pulled low:

1. The load on any channel's IOUT_x pin is in open circuit (> 500 µsec); or
2. The voltage at IOUT_x, when enabled, reaches a level where the accuracy of the output current would be compromised. This condition is detected by monitoring internal voltage levels of the IOUT_x circuitry and will typically be below the specified compliance voltage minimum of 3 V (> 500 µsec). Note that, when the buck boost converter is enabled in full tracking mode (CCLP[1:0] = "00"), a transient alarm signal can be observed during the current output transition. This condition occurs because the compliance voltage for current output is violated as the buck boost converter is adjusting the power supply. Alternatively the alarm can be programmed to only indicate an alarm once the DC/DC has reached saturation and the compliance voltage condition is still being violated; or
3. The die temperature has exceeded +150°C; or
4. The SPI watchdog timer exceeded the timeout period (if enabled); or
5. The SPI frame error check (CRC) encountered an error (if enabled).
6. A short circuit current limit is reached (> 500 µsec) on any VOUT_x when enabled in voltage output mode.
7. The Buck-Boost converter has reached the maximum output voltage (set by bit HSCLMP, 表 6 address 0x0E).

When connecting the $\overline{\text{ALARM}}$ pins of multiple DAC8775 devices together, forming a wired-AND function, the host processor should read the status register of each device to know all the fault conditions that are present.

The $\overline{\text{ALARM}}$ pin continuously monitors the above mentioned conditions and returns to open drain condition if the alarm condition is removed (non-latched behavior - default). For condition (1) mentioned above and Buck-Boost converter used to power the DAC, the $\overline{\text{ALARM}}$ pin if pulled low due to the alarm condition will remain pulled low even after the alarm condition is removed (latched behavior). In this condition the alarm pin can be reset by

1. Resetting the corresponding fault bits in the status register (address 0x0B, 表 6); or
2. Performing software reset (write to address 0x01, 表 6); or
3. Toggling hardware reset pin; or
4. Performing power on reset.

Note that if the alarm action bits are programmed to "10" (AC_IOC[1:0], the Buck-Boost converter and the current output amplifier are automatically disabled upon the event of open circuit on current output. In this case, the ALARM automatically resets to the default behavior (non-latched behavior).

8.3.9 Power GOOD Bits

Each Buck-Boost converter in DAC8775 has a read only bit called power good (PGx) (address 0x0B, 表 6). This bit is set to logic '1' when both of the following conditions are met:

1. The VPOS_IN_x > 4 V (if enabled) and
2. The VNEG_IN_x < –3 V (if enabled)

The PGx bit indicates the status of the outputs of the enabled Buck-Boost converters. For example if the output of Buck-Boost converter A is the only one enabled, then the PGA bit will be set to a logic '1' only after the positive output pins of the Buck-Boost converter A are ≥ 3.0 V and the negative output pin of Buck-boost converter A is ≤ -3.0 V.

8.3.10 Status Register

Since, DAC8775 contains one ALARM pin for the entire chip, the status of individual fault condition can be checked using the status register. This register (see *Register Maps and Bit Functions* section) consists of five types of ALARM status bits (Faults on current and voltage outputs , Over temperature condition, CRC errors, Watchdog timeout and Buck-Boost converter power good) and two status bit (User toggle, Auto Learn status). The device continuously monitors these conditions. When an alarm occurs, the ALARM pin is pulled low and the corresponding status bit is set ('1'). Whenever one of these status bits is set, it remains set until the user clears it by writing '1' to corresponding bit on address 0x0B. The status bit can also be cleared by performing a hardware reset, software reset, or power-on reset, note that it takes a minimum of 8 µsec for the status register to get reset. These bits are reasserted if the ALARM condition continues to exist in the next monitoring cycle.

8.3.11 Status Mask

The ALARM pin for DAC8775 is triggered by any of the alarm conditions (see *ALARM Pin* section). However, these different alarm conditions can be masked from creating the alarm signal at the pin by using the status mask register. The status mask register (address 0x0C, Table 6) has the same bit order as the status register except that it can be set to mask any or all status bits that create the alarm signal.

8.3.12 Alarm Action

The DAC8775 implements an alarm action register (address 0x0D,Table 6). By writing to this register, the user can select the action that the device will take automatically in case of a specific alarm condition. In case, different setting are chosen for different alarm conditions, the following priority (high to low) will be considered when taking action:

1. Over temperature alarm
2. Output fault alarm
3. CRC error/Watchdog timer fault alarm

This device also contains a 6-bit alarm code register (address 0x0E, 表 6) which can be loaded to the DACs if the alarm action register is set to "01". Note that the alarm code, once set, remains set even if the alarm condition is removed. Also note that the alarm action change to the programmed code is a step function even if slew rate control is enabled.

8.3.13 Watchdog Timer

This feature is useful to ensure that communication between the host processor and the DAC8775 has not been lost. It can be enabled by setting the WEN (address 0x03) bit to '1', see Table 6. The watchdog timeout period can be set using the WPD[1:0] address 0x03) bits. The timer period is based off an internal oscillator with a typical value of 8 MHz.

If enabled, the chip must have an SPI frame with 0x10 as the write address byte written to the device within the programmed timeout period. Otherwise, the ALARM pin asserts low and the WDT bit (address 0x0B) of the status register is set to '1'. The WDT bit is set to '0' with a software/hardware reset, or by disabling the watchdog timer (WEN = '0'), or powering down the device.

When using multiple DAC8775 devices in a daisy-chain configuration, the open-drain $\overline{\text{ALARM}}$ pins of all devices can be connected together to form a wired-AND network. The watchdog timer can be enabled in any number of the devices in the chain although enabling it in one device in the chain should be sufficient. The wired-AND $\overline{\text{ALARM}}$ pin may get pulled low because of the simultaneous presence of different trigger conditions in the devices in the daisy-chain. The host processor should read the status register of each device to know all the fault conditions present in the chain.

8.3.14 Programmable Slew Rate

The slew rate control feature allows the user to control the rate at which the output voltage or current changes. This feature is disabled by default and can be enabled for the selected channel by writing logic '1' to the SREN bit at address 0x04 (see Table 6). With the slew rate control feature disabled, the output changes smoothly at a rate limited by the output drive circuitry and the attached load.

With this feature enabled, the output does not slew directly between the two values. Instead, the output steps digitally at a rate defined by bits [2:0] (SR_STEP) and bits [3:0] (SRCLK_RATE) on address 0x04 (see Table 6). SR_RATE defines the rate at which the digital slew updates; SRCLK_STEP defines the amount by which the output value changes at each update. Table 6 shows different settings for SRCLK_STEP and SR_RATE.

The time required for the output to slew over a given range can be expressed as 公式 8:

$$\text{Slew Time} = \frac{\text{Output Change}}{\text{Step Size.Update Clock Frequency.LSB Size}} \tag{8}$$

Where:

- *Slew Time* is expressed in seconds
- *Output Change* is expressed in amps (A) for current output mode or volts (V) for voltage output mode

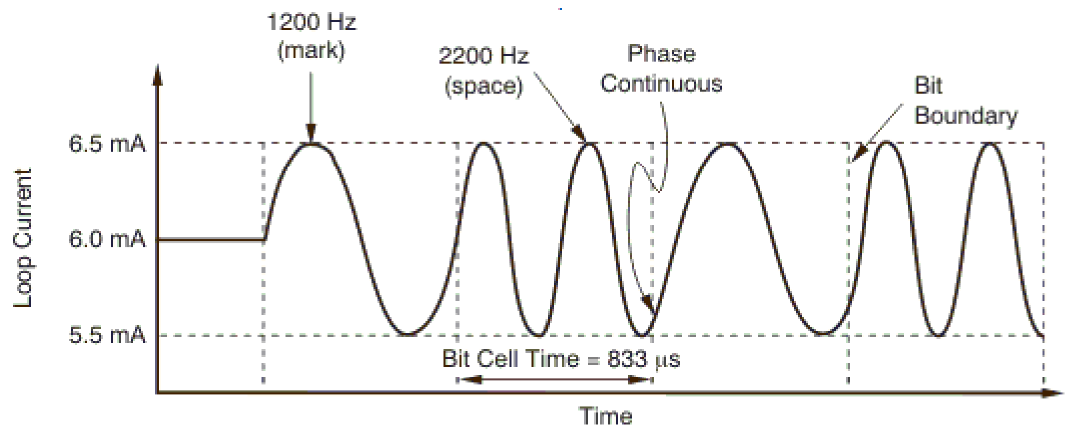
When the slew rate control feature is enabled, the output changes happen at the programmed slew rate. This configuration results in a staircase formation at the output. If the CLR pin is asserted, the output slews to the zero-scale value at the programmed slew rate. When a new DAC data is written, the output starts slewing to the new value at the slew rate determined by the current DAC code and the new DAC data. The update clock frequency for any given value is the same for all output ranges. The step size, however, varies across output ranges for a given value of step size because the LSB size is different for each output range.

Note that disabling the slew rate feature while the DAC is executing the slew rate command will abort the slew rate operation and the DAC output will stay at the last code after which the slew rate disable command was acknowledged.

8.3.15 HART Interface

On the DAC8775, digital communication such as HART can be modulated onto the input signal for each channel.

In the case where the RANGE (address 0x04) bits are programmed such that the IOUT_x is enabled, the external HART signal (ac voltage; 500 mV_{PP}, 1200 Hz and 2200 Hz) can be capacitively coupled in through the HARTIN_x pin and transferred to a current that is superimposed on the current output. The HARTIN_x pin has a typical input impedance of 20 kΩ to 30 kΩ, depending on the selected current output range, which together with the input capacitor used to couple the external HART signal into the HARTIN_x pin can be used to form a high-pass filter to attenuate frequencies below the HART bandpass region. In addition to this filter, an external passive filter is recommended to complete the filtering requirements of the HART specifications. 图 105 illustrates the output current versus time operation for a typical HART interface.



Note: DC current = 6 mA.

图 105. Output Current vs Time

The HART pin for the selected channel can be enabled by writing logic '1' to the HTEN bit at address 0x04 (see 表 5 and 表 6).

8.4 Device Functional Modes

8.4.1 Serial Peripheral Interface (SPI)

The device is controlled over a versatile four-wire serial interface (SDIN, SDO, SCLK, and $\overline{SYNC}$) that operates at clock rates of up to 25 MHz and is compatible with SPI, QSPI™, Microwire™, and digital signal processing (DSP) standards. The SPI communication command consists of a write address byte and a data word for a total of 24 bits (when CRC is disabled). The timing for the digital interface is shown in the *Timing Requirements: Write and Readback Mode* section.

8.4.1.1 Stand-Alone Operation

The serial clock SCLK can be a continuous or a gated clock. When $\overline{SYNC}$ is high, the SCLK and SDIN signals are blocked and the SDO pin is in a HiZ state. Exactly 24 falling clock edges must be applied before $\overline{SYNC}$ is brought high. If $\overline{SYNC}$ is brought high before the 24th falling SCLK edge, then the data written are not transferred into the internal registers. If more than 24 falling SCLK edges are applied before $\overline{SYNC}$ is brought high, then the last 24 bits are used. The device internal registers are updated from the Shift Register on the rising edge of $\overline{SYNC}$. In order for another serial transfer to take place, $\overline{SYNC}$ must be brought low again.

8.4.1.2 Daisy-Chain Operation

For systems that contain more than one device, the SDO pin can be used to daisy-chain multiple devices together. Daisy-chain operation can be useful for system diagnostics and in reducing the number of serial interface lines. The daisy chain feature can be enabled by writing logic '0' to DSDO bit address 0x03 (see Table 6), the SDO pin is set to HiZ when DSDO bit is set to 1. By connecting the SDO of the first device to the SDIN input of the next device in the chain, a multiple-device interface is constructed, as Figure 11 illustrates.

Device Functional Modes (接下页)

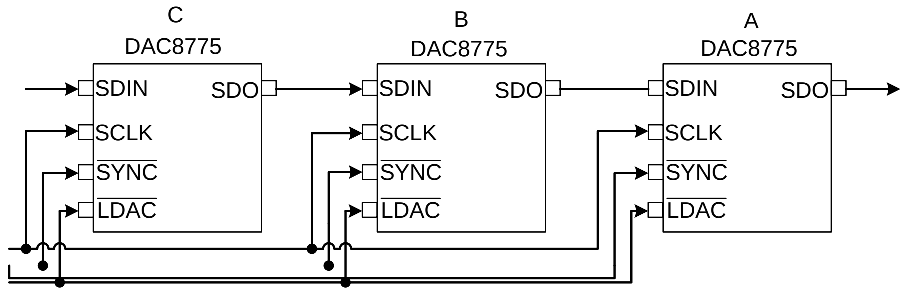


图 106. Three DAC8775s in Daisy-Chain Mode

The DAC8775 provides two modes for daisy-chain operation: normal and transparent. The TRN bit in the Reset config register determines which mode is used. In Normal mode (TRN bit = '0'), the data clocked into the SDIN pin are transferred into the shift register. The first falling edge of SYNC starts the operating cycle. SCLK is continuously applied to the SPI Shift Register when SYNC is low. If more than 24 clock pulses are applied, the data ripple out of the shift register and appear on the SDO line. These data are clocked out on the rising edge of SCLK and are valid on the falling edge. By connecting the SDO pin of the first device to the SDIN input of the next device in the chain, a multiple-device interface is constructed. Each device in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal 24 × N, where N is the total number of DAC8775s in the chain. When the serial transfer to all devices is complete, SYNC is taken high. This action latches the data from the SPI Shift registers to the device internal registers synchronously for each device in the daisy-chain, and prevents any further data from being clocked in. Note that a continuous SCLK source can only be used if SYNC is held low for the correct number of clock cycles. For gated clock mode, a burst clock containing the exact number of clock cycles must be used and SYNC must be taken high after the final clock in order to latch the data.

In Transparent mode (address 0x02h, TRN bit = '1' 表 6), the data clocked into SDIN are routed to the SDO pin directly; the Shift Register is bypassed. When SCLK is continuously applied with SYNC low, the data clocked into the SDIN pin appear on the SDO pin almost immediately (with approximately a 12 ns delay); there is no 24 clock delay, as there is in normal operating mode. While in Transparent mode, no data bits are clocked into the Shift Register, and the device does not receive any new data or commands. Putting the device into transparent mode eliminates the 24 clock delay from SDIN to SDO caused by the Shift Register, thus greatly speeding up the data transfer. For example, consider three DAC8775s (C, B, and A) in a daisy-chain configuration (see Figure 11). The data from the SPI controller are transferred first to C, then to B, and finally to A. In normal daisy-chain operation, a total of 72 clocks are needed to transfer one word to A. However, if C and B are placed into Sleep mode, the first 24 data bits are directly transferred to A (through C and B); therefore, only 24 clocks are needed.

To wake the device up from transparent mode and return to normal operation, the hardware RESET pin must be toggled.

8.4.2 SPI Shift Register

The SPI Shift Register is 24 bits wide (refer to the *Frame Error Checking* section for 32-bit frame mode). The default 24-bit input frame consists of an 8-bit address byte followed by a 16-bit data word as shown in 表 2.

表 2. Default SPI Frame

BIT 23:BIT 16	BIT 15:BIT 0
Address byte	Data word

8.4.3 Write Operation

A typical write to program a channel of the DAC8775 consists of writing to the following registers in the sequence shown in Figure 12.

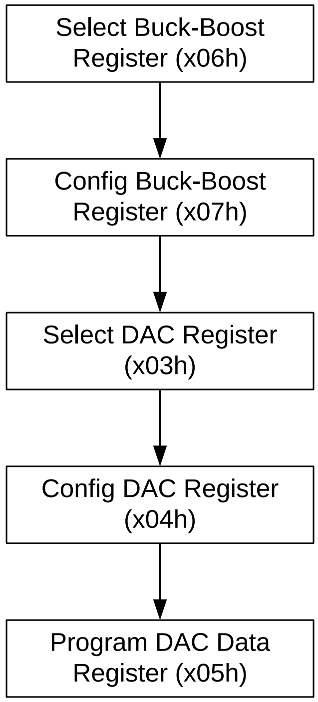


图 107. Typical Write to DAC8775

8.4.4 Read Operation

A read operation is accomplished when DB 23 is '1' (see Table 3). A no-operation (NOP) command should follow the read operation in order to clock out an addressed register. The read register value is output MSB first on SDO on successive falling edges of SCLK.

表 3. Register Read Address Functions(1)

ADDRESS BYTE	
DB23	DB 22: DB 16
Read/Write Bit	Register Addresses

(1) 'X' denotes *don't care* bits.

8.4.5 Updating the DAC Outputs and LDAC Pin

Depending on the status of both SYNC and LDAC, and after data have been transferred into the DAC Data registers, the DAC outputs can be updated either in asynchronous mode or synchronous mode.

8.4.5.1 Asynchronous Mode

In this mode, the LDAC pin is set low before the rising edge of SYNC. This action places the DAC8775 into Asynchronous mode, and the LDAC signal is ignored. The DAC latches are updated immediately when SYNC goes high.

8.4.5.2 Synchronous Mode

To use this mode, set LDAC high before the rising edge of SYNC, and then take LDAC low after SYNC goes high. In this mode, when LDAC stays high, the DAC latch is not updated; therefore, the DAC output does not change. The DAC latch is updated by taking LDAC low any time after a certain delay from the rising edge of SYNC (see Figure 1). If this delay requirement is not satisfied, invalid data are loaded. Refer to the *Timing Requirements: Write and Readback Mode* section for details.

8.4.6 Hardware RESET Pin

When the RESET pin is low, the device is in hardware reset. All the analog outputs (VOUT_A to VOUT_D and IOUT_A to IOUT_D), all the registers except the POC register, and the DAC latches are set to the default reset values. In addition, the Gain and Zero registers are loaded with default values, communication is disabled, and the signals on SYNC and SDIN are ignored (note that SDO is in a high-impedance state). When the RESET pin is high, the serial interface returns to normal operation and all the analog outputs (VOUT_A to VOUT_D and IOUT_A to IOUT_D) maintain the reset value until a new value is programmed.

8.4.7 Hardware CLR Pin

The CLR pin is an active high input that should be low for normal operation. When this pin is a logic '1', all the outputs are cleared to either zero-scale code or midscale code depending on the status of the CLSLx bit (see *Reset Register (address = 0x01) [reset = 0x0000]*). While CLR is high, all LDAC pulses are ignored. When CLR is taken low again, the DAC outputs remain cleared until new data is written to the DACs. The contents of the Offset registers, Gain registers, and DAC input registers are not affected by taking CLR high. Note that the clear action will result in the outputs clearing to the default value instantaneously even if slew rate control is enabled.

8.4.8 Frame Error Checking

If the DAC8775 is used in a noisy environment, error checking can be used to check the integrity of SPI data communication between the device and the host processor. This feature can be enabled by setting the CREN bit address 0x03 (see Table 6).

The frame error checking scheme is based on the CRC-8-ATM (HEC) polynomial $x^8 + x^2 + x + 1$ (that is, *100000111*). When error checking is enabled, the SPI frame width is 32 bits, as shown in Table 1. The normal 24-bit SPI data are appended with an 8-bit CRC polynomial by the host processor before feeding it to the device. For a register readback, the CRC polynomial is output on the SDO pins by the device as part of the 32 bit frame.

Note that the user has to start with the default 24 bit frame and enable frame error checking through the CREN bit and switch to the 32 bit frame. Alternatively, the user can use a 32-bit frame from the beginning and pad the 8 MSB bits as the device will only use the last 24 bits until the CRCEN bit is set. The frame length has to be carefully managed, especially when using daisy-chaining in combination with CRC checking to ensure correct operation.

表 4. SPI Frame with Frame Error Checking Enabled

BIT 31:BIT 8	BIT 7:BIT 0
Normal SPI frame data	8-bit CRC polynomial

The DAC8775 decodes the 32-bit input frame data to compute the CRC remainder. If no error exists in the frame, the CRC remainder is zero. When the remainder is non-zero (that is, the input frame has single- or multiple-bit errors), the ALARM pin asserts low and the CRE bit of the status register (address 0x0B) is also set to '1'. Note that the ALARM pin can be asserted low for any of the different conditions as explained in the *ALARM Pin* section. The CRE bit is set to '0' with a software or hardware reset, or by disabling the frame error checking, or by powering down the device. In the case of a CRC error, the specific SPI frame is blocked from writing to the device.

Frame error checking can be enabled for any number of DAC8775 devices connected in a daisy-chain configuration. However, it is recommended to enable error checking for none or all devices in the chain. When connecting the ALARM pins of all combined devices, forming a wired-AND function, the host processor should read the status register of each device to know all the fault conditions present in the chain. For proper operation, the host processor must provide the correct number of SCLK cycles in each frame, taking care to identify whether or not error checking is enabled in each device in the daisy-chain.

8.4.9 DAC Data Calibration

Each channel of the DAC8775 contains a dedicated user calibration register set. This feature allows the user to trim the system gain and offset errors. Both the voltage output and the current output have common user calibration registers available. The user calibration feature is disabled by default. To enable this feature for a selected channel(s), the CLEN bit (DB0) on address 0x08 must be set to logic '1 (see Table 6).

8.4.9.1 DAC Data Gain and Offset Calibration Registers

The DAC calibration register set includes one gain calibration and one offset calibration register (16 bits for DAC8775) per channel (address 0x09 and 0x0A). The range of gain adjustment is typically ±50% of full-scale with 1 LSB per step. The power-on value of the gain register is 0x8000 which is equivalent to a gain of 1. The offset code adjustment is typically ±32,768 LSBs with 1 LSB per step. The input data format of the gain register is unsigned straight binary, and the input data format of the offset register is twos complement. The gain and offset calibration is described by 公式 9.

$$CODE\_OUT = \left[CODE.\left(\frac{User\_Gain + 2^{15}}{2^{16}} \right) + User\_Zero \right] \quad (9)$$

Where:

- *CODE* is the decimal equivalent of the code loaded to the DAC.
- VREFIN is the reference voltage; for internal reference, VREFIN = +5 V.
- *GAIN* is automatically selected for a desired voltage output range as shown in 表 7.
- *User_Offset* is the signed 16-bit code in the offset register.
- *User_GAIN* is the unsigned 16-bit code in the gain register.

It is important to note that this is a purely digital implementation and the output is still limited by the programmed value at both ends of the voltage or current output range. Therefore, the user must remember that the correction only makes sense for endpoints inside of the true device end points. If the user desires to correct more than just the actual device error, for example a system offset, the valid range for the adjustment would change accordingly and must be taken into account. This range is set by the RANGE bits as described in Table 6.

8.5 Register Maps

8.5.1 DAC8775 Commands

表 5. Address Functions

ADDRESS BYTE	FUNCTION	READ/WRITE	PER CHANNEL	POWER-ON RESET VALUE
0x00	No operation (NOP)	Write	No	0x0000
0x01	Reset register	Read+Write	No	0x0000
0x02	Reset config register	Read+Write	No	0x0000
0x03	Select DAC register	Read+Write	No	0x0000
0x04	Configuration DAC register	Read+Write	Yes	0x0000
0x05	DAC data register	Read+Write	Yes	0x0000
0x06	Select Buck-Boost converter register	Read+Write	No	0x0000
0x07	Configuration Buck-Boost converter register	Read+Write	Yes	0x0000
0x08	DAC channel calibration enable register	Read+Write	Yes	0x0000
0x09	DAC channel gain calibration register	Read+Write	Yes	0x0000
0x0A	DAC channel offset calibration register	Read+Write	Yes	0x0000
0x0B	Status register	Read+Write	No	0x1000
0x0C	Status mask register	Read+Write	No	0x0000
0x0D	Alarm action register	Read+Write	No	0x0000
0x0E	User alarm code register	Read+Write	Yes	0x0000
0x0F	Reserved	N/A	N/A	N/A
0x10	Write watchdog timer reset	Write	No	0x0000
0x11	Device ID	Read	No	0x0000
0x12 - 0xFF	Reserved	N/A	N/A	N/A

Note that, in order to write to (or read from) a per channel address, corresponding Buck-Boost converter and DAC channel must be selected using commands 0x06 and 0x03.

8.5.2 Register Maps and Bit Functions

表 6. Register Map

ADDRESS	BITS															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x01	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	RST
0x02	x	x	x	CLREND	CLRENC	CLRENB	CLRENA	x	x	x	x	REF_EN	TRN	CLR	POC	UBT
0x03	x	x	x	CLSLD	CLSLC	CLSLB	CLSLA	CHD	CHC	CHB	CHA	DSDO	CREN	WPD[1:0]		WEN
0x04	SCLIM[1:0]		HTEN	OTEN	SRCLK_RATE[3:0]				SR_STEP[2:0]			SREN	RANGE[3:0]			
0x05	DAC_DATA[15:0]															
0x06	x	x	x	x	x	x	x	x	x	x	x	x	DCD	DCC	DCB	DCA
0x07	x	x	x	x	CCLP[1:0]		PCLMP[3:0]				NCLMP[3:0]				PNSEL[1:0]	
0x08	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CLEN
0x09	UGAIN[15:0]															
0x0A	UOFF[15:0]															
0x0B	x	x	x	CLST	WDT	PGD	PGC	PGB	PGA	UTGL	CRE	TMP	FD	FC	FB	FA
0x0C	x	x	x	x	MWT	x	x	x	x	x	MCRE	MTMP	MFD	MFC	MFB	MFA
0x0D	x	x	x	x	x	x	x	x	AC_CRE_WDT[1:0]		AC_IOC[1:0]		AC_VSC[1:0]		AC_TMP[1:0]	
0x0E	ACODE[15:10]						HSCLMP	0	x	x	x	x	x	x	x	x
0x10	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	RWD
0x11	x	x	x	x	x	x	x	x	x	x	x	x	x	DID[2:0]		

表 7. Voltage Output GAIN vs DAC Range

BIT 3: Bit 0 (RANGE)	GAIN
0000	1
0001	2
0010	2
0011	4
1000	1.2 (20% Over-range)
1001	2.4 (20% Over-range)
1010	2.4 (20% Over-range)
1011	4.8 (20% Over-range)

8.5.2.1 No Operation Register (address = 0x00) [reset = 0x0000]

图 108. No Operation Register

15	14	13	12	11	10	9	8
Reserved							
W							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							
W							

LEGEND: R/W = Read/Write; R = Read only; W = Write Only; -n = value after reset

表 8. No Operation Field Descriptions

Bit	Field	Type	Reset	Description
15:10	Reserved	W	00000000 00000000	Reserved

8.5.2.2 Reset Register (address = 0x01) [reset = 0x0000]

图 109. Reset Register

15	14	13	12	11	10	9	8
Reserved							
R/W							
7	6	5	4	3	2	1	0
Reserved							RST
R/W							R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9. Reset Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	Reserved	R/W	00000000 0000000	Reserved
0	RST	R/W	0	Reset. When set, it resets all registers except POC register bit to the respective power-on reset default value. After reset completes the RST bit clears

8.5.2.3 Reset Config Register (address = 0x02) [reset = 0x0000]

图 110. Reset Config Register

15	14	13	12	11	10	9	8
Reserved			CLREND	CLRENC	CLRENB	CLRENA	Reserved
R/W			R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Reserved			REF_EN	TRN	CLR	POC	UBT
R/W			R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 10. Reset Config Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	Reserved	R/W	000	Reserved
12	CLREND	R/W	0	Clear Enable 0 - DACD hardware and software clear is disabled 1 - DACD hardware and software clear is enabled
11	CLRENC	R/W	0	Clear Enable 0 - DACC hardware and software clear is disabled 1 - DACC hardware and software clear is enabled
10	CLRENB	R/W	0	Clear Enable 0 - DACB hardware and software clear is disabled 1 - DACB hardware and software clear is enabled
9	CLRENA	R/W	0	Clear Enable 0 - DACA hardware and software clear is disabled 1 - DACA hardware and software clear is enabled
8:5	Reserved	R/W	0000	Reserved
4	REF_EN	R/W	0	Internal reference enable/disable 0 - Internal reference disabled (default) 1 - Internal reference enabled
3	TRN	R/W	0	Enable transparent mode (see section "daisy chain operation")
2	CLR	R/W	0	Active high, clears all DAC registers to either zero or full scale based on CLSL bit. After clear completes the CLR bit resets.

表 10. Reset Config Register Field Descriptions (接下页)

Bit	Field	Type	Reset	Description
1	POC	R/W	0	Power-Off-Condition 0 - IOUT_x to HIZ, VOUT_x to 30K-to-PBKG at power up, hardware or software reset (default) 1 - IOUT_x and VOUT_x to HIZ at power up, hardware and software reset
0	UBT	R/W	0	User Bit - This bit can be used to check if the communication to the chip is working correctly by writing a known value to this bit and reading that value from the status register toggle bit. The toggle resister bit UTGL (address 0x0B) is set to the same value as the UBT bit.

8.5.2.4 Select DAC Register (address = 0x03) [reset = 0x0000]

图 111. Select DAC Register

15	14	13	12	11	10	9	8
Reserved			CLSLD	CLSLC	CLSLB	CLSLA	CHD
R/W			R/W	R/W	R/W	R/W	R/W
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHC	CHB	CHA	DSDO	CREN	WPD[1:0]		WEN
R/W	R/W	R/W	R/W	R/W	R/W		R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 11. Select DAC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	Reserved	R/W	000	Reserved
12	CLSLD	R/W	0	Clear Select 0 - DACD DAC registers cleared to zero scale upon hardware or software clear (default) 1 - DACD DAC registers cleared to mid scale upon hardware or software clear
11	CLSLC	R/W	0	Clear Select 0 - DACC DAC registers cleared to zero scale upon hardware or software clear (default) 1 - DACC DAC registers cleared to mid scale upon hardware or software clear
10	CLSLB	R/W	0	Clear Select 0 - DACB DAC registers cleared to zero scale upon hardware or software clear (default) 1 - DACB DAC registers cleared to mid scale upon hardware or software clear
9	CLSLA	R/W	0	Clear Select 0 - DACA DAC registers cleared to zero scale upon hardware or software clear (default) 1 - DACA DAC registers cleared to mid scale upon hardware or software clear
8	CHD	R/W	0	Channel D selected
7	CHC	R/W	0	Channel C selected
6	CHB	R/W	0	Channel B selected
5	CHA	R/W	0	Channel A selected
4	DSDO	R/W	0	Disable SDO - When set, this bit disables daisy chain operation and SDO pin is set to HiZ, enabled by default
3	CREN	R/W	0	Enable CRC - When set, this bit enables frame error checking, disabled by default

表 11. Select DAC Register Field Descriptions (接下页)

Bit	Field	Type	Reset	Description
2:1	WPD[1:0]	R/W	00	Watchdog Timer Period 00 - 10 ms (typical) 01 - 51 ms (typical) 10 - 102 ms (typical) 11 - 204 ms (typical)
0	WEN	R/W	0	Enable Watchdog Timer - When set, this bit enables watchdog timer, disabled by default

8.5.2.5 Configuration DAC Register (address = 0x04) [reset = 0x0000]

图 112. Configuration DAC Register

15	14	13	12	11	10	9	8
SCLIM[1:0]		HTEN	OTEN	SRCLK_RATE[3:0]			
R/W		R/W	R/W	R/W			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SR_STEP[2:0]			SREN	RANGE[3:0]			
R/W			R/W	R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 12. Configuration DAC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	SCLIM[1:0]	R/W	00	Voltage output short circuit limit 00 - 16 mA (default). Actual value will be between the minimum and maximum values specified in *Electrical Characteristics*. 01 - 8 mA. Actual value will be between the minimum and maximum values specified in *Electrical Characteristics*. 10 - 20 mA. Actual value will be between the minimum and maximum values specified in *Electrical Characteristics*. 11 - 24 mA. Actual value will be between the minimum and maximum values specified in *Electrical Characteristics*.
13	HTEN	R/W	0	Enable HART - When set, this bit enables HART, disabled by default
12	OTEN	R/W	0	Output Enabled - When set, this bit enables DAC (Voltage or Current) outputs, disabled by default
11:8	SRCLK_RATE[3:0]	R/W	0000	Slew Clock Rate 0000 - DAC updates at 258,065 Hz (default) 0001 - DAC updates at 200,000 Hz 0010 - DAC updates at 153,845 Hz 0011 - DAC updates at 131,145 Hz 0100 - DAC updates at 115,940 Hz 0101 - DAC updates at 69,565 Hz 0110 - DAC updates at 37,560 Hz 0111 - DAC updates at 25,805 Hz 1000 - DAC updates at 20,150 Hz 1001 - DAC updates at 16,030 Hz 1010 - DAC updates at 10,295 Hz 1011 - DAC updates at 8,280 Hz 1100 - DAC updates at 6,900 Hz 1101 - DAC updates at 5,530 Hz 1110 - DAC updates at 4,240 Hz 1111 - DAC updates at 3,300 Hz
7:5	SR_STEP[2:0]	R/W	000	Slew Rate Step Size 000 - 1 LSB (default) 001 - 2 LSB 010 - 4 LSB 011 - 8 LSB 100 - 16 LSB 101 - 32 LSB 110 - 64 LSB 111 - 128 LSB

表 12. Configuration DAC Register Field Descriptions (接下页)

Bit	Field	Type	Reset	Description
4	SREN	R/W	0	Slew Rate Enabled - When set, this bit enables slew rate feature, disabled by default
3:0	RANGE[3:0]	R/W	0000	Range, Please note that upon changing the range, the DAC output changes based on CLSLx (Address 0x03) 0000 - Voltage output 0 to +5 V (default) 0001 - Voltage output 0 to +10 V 0010 - Voltage output ±5 V 0011 - Voltage output ±10 V 0100 - Current output 3.5 mA to 23.5 mA 0101 - Current output 0 to 20 mA 0110 - Current output 0 to 24 mA 0111 - Current output ±24 mA 1000 - Voltage output 0 to +6 V 1001 - Voltage output 0 to +12 V 1010 - Voltage output ±6 V 1011 - Voltage output ±12 V 11xx - Current output 4 mA to 20 mA

8.5.2.6 DAC Data Register (address = 0x05) [reset = 0x0000]

图 113. DAC Data Register

15	14	13	12	11	10	9	8
DAC_DATA[15:8]							
R/W							
7	6	5	4	3	2	1	0
DAC_DATA[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 13. DAC Data Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DAC_DATA[15:0]	R/W		16-bit DAC data

8.5.2.7 Select Buck-Boost Converter Register (address = 0x06) [reset = 0x0000]

图 114. Select Buck-Boost Converter Register

15	14	13	12	11	10	9	8
Reserved							
R/W							
7	6	5	4	3	2	1	0
Reserved				DCD	DCC	DCB	DCA
R/W				R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 14. Select Buck-Boost Converter Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	Reserved	R/W	000000000000	Reserved
3	DCD	R/W	0	Buck-Boost converter D selected
2	DCC	R/W	0	Buck-Boost converter C selected
1	DCB	R/W	0	Buck-Boost converter B selected
0	DCA	R/W	0	Buck-Boost converter A selected

8.5.2.8 Configuration Buck-Boost Register (address = 0x07) [reset = 0x0000]

图 115. Configuration Buck-Boost Register

15	14	13	12	11	10	9	8
Reserved				CCLP[1:0]		PCLMP[3:2]	
R/W				R/W		R/W	

7	6	5	4	3	2	1	0
PCLMP[1:0]		NCLMP[3:0]				PNSEL[1:0]	
R/W		R/W				R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 15. Configuration Buck-Boost Register Field Descriptions

Bit	Field	Type	Reset	Description		
15:12	Reserved	R/W	0000	Reserved		
11:10	CCLP[1:0]	R/W	00	Buck-Boost converter configurable clamp setting 00 - Buck-Boost converter in full tracking mode (default) 01 - User can write to PCLMP and NCLMP bits 10 - PCLMP bits are populated automatically to optimum value - "Auto Learn mode", User cannot write to PCLMP bits 11 - Invalid		
9:6	PCLMP[3:0]	R/W	0000	Buck-Boost converter positive clamp setting, DAC output unloaded - Buck-Boost converter positive arm low side clamp		
					Current Output Mode	Voltage Output Mode
				0000	4.0 V (default)	Invalid
				0001	5.0 V	Invalid
				0010	6.0 V	Invalid
				0011	9.0 V	9.0 V
				0100	11.0 V	Invalid
				0101	12.0 V	Invalid
				0110	13.0 V	Invalid
				0111	14.0 V	Invalid
				1000	15.0 V	15.0 V
				1001	18.0 V	18.0 V
				1010	20.0 V	Invalid
				1011	23.0 V	Invalid
				1100	25.0 V	Invalid
				1101	27.0 V	Invalid
				1110	30.0 V	Invalid
				1111	32.0 V	Invalid

表 15. Configuration Buck-Boost Register Field Descriptions (接下页)

Bit	Field	Type	Reset	Description		
5:2	NCLMP[3:0]	R/W	0000	Buck-Boost converter negative clamp setting, DAC output unloaded - Buck-Boost converter negative arm low side clamp		
					Current Output Mode	Voltage Output Mode
				0000	–5.0 V	Invalid
				0001	–6.0 V	Invalid
				0010	–9.0 V	–9.0 V
				0011	–11.0 V	Invalid
				0100	–12.0 V	Invalid
				0101	–13.0 V	Invalid
				0110	–14.0 V	Invalid
				0111	–15.0 V	–15.0 V (default)
				1000	–18.0 V	Invalid
				1001	–18.0 V	–18.0 V
				101x	Invalid	Invalid
				11xx	Invalid	Invalid
1:0	PNSEL[1:0]	R/W	00	Enable Buck-Boost converter positive and negative arm 00 - Buck-Boost converter positive and negative arm disabled (default) 01 - Buck-Boost converter positive arm enabled and negative arm disabled 10 - Buck-Boost converter positive arm disabled and negative arm enabled 11 - Buck-Boost converter positive arm and negative arm enabled		

8.5.2.9 DAC Channel Calibration Enable Register (address = 0x08) [reset = 0x0000]

图 116. DAC Channel Calibration Enable Register

15	14	13	12	11	10	9	8
Reserved							
R/W							
7	6	5	4	3	2	1	0
Reserved							CLEN
R/W							R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 16. DAC Channel Calibration Enable Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	Reserved	R/W	00000000 0000000	Reserved
0	CLEN	R/W	0	Enable DAC calibration - When set, this bit enables DAC data calibration, disabled by default

8.5.2.10 DAC Channel Gain Calibration Register (address = 0x09) [reset = 0x0000]

图 117. DAC Channel Gain Calibration Register

15	14	13	12	11	10	9	8
UGAIN[15:8]							
R/W							
7	6	5	4	3	2	1	0
UGAIN[7:0]							

R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 17. DAC Channel Gain Calibration Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	UGAIN[15:0]	R/W	00000000 00000000	16-bit user gain data

8.5.2.11 DAC Channel Offset Calibration Register (address = 0x0A) [reset = 0x0000]

图 118. DAC Channel Offset Calibration Register

15	14	13	12	11	10	9	8
UOFF[15:8]							
R/W							
7	6	5	4	3	2	1	0
UOFF[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 18. DAC Channel Offset Calibration Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	UOFF[15:0]	R/W	00000000 00000000	16-bit user offset data

8.5.2.12 Status Register (address = 0x0B) [reset = 0x1000]

图 119. Status Register

15	14	13	12	11	10	9	8
Reserved			CLST	WDT	PGF	PGC	PGB
R/W			R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
PGA	UTGL	CRE	TMP	FD	FC	FB	FA
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 19. Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	Reserved	R/W	000	Reserved
12	CLST	R/W	1	Auto Learn status - Indicates that Auto Learn operation is finished
11	WDT	R/W	0	Watchdog timer fault - Indicates that watchdog timer fault has occurred
10	PGF	R/W	0	Buck-Boost D power good - Indicates the power good condition on Buck-Boost converter D
9	PGC	R/W	0	Buck-Boost C power good - Indicates the power good condition on Buck-Boost converter C
8	PGB	R/W	0	Buck-Boost B power good - Indicates the power good condition on Buck-Boost converter B
7	PGA	R/W	0	Buck-Boost A power good - Indicates the power good condition on Buck-Boost converter A
6	UTGL	R/W	0	User toggle - Copy of user bit (UBT)
5	CRE	R/W	0	CRC error - Indicates CRC error condition
4	TMP	R/W	0	Over temperature - Indicates over temperature condition

表 19. Status Register Field Descriptions (接下页)

Bit	Field	Type	Reset	Description
3	FD	R/W	0	Fault channel D - Indicates fault condition channel D
2	FC	R/W	0	Fault channel C - Indicates fault condition channel C
1	FB	R/W	0	Fault channel B - Indicates fault condition channel B
0	FA	R/W	0	Fault channel A - Indicates fault condition channel A

8.5.2.13 Status Mask Register (address = 0x0C) [reset = 0x0000]

图 120. Status Mask Register

15	14	13	12	11	10	9	8
Reserved				MWT	Reserved		
R/W				R/W	R/W		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved		MCRE	MTMP	MFD	MFC	MFB	MFA
R/W		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 20. Status Mask Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	Reserved	R/W	0000	Reserved
11	MWT	R/W	0	Mask WDT - When set, it masks the alarm pin from watchdog timer fault condition
10:6	Reserved	R/W	00000	Reserved
5	MCRE	R/W	0	CRC error - When set, it masks the alarm pin from CRC error condition
4	MTMP	R/W	0	Mask TMP - When set, it masks the alarm pin from over temperature condition
3	MFD	R/W	0	Mask FD - When set, it masks the alarm pin from fault condition channel D
2	MFC	R/W	0	Mask FC - When set, it masks the alarm pin from fault condition channel C
1	MFB	R/W	0	Mask FB - When set, it masks the alarm pin from fault condition channel B
0	MFA	R/W	0	Mask FA - When set, it masks the alarm pin from fault condition channel A

8.5.2.14 Alarm Action Register (address = 0x0D) [reset = 0x0000]

图 121. Alarm Action Register

15	14	13	12	11	10	9	8
Reserved							
R/W							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
AC_CRE_WDT[1:0]		AC_IOC[1:0]		AC_VSC[1:0]		AC_TMP[1:0]	
R/W		R/W		R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 21. Alarm Action Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	Reserved	R/W	00000000	Reserved
7:6	AC_CRE_WDT[1:0]	R/W	00	Action CRC error and Watchdog timer fault circuit condition 00 - No action on Buck-Boost converters, no action on DACs (default) 01 - No action on Buck-Boost converters, respective user alarm code on all DACs 10 - All Buck-Boost converters and DACs disabled and remain disabled even after the alarm condition is removed. 11 - Invalid
5:4	AC_IOC[1:0]	R/W	00	Action current output open circuit condition 00 - No action on Buck-Boost converters, no action on DACs (default) 01 - No action on Buck-Boost converters, respective user alarm code on DAC(s) initiating the alarm 10 - All Buck-Boost converters and DACs disabled and remain disabled even after the alarm condition is removed. 11 - Invalid
3:2	AC_VSC[1:0]	R/W	00	Action voltage output short circuit condition 00 - No action on Buck-Boost converters, no action on DACs (default) 01 - No action on Buck-Boost converters, respective user alarm code on DAC(s) initiating the alarm 10 - All Buck-Boost converters and DACs disabled and remain disabled even after the alarm condition is removed. 11 - Invalid
1:0	AC_TMP[1:0]	R/W	00	Action over temperature condition 00 - No action on Buck-Boost converters, no action on DACs (default) 01 - No action on Buck-Boost converters, respective user alarm code on all DACs 10 - All Buck-Boost converters and DACs disabled and remain disabled even after the alarm condition is removed. 11 - Invalid

8.5.2.15 User Alarm Code Register (address = 0x0E) [reset = 0x0000]

图 122. User Alarm Code Register

15	14	13	12	11	10	9	8
ACODE[15:10]						HSCLMP	0
R/W						R/W	R/W
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 22. User Alarm Code Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	ACODE[15:10]	R/W	000000	6 bit alarm code data
9	HSCLMP	R/W	0	Buck-Boost positive output high side clamp 0 - Buck-Boost converter positive output high side clamp set to 32 V (default) 1 - Buck-Boost converter positive output high side clamp set to 26 V (default)
8	0	R/W	0	0
7:0	Reserved	R/W	00000000	Reserved

8.5.2.16 Reserved Register (address = 0x0F) [reset = N/A]

图 123. Reserved Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 23. Reserved Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	Reserved	–	N/A	Reserved

8.5.2.17 Write Watchdog Timer Register (address = 0x10) [reset = 0x0000]

图 124. Write Watchdog Timer Register

15	14	13	12	11	10	9	8
Reserved							
W							
7	6	5	4	3	2	1	0
Reserved							RWD
W							W

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

表 24. Write Watchdog Timer Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	Reserved	–	00000000 0000000	Reserved
0	RWD	W	0	Reset watchdog timer, this bit clears itself after resetting watch dog timer

8.5.2.18 Device ID Register (address = 0x11) [reset = 0x0000]

图 125. Device ID Register

15	14	13	12	11	10	9	8
Reserved							
R							
7	6	5	4	3	2	1	0
Reserved					DID[2:0]		
R					R		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 25. Device ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	Reserved	–	00000000 00000	Reserved
2:0	DID [2:0]	R	000	3-bit device identification code

8.5.2.19 Reserved Register (address 0x12 - 0xFF) [reset = N/A]

图 126. Reserved Register

15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 26. Reserved Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	Reserved	–	N/A	Reserved

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Buck-Boost Converter External Component Selection

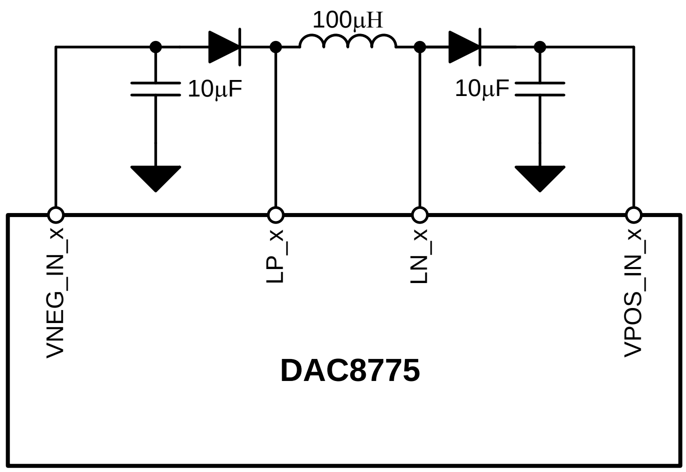


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图 127. DAC8775 External Buck-Boost Components with Recommended Values

The buck-boost converters integrated in the DAC8775 each require three external passive components for operation: a single inductor per channel as well as storage capacitors and switching diodes for each VPOS_IN_x and VNEG_IN_x channels that are active. If only one output is used, either VPOS_IN_x or VNEG_IN_x, the inactive output components may be removed and the respective inputs tied to ground. In order to meet the parametric performance outlined in the *Electrical Characteristics* section for the voltage output, 500 mV of foot-room is required on VNEG_IN_x.

The recommended value for the external inductor is 100 µH with at least 500 mA peak inductor current. Reducing the inductor value to as low as 80 µH is possible, though this will limit the buck-boost converter maximum input voltage to output voltage ratio, reduce efficiency, and increase ripple. Reducing the inductor below 80 µH will result in device damage. Peak inductor current should be rated at 500 mA or greater with 20% inductance tolerance at peak current. If peak inductor current for an inductor is violated the effective inductance is reduced, which will impact maximum input to output voltage ratio, efficiency, and ripple.

An output, or storage, X7R capacitor with value of 10 µF and voltage rating of 50 V is recommended though other values and dielectric materials may be used without damaging the DAC8775. Reducing capacitor value will increase buck-boost converter output ripple and reduced voltage rating will reduce effective capacitance at full-scale buck-boost converter outputs. X7R capacitors are rated for –55°C to 125°C operation with 15% maximum capacitance variance over temperature. Designs operating over reduced temperature spans and with loose efficiency requirements may use different dielectric material. C0G capacitor typically offer tighter capacitance variance but come in larger packages, but may be beneficial substitutes.

Application Information (接下页)

The external diode switches illustrated on the left and right side of the 100 µH inductor shown in 图 127 should be selected based on reverse voltage rating, reverse recovery time, leakage or parasitic capacitance, and current or power ratings. Breakdown voltage rating of at least 60 V is recommended to accommodate for the maximum voltage that may be across the diode when both VPOS_x and VNEG_x are both active during switching of the DC/DCs. Minimal reverse recovery time and parasitic capacitance is recommended in order to preserve efficiency of the DC/DCs. The external diode should be rated for at least 500 mA average forward current.

9.1.2 Voltage and Current Ouputs on a Shared Terminal

图 128 illustrates a simplified block diagram of the voltage output stages of the DAC8775.

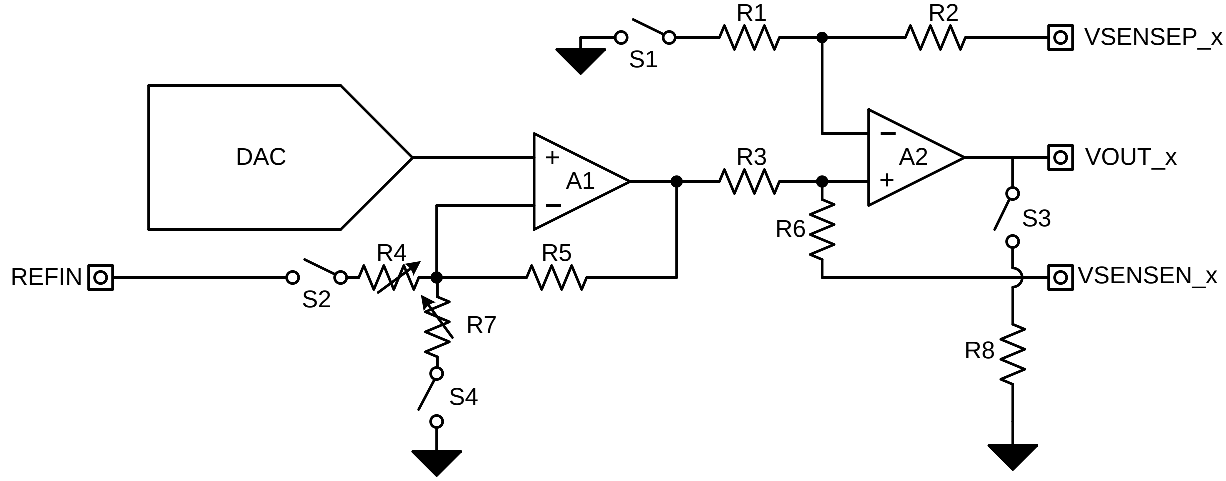

图 128. Simplified Block Diagram of Voltage Output Architecture

When designing for a shared voltage and current output terminal it is important to consider leakage paths that may corrupt the voltage or current output stages.

When the voltage output is active and the current output is inactive the IOUT_x pin becomes a high-impedance node and therefore does not significantly load the voltage output in a way that would degrade VOUT_x performance. When the voltage output is inactive and the current output is active switches S1, S2, and S4 all become open while switch S3 is controlled by the POC bit in the Reset Config Register for each respective channel. When the POC bit is set to a 0, the default value, switch S3 is closed when VOUT is disabled. This creates a leakage path with respect to the current output when the terminals are shared which will create a load-dependent error. In order to reduce this error the POC bit can be set to a 1 which opens switch S3, effectively making the VOUT pin high-impedance and reducing the magnitude of leakage current.

9.1.3 Optimizing Current Output Settling time with Auto learn Mode

When the buck-boost converters are active power and heat dissipation of the device are at a minimum, however settling time of the current output is dominated by the slew rate of the buck-boost converter, which is significantly slower that the current output signal chain alone. When the buck-boost converters are bypassed settling time of the current output is minimized while power and heat dissipation are significant.

Auto-learn mode offers an alternative mode which allows the buck-boost converter to learn the size of the load and choose a clamped output value that does not change over the full range of the selected current output. This allows a balance between settling time and power dissipation. There are two options for entering auto-learn mode:

- Enable the buck-boost converter in full-tracking mode followed by enabling the current output. Until the DAC code 0x4000 is passed, settling time will be dominated by the buck-boost converter. After code 0x400 is surpassed the buck-boost converter detects the load and sets the clamp value appropriately.
- Enable the buck-boost converter in clamp-mode with clamp value set to a greater voltage than required by the largest load the current output will be expected to drive, followed by enabling the current output. Enter full-

Application Information (接下页)

tracking mode. In this case the clamp value of maintained without the buck-boost converter output changing, therefore settling time is set by the IOUT_x signal chain. After code 0x4000 is surpassed the buck-boost converter detects the load and adjusts the clamp value appropriately. At all times using this initialization procedure the settling time is defined by the IOUT_x signal chain.

9.1.4 Protection for Industrial Transients

In order to successfully protect the DAC8775, or any integrated circuit, against industrial transient testing the internal structures and how they may behave when exposed to said signals must be understood. 图 129 depicts a simplified representation of internal structures present on the device's output pins which are represented as a pair of clamp-to-rail diodes connected to the VPOS_IN_x and VNEG_IN_x supply rails.

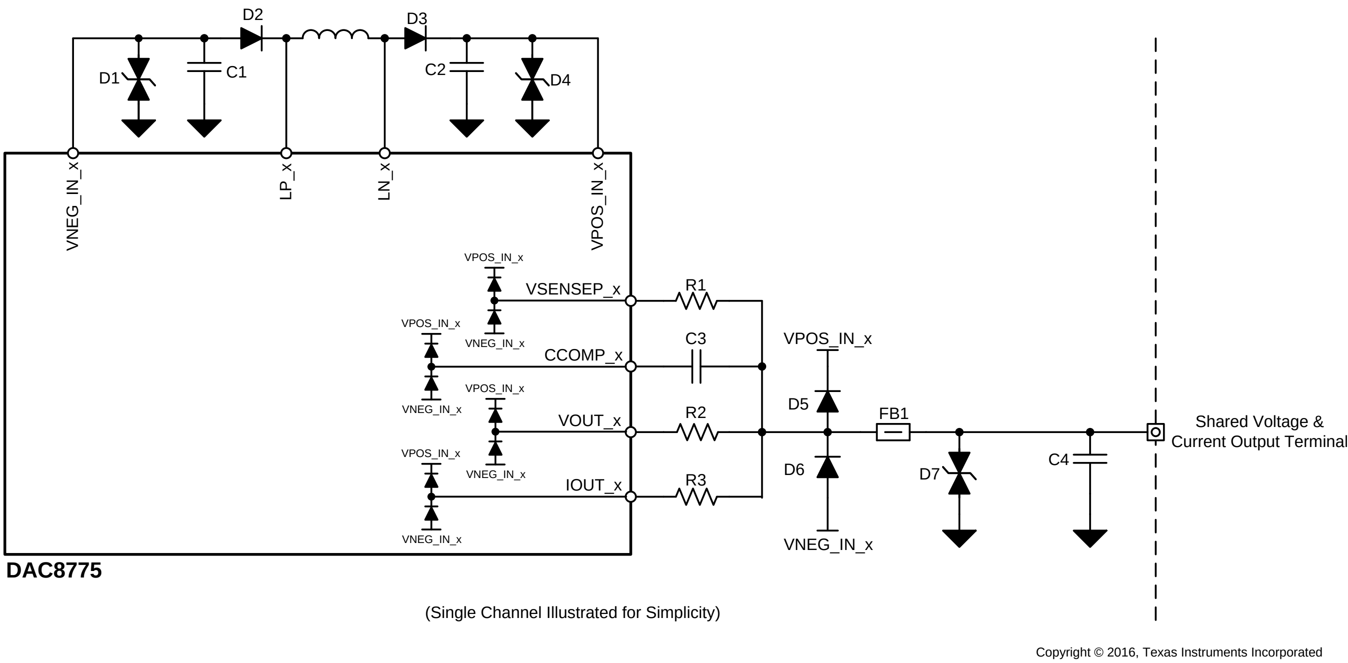

图 129. Simplified Block Diagram of Internal Structures and External Protection

When these internal structures are exposed to industrial transient testing, without the external protection components, the diode structures will become forward biased and conduct current. If the conducted current is too large, which is often true for high-voltage industrial transient tests, the structures will become permanently damaged and impact device functionality.

Both attenuation and diversion strategies are implemented to protect the internal structures as well as the device itself. Attenuation is realized by capacitor C4 which forms an R/C low-pass filter when interacting with the source impedance of the transient generator, ferrite bead FB1 also helps attenuate high-frequency current, along with both AC and DC current limiters realized by series pass elements R1, R2, and R3. Diversion is achieved by transient voltage suppressor (TVS) diode D7 and clamp-to-rail diodes D5 and D6. The combined effects of both strategies effectively limit the current flowing into the device and through the internal diode structures such that the device is not damaged and remains functional.

It is important to also include TVS diodes D1 and D4 at the VPOS_IN_x and VNEG_IN_x nodes in order to provide a discharge path for the energy that is going to be sent to these nodes through diodes D5, D6, and the internal diode structures. Without these diodes when current is diverted to these nodes the DC/DC converter storage capacitors C1 and C2 will charge, slowly increasing the voltage at these nodes.

Application Information (接下页)

9.1.5 Implementing HART with DAC8775

The DAC8775 features internal resistors to convert a 500-mVpp HART FSK signal sourced by an external HART modem. These resistors are ratiometrically matched to the gain-setting resistors for the current output signal chain to ensure that a 500-mVpp input at the HART_IN_x pin is delivered as a 1-mApp signal at the respective IOUT_x pin regardless of which gain mode is selected.

An external capacitor, placed in series between the HART_IN_x pin and HART FSK source, is required to AC couple the HART FSK signal to the HART_IN_x pin. The recommended capacitance for this external capacitor is from 10 nF to 22 nF.

9.2 Typical Application

9.2.1 1W Power Dissipation, Quad Channel, EMC and EMI Protected Analog Output Module with Adaptive Power Management

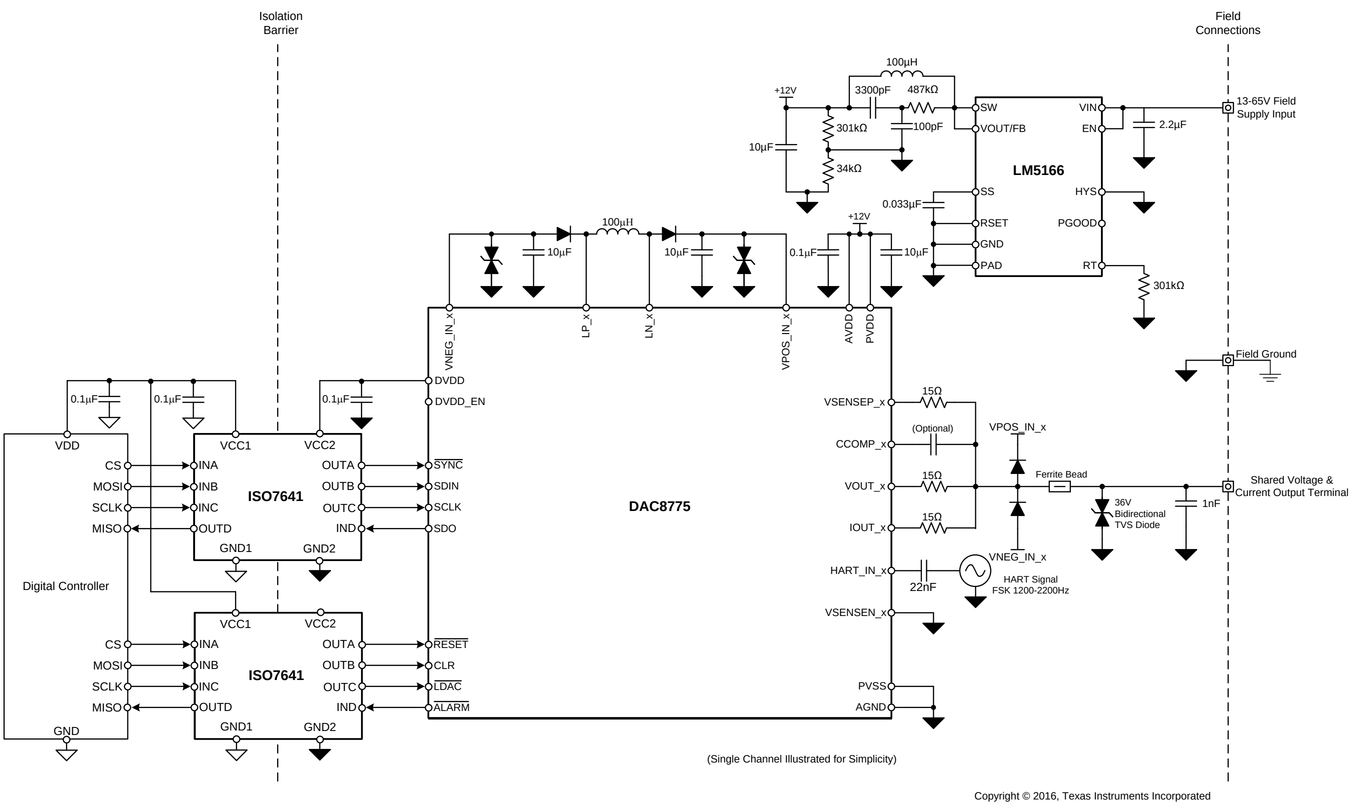

图 130. DAC8775 in Quad-Channel PLC AO Module

9.2.2 Design Requirements

Analog I/O modules are used by programmable logic controllers (PLCs) to interface sensors, actuators, and other field instruments. These modules must meet stringent electrical specifications for both accuracy and robust protection. These outputs are typically current outputs based on the 4-mA to 20-mA range and derivatives or voltage outputs ranging from 0 V to 5 V, 0 V to 10 V, ±5 V, and ±10 V. Common error budgets accommodate 0.1% full-scale range total unadjusted error (% FSR TUE) at room temperature. Designs that desire stronger accuracy over temperature frequently implement calibration. Often the PLC back-plane provides access to a 12-V to 36-V analog supply from which a majority of analog supply voltages are derived.

Typical Application (接下页)

Analog output modules are frequently multi-channel modules featuring either channel-to-channel isolation between each channel or group isolation where several channels share a common ground connection. As channel count increases it is desirable to maintain small form-factor requiring high levels of integration and reduced power dissipation in order to control heat inside of the PLC enclosure.

Therefore the design requirements are:

- Support of standard industrial automation voltage and current output spans
- Operation with standard industrial automation supply voltages from 12 V to 36 V
- Current and voltage outputs with TUE less than 0.1% at 25°C
- Total on-board power dissipation less than or equal to 1 W
- At minimum criteria B IEC61000-4 ESD, EFT, CI, and Surge immunity

9.2.3 Detailed Design Procedure

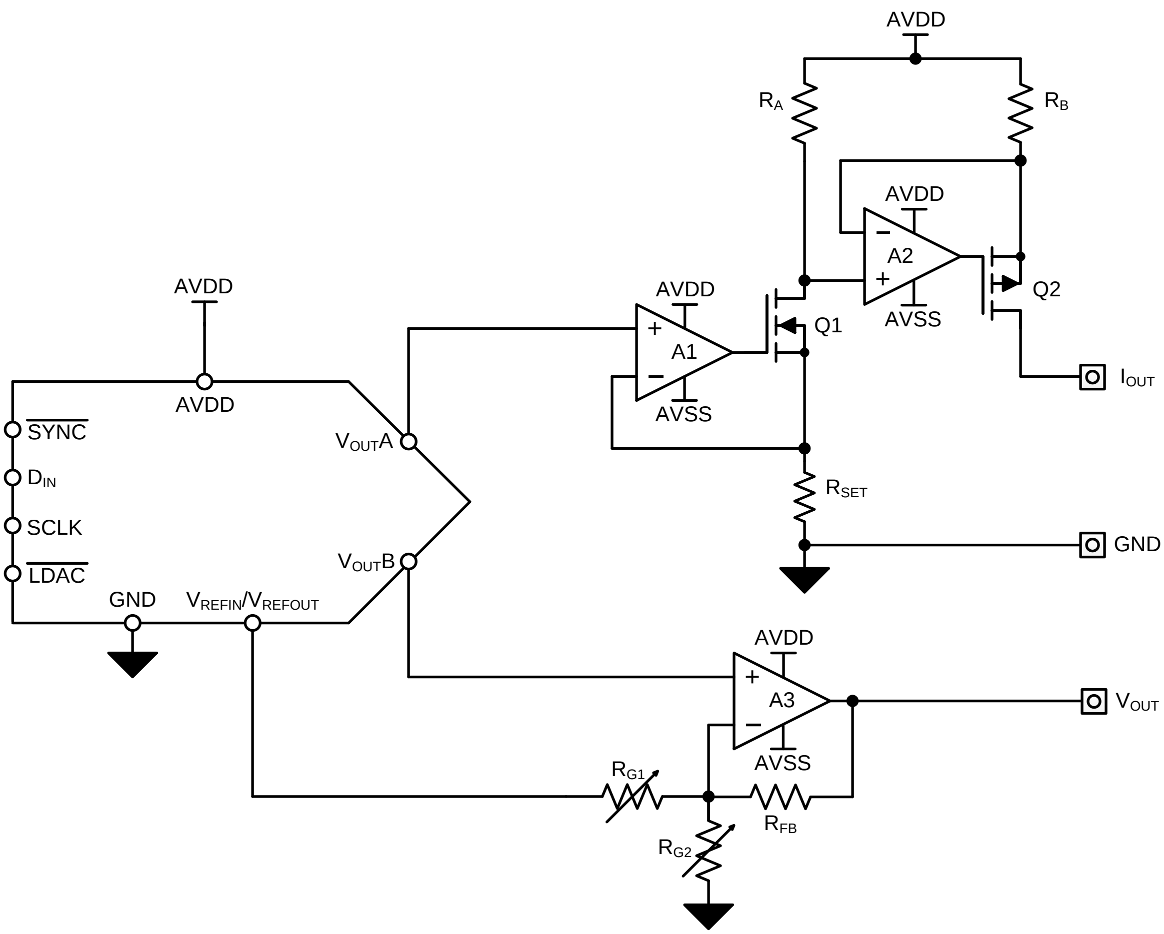

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图 131. Generic Design for Typical PLC Current and Voltage Outputs

图 131 illustrates a common generic solution for realizing the desired voltage and current output spans for industrial automation applications.

The current output circuit is comprised of amplifiers A1 and A2, MOSFETs Q1 and Q2, and the three resistors RSET, RA, and RB. This two-stage current source enables the ground-referenced DAC output voltage to drive the high-side amplifier required for the current-source.

Typical Application (接下页)

The voltage output circuit is composed of amplifier A3 and the resistor network consisting of RFB, RG1, and RG2. A3 operates as a modified summing amplifier, where the DAC controls the non-inverting input and inverting input has one path to GND and a second to VREF. This configuration allows the single-ended DAC to create both the unipolar 0-V to 5-V and 0-V to 10-V outputs and the bipolar ±5-V and ±10-V outputs by modifying the values of RG1 and RG2.

Though this generic circuit realizes the desired spans, both the voltage and current outputs have short-comings. The current output high-side supply voltage is typically 24 V, when driving low impedance loads with this supply voltage a considerable amount of power is dissipated on RB and Q2. This power dissipation results in increased heat which leads to drift errors for amplifiers A1 and A2 as well as the DAC, resistors, and the reference voltage. In order to reduce the power dissipation in the high-side voltage to current converter circuit a feedback system which monitors the voltage drop across Q2 and adaptively adjusts the high-side supply voltage can be implemented. This feedback system adjusts the high side supply voltage to the minimum supply required to keep Q2 in the linear region of operation, avoiding compliance voltage saturation, reducing power dissipation and heat to a minimum which helps maintain accuracy.

The generic voltage output circuit performs well but does not compensate for errors associated with excessive output impedance or differences in ground potential from the local PLC ground and the load ground. A modified circuit can be implemented which provides connections to sense errors associated with both output impedance voltage drops and differences in ground potentials, this circuit is shown in 图 128.

图 130 illustrates the DAC8775 along with the LM5166 in a quad-channel PLC analog output module. The DAC8775 includes the generic voltage and current output circuits along with buck-boost converter and feedback circuits for the current output and positive and negative sense connections for the voltage output circuit. The DAC8775 includes an internal reference and internal LDO for supplying the field-side of a digital isolator along with the buck-boost converter generating the single or dual high voltage supplies required for the output circuits, all powered from a single supply.

The DAC8775 buck-boost converter operates at peak efficiency with 12-V input voltage with peak power consumption of approximately 780mW. The LM5166 circuit accepts a wide range of input voltages from just above 12 V to 65 V, providing coverage for most standard PLC supply voltages, and buck-converts this supply voltage to the optimal 12-V supply for the DAC8775. Cumulative power dissipation for the DAC8775 and LM5166 is under 1 W.

Two ISO7641 devices implement galvanic isolation for all of the digital communication lines, though only a single ISO7641 is required for basic communication with the DAC8775 SPI compatible interface. An output protection circuit is included which is designed to provide immunity to the IEC61000-4 industrial transient and radiation test suite. The protection circuit includes transient voltage suppressor (TVS) diodes, clamp-to-rail steering diodes, and pass elements in the form of resistors and ferrite beads.

9.2.4 Application Curves

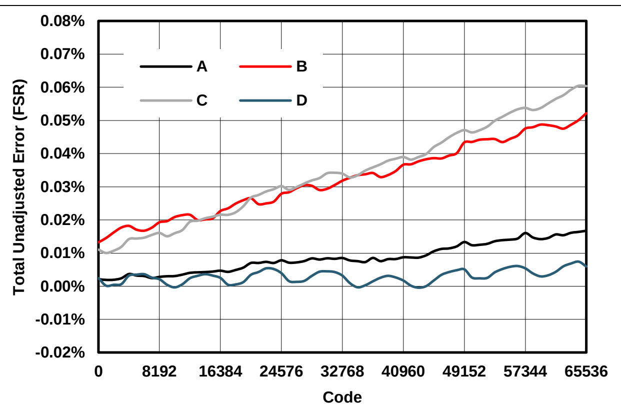


图 132. 4-mA to 20-mA IOUT TUE vs Code

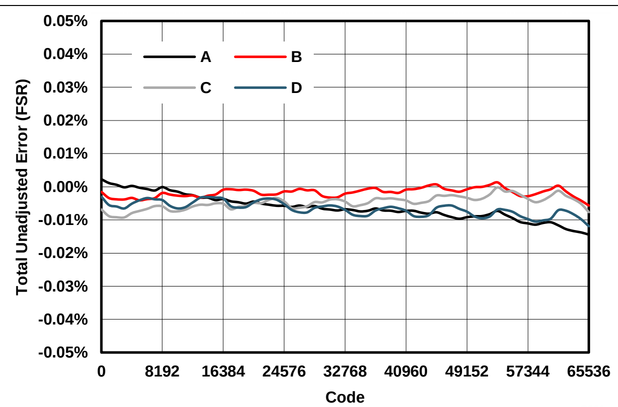


图 133. ±10-V VOUT TUE vs Code

Typical Application (接下页)

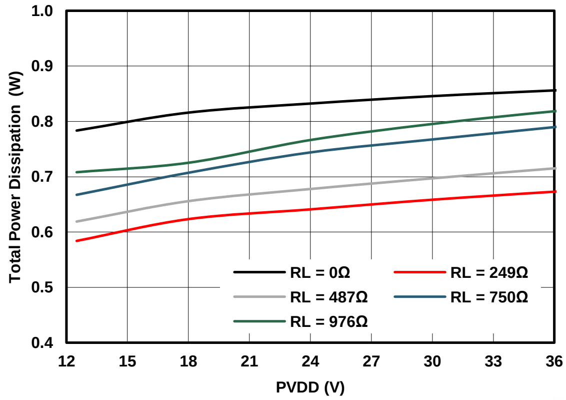
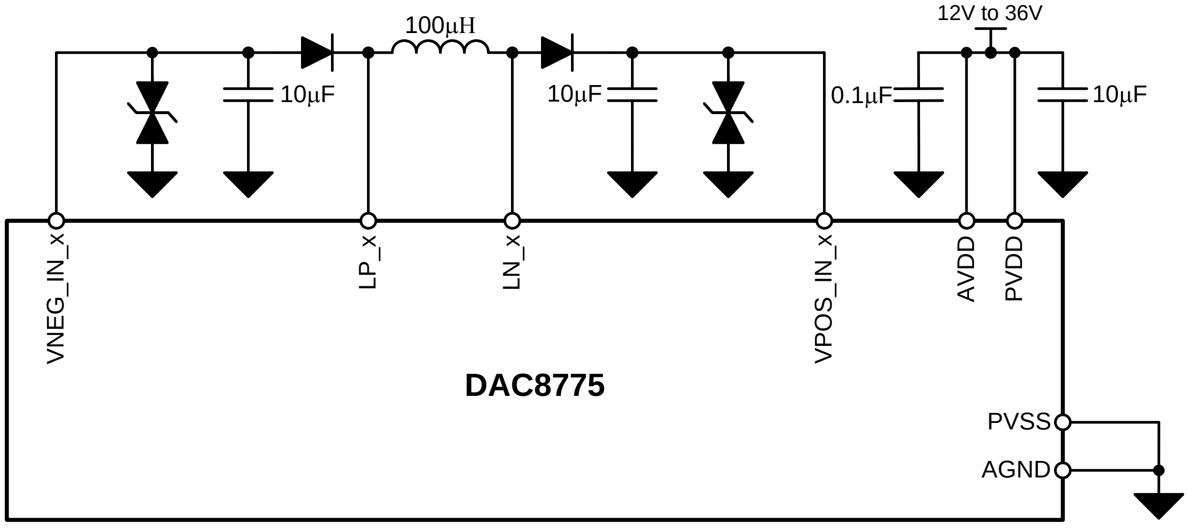


图 134. Total On-Board Power Dissipation vs Supply

10 Power Supply Recommendations

There are three possible hardware power supply configurations for the DAC8775: the internal DC/DC provides both positive and negative supply voltages, the internal DC/DC provides only one of the supply voltages with an external supply provided on the other, or the internal DC/DC is not used at all and external supply voltages are provided for both positive and negative supply voltages. Simple illustrations for each case are shown below.



(Single Channel Illustrated for Simplicity)

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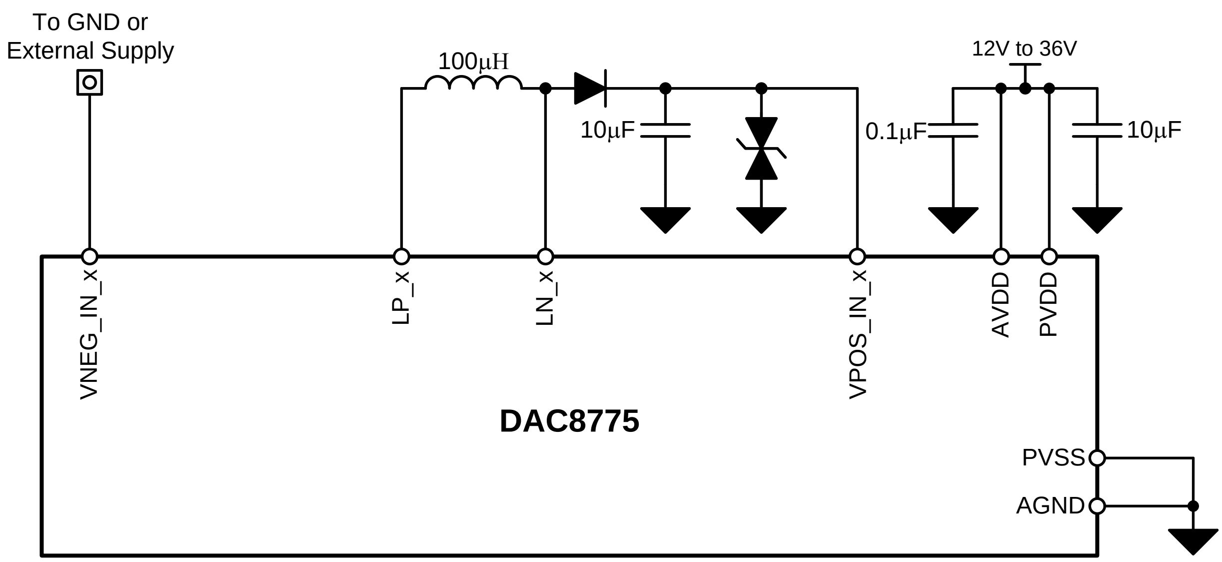
图 135. DAC8775 With Dual Supplies from Internal DC/DC

图 136 illustrates using a single supply from the DAC8775 internal DC/DC and the other supply from an external source. In this example the VNEG_IN_x supply is the input being supplied by an external supply, or ground for unipolar output spans. A similar scheme could be used if VPOS_IN_x was supplied by an external supply and VNEG_IN_x was supplied by the internal DC/DC.



(Single Channel Illustrated for Simplicity)

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图 136. DAC8775 With Single Supply from Internal DC/DC

The scheme in 图 137 should be used if the internal DC/DC is not used at all and external supplies are selected for VPOS_IN_x and VNEG_IN_x. When using external supplies for VPOS_IN_x it is important that VPOS_IN_x, PVDD, and AVDD nodes are tied to the same voltage potential with the same ramp-rate.

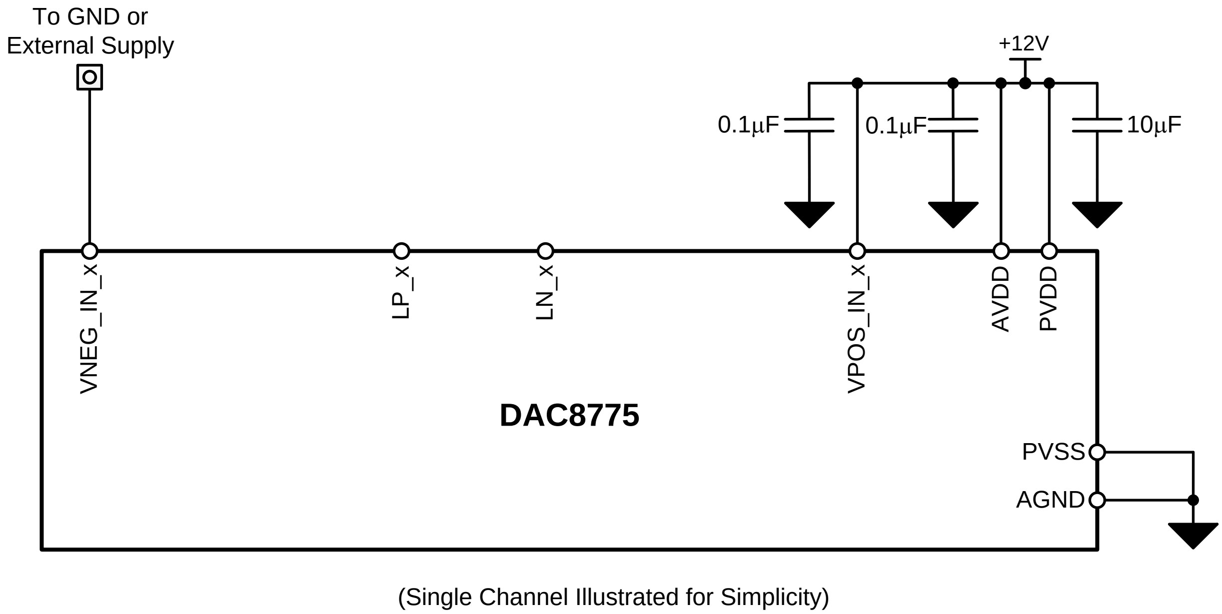

图 137. DAC8775 with External Supplies

11 Layout

11.1 Layout Guidelines

An example layout based on the design discussed in the *Typical Application* section is shown in the *Layout Example* section. 图 139 shows the top-layer of the design which illustrates all component placement as no components are placed on the bottom layer. 图 140 shows two of the internal power-layers: the layer on the left contains VPOS_IN_B, VPOS_IN_C, VNEG_IN_B, and VNEG_IN_D nets while the layer on the right contains VPOS_IN_A, VPOS_IN_D, VNEG_IN_A, and VNEG_IN_C nets.

The layer stack-up for this 6-layer example layout is shown below. A 6-layer design is not required, however provides optimal conditions for ground and power-supply planes. The solid ground plane beneath the majority of the signal traces, which are placed on the top layer, allows for a clean return path for sensitive analog traces and keeps them isolated from the internal power supply nets which will exhibit ripple from the DC/DC converter.

Signal Traces and Ground Fill
Solid Ground Plane
Split Power Supply Plane for 13V to 66V Field Supply Connection and PVDD/AVDD net
Split VPOS_IN_B, VPOS_IN_C, VNEG_IN_B, and VNEG_IN_D net Planes
Split VPOS_IN_A, VPOS_IN_D, VNEG_IN_A, and VNEG_IN_C net Planes
Signal Traces and Ground Fill

图 138. Example Layout Layer Stack-Up

Traces for the DC/DC external components should be as low impedance, low inductance, and low capacitance as possible in order to maintain optimum performance. As such wide traces should be used to minimize inductance with minimal use of vias as vias will contribute large inductance and capacitance to the trace. For this reason it is recommended that all DC/DC components placed on the top layer.

The industrial transient protection circuit should be placed as close to the output connectors as possible to ensure that the return currents from these transients have a controlled path to exit the PCB which does not impact the analog circuitry.

Split ground planes for the DC/DC, digital, and analog grounds are not required but may be helpful to isolated ground return currents from cross-talk. If split ground planes are used care should be taken to ensure that signal traces are only placed above or below the locations where their respective grounds are placed in order to mitigate unexpected return paths or coupling to the other ground planes. If a single ground plane is used it is advisable to follow similar practices implementing a star-ground where the respective return currents interact with one another minimally. The example layout uses a single ground plane, based on measured results, performs similarly to an identical version with split ground planes.

The perimeter of the board is stitched with vias in order to enhance design performance against environments which may include radiated emissions. Additional vias are placed in critical areas nearby the design in order to place ground pours in between nodes to reduce cross-talk between adjacent traces.

Standard best-practices should be applied to the remaining components, including but not limited to, placing decoupling capacitors close to their respective pins and using wide traces or copper pours where possible, particularly for power traces where high current may flow.

11.2 Layout Example

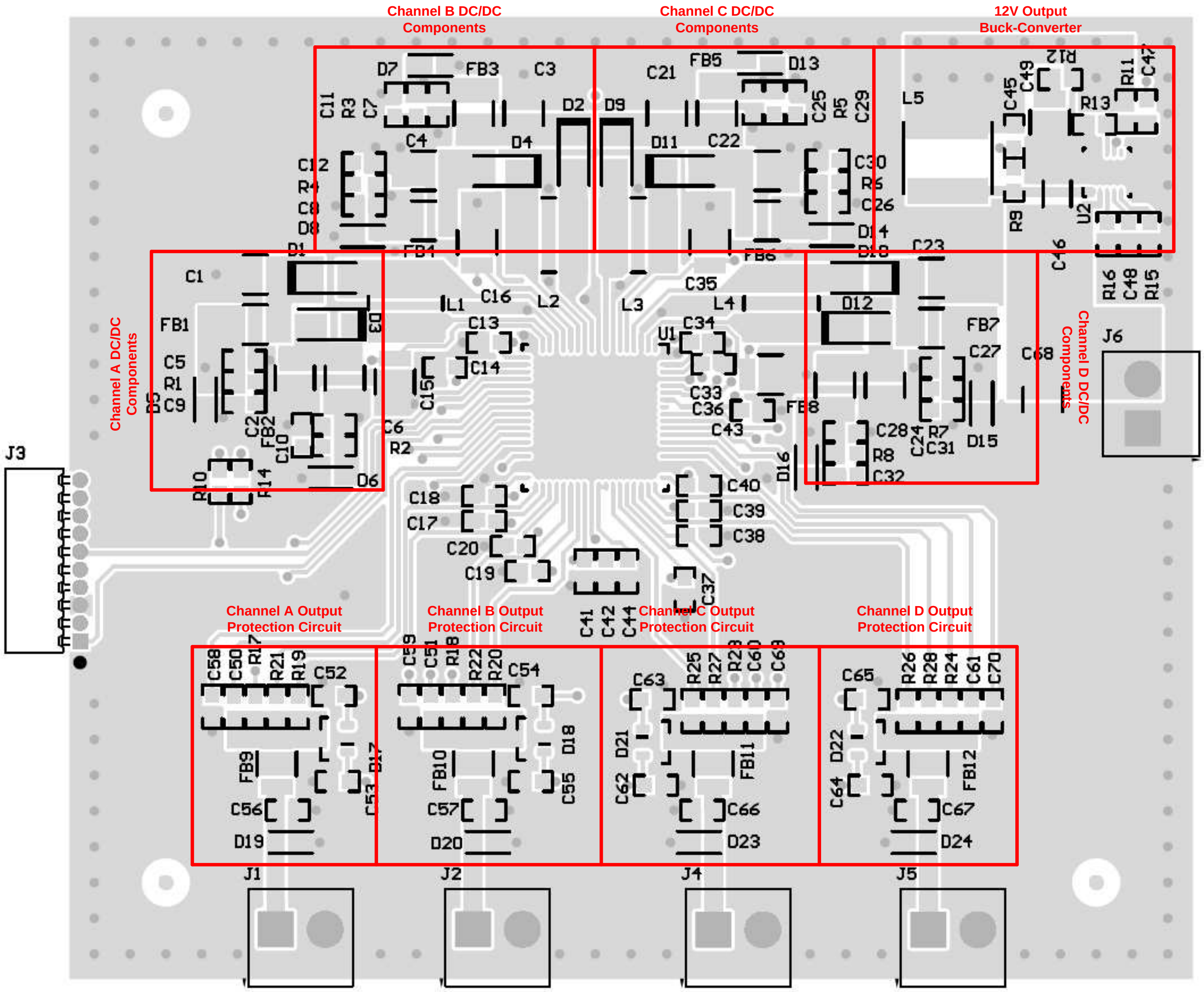

图 139. Application Example Layout

Layout Example (接下页)

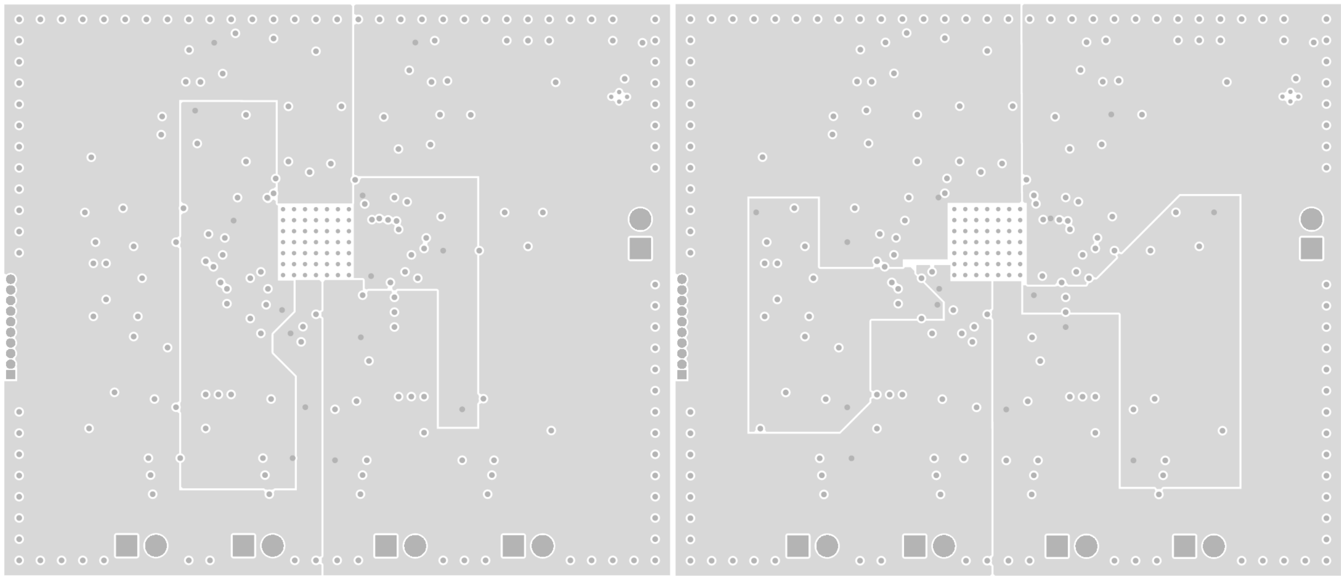

图 140. Example Design Internal Copper Pours

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档请参见以下部分：

- 《DAC8775 EVM 用户指南》（文献编号：SBAU248）
- 《LM5166 I_Q 超低的 3V 至 65V 输入、500mA 同步降压转换器数据表》（文献编号：SNVSA67）
- 《ISO76x1 低功耗三通道和四通道数字隔离器》（文献编号：SLLSEC3）

12.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.3 社区资源

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC8775IRWFR	ACTIVE	VQFN	RWF	72	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8775	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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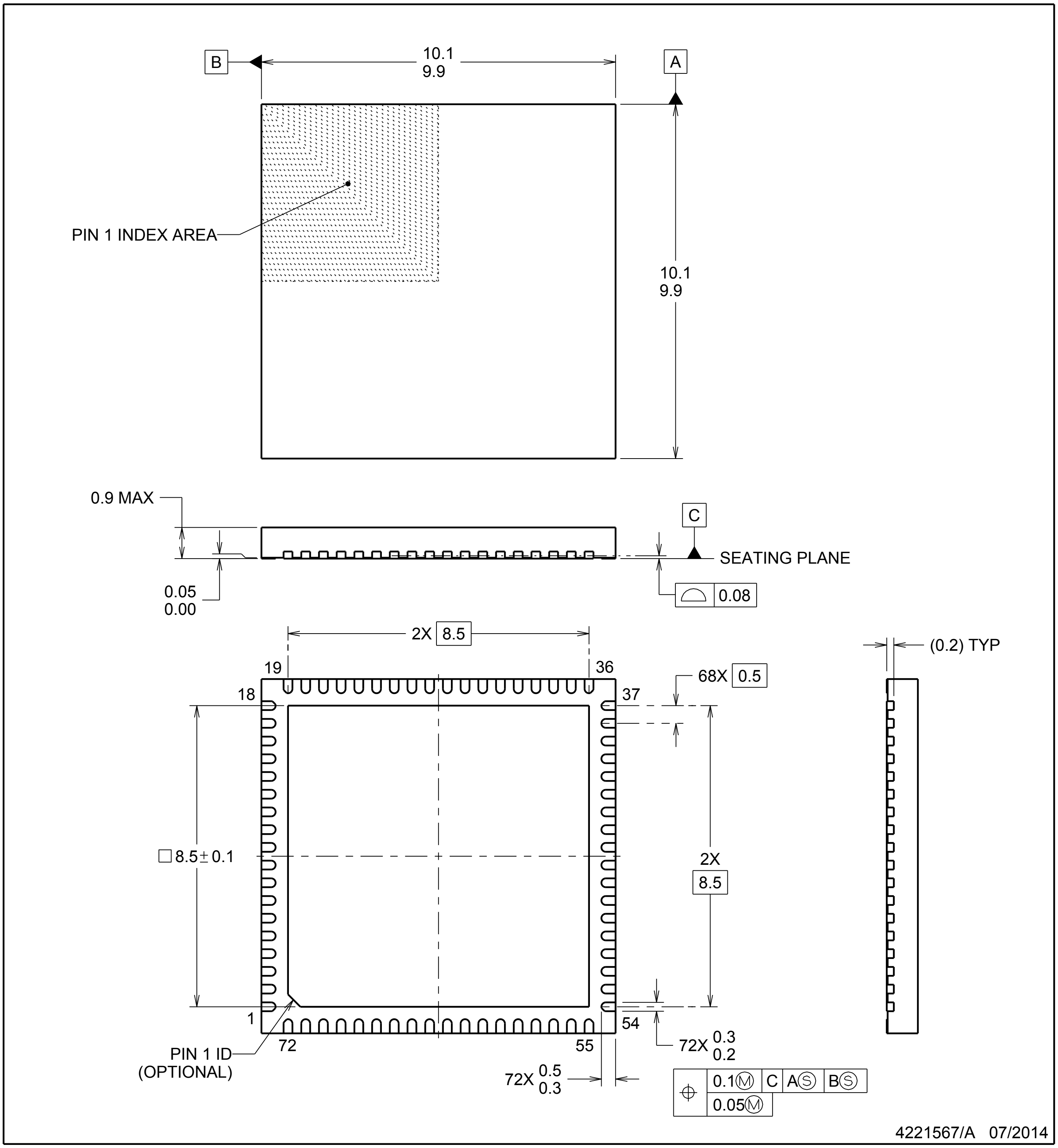
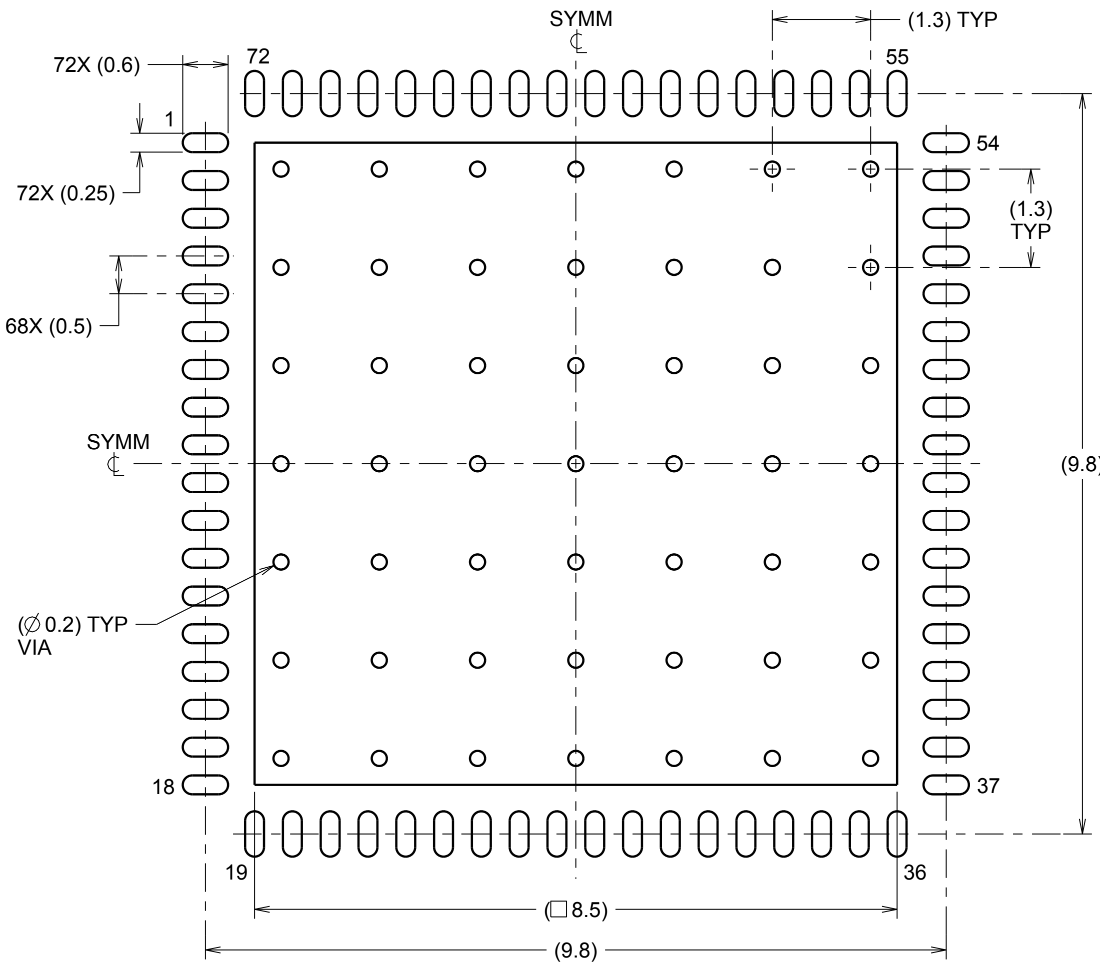
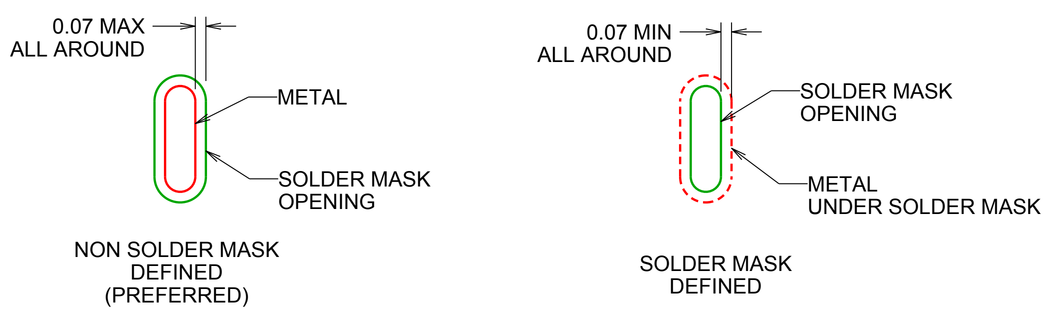


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:10X

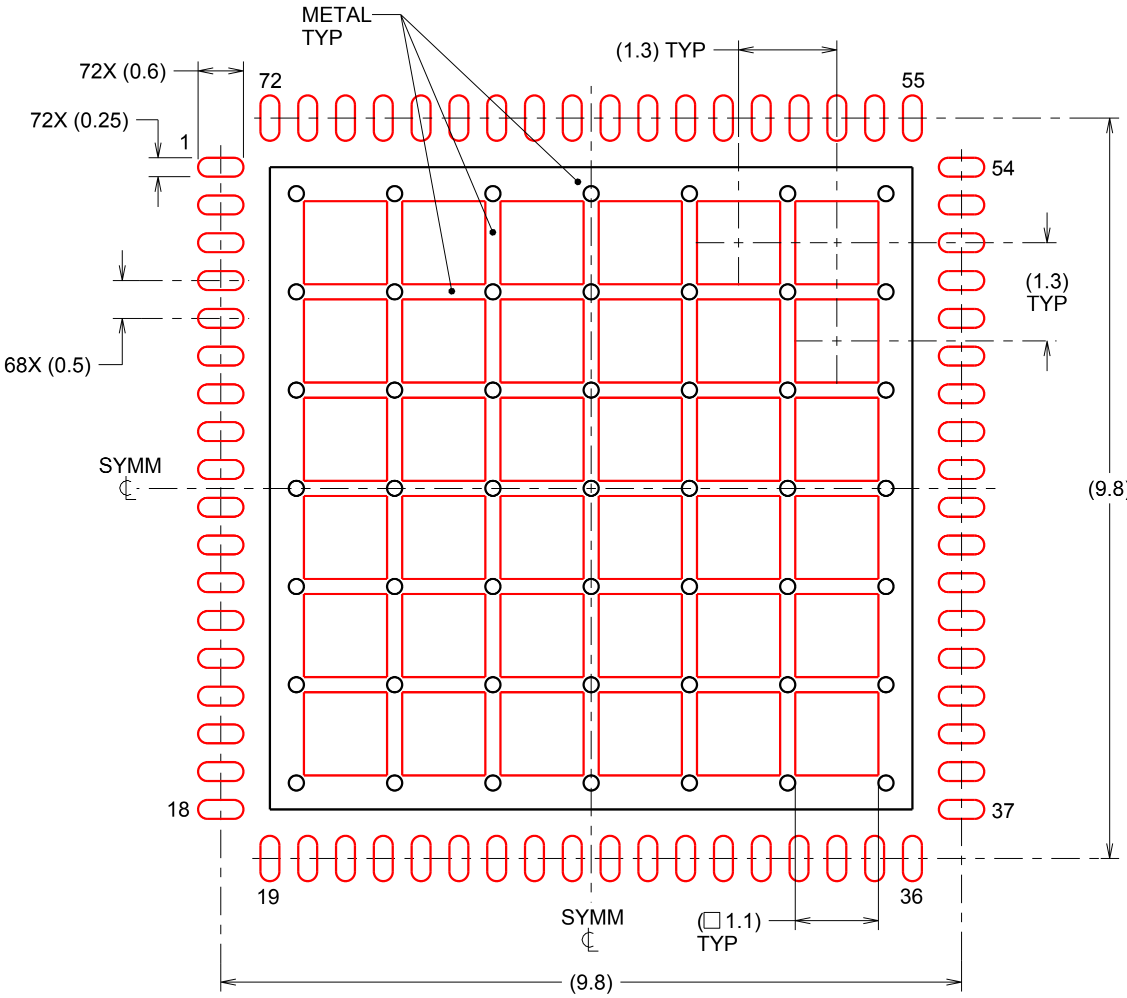


SOLDER MASK DETAILS

4221567/A 07/2014

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
60% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

4221567/A 07/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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