

## LM25019 48V、100mA 恒定导通时间同步降压/Fly-Buck™ 稳压器

## 1 特性

- 7.5V 至 48V 宽输入范围
- 集成了 100mA 高侧和低侧开关
- 无需肖特基二极管
- 恒定导通时间控制
- 无需环路补偿
- 超快瞬态响应
- 接近恒定的运行频率
- 智能峰值电流限制
- 可调节输出电压 (以 1.225V 为基准电压)
- 精度为 2% 的反馈基准电压
- 频率可调至 1MHz
- 可调节的欠压锁定
- 远程关断
- 热关断
- 封装：
  - 8 引脚 WSON
  - 8 引脚 SO PowerPAD™

## 2 应用

- 工业设备
- 智能电表
- 电信系统
- 隔离式偏置电源 (Fly-Buck™)

## 3 说明

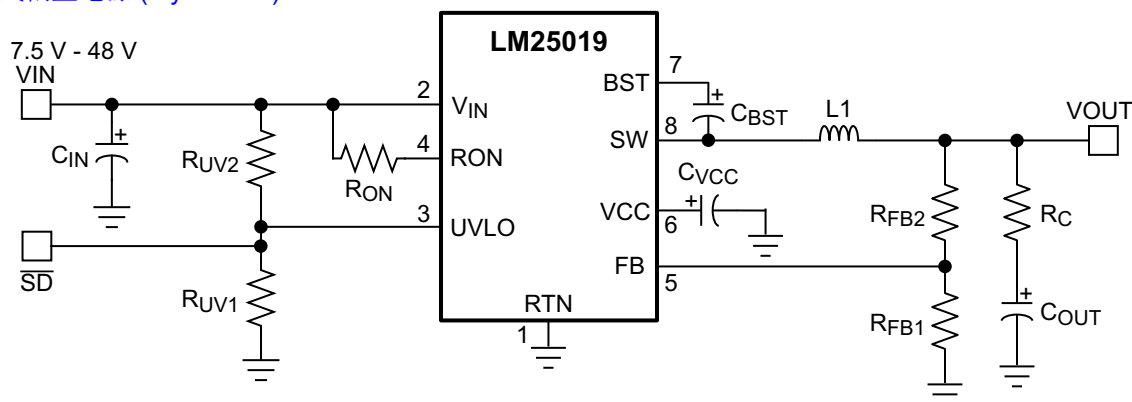
LM25019 是一款集成了高侧和低侧 MOSFET 的 48V、100mA 同步降压稳压器。LM25019 所采用的恒定导通时间 (COT) 控制方案无需环路补偿, 可提供出色的瞬态响应, 并且可实现超高降压比。导通时间与输入电压成反比, 这使得整个输入电压范围内的频率几乎保持恒定。高压启动稳压器为 IC 的内部运行以及集成栅极驱动器提供了偏置电源。

峰值电流限制电路可防止出现过载情况。欠压锁定 (UVLO) 电路支持对输入欠压阈值和迟滞进行单独编程。其他保护特性包括: 热关断和偏置电源欠压锁定。

LM25019 采用 8 引脚 WSON 和 8 引脚 SO PowerPAD 塑料封装。

## 器件信息

器件型号	封装	封装尺寸 (标称值)
LM25019	SO PowerPAD (8)	4.89mm x 3.90mm
	WSON (8)	4.00mm x 4.00mm



典型应用



## Table of Contents

<b>1 特性</b> .....	<b>1</b>	7.4 Device Functional Modes.....	<b>15</b>
<b>2 应用</b> .....	<b>1</b>	<b>8 Application and Implementation</b> .....	<b>16</b>
<b>3 说明</b> .....	<b>1</b>	8.1 Application Information.....	16
<b>4 Revision History</b> .....	<b>2</b>	8.2 Typical Application.....	16
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	<b>9 Power Supply Recommendations</b> .....	<b>20</b>
<b>6 Specifications</b> .....	<b>4</b>	<b>10 Layout</b> .....	<b>21</b>
6.1 Absolute Maximum Ratings.....	4	10.1 Layout Guidelines.....	21
6.2 ESD Ratings.....	4	10.2 Layout Example.....	21
6.3 Recommended Operating Conditions.....	4	<b>11 Device and Documentation Support</b> .....	<b>22</b>
6.4 Thermal Information.....	4	11.1 Documentation Support.....	22
6.5 Electrical Characteristics.....	6	11.2 接收文档更新通知.....	22
6.6 Switching Characteristics.....	6	11.3 支持资源.....	22
6.7 Typical Characteristics.....	7	11.4 Trademarks.....	22
<b>7 Detailed Description</b> .....	<b>9</b>	11.5 Electrostatic Discharge Caution.....	22
7.1 Overview.....	9	11.6 Glossary.....	22
7.2 Functional Block Diagram.....	9	<b>12 Mechanical, Packaging, and Orderable Information</b> .....	<b>22</b>
7.3 Feature Description.....	9		

## 4 Revision History

<b>Changes from Revision E (April 2015) to Revision F (May 2021)</b> .....	<b>Page</b>
• 在标题中添加了“同步 Fly-Buck” .....	1
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
<b>Changes from Revision D (December 2014) to Revision E (November 2015)</b> .....	<b>Page</b>
• Changed 14 V to 13 V in <i>V<sub>CC</sub> Regulator</i> section.....	10
• Changed 8 to 4 on equation in <i>Input Capacitor</i> section.....	18
• Changed 0.06 $\mu$ F to 0.12 $\mu$ F in <i>Input Capacitor</i> section.....	18
<b>Changes from Revision C (December 2013) to Revision D (November 2014)</b> .....	<b>Page</b>
• 添加了 引脚配置和功能 部分、ESD 等级表、特性说明 部分、器件功能模式、应用和实施 部分、电源相关建议 部分、布局 部分、器件和文档支持 部分以及机械、封装和可订购信息 部分.....	1
• Changed <i>Soft-Start Circuit</i> graphic.....	14
• Changed <i>Frequency Selection</i> section, <i>Inductor Selection</i> section, <i>Output Capacitor</i> section, <i>Input Capacitor</i> section, and <i>UVLO Resistors</i> section.....	17
• Changed <i>Series Ripple Resistor R<sub>C</sub></i> section to <i>Type III Ripple Circuit</i> .....	18
<b>Changes from Revision B (December 2013) to Revision C (December 2013)</b> .....	<b>Page</b>
• Added Thermal Parameters .....	4
<b>Changes from Revision A (September 2013) to Revision B (December 2013)</b> .....	<b>Page</b>
• 将文档中的格式更改为符合 TI 标准的格式.....	1
• 将 特性 中的最低工作输入电压从 9V 更改为 7.5V.....	1
• 将 典型应用 中的最低工作输入电压从 9V 更改为 7.5V.....	1
• Added Absolute Maximum Junction Temperature.....	4
• Changed minimum operating input voltage from 9 V to 7.5 V in <i>Recommended Operating Conditions</i> .....	4
<b>Changes from Revision * (December 2012) to Revision A (September 2013)</b> .....	<b>Page</b>
• Added SW to RTN (100 ns transient) in <i>Absolute Maximum Ratings</i> table.....	4

## 5 Pin Configuration and Functions

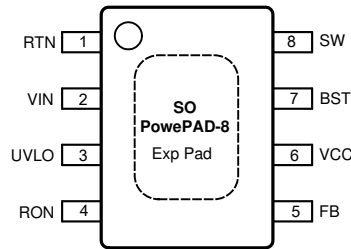


图 5-1. 8-Pin SO PowerPAD DDA Package Top View

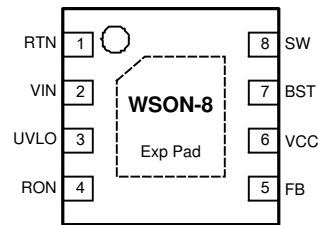


图 5-2. 8-Pin WSON NGU Package Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
1	RTN	—	Ground	Ground connection of the integrated circuit
2	VIN	I	Input Voltage	Operating input range is 7.5 V to 48 V.
3	UVLO	I	Input Pin of Undervoltage Comparator	Resistor divider from $V_{IN}$ to UVLO to GND programs the undervoltage detection threshold. An internal current source is enabled when UVLO is above 1.225 V to provide hysteresis. When UVLO pin is pulled below 0.66 V externally, the regulator is in shutdown mode.
4	RON	I	On-Time Control	A resistor between this pin and $V_{IN}$ sets the buck switch on-time as a function of $V_{IN}$ . Minimum recommended on-time is 100 ns at max input voltage.
5	FB	I	Feedback	This pin is connected to the inverting input of the internal regulation comparator. The regulation level is 1.225 V.
6	VCC	O	Output from the Internal High Voltage Series Pass Regulator. Regulated at 7.6 V	The internal $V_{CC}$ regulator provides bias supply for the gate drivers and other internal circuitry. A 1.0- $\mu$ F decoupling capacitor is recommended.
7	BST	I	Bootstrap Capacitor	An external capacitor is required between the BST and SW pins (0.01- $\mu$ F ceramic). The BST pin capacitor is charged by the $V_{CC}$ regulator through an internal diode when the SW pin is low.
8	SW	O	Switching Node	Power switching node. Connect to the output inductor and bootstrap capacitor.
—	EP	—	Exposed Pad	Exposed pad must be connected to the RTN pin. Solder to the system ground plane on application board for reduced thermal resistance.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

	MIN <sup>(1)</sup>	MAX	UNIT
V <sub>IN</sub> , UVLO to RTN	- 0.3	53	V
SW to RTN	- 1.5	V <sub>IN</sub> + 0.3	V
SW to RTN (100 ns transient)	- 5	V <sub>IN</sub> + 0.3	V
BST to VCC		53	V
BST to SW		13	V
RON to RTN	- 0.3	53	V
VCC to RTN	- 0.3	13	V
FB to RTN	- 0.3	5	V
Lead Temperature <sup>(2)</sup>		200	°C
Maximum Junction Temperature <sup>(3)</sup>		150	°C
Storage temperature, T <sub>stg</sub>	- 55	150	°C

- (1) *Absolute Maximum Ratings* are limits beyond which damage to the device may occur. [§ 6.3](#) are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see [§ 6.5](#). The RTN pin is the GND reference electrically connected to the substrate.
- (2) For detailed information on soldering plastic SO Power PAD-8 package, refer to the Packaging Data Book available from Texas Instruments. Max solder time not to exceed 4 seconds.
- (3) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
V <sub>IN</sub> Voltage	7.5	48	V
Operating Junction Temperature <sup>(2)</sup>	-40	125	°C

- (1) *Recommended Operating Conditions* are conditions under the device is intended to be functional. For specifications and test conditions, see [§ 6.5](#).
- (2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

### 6.4 Thermal Information

THERMAL METRICS <sup>(1)</sup>		LM25019		UNIT
		WSO8 NGU	SO PowerPAD DDA	
		8 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	41.3	41.1	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	3.2	2.4	°C/W
Ψ <sub>JB</sub>	Junction-to-board thermal characteristic parameter	19.2	24.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	19.1	30.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	34.7	37.3	°C/W

THERMAL METRICS <sup>(1)</sup>		LM25019		UNIT
		WSO8 NGU	SO PowerPAD DDA	
		8 PINS		
$\Psi_{JT}$	Junction-to-top thermal characteristic parameter	0.3	6.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

## 6.5 Electrical Characteristics

Typical values correspond to  $T_J = 25^\circ\text{C}$ . Minimum and maximum limits apply over  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  junction temperature range unless otherwise stated.  $V_{IN} = 48\text{V}$  unless stated otherwise. See <sup>(1)</sup>.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
<b>V<sub>CC</sub> SUPPLY</b>						
V <sub>CC</sub> Reg	V <sub>CC</sub> Regulator Output	$V_{IN} = 48\text{ V}, I_{CC} = 20\text{ mA}$	6.25	7.6	8.55	V
	V <sub>CC</sub> Current Limit	$V_{IN} = 48\text{ V}$ <sup>(2)</sup>	26			mA
	V <sub>CC</sub> Undervoltage Lockout Voltage (V <sub>CC</sub> Increasing)		4.15	4.5	4.9	V
	V <sub>CC</sub> Undervoltage Hysteresis			300		mV
	V <sub>CC</sub> Drop Out Voltage	$V_{IN} = 9\text{ V}, I_{CC} = 20\text{ mA}$		2.3		V
	I <sub>IN</sub> Operating Current	Nonswitching, FB = 3 V		1.75		mA
	I <sub>IN</sub> Shutdown Current	UVLO = 0 V		50	225	μA
<b>SWITCH CHARACTERISTICS</b>						
	Buck Switch R <sub>DS(ON)</sub>	$I_{TEST} = 100\text{ mA}, \text{BST-SW} = 7\text{ V}$		0.8	1.8	Ω
	Synchronous R <sub>DS(ON)</sub>	$I_{TEST} = 200\text{ mA}$		0.45	1	Ω
	Gate Drive UVLO	$V_{BST} - V_{SW}$ Rising	2.4	3	3.6	V
	Gate Drive UVLO Hysteresis			260		mV
<b>CURRENT LIMIT</b>						
	Current Limit Threshold		150	270	370	mA
	Current Limit Response Time	Time to Switch Off		150		ns
	Off-Time Generator (Test 1)	FB = 0.1 V, $V_{IN} = 48\text{ V}$		12		μs
	Off-Time Generator (Test 2)	FB = 1 V, $V_{IN} = 48\text{ V}$		2.5		μs
<b>REGULATION AND OVERVOLTAGE COMPARATORS</b>						
	FB Regulation Level	Internal Reference Trip Point for Switch ON	1.2	1.225	1.25	V
	FB Overvoltage Threshold	Trip Point for Switch OFF		1.62		V
	FB Bias Current			60		nA
<b>UNDERVOLTAGE SENSING FUNCTION</b>						
	UV Threshold	UV Rising	1.19	1.225	1.26	V
	UV Hysteresis Input Current	UV = 2.5 V	- 10	- 20	- 29	μA
	Remote Shutdown Threshold	Voltage at UVLO Falling	0.32	0.66		V
	Remote Shutdown Hysteresis			110		mV
<b>THERMAL SHUTDOWN</b>						
T <sub>sd</sub>	Thermal Shutdown Temperature			165		°C
	Thermal Shutdown Hysteresis			20		°C

(1) All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

(2) V<sub>CC</sub> provides self bias for the internal gate drive and control circuits. Device thermal limitations limit external loading.

## 6.6 Switching Characteristics

Typical values correspond to  $T_J = 25^\circ\text{C}$ . Minimum and maximum limits apply over  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  junction temperature range unless otherwise stated.  $V_{IN} = 48\text{ V}$  unless otherwise stated.

		MIN	TYP	MAX	UNIT
<b>ON-TIME GENERATOR</b>					
T <sub>ON</sub> Test 1	$V_{IN} = 32\text{ V}, R_{ON} = 100\text{ k}\Omega$	270	350	460	ns
T <sub>ON</sub> Test 2	$V_{IN} = 48\text{ V}, R_{ON} = 100\text{ k}\Omega$	188	250	336	ns
T <sub>ON</sub> Test 4	$V_{IN} = 10\text{ V}, R_{ON} = 250\text{ k}\Omega$	1880	3200	4425	ns

Typical values correspond to  $T_J = 25^\circ\text{C}$ . Minimum and maximum limits apply over  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  junction temperature range unless otherwise stated.  $V_{IN} = 48\text{ V}$  unless otherwise stated.

	MIN	TYP	MAX	UNIT
<b>MINIMUM OFF-TIME</b>				
Minimum Off-Time	FB = 0 V	144		ns

## 6.7 Typical Characteristics

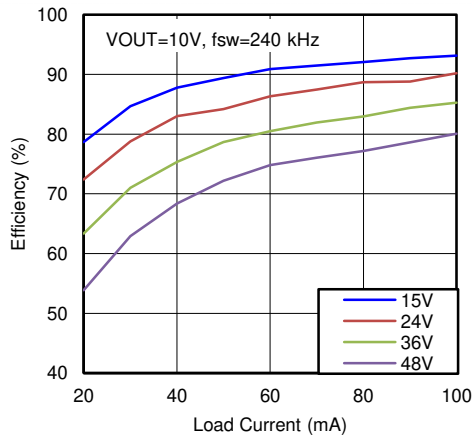


图 6-1. Efficiency at 240 kHz, 10 V

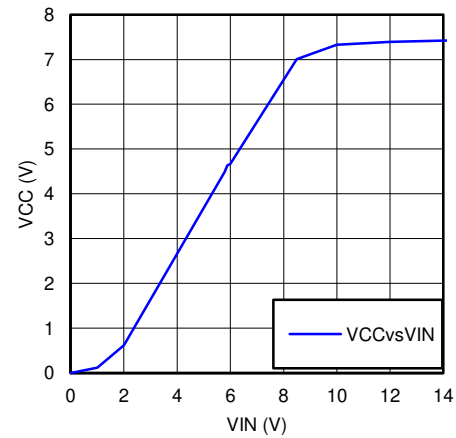


图 6-2.  $V_{CC}$  versus  $V_{IN}$

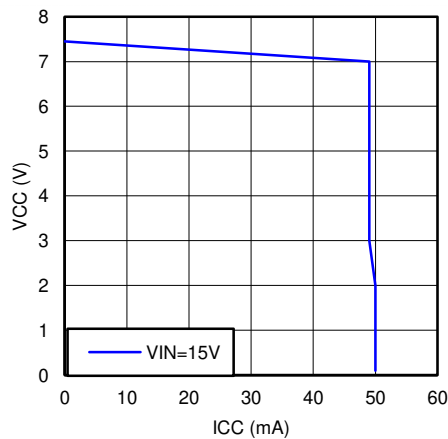


图 6-3.  $V_{CC}$  versus  $I_{CC}$

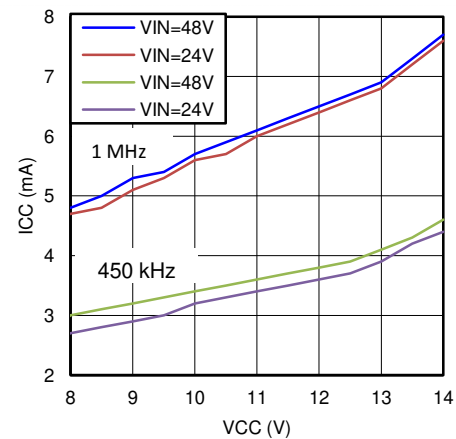
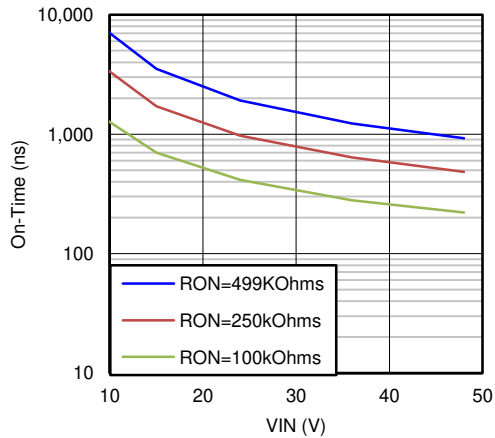
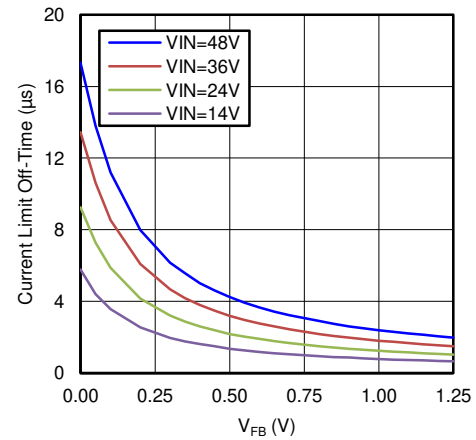
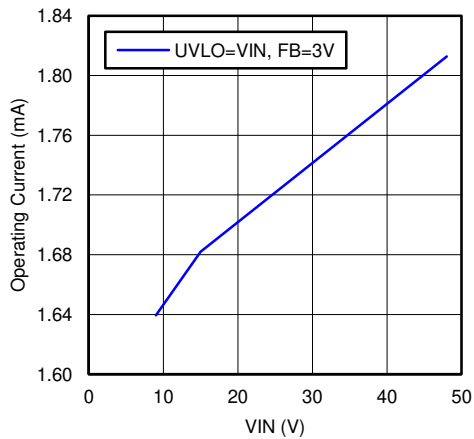
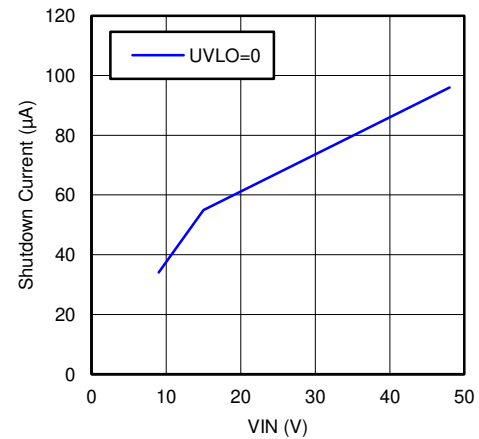
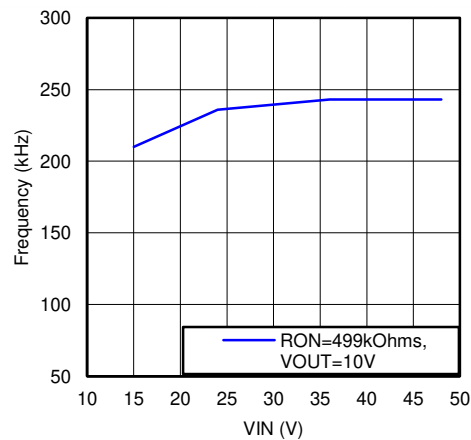


图 6-4.  $I_{CC}$  vs External  $V_{CC}$

图 6-5. T<sub>ON</sub> versus V<sub>IN</sub> and R<sub>ON</sub>图 6-6. T<sub>OFF</sub> (I<sub>LIM</sub>) versus V<sub>FB</sub> and V<sub>IN</sub>图 6-7. I<sub>IN</sub> versus V<sub>IN</sub> (Operating, Nonswitching)图 6-8. I<sub>IN</sub> versus V<sub>IN</sub> (Shutdown)图 6-9. Switching Frequency versus V<sub>IN</sub>



## 7 Detailed Description

### 7.1 Overview

The LM25019 step-down switching regulator features all the functions needed to implement a low-cost, efficient, buck converter that can supply up to 100 mA to the load. This high-voltage regulator contains 48-V, N-channel buck and synchronous switches, is easy to implement, and is provided in thermally-enhanced SO PowerPAD-8 and WSON-8 packages. The regulator operation is based on a constant on-time control scheme using an on-time inversely proportional to  $V_{IN}$ . This control scheme does not require loop compensation. The current limit is implemented with a forced off-time inversely proportional to  $V_{OUT}$ . This scheme ensures short circuit protection while providing minimum foldback. The simplified block diagram of the LM25019 device is shown in the 图 7-1.

The LM25019 device can be applied in numerous applications to efficiently regulate down higher voltages. This regulator is well suited for 12-V and 24-V rails. Protection features include: thermal shutdown, undervoltage lockout, minimum forced off-time, and an intelligent current limit.

### 7.2 Functional Block Diagram

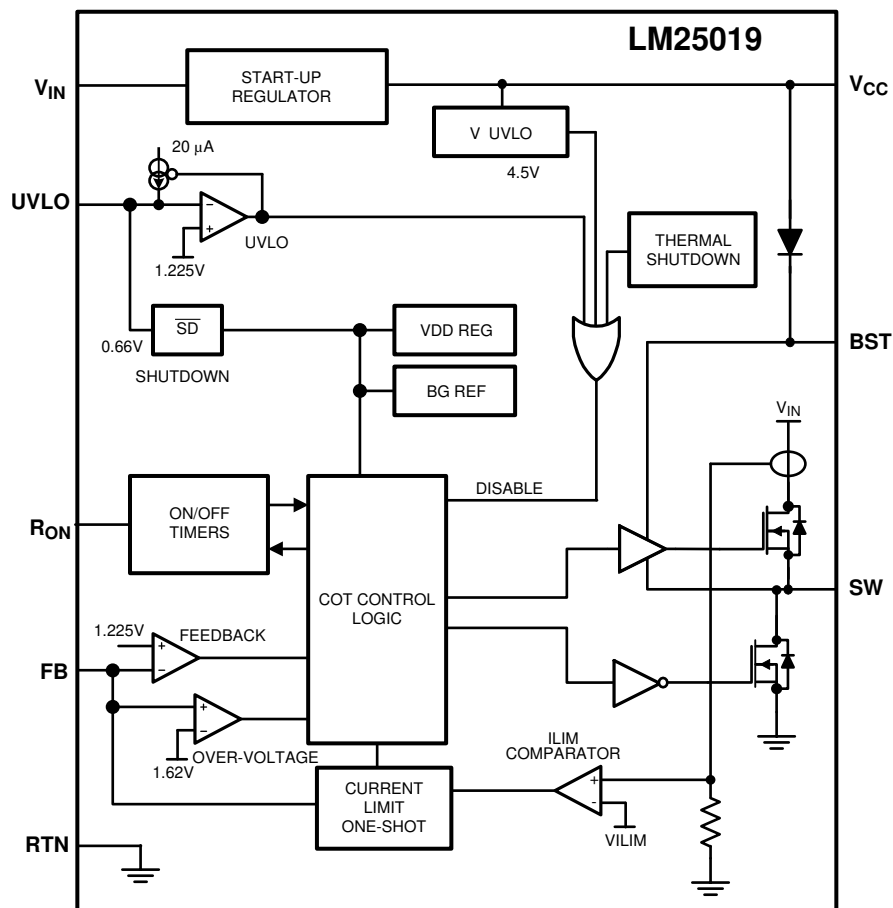


图 7-1. Functional Block Diagram

### 7.3 Feature Description

#### 7.3.1 Control Overview

The LM25019 buck regulator employs a control principle based on a comparator and a one-shot on-timer, with the output voltage feedback (FB) compared to an internal reference (1.225 V). If the FB voltage is below the reference, the internal buck switch is turned on for the one-shot timer period, which is a function of the input voltage and the programming resistor ( $R_{ON}$ ). Following the on-time, the switch remains off until the FB voltage falls below the reference, but never before the minimum off-time forced by the minimum off-time one-shot timer.

When the FB pin voltage falls below the reference and the minimum off-time one-shot period expires, the buck switch is turned on for another on-time one-shot period. This continues until regulation is achieved and the FB voltage is approximately equal to 1.225 V (typ).

In a synchronous buck converter, the low-side (sync) FET is on when the high-side (buck) FET is off. The inductor current ramps up when the high-side switch is on and ramps down when the high-side switch is off. There is no diode emulation feature in this IC, and therefore, the inductor current can ramp in the negative direction at light load. This causes the converter to operate in continuous conduction mode (CCM) regardless of the output loading. The operating frequency remains relatively constant with load and line variations. The operating frequency can be calculated as shown in 方程式 1.

$$f_{SW} = \frac{V_{OUT}}{9 \times 10^{-11} \times R_{ON}} \quad (1)$$

The output voltage ( $V_{OUT}$ ) is set by two external resistors ( $R_{FB1}$ ,  $R_{FB2}$ ). The regulated output voltage is calculated as shown in 方程式 2.

$$V_{OUT} = 1.225V \times \frac{R_{FB2} + R_{FB1}}{R_{FB1}} \quad (2)$$

This regulator regulates the output voltage based on ripple voltage at the feedback input, requiring a minimum amount of ESR for the output capacitor ( $C_{OUT}$ ). A minimum of 25 mV of ripple voltage at the feedback pin (FB) is required for the LM25019. In cases where the capacitor ESR is too small, additional series resistance can be required ( $R_C$  in 图 7-2).

For applications where lower output voltage ripple is required the output can be taken directly from a low ESR output capacitor, as shown in 图 7-2. However,  $R_C$  slightly degrades the load regulation.

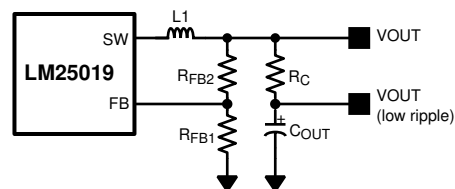


图 7-2. Low Ripple Output Configuration

### 7.3.2 $V_{CC}$ Regulator

The LM25019 device contains an internal high-voltage linear regulator with a nominal output of 7.6 V. The input pin ( $V_{IN}$ ) can be connected directly to the line voltages up to 48 V. The  $V_{CC}$  regulator is internally current limited to 30 mA. The regulator sources current into the external capacitor at  $V_{CC}$ . This regulator supplies current to internal circuit blocks including the synchronous MOSFET driver and the logic circuits. When the voltage on the  $V_{CC}$  pin reaches the UVLO threshold of 4.5 V, the IC is enabled.

The  $V_{CC}$  regulator contains an internal diode connection to the BST pin to replenish the charge in the gate drive boot capacitor when SW pin is low.

At high input voltages, the power dissipated in the high-voltage regulator is significant and can limit the overall achievable output power. As an example, with the input at 48 V and switching at high frequency, the  $V_{CC}$  regulator can supply up to 7 mA of current resulting in  $48 V \times 7 mA = 336 mW$  of power dissipation. If the  $V_{CC}$  voltage is driven externally by an alternate voltage source, between 8.55 V and 13 V, the internal regulator is disabled. This reduces the power dissipation in the IC.

### 7.3.3 Regulation Comparator

The feedback voltage at FB is compared to an internal 1.225 V reference. In normal operation, when the output voltage is in regulation, an on-time period is initiated when the voltage at FB falls below 1.225 V. The high-side switch stays on for the on-time, causing the FB voltage to rise above 1.225 V. After the on-time period, the high-side switch stays off until the FB voltage again falls below 1.225 V. During start-up, the FB voltage is below 1.225

V at the end of each on-time, causing the high-side switch to turn on immediately after the minimum forced off-time of 144 ns. The high-side switch can be turned off before the on-time is over if the peak current in the inductor reaches the current limit threshold.

### 7.3.4 Overvoltage Comparator

The feedback voltage at FB is compared to an internal 1.62-V reference. If the voltage at FB rises above 1.62 V, the on-time pulse is immediately terminated. This condition can occur if the input voltage, the output load, or both, changes suddenly. The high-side switch does not turn on again until the voltage at FB falls below 1.225 V.

### 7.3.5 On-Time Generator

The on-time for the LM25019 device is determined by the  $R_{ON}$  resistor, and is inversely proportional to the input voltage ( $V_{IN}$ ), resulting in a nearly constant frequency as  $V_{IN}$  is varied over its range. The on-time equation for the LM25019 device is shown in [方程式 3](#).

$$T_{ON} = \frac{10^{-10} \times R_{ON}}{V_{IN}} \quad (3)$$

See [图 6-5](#).  $R_{ON}$  must be selected for a minimum on-time (at maximum  $V_{IN}$ ) greater than 100 ns, for proper operation. This requirement limits the maximum switching frequency for high  $V_{IN}$ .

### 7.3.6 Current Limit

The LM25019 device contains an intelligent current limit off-timer. If the current in the buck switch exceeds 240 mA, the present cycle is immediately terminated, and a nonresetable off-timer is initiated. The length of off-time is controlled by the FB voltage and the input voltage  $V_{IN}$ . As an example, when  $FB = 0$  V and  $V_{IN} = 48$  V, the maximum off-time is set to 16  $\mu$ s. This condition occurs when the output is shorted, and during the initial part of start-up. This amount of time ensures safe short circuit operation up to the maximum input voltage of 48 V.

In cases of overload where the FB voltage is above zero volts (not a short circuit), the current limit off-time is reduced. Reducing the off-time during less severe overloads reduces the amount of foldback, recovery time, and start-up time. The off-time is calculated from [方程式 4](#).

$$T_{OFF(ILIM)} = \frac{0.07 \times V_{IN}}{V_{FB} + 0.2V} \mu s \quad (4)$$

The current limit protection feature is peak limited. The maximum average output is less than the peak.

### 7.3.7 N-Channel Buck Switch and Driver

The LM25019 device integrates an N-Channel Buck switch and associated floating high-voltage gate driver. The gate driver circuit works in conjunction with an external bootstrap capacitor and an internal high-voltage diode. A 0.01- $\mu$ F ceramic capacitor connected between the BST pin and the SW pin provides the voltage to the driver during the on-time. During each off-time, the SW pin is at approximately 0 V, and the bootstrap capacitor charges from  $V_{CC}$  through the internal diode. The minimum off-timer, set to 144 ns, ensures a minimum time each cycle to recharge the bootstrap capacitor.

### 7.3.8 Synchronous Rectifier

The LM25019 device provides an internal synchronous N-channel MOSFET rectifier. This MOSFET provides a path for the inductor current to flow when the high-side MOSFET is turned off.

The synchronous rectifier has no diode emulation mode, and is designed to keep the regulator in continuous conduction mode even during light loads which would otherwise result in discontinuous operation.

### 7.3.9 Undervoltage Detector

The LM25019 device contains a dual-level UVLO circuit. A summary of threshold voltages and operational states is provided in the [§ 7.4](#). When the UVLO pin voltage is below 0.66 V, the controller is in a low-current shutdown mode. When the UVLO pin voltage is greater than 0.66 V but less than 1.225 V, the controller is in standby mode. In standby mode, the  $V_{CC}$  bias regulator is active while the regulator output is disabled. When the  $V_{CC}$  pin exceeds the  $V_{CC}$  undervoltage threshold and the UVLO pin voltage is greater than 1.225 V, normal operation begins. An external set-point voltage divider from  $V_{IN}$  to GND can be used to set the minimum operating voltage of the regulator.

UVLO hysteresis is accomplished with an internal 20- $\mu$ A current source that is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current source is activated to quickly raise the voltage at the UVLO pin. The hysteresis is equal to the value of this current times the resistance  $R_{UV2}$ .

If the UVLO pin is wired directly to the  $V_{IN}$  pin, the regulator begins operation once the  $V_{CC}$  undervoltage is satisfied.

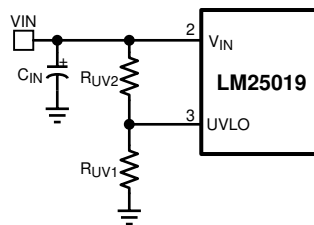


图 7-3. UVLO Resistor Setting

### 7.3.10 Thermal Protection

The LM25019 device must be operated so the junction temperature does not exceed 150°C during normal operation. An internal Thermal Shutdown circuit is provided to protect the LM25019 in the event of a higher than normal junction temperature. When activated, typically at 165°C, the controller is forced into a low-power reset state, disabling the buck switch and the  $V_{CC}$  regulator. This feature prevents catastrophic failures from accidental device overheating. When the junction temperature reduces below 145°C (typical hysteresis = 20°C), the  $V_{CC}$  regulator is enabled, and normal operation is resumed.

### 7.3.11 Ripple Configuration

The LM25019 uses Constant-On-Time (COT) control scheme where the on-time is terminated by an on-timer, and the off-time is terminated by the feedback voltage ( $V_{FB}$ ) falling below the reference voltage ( $V_{REF}$ ). Therefore, for stable operation, the feedback voltage must decrease monotonically, in phase with the inductor current during the off-time. Furthermore, this change in feedback voltage ( $V_{FB}$ ) during off-time must be large enough to suppress any noise component present at the feedback node.

表 7-1 shows three different methods for generating appropriate voltage ripple at the feedback node. Type 1 and Type 2 ripple circuits couple the ripple at the output of the converter to the feedback node (FB). The output voltage ripple has two components:

1. Capacitive ripple caused by the inductor current ripple charging/discharging the output capacitor.
2. Resistive ripple caused by the inductor current ripple flowing through the ESR of the output capacitor.

The capacitive ripple is not in phase with the inductor current. As a result, the capacitive ripple does not decrease monotonically during the off-time. The resistive ripple is in phase with the inductor current and decreases monotonically during the off-time. The resistive ripple must exceed the capacitive ripple at the output node ( $V_{OUT}$ ) for stable operation. If this condition is not satisfied, unstable switching behavior is observed in COT converters, with multiple on-time bursts in close succession followed by a long off-time.

Type 3 ripple method uses  $R_r$  and  $C_r$  and the switch node (SW) voltage to generate a triangular ramp. This triangular ramp is ac coupled using  $C_{ac}$  to the feedback node (FB). Because this circuit does not use the output voltage ripple, it is ideally suited for applications where low output voltage ripple is required. See the [AN-1481 Controlling Output Ripple and Achieving ESR Independence in Constant On-Time \(COT\) Regulator Designs Application Report](#) for more details for each ripple generation method.

表 7-1. Ripple Configurations

TYPE 1 LOWEST COST CONFIGURATION	TYPE 2 REDUCED RIPPLE CONFIGURATION	TYPE 3 MINIMUM RIPPLE CONFIGURATION
$R_C \geq \frac{25 \text{ mV}}{\Delta I_{L(\text{MIN})}} \times \frac{V_{OUT}}{V_{REF}} \quad (5)$	$C \geq \frac{5}{f_{sw} (R_{FB2}    R_{FB1})}$ $R_C \geq \frac{25 \text{ mV}}{\Delta I_{L(\text{MIN})}} \quad (6)$	$C_r = 3300 \text{ pF}$ $C_{ac} = 100 \text{ nF}$ $R_r C_r \leq \frac{(V_{IN(\text{MIN})} - V_{OUT}) \times T_{ON}}{25 \text{ mV}} \quad (7)$

### 7.3.12 Soft Start

A soft-start feature can be implemented with the LM25019 device using an external circuit. As shown in 图 7-4, the soft-start circuit consists of one capacitor  $C_1$ , two resistors,  $R_1$  and  $R_2$ , and a diode, D. During the initial start-up, the VCC voltage is established before the  $V_{OUT}$  voltage. Capacitor  $C_1$  is discharged and D is thereby forward biased. The FB voltage is pulled up above the reference voltage (1.225 V) and switching is thereby disabled. As capacitor  $C_1$  charges, the voltage at node B gradually decreases and switching commences.  $V_{OUT}$  gradually rises to maintain the FB voltage at the reference voltage. Once the voltage at node B is less than a diode drop above the FB voltage, the soft-start sequence is finished and D is reverse-biased.

During the initial part of the start-up, the FB voltage can be approximated as shown in 方程式 8.

$$V_{FB} = (V_{CC} - V_D) \times \frac{R_{FB1} \times R_{FB2}}{R_2 \times (R_{FB1} + R_{FB2}) + R_{FB1} \times R_{FB2}} \quad (8)$$

$C_1$  is charged after the first start-up. Diode D1 is optional and can be added to discharge  $C_1$  and initialize the soft-start sequence when the input voltage experiences a momentary drop.

To achieve the desired soft start, the following design guidance is recommended:

1.  $R_2$  is selected so that  $V_{FB}$  is higher than 1.225 V for a  $V_{CC}$  of 4.5 V, but is lower than 5 V when  $V_{CC}$  is 8.55 V. If an external  $V_{CC}$  is used,  $V_{FB}$  must not exceed 5 V at maximum  $V_{CC}$ .
2.  $C_1$  is selected to achieve the desired start-up time that can be determined from 方程式 9.

$$t_S = C_1 \times \left( R_2 + \frac{R_{FB1} \times R_{FB2}}{R_{FB1} + R_{FB2}} \right) \quad (9)$$

3.  $R_1$  is used to maintain the node B voltage at zero after the soft start is finished. A value larger than the feedback resistor divider is preferred. The effect of resistor  $R_1$  is ignored in 方程式 9.

With component values from the applications schematic shown in 图 8-1, selecting  $C_1 = 1 \mu\text{F}$ ,  $R_2 = 1 \text{ k}\Omega$ , and  $R_1 = 30 \text{ k}\Omega$  results in a soft-start time of about 2 ms.

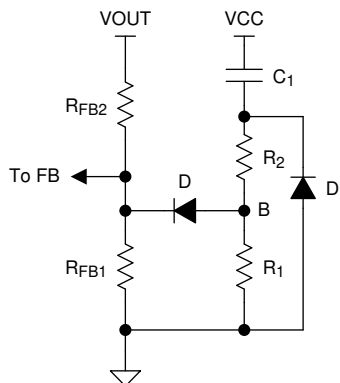


图 7-4. Soft-Start Circuit

## 7.4 Device Functional Modes

The UVLO pin controls the operating mode of the LM25019 device (see 表 7-2 for the detailed functional states).

表 7-2. UVLO Mode

UVLO	V <sub>CC</sub>	MODE	DESCRIPTION
< 0.66 V	Disabled	Shutdown	V <sub>CC</sub> regulator disabled. Switching disabled
0.66 V - 1.225 V	Enabled	Standby	V <sub>CC</sub> regulator enabled Switching disabled
> 1.225 V	V <sub>CC</sub> < 4.5 V	Standby	V <sub>CC</sub> regulator enabled. Switching disabled
	V <sub>CC</sub> > 4.5 V	Operating	V <sub>CC</sub> enabled. Switching enabled

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

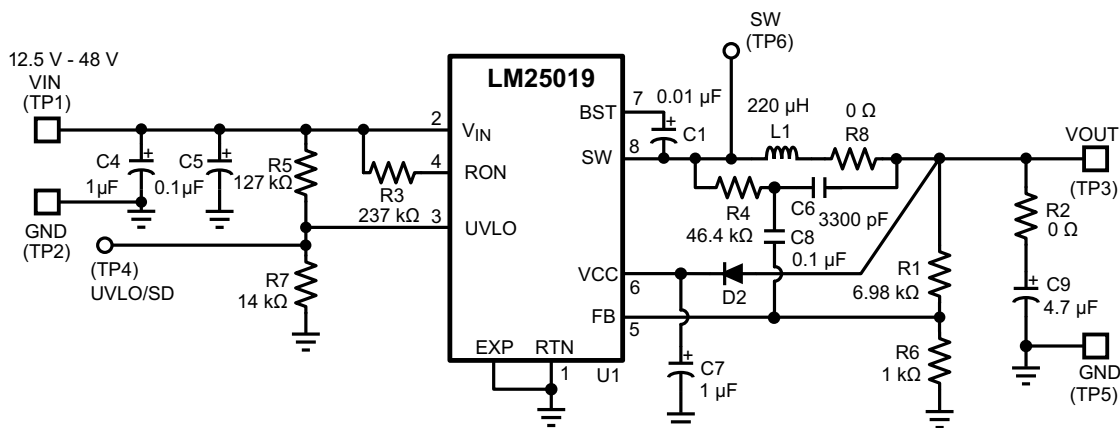
## 8.1 Application Information

The LM25019 device is step-down DC-DC converter. The device is typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 650 mA. Use the following design procedure to select component values for the LM25019 device. Alternately, use the WEBENCH® software to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

## 8.2 Typical Application

The application schematic of a buck supply is shown in 图 8-1. For output voltage ( $V_{OUT}$ ) more than one diode drop higher than the maximum regulation voltage of  $V_{CC}$  (8.55 V, see the 节 6.5), the  $V_{CC}$  pin can be connected to  $V_{OUT}$  through a diode (D2), as shown in 图 8-1, to improve efficiency and reduce power dissipation in the IC.

The design example shown in 图 8-1 uses equations from the 节 7.3 with component names provided in the 图 3-1 schematic. Corresponding component designators from 图 8-1 are also provided for each selected value.



**图 8-1. Final Schematic for 12.5-V to 48-V Input, and 10-V, 100-mA Output Buck Converter**

### 8.2.1 Design Requirements

DESIGN PARAMETERS	VALUE
Input Range	12.5 V to 48 V
Output Voltage	10 V
Maximum Output Current	100 mA
Nominal Switching Frequency	≈ 440 kHz



## 8.2.2 Detailed Design Procedure

### 8.2.2.1 RFB1, RFB2

$V_{OUT} = V_{FB} \times (R_{FB2} / R_{FB1} + 1)$ , and because  $V_{FB} = 1.225$  V, the ratio of  $R_{FB2}$  to  $R_{FB1}$  calculates as 7:1. Standard values are chosen with  $R_{FB2} = R1 = 6.98$  k $\Omega$  and  $R_{FB1} = R6 = 1.00$  k $\Omega$ . Other values can be used as long as the 7:1 ratio is maintained.

### 8.2.2.2 Frequency Selection

At the minimum input voltage, the maximum switching frequency of the LM25019 is restricted by the forced minimum off-time ( $T_{OFF(MIN)}$ ) as shown in [方程式 10](#).

$$f_{SW(MAX)} = \frac{1 - D_{MAX}}{T_{OFF(MIN)}} = \frac{1 - 10/12.5}{200 \text{ ns}} = 1 \text{ MHz} \quad (10)$$

Similarly, at maximum input voltage, the maximum switching frequency of the LM25019 is restricted by the minimum  $T_{ON}$  as shown in [方程式 11](#).

$$f_{SW(MAX)} = \frac{D_{MIN}}{T_{ON(MIN)}} = \frac{10/48}{100 \text{ ns}} = 2.1 \text{ MHz} \quad (11)$$

Resistor  $R_{ON}$  sets the nominal switching frequency based on [方程式 12](#).

$$f_{SW} = \frac{V_{OUT}}{K \times R_{ON}} \quad (12)$$

where

- $K = 9 \times 10^{-11}$

Operation at high switching frequency results in lower efficiency while providing the smallest solution. Using 440 kHz as the target switching frequency, the calculated value of  $R_{ON}$  is 253 k $\Omega$ . The standard value for  $R_{ON} = R3 = 237$  k $\Omega$  is selected.

### 8.2.2.3 Inductor Selection

The inductance selection is a compromise between solution size, output ripple, and efficiency. The peak inductor current at maximum load current must be smaller than the minimum current limit of 150 mA. The maximum permissible peak to peak inductor ripple is determined by [方程式 13](#).

$$\Delta I_L = 2 \times (I_{LIM(min)} - I_{OUT(max)}) = 2 \times 50 = 100 \text{ mA} \quad (13)$$

The minimum inductance is determined by [方程式 14](#).

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \quad (14)$$

Using the maximum  $V_{IN}$  of 48 V, the calculation from [方程式 14](#) results in  $L = 179 \mu\text{H}$ . A standard value of 220  $\mu\text{H}$  is selected. For proper operation, the inductor saturation current must be higher than the peak current encountered in the application. For robust short circuit protection, the inductor saturation current must be higher than the maximum current limit of 300 mA.

### 8.2.2.4 Output Capacitor

The output capacitor is selected to minimize the capacitive ripple across it. The maximum ripple is observed at maximum input voltage and is shown in [方程式 15](#).

$$C_{OUT} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{ripple}} \quad (15)$$

where

- $\Delta V_{\text{ripple}}$  is the voltage ripple across the capacitor
- $\Delta I_L$  is calculated using [方程式 14](#)

Substituting  $\Delta V_{\text{ripple}} = 5 \text{ mV}$  gives  $C_{\text{OUT}} = 4.65 \text{ } \mu\text{F}$ . A 4.7- $\mu\text{F}$  standard value is selected for  $C_{\text{OUT}} = \text{C9}$ . An X5R or X7R type capacitor with a voltage rating 16 V or higher must be selected.

### 8.2.2.5 Type III Ripple Circuit

Type III ripple circuit as described in the [节 7.3.11](#) section is chosen for this example. For a constant on-time converter to be stable, the injected in-phase ripple must be larger than the capacitive ripple on  $C_{\text{OUT}}$ .

Using type III ripple circuit equations, the target ripple must be greater than the capacitive ripple generated at the primary output.

$$C_r = C6 = 3300 \text{ pF}$$

$$C_{\text{ac}} = C8 = 100 \text{ nF}$$

$$R_r \leq \frac{(V_{\text{IN(MIN)}} - V_{\text{OUT}}) \times T_{\text{ON(VINMIN)}}}{(25 \text{ mV} \times C_r)} \quad (16)$$

For  $T_{\text{ON}}$ , refer to [方程式 3](#).

Ripple resistor  $R_r$  is calculated to be 57.6 k $\Omega$ . This value provides the minimum ripple for stable operation. A smaller resistance should be selected to allow for variations in  $T_{\text{ON}}$ ,  $C_{\text{OUT}}$ , and other components.  $R_r = R4 = 46.4 \text{ k}\Omega$  is selected for this example application.

### 8.2.2.6 $V_{\text{CC}}$ and Bootstrap Capacitor

The  $V_{\text{CC}}$  capacitor provides charge to bootstrap capacitor as well as internal circuitry and low-side gate driver. The bootstrap capacitor provides charge to high-side gate driver. The recommended value for  $C_{V_{\text{CC}}} = C7$  is 1- $\mu\text{F}$ . A good value for  $C_{\text{BST}} = C1$  is 0.01  $\mu\text{F}$ .

### 8.2.2.7 Input Capacitor

The input capacitor should be large enough to limit the input voltage ripple and can be calculated using [方程式 17](#).

$$C_{\text{IN}} \geq \frac{I_{\text{OUT(MAX)}}}{4 \times f_{\text{SW}} \times \Delta V_{\text{IN}}} \quad (17)$$

Choosing a  $\Delta V_{\text{IN}} = 0.5 \text{ V}$  gives a minimum  $C_{\text{IN}} = 0.12 \text{ } \mu\text{F}$ . A standard value of 1  $\mu\text{F}$  is selected for  $C_{\text{IN}} = C4$ . The input capacitor should be rated for the maximum input voltage under all conditions. A 50-V, X7R dielectric should be selected for this design.

The input capacitor should be placed directly across  $V_{\text{IN}}$  and RTN (pin 2 and 1) of the IC. If it is not possible to place all of the input capacitor close to the IC, a 0.1- $\mu\text{F}$  capacitor should be placed near the IC to provide a bypass path for the high-frequency component of the switching current. This helps limit the switching noise.

### 8.2.2.8 UVLO Resistors

The UVLO resistors  $R_{\text{UV1}}$  and  $R_{\text{UV2}}$  set the UVLO threshold and hysteresis according to [方程式 18](#) and [方程式 19](#).

$$V_{\text{IN(HYS)}} = I_{\text{HYS}} \times R_{\text{UV2}} \quad (18)$$

$$V_{\text{IN( UVLO, rising)}} = 1.225 \text{ V} \times \left( \frac{R_{\text{UV2}}}{R_{\text{UV1}}} + 1 \right) \quad (19)$$

where

- $I_{HYS} = 20 \mu A$

Selecting UVLO hysteresis of 2.5 V and UVLO rising threshold of 12 V results in  $R_{UV1} = 14.53 k\Omega$  and  $R_{UV2} = 125 k\Omega$ . Selecting a standard value of  $R_{UV1} = R7 = 14 k\Omega$  and  $R_{UV2} = R5 = 127 k\Omega$  results in UVLO thresholds and hysteresis of 12.5 V to 2.5 V, respectively.

### 8.2.3 Application Curves

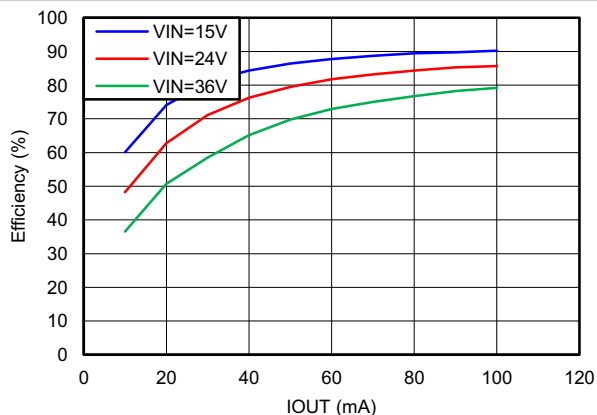


图 8-2. Efficiency versus Load Current

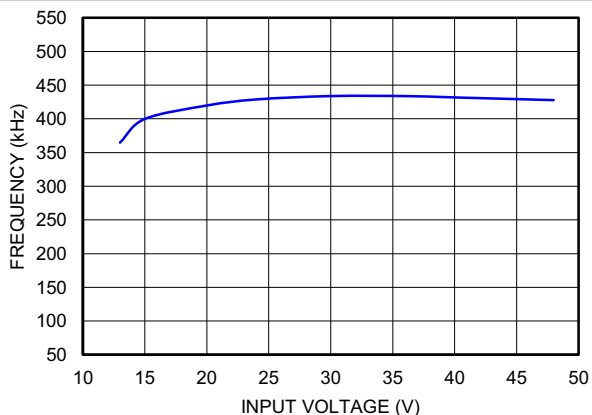


图 8-3. Frequency versus Input Voltage ( $I_{OUT} = 100 mA$ )

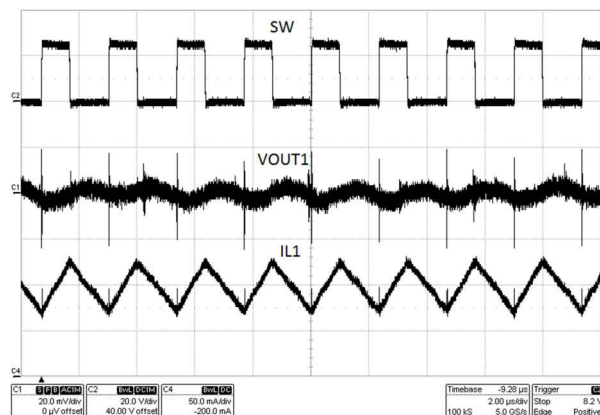


图 8-4. Typical Switching Waveform ( $V_{IN} = 24 V$ ,  $I_{OUT} = 100 mA$ )

## 9 Power Supply Recommendations

The LM25019 is a power-management device. The power supply for the device is any DC voltage source within the specified input range.

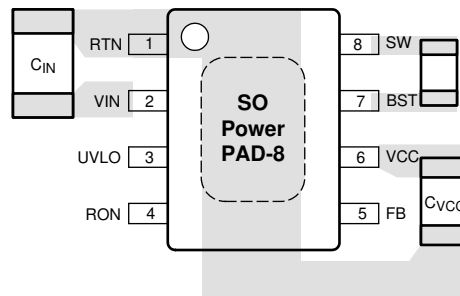
## 10 Layout

### 10.1 Layout Guidelines

A proper layout is essential for optimum performance of the circuit. In particular, the following guidelines should be observed:

1.  $C_{IN}$ : The loop consisting of input capacitor ( $C_{IN}$ ),  $V_{IN}$  pin, and RTN pin carries switching currents. Therefore, the input capacitor must be placed close to the IC, directly across  $V_{IN}$  and RTN pins and the connections to these two pins should be direct to minimize the loop area. In general it is not possible to accommodate all of input capacitance near the IC. A good practice is to use a 0.1-  $\mu$ F or 0.47-  $\mu$ F capacitor directly across the  $V_{IN}$  and RTN pins close to the IC, and the remaining bulk capacitor as close as possible (see [图 10-1](#)).
2.  $C_{VCC}$  and  $C_{BST}$ : The  $V_{CC}$  and bootstrap (BST) bypass capacitors supply switching currents to the high-side and low-side gate drivers. These two capacitors must also be placed as close to the IC as possible, and the connecting trace length and loop area should be minimized (see [图 10-1](#)).
3. The feedback trace carries the output voltage information and a small ripple component that is necessary for proper operation of the LM25019. Therefore, take care while routing the feedback trace to avoid coupling any noise to this pin. In particular, feedback trace must not run close to magnetic components, or parallel to any other switching trace.
4. SW trace: The SW node switches rapidly between  $V_{IN}$  and GND every cycle is therefore a possible source of noise. The SW node area should be minimized. In particular, the SW node must not be inadvertently connected to a copper plane or pour.

### 10.2 Layout Example



**图 10-1. Placement of Bypass Capacitors**

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

- Texas Instruments, [AN-1481 Controlling Output Ripple and Achieving ESR Independence in Constant On-Time \(COT\) Regulator Designs](#)
- Texas Instruments, [AN-2292 Designing an Isolated Buck \(Flyback\) Converter](#)
- Texas Instruments, [LM25019 Isolated Evaluation Board](#)

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#### 11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM25019MR/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L25019 MR	<a href="#">Samples</a>
LM25019MRE/NOPB	ACTIVE	SO PowerPAD	DDA	8	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L25019 MR	<a href="#">Samples</a>
LM25019MRX/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L25019 MR	<a href="#">Samples</a>
LM25019SD/NOPB	ACTIVE	WSO	NGU	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L25019	<a href="#">Samples</a>
LM25019SDE/NOPB	ACTIVE	WSO	NGU	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L25019	<a href="#">Samples</a>
LM25019SDX/NOPB	ACTIVE	WSO	NGU	8	4500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L25019	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM25019MRE/NOPB	SO PowerPAD	DDA	8	250	178.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM25019MRX/NOPB	SO PowerPAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM25019SD/NOPB	WSO	NGU	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM25019SDE/NOPB	WSO	NGU	8	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM25019SDX/NOPB	WSO	NGU	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM25019MRE/NOPB	SO PowerPAD	DDA	8	250	208.0	191.0	35.0
LM25019MRX/NOPB	SO PowerPAD	DDA	8	2500	356.0	356.0	36.0
LM25019SD/NOPB	WSON	NGU	8	1000	210.0	185.0	35.0
LM25019SDE/NOPB	WSON	NGU	8	250	210.0	185.0	35.0
LM25019SDX/NOPB	WSON	NGU	8	4500	367.0	367.0	35.0

## TUBE



\*All dimensions are nominal

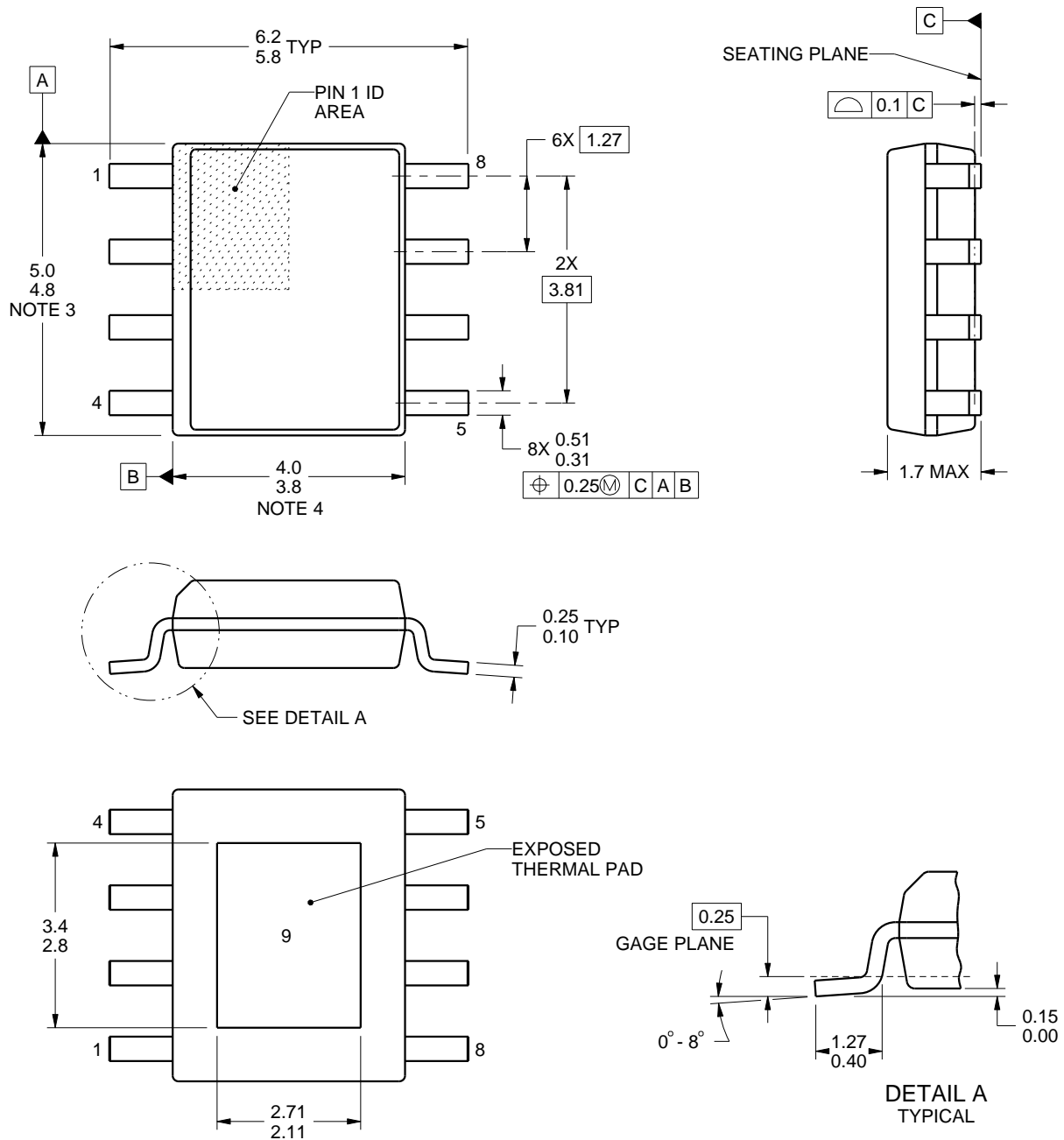
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LM25019MR/NOPB	DDA	HSOIC	8	95	495	8	4064	3.05

**DDA0008B**

# PACKAGE OUTLINE

## PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



4214849/A 08/2016

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

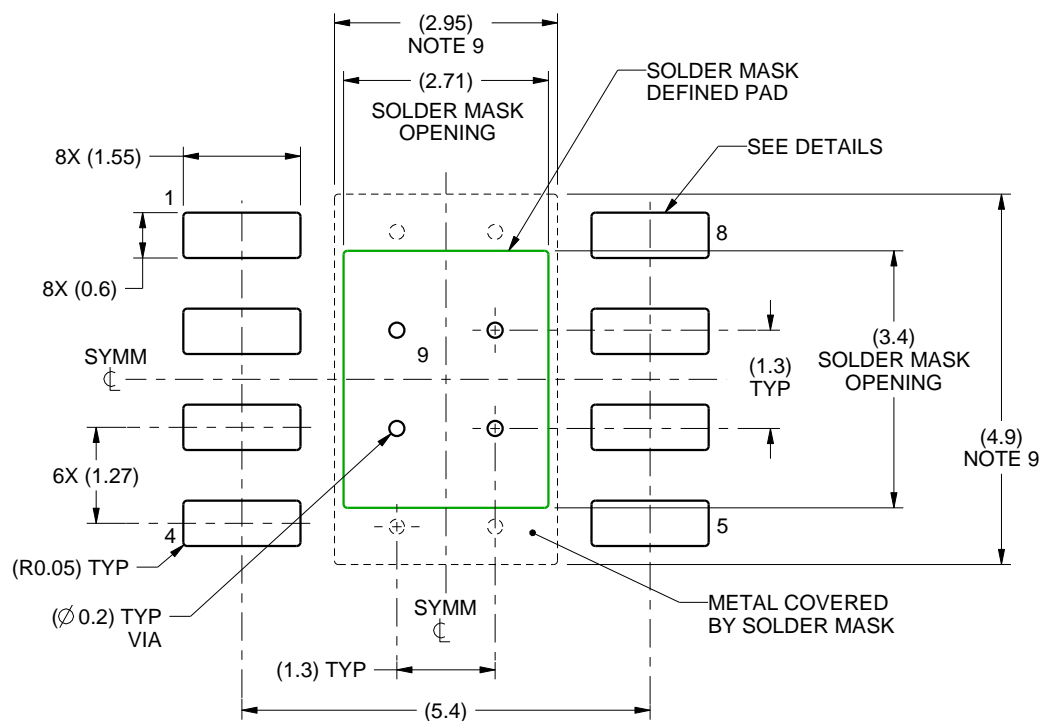
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.

# EXAMPLE BOARD LAYOUT

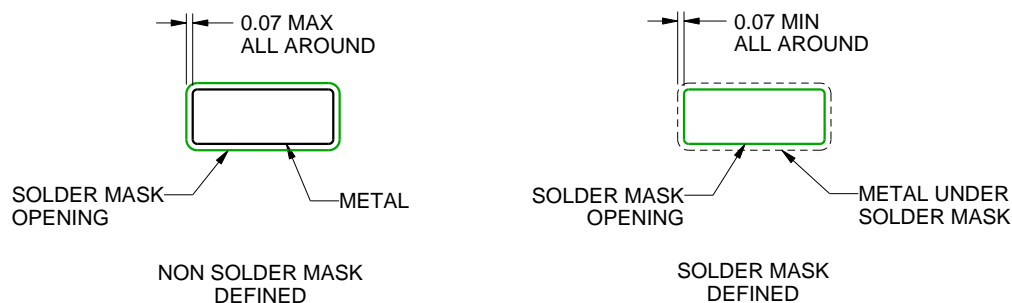
DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
EXPOSED PAD  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



**WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



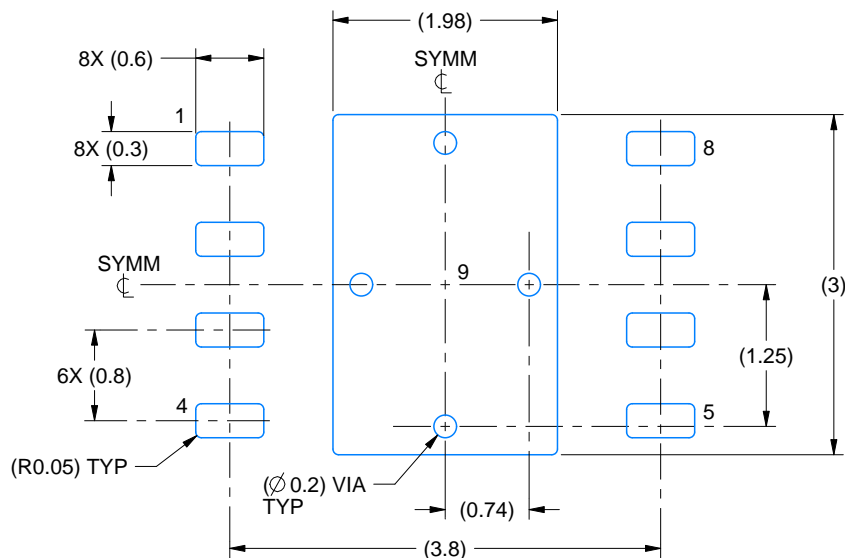
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



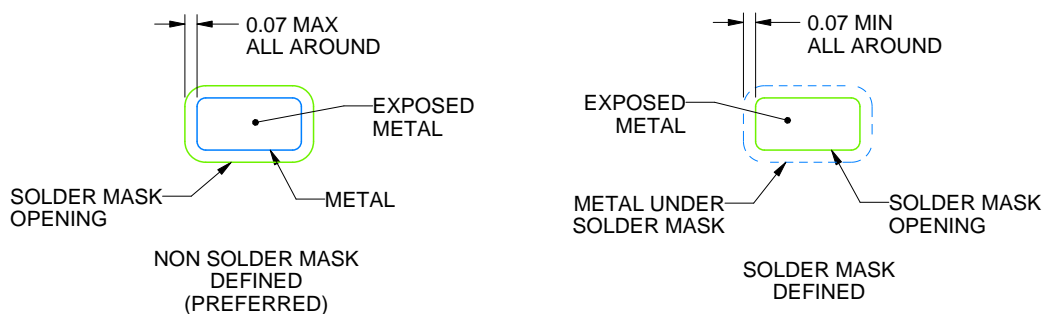
**NGU0008B**

**WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



## SOLDER MASK DETAILS

4214936/A 12/2023

NOTES: (continued)

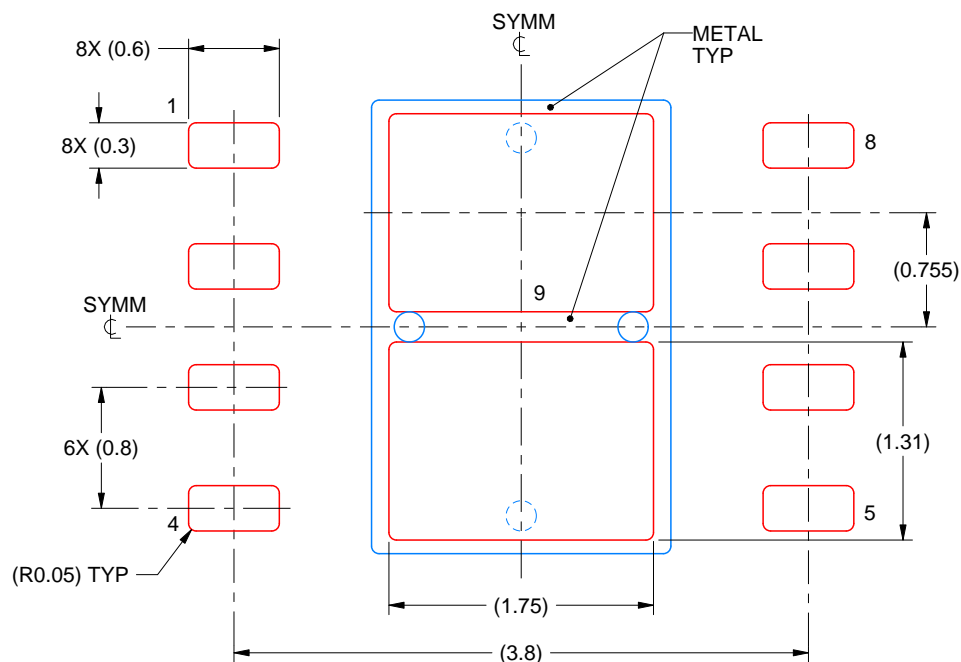
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

NGU0008B

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:  
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

4214936/A 12/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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