SN75ALS174A 四路差分线路驱动器

1 特性

- 符合或超出 ANSI EIA/TIA-422-B 和 RS-485 的要求
- 高速高级低功耗肖特基电路
- 专为在串行和并行应用中达到 20Mbit/s 的运行速度而设计
- 适用于嘈杂环境中长总线上的多点传输
- 低电源电流，最高 55mA
- 宽正负输入/输出总线电压范围
- 驱动器输出容量：60mA
- 热关断保护
- 驱动器正负电流限制
- 与 SN75174 在功能上可以互换

2 应用

- 电机驱动器
- 工厂自动化和控制

3 说明

SN75ALS174A 是一款具有三态差分输出的四路线路驱动器，设计可满足 ANSI 标准 EIA/TIA-422-B 和 RS-485 的要求。该器件经优化，能够以高达 20Mbit/s 的速率实现平衡多点总线传输。

每个驱动器都具有宽的正负共模输出电压范围，因此适用于嘈杂环境中的合用线应用。

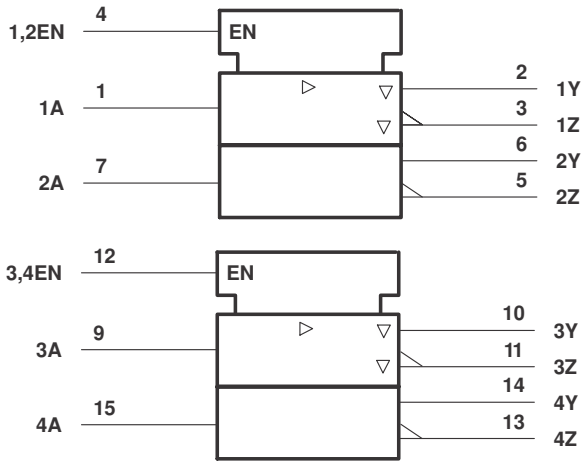
SN75ALS174A 可提供正负电流限制和热关断功能，避免传输总线出现线路故障状况。在结温大概为 150°C 时发生关断。

SN75ALS174A 的工作温度范围是 0°C 至 70°C。

封装信息

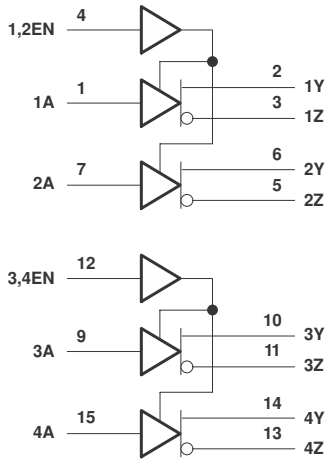
器件型号	封装(1)	封装尺寸(2)
SN75ALS174A	PDIP (N) (16)	19.3mm x 9.4mm
	SOIC (DW) (20)	12.8mm x 10.3mm
	TSSOP (PW) (20)	6.5mm x 6.4mm

(1) 有关更多信息，请参阅节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



A. 所示引脚编号适用于 N 封装。

逻辑符号 [1]



A. 所示引脚编号适用于 N 封装。

逻辑图（正逻辑）

[1] 此符号符合 ANSI/IEEE 标准 91-1984 和 IEC 出版物 617-12。

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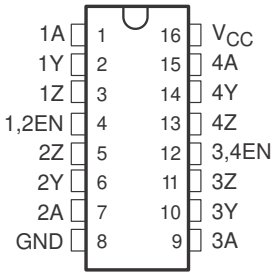
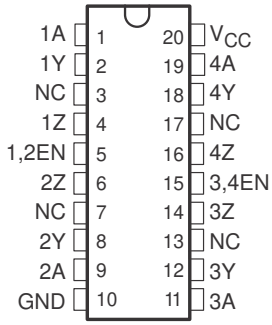
4 Pin Configuration and Functions



N Package (Top View)



NC – No internal connection

DW, PW Package (Top View)

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V_{CC} (2)	-0.5	7	V
Input voltage, V_I	-0.5	7	V
Output voltage range, V_O	–9	14	V
Continuous total dissipation	See the *Dissipation Rating* table		
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network GND.

5.2 Dissipation Rating Table

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	596 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		V_{cc}	V
V_{IL}	Low-level input voltage	0		0.8	V
V_{OC}	Common-mode output voltage	-7		12	V
I_{OH}	High-level output current	0		–60	mA
I_{OL}	Low-level output current	0		60	mA
T_A	Operating free-air temperature	0		70	°C

5.4 Thermal Information

THERMAL METRIC(1)		SN75ALS174A			UNIT
		N (PDIP)	DW (SOIC)	PW	
		16 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.6	66.8	107.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.1	34.4	38.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.6	39.7	53.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.5	8.9	3.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.3	39	53.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18mA				–1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω	See Note 图 6-1	1/2 V_{OD1} or 2(2)			V
		R_L = 54 Ω		1.5	2.5	5	V
$\|V_{OD3}\|$	Differential output voltage	See (5)		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage(3)	R_L = 54 Ω or 100 Ω	See 图 6-1			±0.2	V
V_{OC}	Common-mode output voltage(4)	R_L = 54 Ω or 100 Ω	See 图 6-1			3	V
						–1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(3)	R_L = 54 Ω or 100 Ω	See 图 6-1			±0.2	V
I_O	Output current with power off	V_{CC} = 0, V_O = –7V to 12V				±100	μA
I_{OZ}	High-impedance-state output current	V_O = –7V to 12V				±100	μA
I_{IH}	High-level input current	V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_I = 0.4V				–100	μA
I_{OS}	Short-circuit output current	V_O = –7V to 12V				±250	mA
I_{CC}	Supply current (all drivers)	No load	Outputs enabled		36	55	mA
			Outputs disabled		16	30	mA

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.
(2) The minimum V_{OD2} with a 100 Ω load is either 1/2V_{OD1} or 2V, whichever is greater.
(3) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(4) In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
(5) See EIA Standard RS-485, Figures 3-5, Test Termination Measurement 2.

5.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted), C_L = 50pF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω, See 图 6-2	9	15	22	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω, See 图 6-3	30	45	70	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω, See 图 6-4	25	40	65	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω, See 图 6-3	10	20	35	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, See 图 6-4	10	30	45	ns

6 Parameter Measurement Information

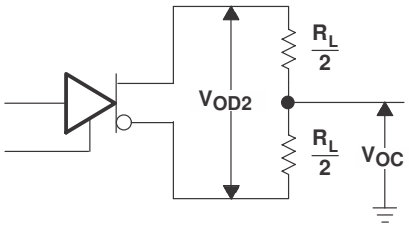
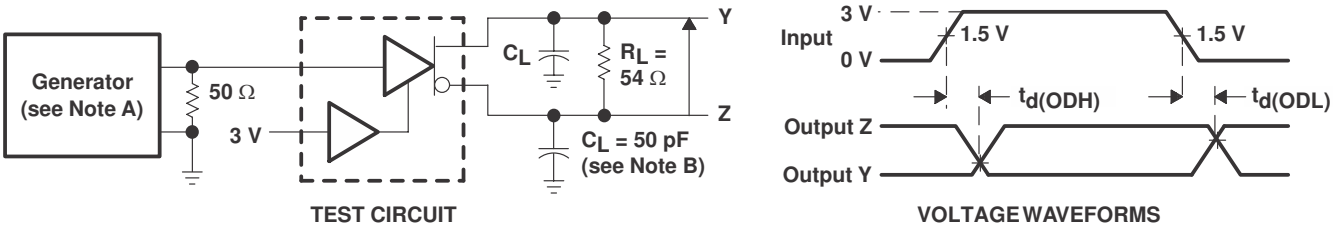
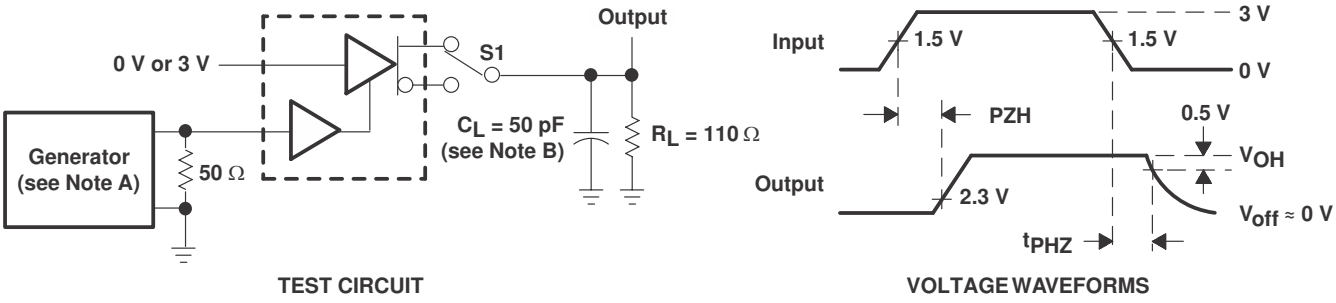


图 6-1. Differential and Common-Mode Output Voltages



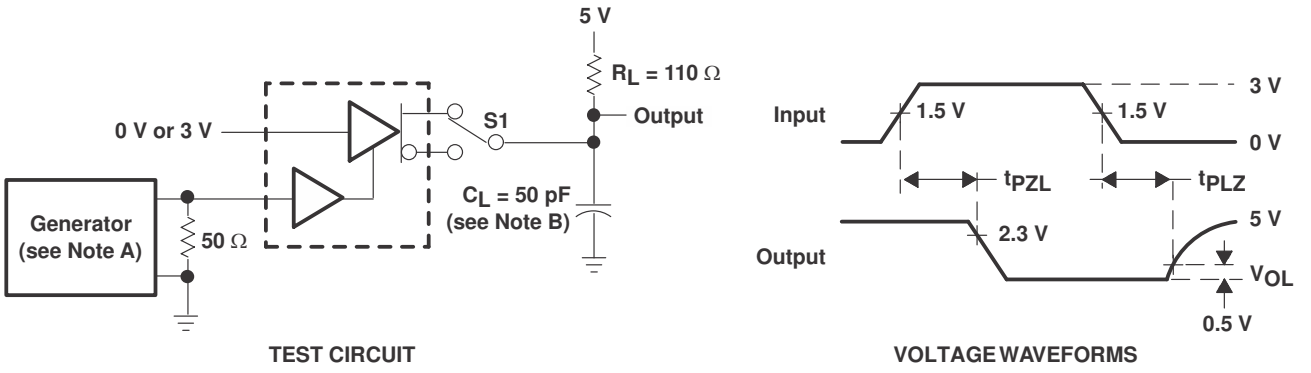
A. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, Z_O = 50 Ω, duty cycle = 50%, t_f 5ns, t_r 5ns.
B. C_L includes probe and stray capacitance.

图 6-2. Differential-Output Test Circuit and Delay and Transition Times Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, Z_O = 50 Ω, duty cycle = 50%, t_f 10ns, t_r 10ns.
B. C_L includes probe and stray capacitance.

图 6-3. Test Circuit and Voltage Waveforms, t_{PZH} and t_{PHZ}



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, Z_O = 50 Ω, duty cycle = 50%, t_f 5ns, t_r 5ns.
B. C_L includes probe and stray capacitance.

图 6-4. Test Circuit and Voltage Waveforms, t_{PZL} and t_{PLZ}

7 Detailed Description

7.1 Device Functional Modes

Function Table (each driver)

INPUT A(1) (2)	ENABLES	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant.
(2) Z = high impedance (off)

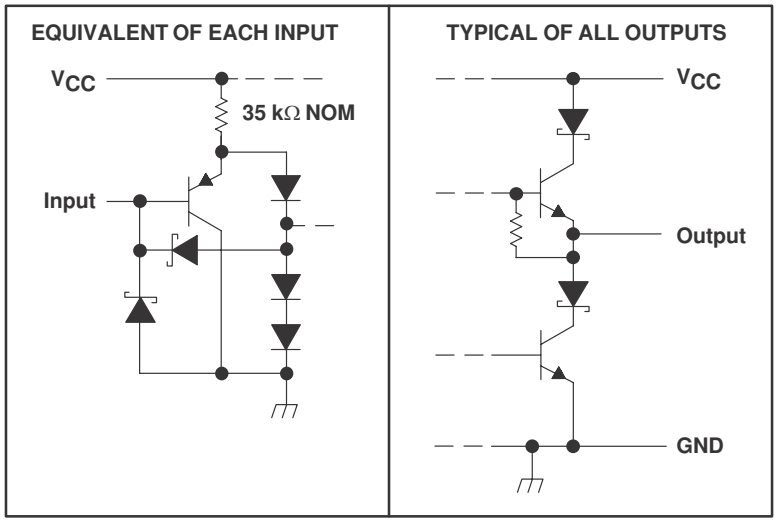


图 7-1. Schematics of Inputs and Outputs

8 Device and Documentation Support

8.1 Documentation Support

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision F (January 2018) to Revision G (January 2018)	Page
• 更改了整个文档中的表格、图和交叉参考的编号格式	1
• Added the *Thermal Information* table	4
• Changed Note A in 图 6-3	6

Changes from Revision E (April 1998) to Revision F (January 2018)	Page
• 添加了 PW 封装、*应用* 列表、*器件信息* 表、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75ALS174ADW	LIFEBUY	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS174A	
SN75ALS174ADWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS174A	Samples
SN75ALS174AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS174AN	Samples
SN75ALS174APWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS174A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

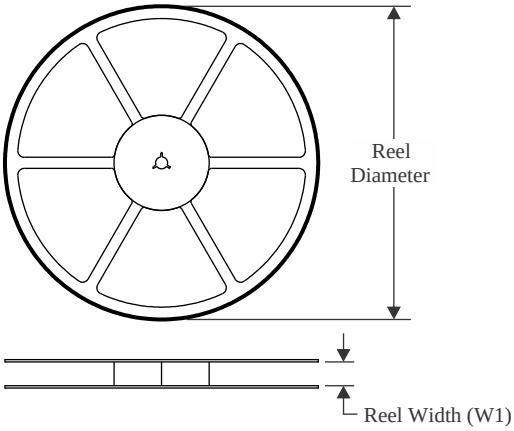
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

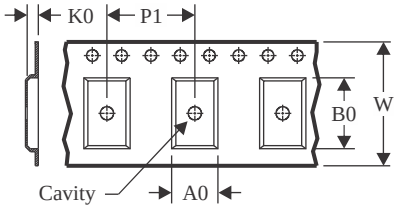
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

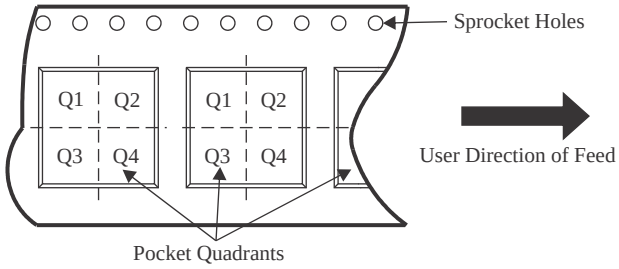


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

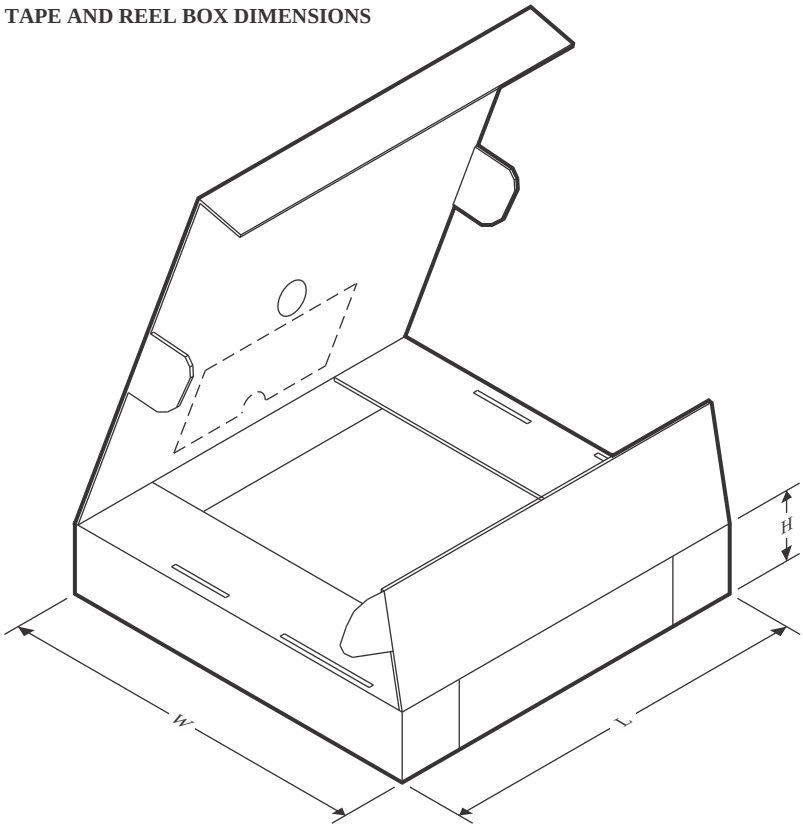
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS174ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN75ALS174APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

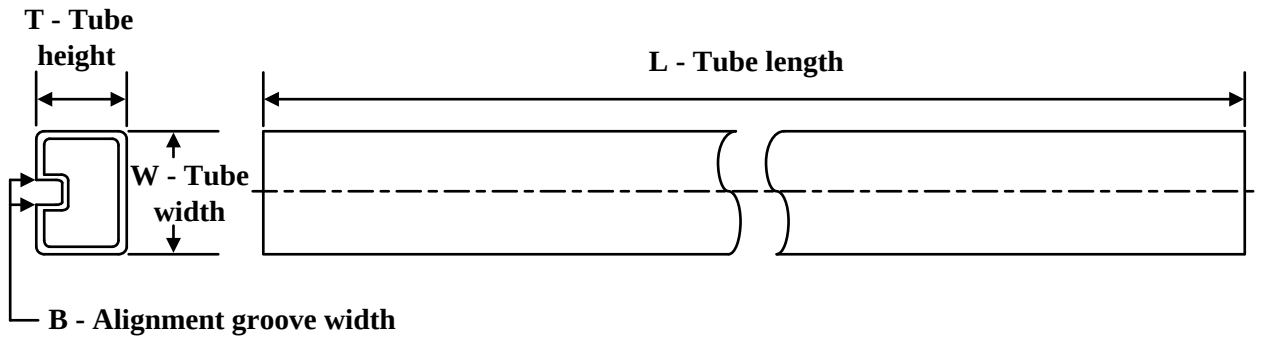
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS174ADWR	SOIC	DW	20	2000	350.0	350.0	43.0
SN75ALS174APWR	TSSOP	PW	20	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

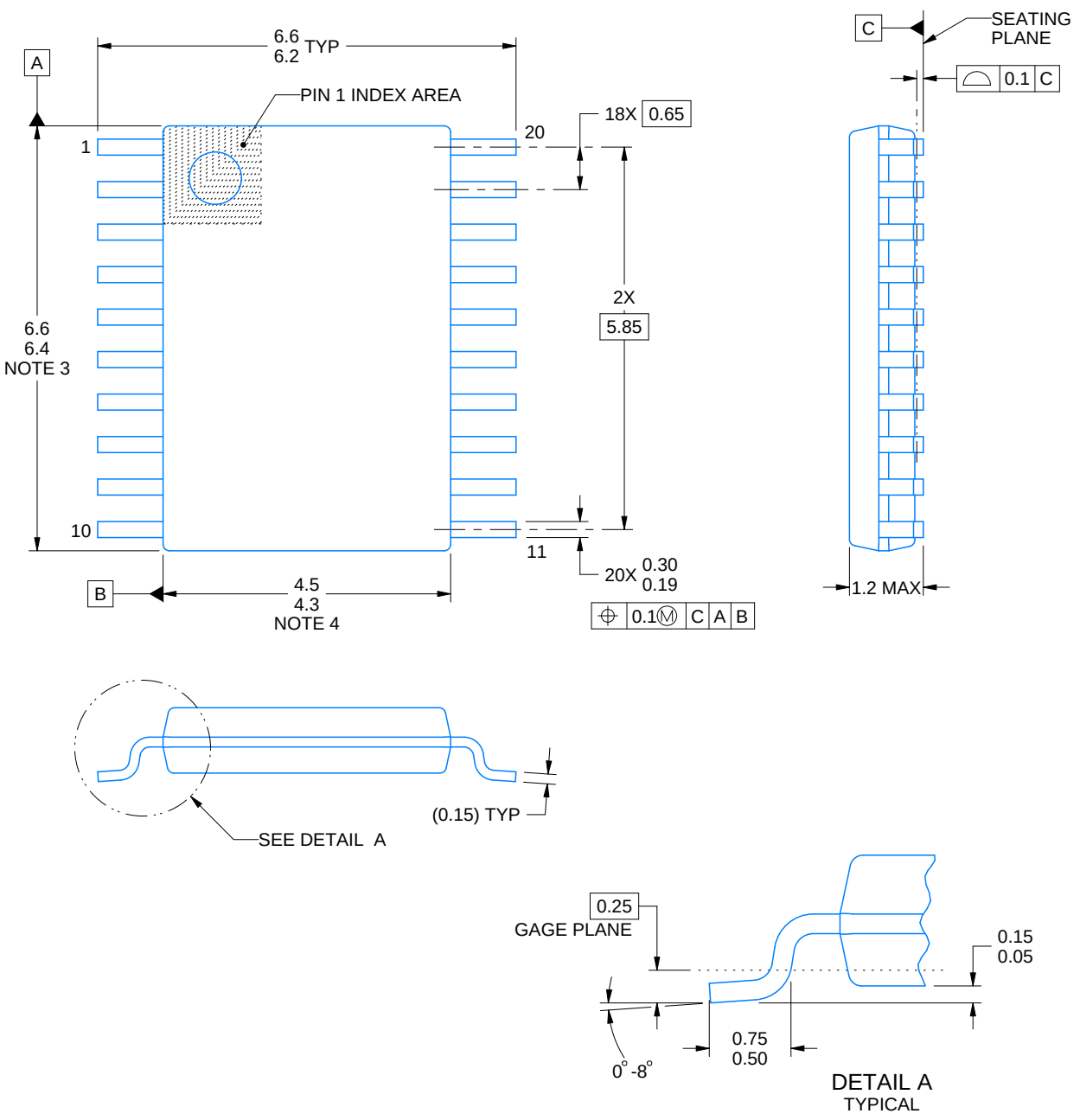
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75ALS174ADW	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN75ALS174AN	N	PDIP	16	25	506	13.97	11230	4.32

PACKAGE OUTLINE

PW0020A

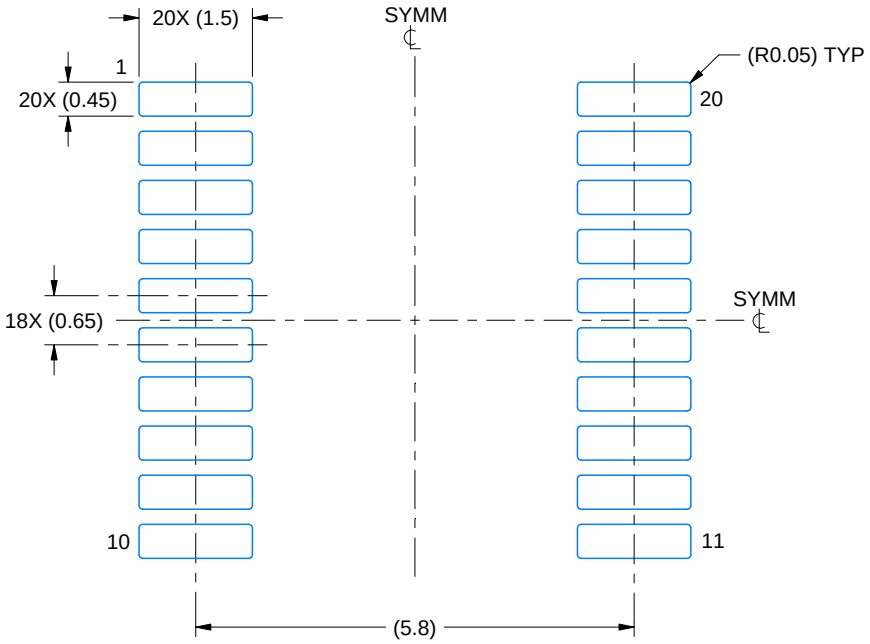
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



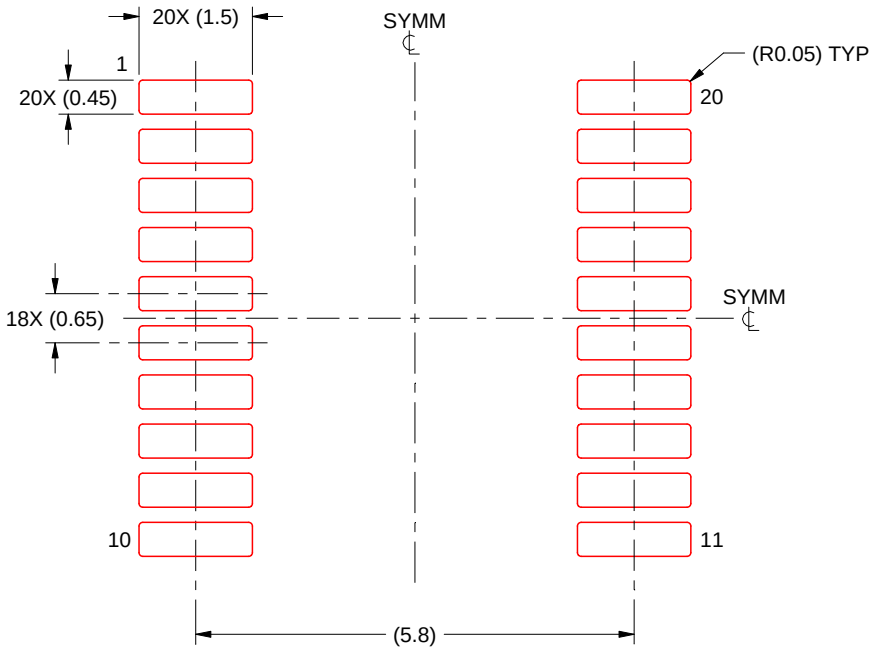
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



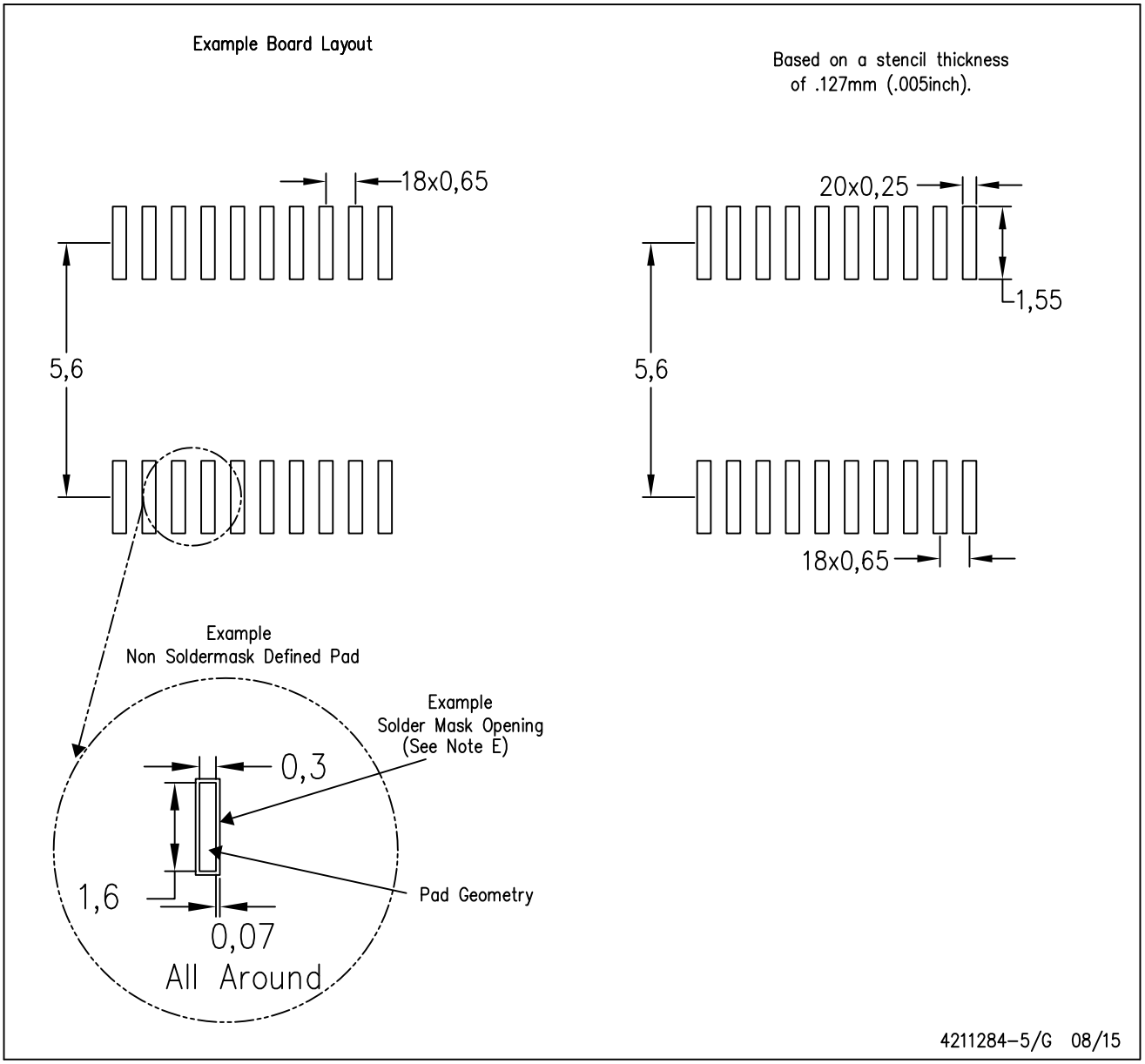
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE

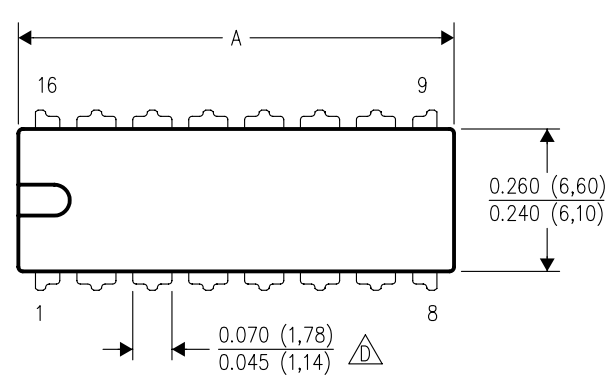


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

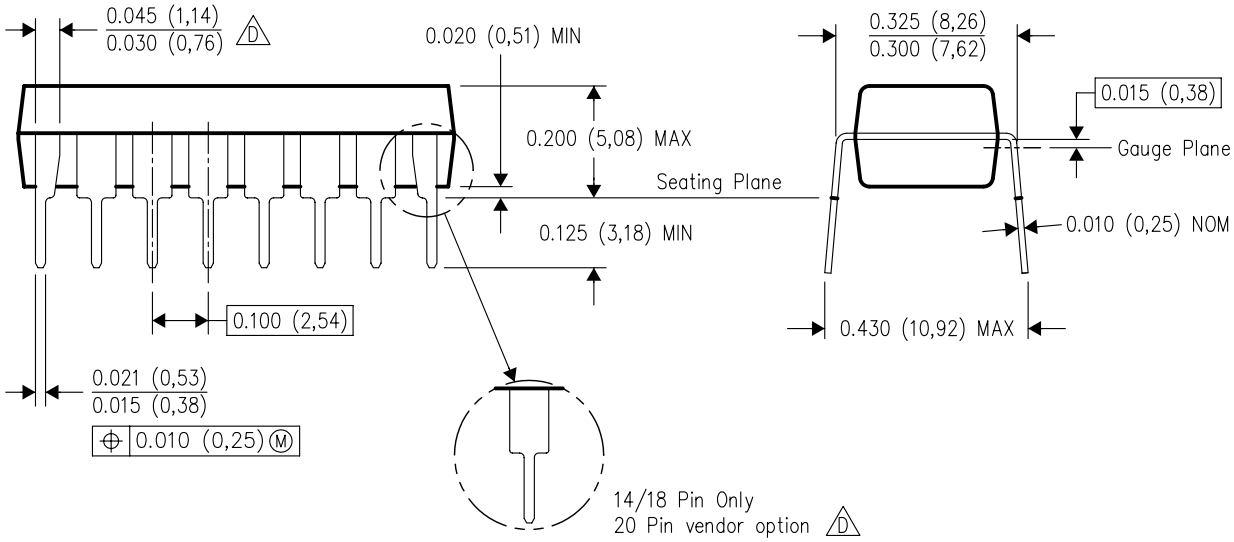
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

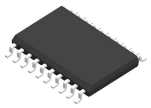


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

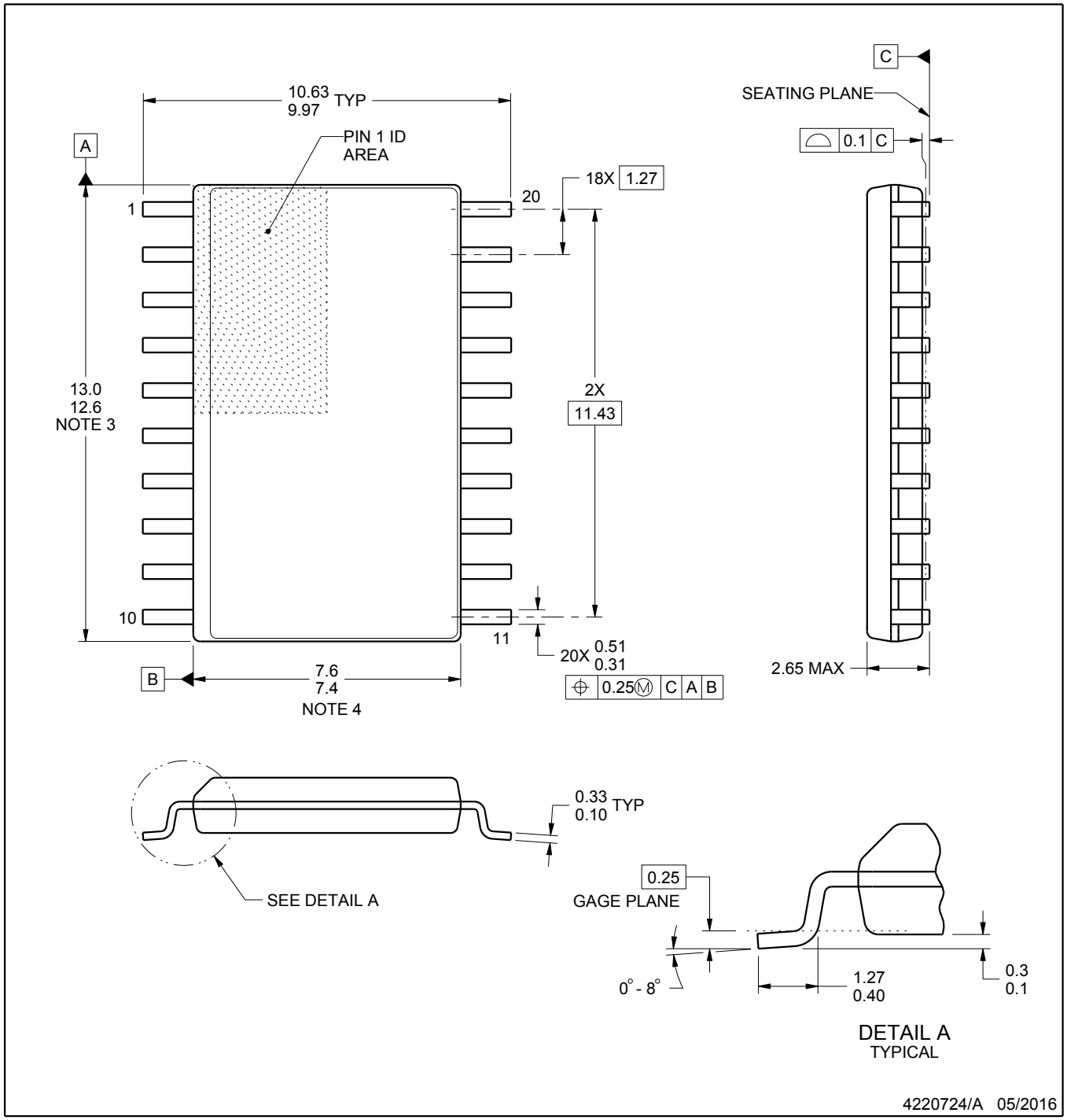


PACKAGE OUTLINE

DW0020A

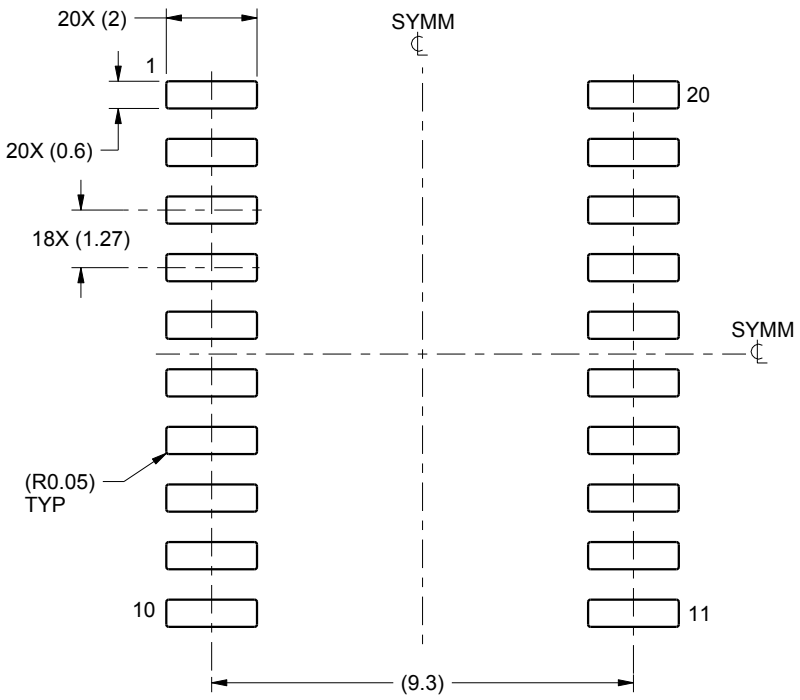
SOIC - 2.65 mm max height

SOIC

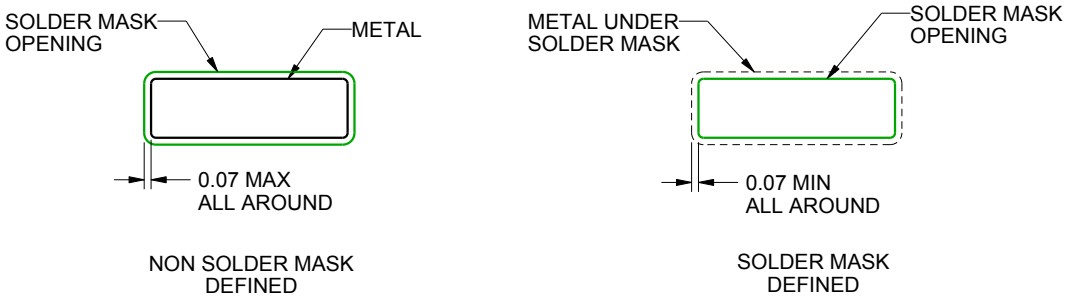


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

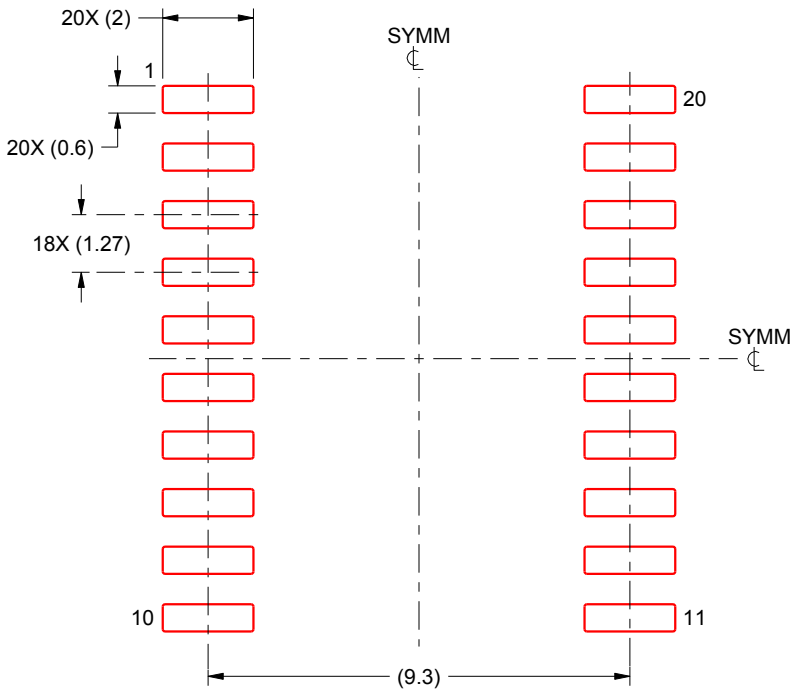


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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