TL08xx FET 输入运算放大器

1 特性

- 高压摆率：20V/μs（TL08xH，典型值）
- 低失调电压：1mV（TL08xH，典型值）
- 低失调电压漂移：2μV/°C
- 低功耗：940μA/通道（TL08xH，典型值）
- 宽共模和差分
  电压范围
  - 共模输入电压范围
    包括 V_{CC+}
- 低输入偏置和失调电流
- 低噪声：
  f = 1kHz 时，V_n = 37nV/√Hz（典型值）
- 输出短路保护
- 低总计谐波失真：0.003%（典型值）
- 宽电源电压：
  ±2.25V 至 ±20V，4.5V 至 40V

2 应用

- 太阳能：串式和中央逆变器
- 电机驱动器：交流和伺服驱动控制及功率级模块
- 单相在线式 UPS
- 三相 UPS
- 专业音频混合器
- 电池测试设备

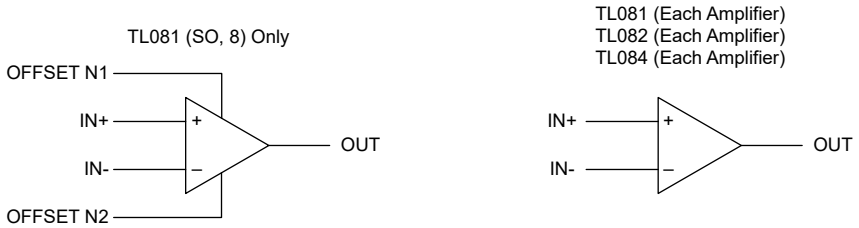
3 说明

TL08xH（TL081H、TL082H 和 TL084H）系列器件是业界通用的 TL08x（TL081、TL082 和 TL084）器件的下一代版本。这些器件为成本敏感型应用提供了卓越的价值，其特性包括低失调电压（1mV，典型值）、高压摆率 (20V/μs) 和正电源的共模输入。得益于高 ESD（1.5kV，HBM）、集成 EMI 和射频滤波器以及 –40°C 至 125°C 的完整运行温度范围，TL08xH 器件可用于要求严苛的应用。

器件信息

器件型号	通道数	封装(1)
TL081x	单通道	P（PDIP，8）
		DCK（SC70，5）
		PS（SO，8）
		D（SOIC，8）
		DBV（SOT-23，5）
TL082x	双通道	P（PDIP，8）
		PS（SO，8）
		D（SOIC，8）
		DDF（SOT-23，8）
		PW（TSSOP，8）
TL082M	双通道	JG（CDIP，8）
		FK（LCCC，20）
TL084x	四通道	N（PDIP，14）
		D（SOIC，14）
		DYY（SOT-23，14）
		PW（TSSOP，14）
TL084M	四通道	J（CDIP，14）
		FK（LCCC，20）

(1) 有关更多信息，请参阅 节 11。



逻辑符号

本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

内容

1 特性 1
2 应用 1
3 说明 1
4 引脚配置和功能 3
5 规格 9
5.1 绝对最大额定值 9
5.2 ESD 等级 9
5.3 建议运行条件 9
5.4 单通道器件的热性能信息 10
5.5 双通道器件的热性能信息 10
5.6 四通道器件的热性能信息 11
5.7 电气特性：TL08xH 12
5.8 电气特性（直流）：TL08xC、TL08xAC、TL08xBC、TL08xI、TL08xM 14
5.9 电气特性（交流）：TL08xC、TL08xAC、TL08xBC、TL08xI、TL08xM 16
5.10 典型特性：TL08xH 17
6 参数测量信息 23
7 详细说明 24
7.1 概述 24
7.2 功能方框图 24
7.3 特性说明 24
7.4 器件功能模式 24
8 应用和实施 25
8.1 应用信息 25
8.2 典型应用 25
8.3 电源相关建议 26
8.4 布局 26
9 器件和文档支持 28
9.1 器件支持 28
9.2 接收文档更新通知 28
9.3 支持资源 28
9.4 商标 28
9.5 静电放电警告 28
9.6 术语表 28
10 修订历史记录 28
11 机械、封装和可订购信息 29

Copyright © 2025 Texas Instruments Incorporated

4 引脚配置和功能

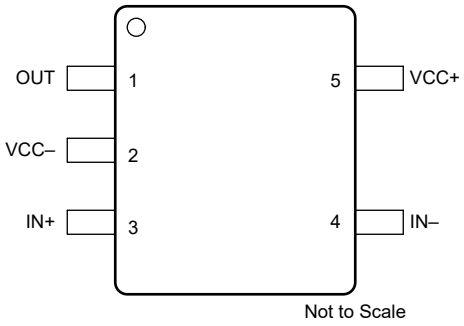


图 4-1. TL081H：DBV 封装，
5 引脚 SOT-23
（顶视图）

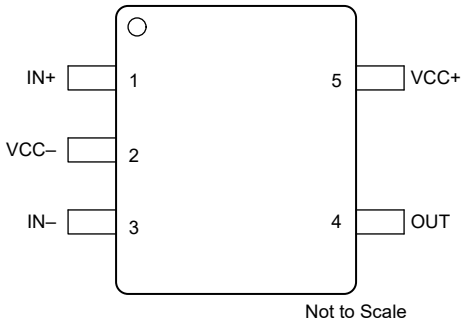


图 4-2. TL081H：DCK 封装，
5 引脚 SC70
（顶视图）

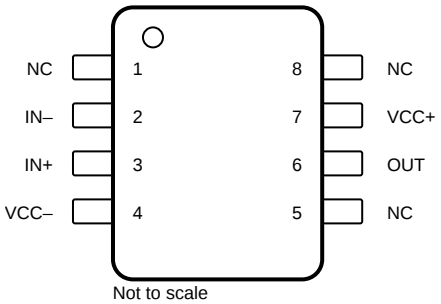


图 4-3. TL081x：D 封装，8 引脚 SOIC，
P 封装，8 引脚 PDIP
（顶视图）

表 4-1. 引脚功能：TL081x

引脚					类型(1)	说明
名称	编号					
	D	DBV	DCK	P		
NC	1	—	—	1	—	不连接
IN –	2	4	3	2	I	反相输入
IN+	3	3	1	3	I	非反相输入
VCC –	4	2	2	4	—	电源
NC	5	—	—	5	—	不连接
OUT	6	1	4	6	O	输出
VCC+	7	5	5	7	—	电源
NC	8	—	—	8	—	不连接

(1) I = 输入，O = 输出。

Copyright © 2025 Texas Instruments Incorporated

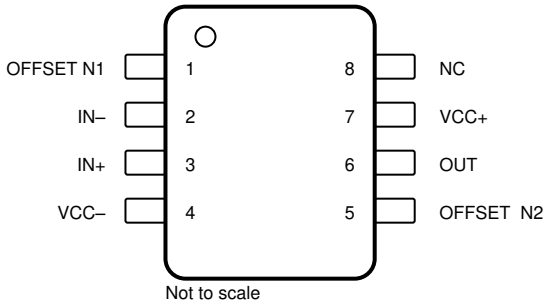


图 4-4. TL081C PS 封装，8 引脚 SO（顶视图）

表 4-2. 引脚功能：TL081C

引脚		类型(1)	说明
名称	编号		
OFFSET N1	1	—	输入偏移调整
IN –	2	I	反相输入
IN+	3	I	非反相输入
VCC –	4	—	电源
OFFSET N2	5	—	输入偏移调整
OUT	6	O	输出
VCC+	7	—	电源
NC	8	—	不连接

(1) I = 输入，O = 输出。

Copyright © 2025 Texas Instruments Incorporated

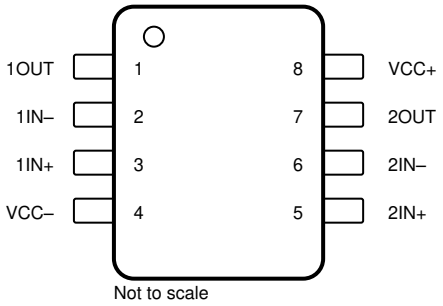


图 4-5. TL082x D，DDF，DGK，JG，P，PS 和 PW 封装，8 引脚 SOIC，SOT-23 (8)，VSSOP，CDIP，PDIP，SO 和 TSSOP（顶视图）

表 4-3. 引脚功能：TL082x

引脚		类型(1)	说明
名称	编号		
1OUT	1	O	输出
1IN –	2	I	反相输入
1IN+	3	I	非反相输入
VCC –	4	—	电源
2IN+	5	I	非反相输入
2IN –	6	I	反相输入
2OUT	7	O	输出
VCC+	8	—	电源

(1) I = 输入，O = 输出。

Copyright © 2025 Texas Instruments Incorporated

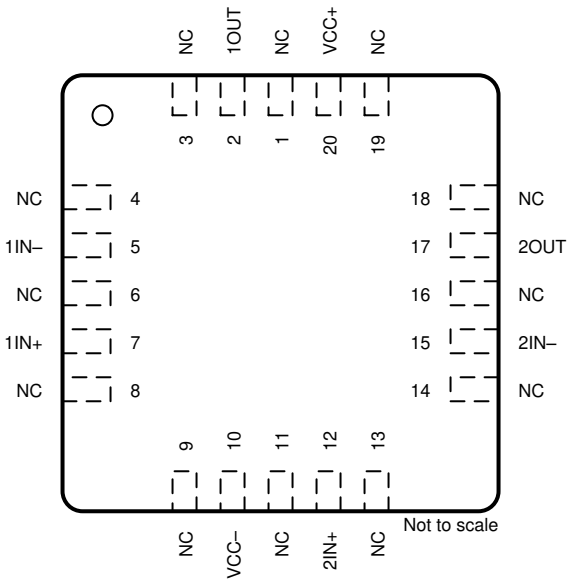


图 4-6. TL082 FK 封装，
20 引脚 LCCC
（顶视图）

表 4-4. 引脚功能：TL082x

引脚		类型(1)	说明
名称	编号		
1IN –	5	I	反相输入
1IN+	7	I	非反相输入
1OUT	2	O	输出
2IN –	15	I	反相输入
2IN+	12	I	非反相输入
2OUT	17	O	输出
NC	1、3、4、6、8、9、11、13、14、16、18、19	—	不连接
VCC –	10	—	电源
VCC+	20	—	电源

(1) I = 输入，O = 输出。

Copyright © 2025 Texas Instruments Incorporated

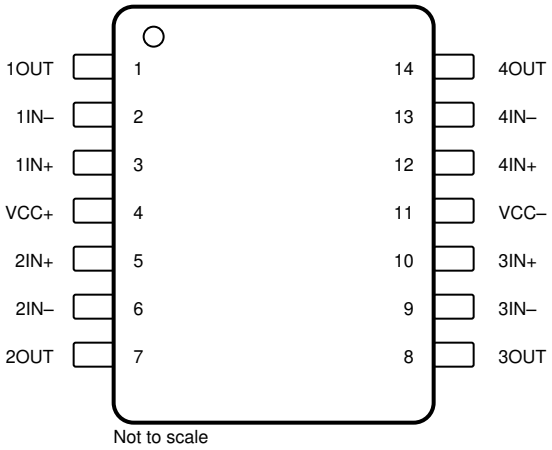


图 4-7. TL084x D，N，NS，PW，J 和 DYY 封装，
14 引脚 SOIC，PDIP，SO，TSSOP，CDIP 和 SOT-23 (14)
（顶视图）

表 4-5. 引脚功能：TL084x

引脚		类型(1)	说明
名称	编号		
1IN –	2	I	反相输入
1IN+	3	I	非反相输入
1OUT	1	O	输出
2IN –	6	I	反相输入
2IN+	5	I	非反相输入
2OUT	7	O	输出
3IN –	9	I	反相输入
3IN+	10	I	非反相输入
3OUT	8	O	输出
4IN –	13	I	反相输入
4IN+	12	I	非反相输入
4OUT	14	O	输出
V_{CC-}	11	—	电源
V_{CC+}	4	—	电源

(1) I = 输入，O = 输出。

Copyright © 2025 Texas Instruments Incorporated

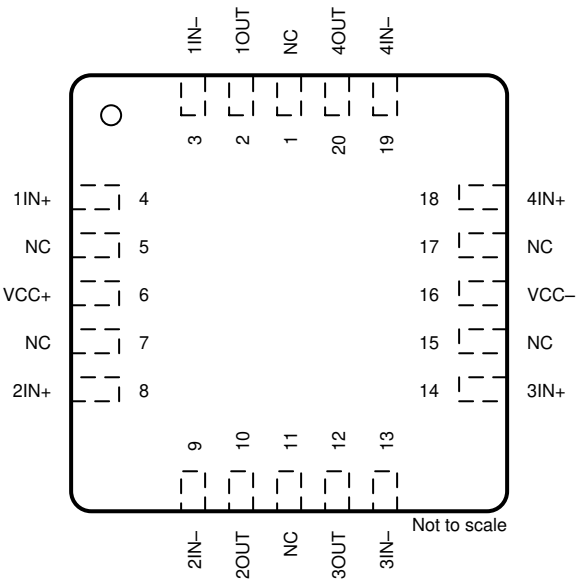


图 4-8. TL084 FK 封装，
20 引脚 LCCC
（顶视图）

表 4-6. 引脚功能：TL084x

引脚		类型(1)	说明
名称	编号		
1IN –	3	I	反相输入
1IN+	4	I	非反相输入
1OUT	2	O	输出
2IN –	9	I	反相输入
2IN+	8	I	非反相输入
2OUT	10	O	输出
3IN –	13	I	反相输入
3IN+	14	I	非反相输入
3OUT	12	O	输出
4IN –	19	I	反相输入
4IN+	18	I	同相输入
4OUT	20	O	输出
NC	1、5、7、11、15、17	—	不连接
VCC –	16	—	电源
VCC+	6	—	电源

(1) I = 输入，O = 输出。

Copyright © 2025 Texas Instruments Incorporated

5 规格

5.1 绝对最大额定值

在工作环境温度范围内测得（除非另有说明）(1)

			最小值	最大值	单位
电源电压，V_S = (V+) – (V–)		所有 NS 和 PS 封装；所有 TL08xM 器件	-0.3	36	V
		所有其他器件	0	42	V
信号输入引脚	共模电压(3)	所有 NS 和 PS 封装；所有 TL08xM 器件	(V–) – 0.3	(V–) + 36	V
		所有其他器件	(V–) – 0.5	(V+) + 0.5	V
	差分电压(3)	所有 NS 和 PS 封装；所有 TL08xM 器件(4)	(V–) – 0.3	(V–) + 36	V
		所有其他器件		V_S + 0.2	V
	电流(3)	所有 NS 和 PS 封装；所有 TL07xM 器件		50	mA
		所有其他器件	-10	10	mA
输出短路(2)			持续		
工作环境温度，T_A			-55	150	°C
结温，T_J				150	°C
60 秒内的管壳温度 - FK 封装				260	°C
10 秒内距离外壳 1.8mm（1/16 英寸）的引线温度				300	°C
贮存温度，T_{stg}			-65	150	°C

(1) 应力超出*绝对最大额定值*中列出的值时可能会对器件造成永久损坏。这些列出的值仅为应力等级，并不表示器件在这些条件下以及在*建议工作条件*以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
(2) 接地短路，每个封装对应一个放大器。
(3) 输入引脚被二极管钳制至电源轨。对于摆幅超过电源轨 0.5V 以上的输入信号，其电流必须限制在 10mA 或者更低。
(4) 差动电压仅受输入电压限制。

5.2 ESD 等级

			值	单位
$V_{(ESD)}$	静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001 标准(1)	±1500	V
		充电器件模型 (CDM)，符合 JEDEC 规范 JESD22-C101(2)	±1000	

(1) JEDEC 文档 JEP155 指出：500V HBM 可通过标准 ESD 控制流程实现安全生产。
(2) JEDEC 文档 JEP157 指出：250V CDM 能够在标准 ESD 控制流程下安全生产。

5.3 建议运行条件

在工作环境温度范围内测得（除非另有说明）

			最小值	最大值	单位
V_S	电源电压，(V_{CC}+) – (V_{CC} –)	所有 NS 和 PS 封装；所有 TL08xM 器件(1)	10	30	V
		所有其他器件	4.5	40	V
V_I	输入电压范围	所有 NS 和 PS 封装；所有 TL08xM 器件	(V_{CC} –) + 2	(V_{CC}+) + 0.1	V
		所有其他器件	(V_{CC} –) + 4	(V_{CC}+) + 0.1	V
T_A	额定温度	TL08xM	-55	125	°C
		TL08xH	-40	125	°C
		TL08xI	-40	85	°C
		TL08xC	0	70	°C

(1) V+ 和 V – 不要求具有相同的幅度，只要总 V_S (V+ – V –) 介于 10V 与 30V 之间即可。

Copyright © 2025 Texas Instruments Incorporated

5.4 单通道器件的热性能信息

热指标 (1)		TL081xx					单位
		D (SOIC)	DCK (SC70)	DBV (SOT-23)	P (PDIP)	PS (SO)	
		8 引脚	5 引脚	5 引脚	8 引脚	8 引脚	
$R_{\theta JA}$	结至环境热阻	158.8	217.5	212.2	85	95	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	98.6	113.1	111.1	–	–	°C/W
$R_{\theta JB}$	结至电路板热阻	102.3	63.8	79.4	–	–	°C/W
ψ_{JT}	结至顶部特征参数	45.8	34.8	51.8	–	–	°C/W
ψ_{JB}	结至电路板特征参数	101.5	63.5	79.0	–	–	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	不适用	不适用	不适用	不适用	不适用	°C/W

(1) 有关新旧热指标的更多信息，请参阅*半导体和 IC 封装热指标*应用报告。

5.5 双通道器件的热性能信息

热指标 (1)		TL082xx								单位
		D (SOIC)	DDF (SOT-23)	FK (LCCC)	JG (CDIP)	P (PDIP)	PS (SO)	PW (TSSOP)	U (CFP)	
		8 引脚	8 引脚	20 引脚	8 引脚	8 引脚	8 引脚	8 引脚	10 引脚	
$R_{\theta JA}$	结至环境热阻	147.8	181.5	–	–	85	95	200.3	169.8	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	88.2	112.5	5.61	15.05	–	–	89.4	62.1	°C/W
$R_{\theta JB}$	结至电路板热阻	91.4	98.2	–	–	–	–	131.0	176.2	°C/W
ψ_{JT}	结至顶部特征参数	36.8	17.2	–	–	–	–	22.2	48.4	°C/W
ψ_{JB}	结至电路板特征参数	90.6	97.6	–	–	–	–	129.3	144.1	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	不适用	不适用	–	–	–	–	不适用	5.4	°C/W

(1) 有关新旧热指标的更多信息，请参阅*半导体和 IC 封装热指标*应用报告。

Copyright © 2025 Texas Instruments Incorporated

5.6 四通道器件的热性能信息

热指标 (1)		TL084xx								单位
		D (SOIC)	DYY (SOT-23)	FK (TSSOP)	J (TSSOP)	N (TSSOP)	NS (TSSOP)	PW (TSSOP)	W (TSSOP)	
		14 引脚	14 引脚	20 引脚	14 引脚	14 引脚	14 引脚	14 引脚	14 引脚	
$R_{\theta JA}$	结至环境热阻	114.2	153.2	–	–	80	76	–	128.8	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	70.3	88.7	5.61	14.5	–	–	14.5	56.1	°C/W
$R_{\theta JB}$	结至电路板热阻	70.2	65.4	–	–	–	–	–	127.6	°C/W
ψ_{JT}	结至顶部特征参数	28.8	9.5	–	–	–	–	–	29	°C/W
ψ_{JB}	结至电路板特征参数	69.8	65.0	–	–	–	–	–	106.1	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	不适用	不适用	–	–	–	–	–	0.5	°C/W

(1) 有关新旧热指标的更多信息，请参阅*半导体和 IC 封装热指标*应用报告。

5.7 电气特性：TL08xH

对于 $V_S = (V_{CC+}) - (V_{CC-}) = 4.5V$ 至 40V（±2.25V 至 ±20V），当 $T_A = 25°C$，$R_L = 10k\Omega$ 连接至 $V_S/2$，$V_{CM} = V_S/2$，且 $V_{OUT} = V_S/2$ 时（除非另有说明）。

参数		测试条件		最小值	典型值	最大值	单位
失调电压							
V_{OS}	输入偏移电压				±1	±4	mV
			T_A = -40°C 至 +125°C			±5	
dV_{OS}/dT	输入失调电压漂移		T_A = -40°C 至 +125°C		±2		μV/℃
PSRR	输入失调电压与电源间的关系	V_S = 5V 至 40V，$V_{CM} = V_S / 2$	T_A = -40°C 至 +125°C		±1	±10	μV/V
	通道隔离	f = 0Hz			10		μV/V
输入偏置电流							
I_B	输入偏置电流				±1	±120	pA
			DCK 和 DBV 封装		±1	±300	pA
			T_A = –40°C 至 +125°C(1)			±5	nA
I_{OS}	输入失调电流				±0.5	±120	pA
			DCK 和 DBV 封装		±0.5	±250	pA
			T_A = –40°C 至 +125°C(1)			±5	nA
噪声							
E_N	输入电压噪声	f = 0.1Hz 至 10Hz			9.2		μV_{PP}
					1.4		μV_{RMS}
e_N	输入电压噪声密度	f = 1kHz			37		nV/√Hz
		f = 10kHz			21		
i_N	输入电流噪声	f = 1kHz			80		fA/√Hz
输入电压范围							
V_{CM}	共模电压范围			$(V_{CC-}) + 1.5$		(V_{CC+})	V
CMRR	共模抑制比	V_S = 40V，$(V_{CC-}) + 2.5V < V_{CM} < (V_{CC+}) - 1.5V$		100	105		dB
			T_A = -40°C 至 +125°C	95			dB
		V_S = 40V，$(V_{CC-}) + 2.5V < V_{CM} < (V_{CC+})$		90	105		dB
			T_A = -40°C 至 +125°C	80			dB
输入电容							
Z_{ID}	差分				100 || 2		MΩ || pF
Z_{ICM}	共模				6 || 1		TΩ || pF
开环增益							
A_{OL}	开环电压增益	V_S = 40V，$V_{CM} = V_S / 2$，$(V_{CC-}) + 0.3V < V_O < (V_{CC+}) - 0.3V$	T_A = -40°C 至 +125°C	118	125		dB
A_{OL}	开环电压增益	V_S = 40V，$V_{CM} = V_S/2$，R_L = 2kΩ，$(V_{CC-}) + 1.2V < V_O < (V_{CC+}) - 1.2V$	T_A = -40°C 至 +125°C	115	120		dB
频率响应							
GBW	增益带宽积				5.25		MHz
SR	压摆率	V_S = 40V，G = +1，C_L = 20pF			20		V/μs
t_S	趋稳时间	精度达到 0.1%，V_S = 40V，V_{STEP} = 10V，G = +1，C_L = 20pF			0.63		μs
		精度达到 0.1%，V_S = 40V，V_{STEP} = 2V，G = +1，C_L = 20pF			0.56		
		精度达到 0.01%，V_S = 40V，V_{STEP} = 10V，G = +1，C_L = 20pF			0.91		
		精度达到 0.01%，V_S = 40V，V_{STEP} = 2V，G = +1，C_L = 20pF			0.48		

Copyright © 2025 Texas Instruments Incorporated

5.7 电气特性：TL08xH（续）

对于 $V_S = (V_{CC+}) - (V_{CC-}) = 4.5V$ 至 40V（±2.25V 至 ±20V），当 $T_A = 25°C$，$R_L = 10k\Omega$ 连接至 $V_S/2$，$V_{CM} = V_S/2$，且 $V_{OUT} = V_S/2$ 时（除非另有说明）。

参数		测试条件		最小值	典型值	最大值	单位
	相位裕度	G = +1，$R_L = 10k\Omega$，$C_L = 20pF$			56		°
	过载恢复时间	V_{IN} × 增益 > V_S			300		ns
THD+N	总谐波失真 + 噪声	$V_S = 40V$，$V_O = 6V_{RMS}$，G = +1，f = 1kHz			0.00012		%
EMIRR	EMI 抑制比	f = 1GHz			53		dB
输出							
	相对于电源轨的电压输出摆幅	正电源轨余量	$V_S = 40V$，$R_L = 10k\Omega$		115	210	mV
			$V_S = 40V$，$R_L = 2k\Omega$		520	965	
		负电源轨余量	$V_S = 40V$，$R_L = 10k\Omega$		105	215	
			$V_S = 40V$，$R_L = 2k\Omega$		500	1030	
I_{SC}	短路电流				±26		mA
C_{LOAD}	容性负载驱动				300		pF
Z_O	开环输出阻抗	f = 1MHz，$I_O = 0A$			125		Ω
电源							
I_Q	每个放大器的静态电流	$I_O = 0A$			937.5	1125	μA
		$I_O = 0A$，(TL081H)			960	1156	
		$I_O = 0A$	T_A = -40°C 至 +125°C			1130	
		$I_O = 0A$，(TL082H)				1143	
		$I_O = 0A$，(TL071H)				1160	
	导通时间	$T_A = 25°C$，$V_S = 40V$，V_S 升降速率 > 0.3V/μs			60		μs

(1) 根据表征结果指定最大 I_B 和 I_{os}。

Copyright © 2025 Texas Instruments Incorporated

5.8 电气特性（直流）：TL08xC、TL08xAC、TL08xBC、TL08xI、TL08xM

对于 $V_S = (V_{CC+}) - (V_{CC-}) = \pm 15V$，$T_A = 25°C$ 时（除非另有说明）

参数		测试条件(1) (2)			最小值	典型值	最大值	单位
V_{OS}	输入失调电压	$V_O = 0V$ $R_S = 50\Omega$	TL08xC			3	10	mV
				T_A = 完整范围			13	
			TL08xAC			3	6	
				T_A = 完整范围			7.5	
			TL08xBC			2	3	
				T_A = 完整范围			5	
			TL08xI			3	6	
				T_A = 完整范围			8	
			TL081M、TL082M			3	6	
				T_A = 完整范围			9	
			TL084M			3	9	
				T_A = 完整范围			15	
dV_{OS}/dT	输入失调电压漂移	$V_O = 0V$，$R_S = 50\Omega$	T_A = 完整范围			±18		μV/℃
I_{OS}	输入失调电流	$V_O = 0V$	TL08xC			5	100	pA
				T_A = 完整范围			10	nA
			TL08xAC、TL08xBC、TL08xI			5	100	pA
				T_A = 完整范围			2	nA
			TL08xM			5	100	pA
				T_A = 完整范围			20	nA
I_B	输入偏置电流	$V_O = 0V$	TL08xC、TL08xAC、TL08xBC、TL08xI			65	200	pA
				T_A = 完整范围			7	nA
			TL081M、TL082M			65	200	pA
				T_A = 完整范围			50	nA
			TL084M			65	200	pA
				T_A = 完整范围			20	nA
V_{CM}	共模电压范围				±11	-12 至 15		V
VOM	最大峰值输出电压摆幅	$R_L = 10k\Omega$			±12	±13.5		V
		$R_L \geq 10k\Omega$	T_A = 完整范围		±12			
		$R_L \geq 2k\Omega$			±10			
A_{OL}	开环电压增益	$V_O = 0V$	TL08xC		25	200		V/mV
				T_A = 完整范围	15			
			TL08xAC、TL08xBC、TL08xI		50	200		
				T_A = 完整范围	25			
			TL08xM		35	200		
				T_A = 完整范围	15			
GBW	增益带宽积	所有 NS 和 PS 封装；所有 TL08xM 器件				3		MHz
		所有其他器件				5.25		
R_{ID}	共模输入电阻					1		TΩ
CMRR	共模抑制比	$V_{IC} = V_{ICR(min)}$ $V_O = 0V$ $R_S = 50\Omega$	TL08xC		70	100		dB
			TL08xAC、TL08xBC、TL08xI		75	100		
			TL08xM		80	86		
PSRR	输入失调电压与电源间的关系	$V_S = \pm 9V$ 至 $\pm 18V$ $V_O = 0V$ $R_S = 50\Omega$	TL08xC		70	100		dB
			TL08xAC、TL08xBC、TL08xI		80	100		
			TL08xM		80	86		

Copyright © 2025 Texas Instruments Incorporated

5.8 电气特性（直流）：TL08xC、TL08xAC、TL08xBC、TL08xI、TL08xM（续）

对于 $V_S = (V_{CC+}) - (V_{CC-}) = \pm 15V$，$T_A = 25°C$ 时（除非另有说明）

参数		测试条件(1) (2)	最小值	典型值	最大值	单位
I_Q	每个放大器的静态电流	$V_O = 0$ V；空载		1.4	2.5	mA
	通道隔离	f = 0Hz		1		μV/V

(1) 除非另有说明，否则所有特性均在开环条件下以零共模电压测定。
(2) 对于 TL07xC、TL07xAC 和 TL07xBC，完整范围为 $T_A = 0°C$ 至 70°C；对于 TL07xI，$T_A = -40°C$ 至 85°C；对于 TL07xM，$T_A = -55°C$ 至 125°C。

Copyright © 2025 Texas Instruments Incorporated

5.9 电气特性（交流）：TL08xC、TL08xAC、TL08xBC、TL08xI、TL08xM

对于 $V_S = (V_{CC+}) - (V_{CC-}) = \pm 15V$，$T_A = 25°C$ 时（除非另有说明）

参数		测试条件		最小值	典型值	最大值	单位
SR	压摆率	$V_I = 10V$，$C_L = 100pF$，$R_L = 2k\Omega$	TL08xM	5	20		V/μs
			TL08xC、TL08xAC、TL08xBC、TL08xI	8	20		V/μs
t_S	趋稳时间	$V_I = 20V$，$C_L = 100pF$，$R_L = 2k\Omega$			0.1		μs
					20%		
e_N	输入电压噪声密度	所有 PS 和 NS 封装；所有 TL08xM 器件	$R_S = 20\Omega$，f = 1kHz		18		$nV/\sqrt{Hz}$
		所有其他器件	f = 1kHz		37		$nV/\sqrt{Hz}$
			f = 10kHz		21		
E_N	输入电压噪声	所有 PS 和 NS 封装；所有 TL08xM 器件	$R_S = 20\Omega$，f = 10Hz 至 10kHz		4		μV_{RMS}
		所有其他器件	f = 0.1Hz 至 10Hz		1.4		μV_{RMS}
i_N	输入电流噪声	$R_S = 20\Omega$，f = 1kHz			10		$fA/\sqrt{Hz}$
	相位裕度	TL08xC、TL08xAC、TL08xBC、TL08xI	G = +1，$R_L = 10k\Omega$，C_L = 20pF		56		°
	过载恢复时间	V_{IN} × 增益 > V_S			300		ns
THD+N	总谐波失真 + 噪声	所有 PS 和 NS 封装；所有 TL08xM 器件	$V_O = 6V_{RMS}$，$R_L \geq 2k\Omega$，f = 1kHz，G = +1，$R_S \leq 1k\Omega$		0.003		%
		所有其他器件	$V_S = 40V$，$V_O = 6V_{RMS}$，G = +1，f = 1kHz		0.00012		%
EMIRR	EMI 抑制比	TL08xC、TL08xAC、TL08xBC、TL08xI	f = 1GHz		53		dB
Z_O	开环输出阻抗	TL07xC、TL07xAC、TL07xBC、TL07xI	f = 1MHz，$I_O = 0A$		125		Ω

Copyright © 2025 Texas Instruments Incorporated

5.10 典型特性：TL08xH

当 T_A = 25°C，V_S = 40V (±20V)，V_{CM} = V_S / 2，R_{LOAD} = 10kΩ 连接至 V_S / 2，且 C_L = 20pF 时（除非另有说明）

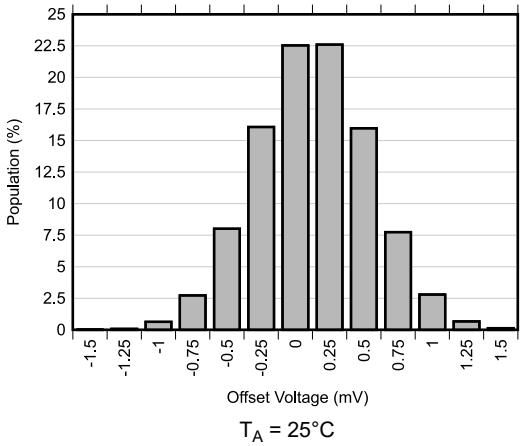


图 5-1. 失调电压产生分布

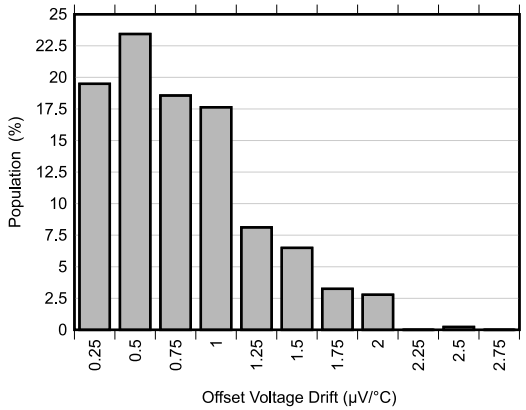


图 5-2. 失调电压漂移分布

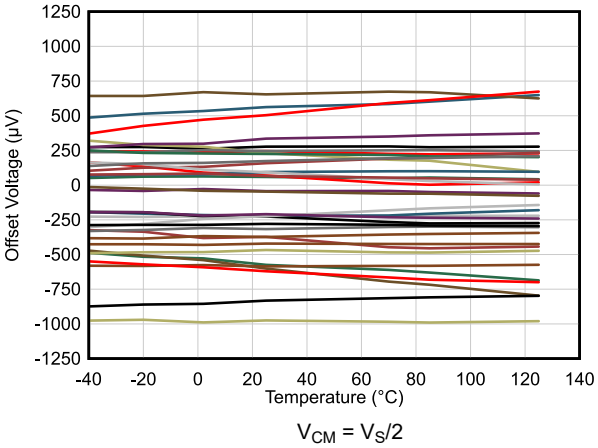


图 5-3. 失调电压与温度间的关系

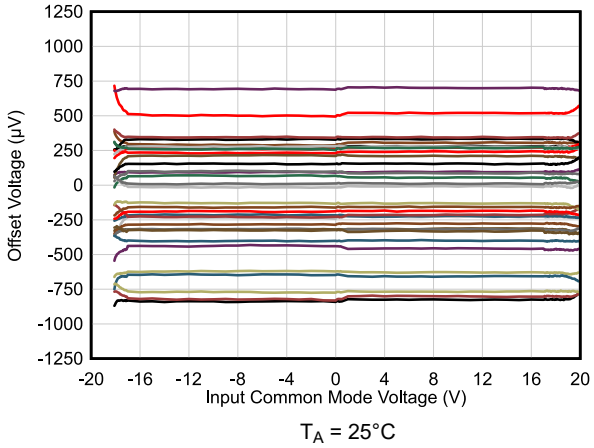


图 5-4. 失调电压与共模电压间的关系

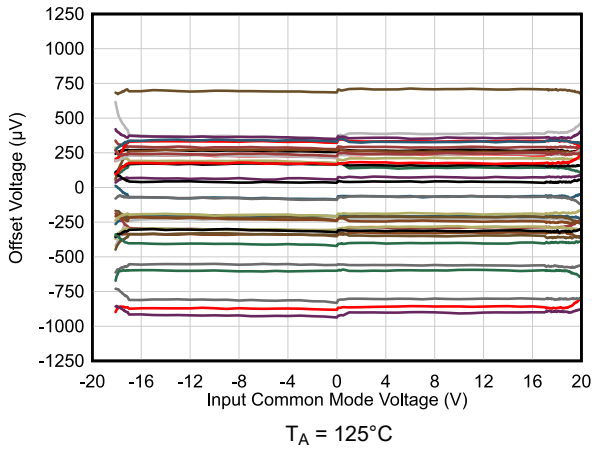


图 5-5. 失调电压与共模电压间的关系

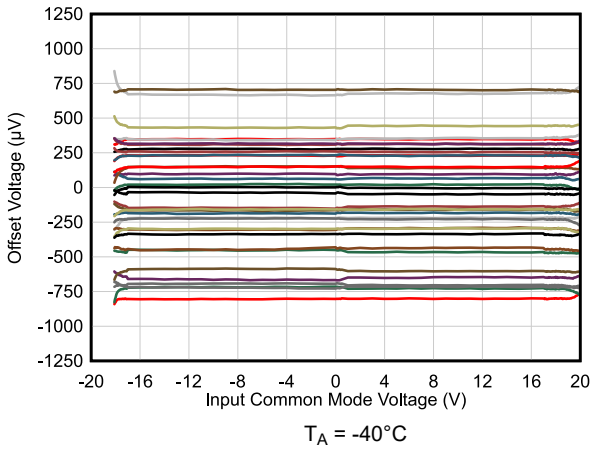


图 5-6. 失调电压与共模电压间的关系

Copyright © 2025 Texas Instruments Incorporated

5.10 典型特性：TL08xH（续）

当 T_A = 25°C，V_S = 40V (±20V)，V_{CM} = V_S / 2，R_{LOAD} = 10kΩ 连接至 V_S / 2，且 C_L = 20pF 时（除非另有说明）

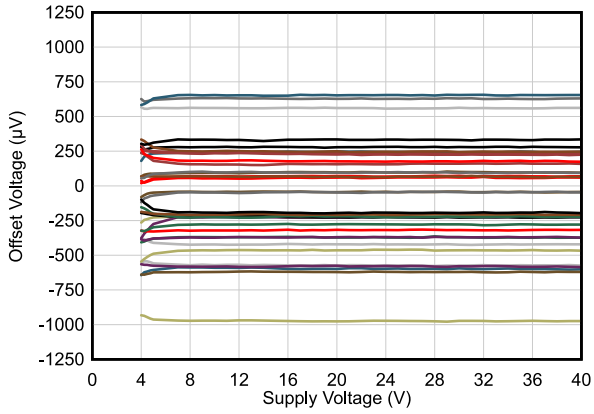


图 5-7. 失调电压与电源间的关系

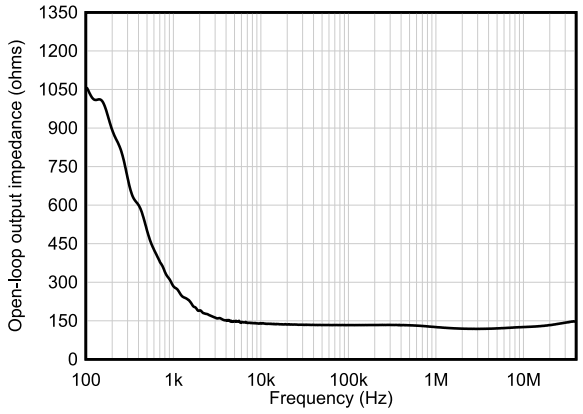


图 5-8. 开环输出阻抗与频率间的关系

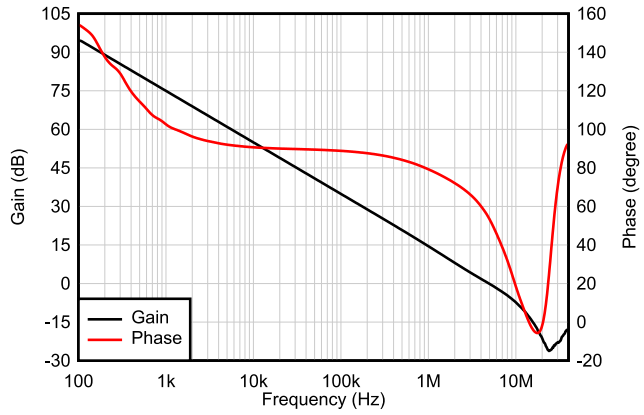


图 5-9. 开环增益和相位与频率间的关系

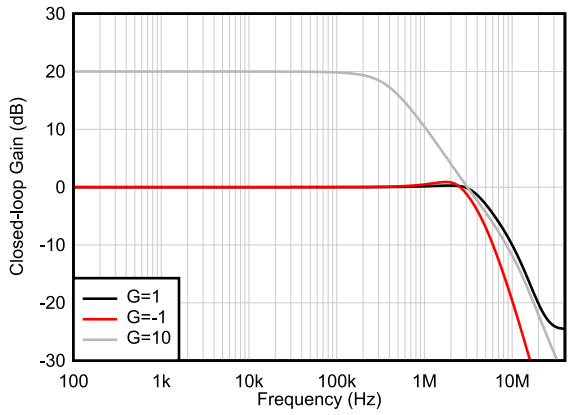


图 5-10. 闭环增益与频率间的关系

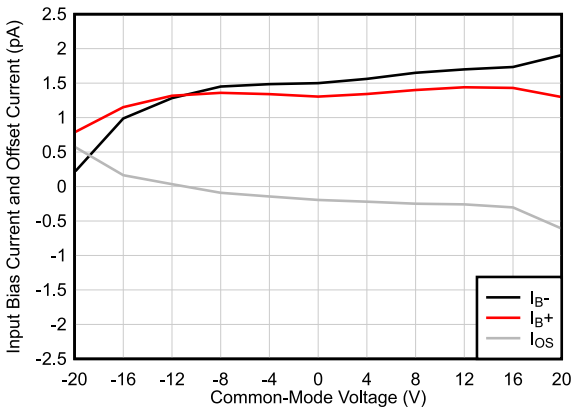


图 5-11. 输入偏置电流与共模电压间的关系

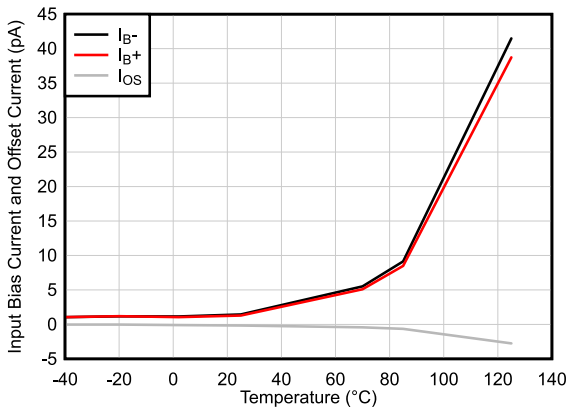


图 5-12. 输入偏置电流与温度间的关系

Copyright © 2025 Texas Instruments Incorporated

5.10 典型特性：TL08xH（续）

当 T_A = 25°C，V_S = 40V (±20V)，V_{CM} = V_S / 2，R_{LOAD} = 10kΩ 连接至 V_S / 2，且 C_L = 20pF 时（除非另有说明）

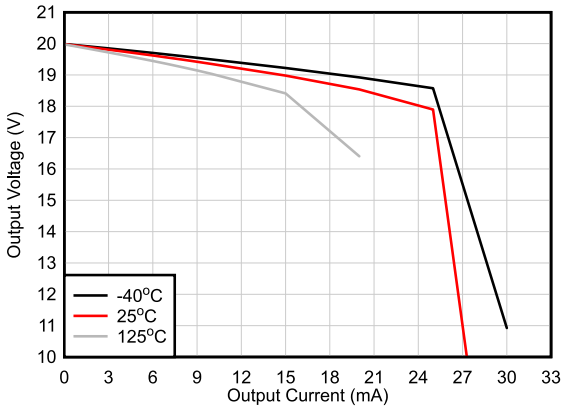


图 5-13. 输出电压摆幅与输出电流（拉电流）间的关系

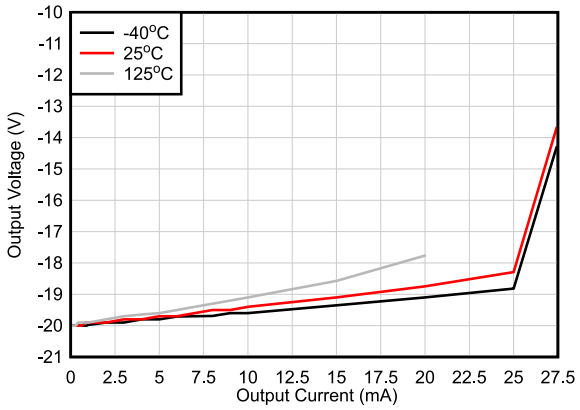


图 5-14. 输出电压摆幅与输出电流（灌电流）间的关系

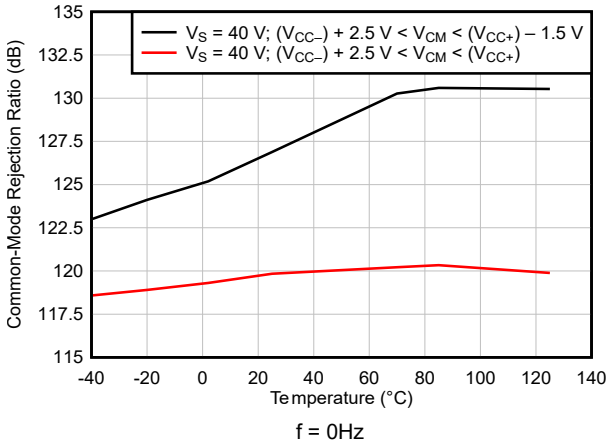


图 5-15. CMRR 与温度间的关系 (dB)

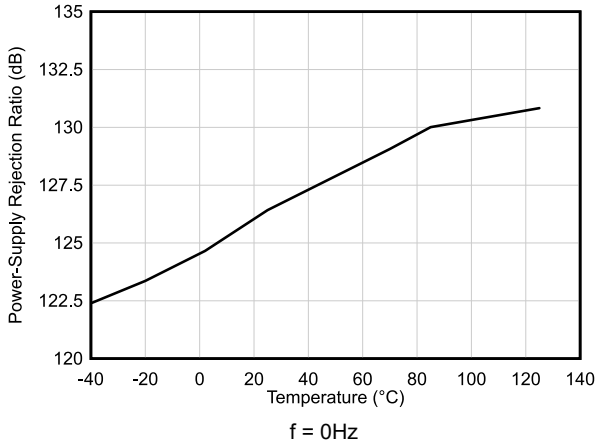


图 5-16. PSRR 与温度间的关系 (dB)

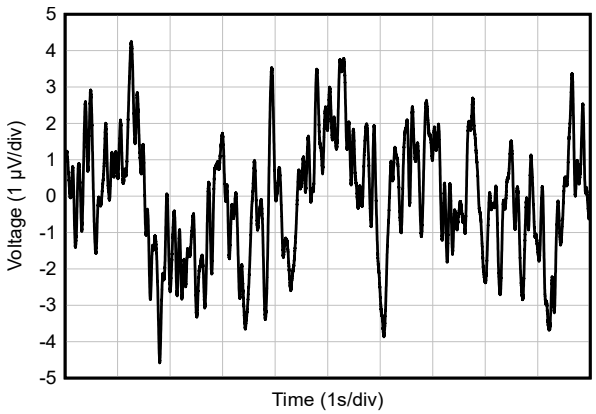


图 5-17. 0.1Hz 至 10Hz 噪声

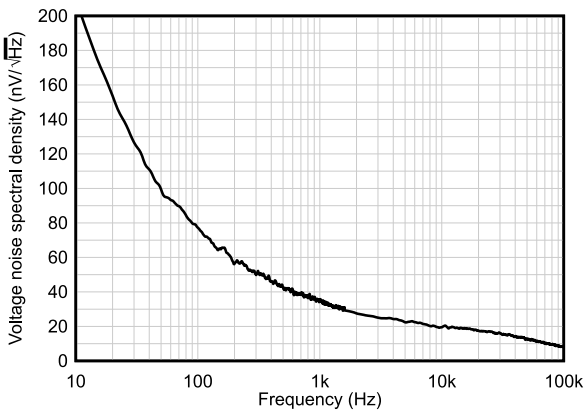


图 5-18. 输入电压噪声频谱密度与频率间的关系

Copyright © 2025 Texas Instruments Incorporated

5.10 典型特性：TL08xH（续）

当 T_A = 25°C，V_S = 40V (±20V)，V_{CM} = V_S / 2，R_{LOAD} = 10kΩ 连接至 V_S / 2，且 C_L = 20pF 时（除非另有说明）

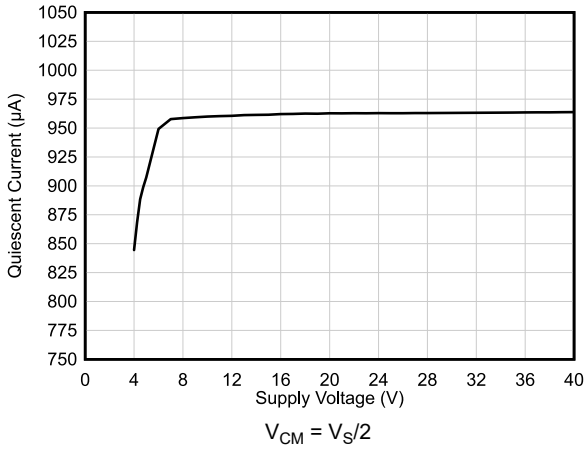


图 5-19. 静态电流与电源电压间的关系

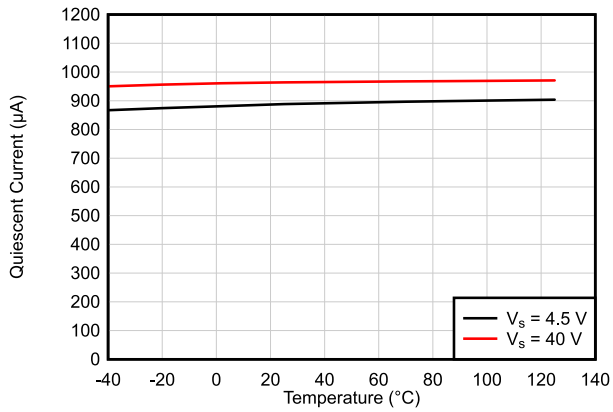


图 5-20. 静态电流与温度间的关系

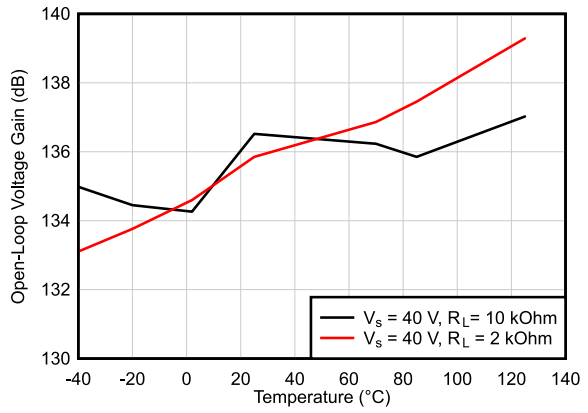


图 5-21. 开环电压增益与温度间的关系 (dB)

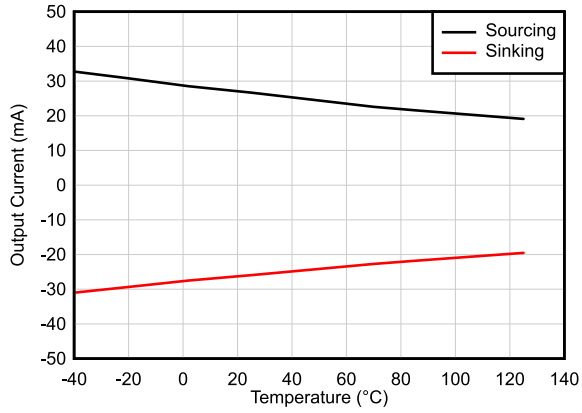


图 5-22. 短路电流与温度间的关系

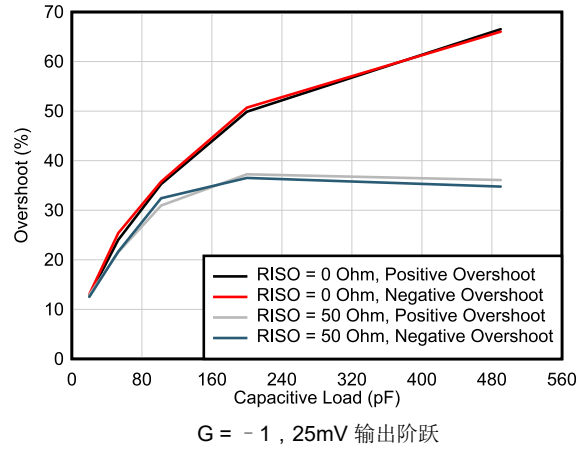


图 5-23. 小信号过冲与容性负载间的关系

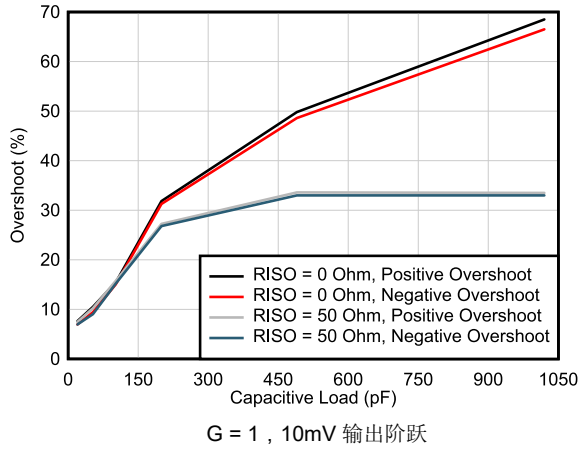


图 5-24. 小信号过冲与容性负载间的关系

Copyright © 2025 Texas Instruments Incorporated

5.10 典型特性：TL08xH（续）

当 T_A = 25°C，V_S = 40V (±20V)，V_{CM} = V_S / 2，R_{LOAD} = 10kΩ 连接至 V_S / 2，且 C_L = 20pF 时（除非另有说明）

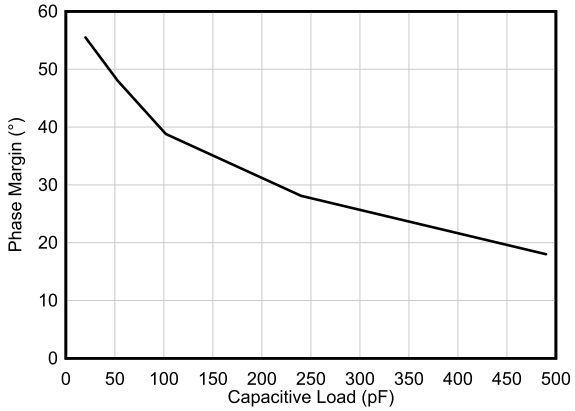
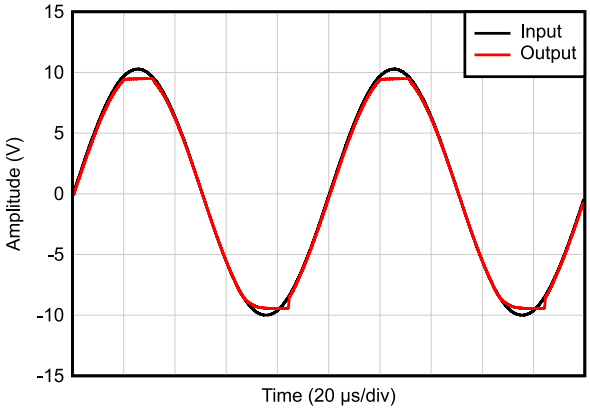
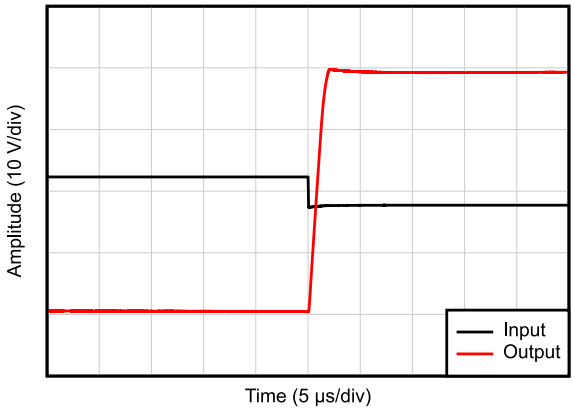


图 5-25. 相位裕度与容性负载间的关系



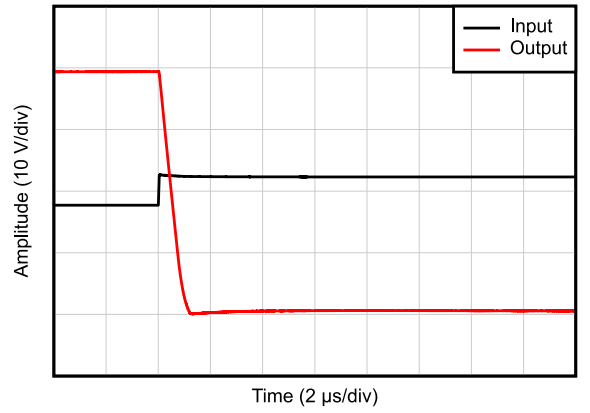
V_S = ±10V，V_{IN} = V_{OUT}

图 5-26. 无相位反转



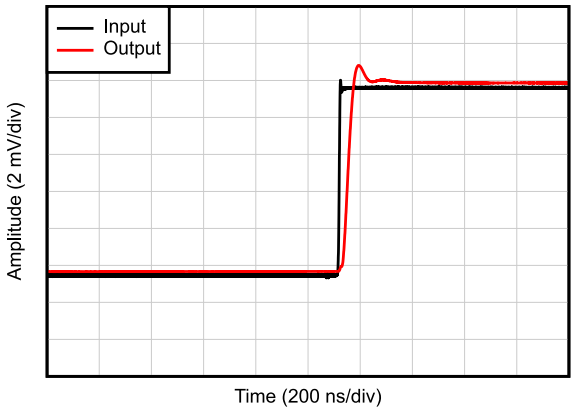
G = -10

图 5-27. 正过载恢复



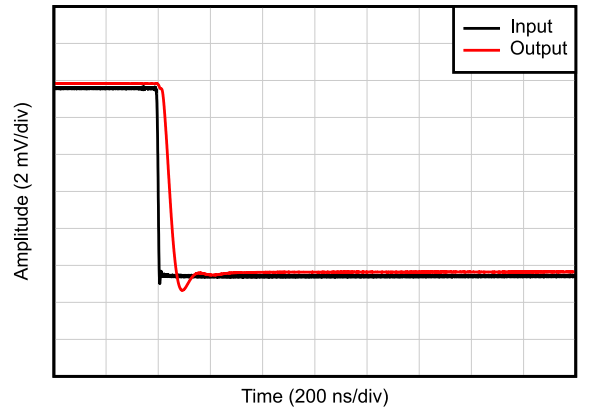
G = -10

图 5-28. 负过载恢复



C_L = 20pF，G = 1，10mV 阶跃响应

图 5-29. 小信号阶跃响应，上升



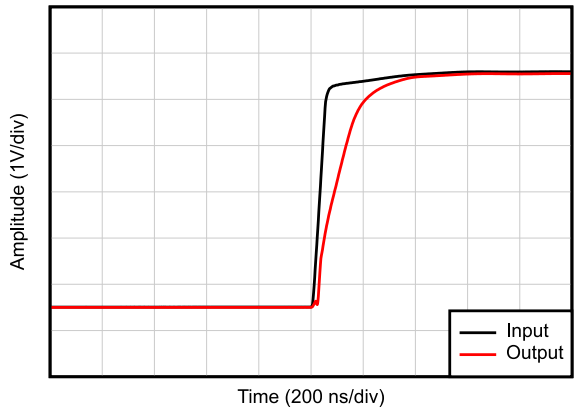
C_L = 20pF，G = 1，10mV 阶跃响应

图 5-30. 小信号阶跃响应，下降

Copyright © 2025 Texas Instruments Incorporated

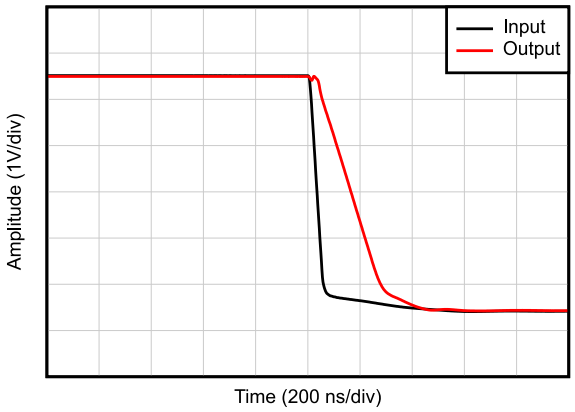
5.10 典型特性：TL08xH（续）

当 T_A = 25°C，V_S = 40V (±20V)，V_{CM} = V_S / 2，R_{LOAD} = 10kΩ 连接至 V_S / 2，且 C_L = 20pF 时（除非另有说明）



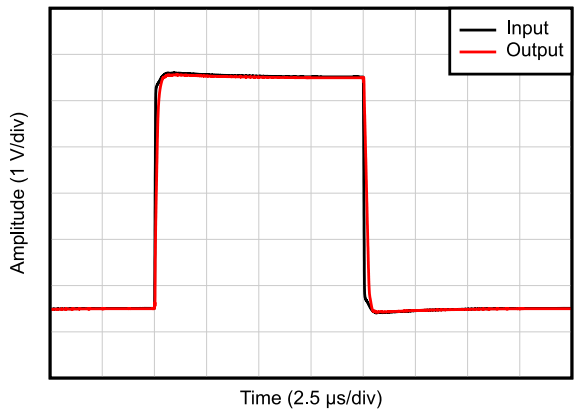
C_L = 20pF，G = 1

图 5-31. 大信号阶跃响应（上升）



C_L = 20pF，G = 1

图 5-32. 大信号阶跃响应（下降）



C_L = 20pF，G = 1

图 5-33. 大信号阶跃响应

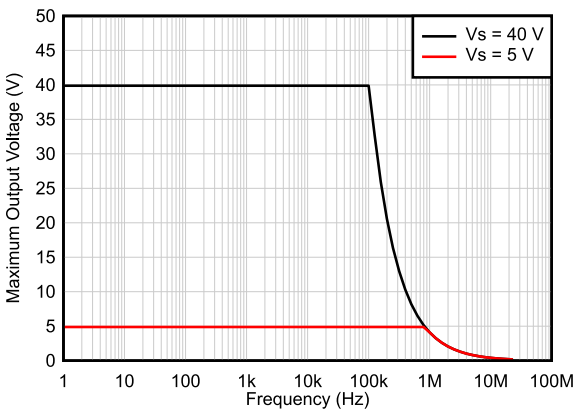


图 5-34. 最大输出电压与频率间的关系

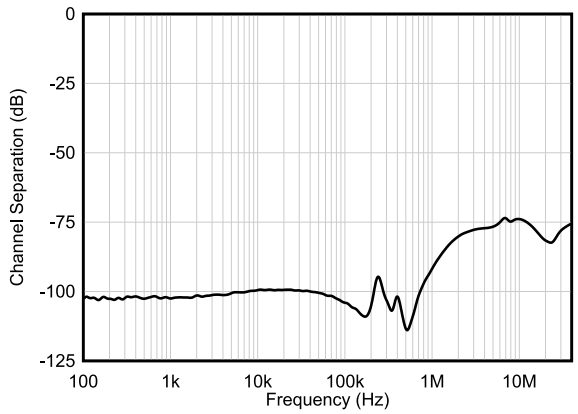


图 5-35. 通道隔离与频率间的关系

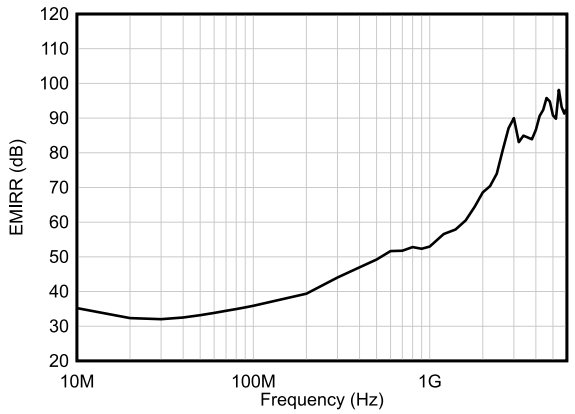


图 5-36. EMIRR（电磁干扰抑制比）与频率间的关系

Copyright © 2025 Texas Instruments Incorporated

6 参数测量信息

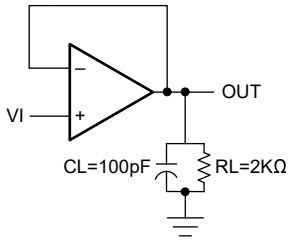


图 6-1. 测试图 1

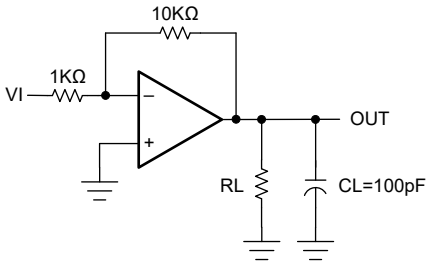


图 6-2. 测试图 2

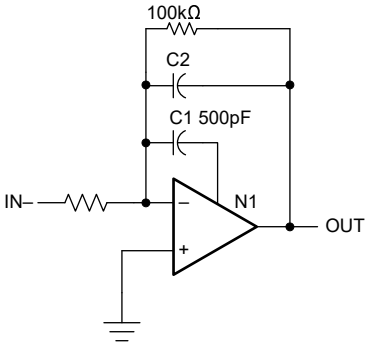


图 6-3. 测试图 3

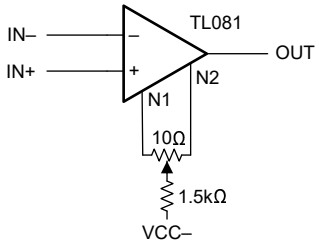


图 6-4. 测试图 4 (仅适用于 SO 封装)

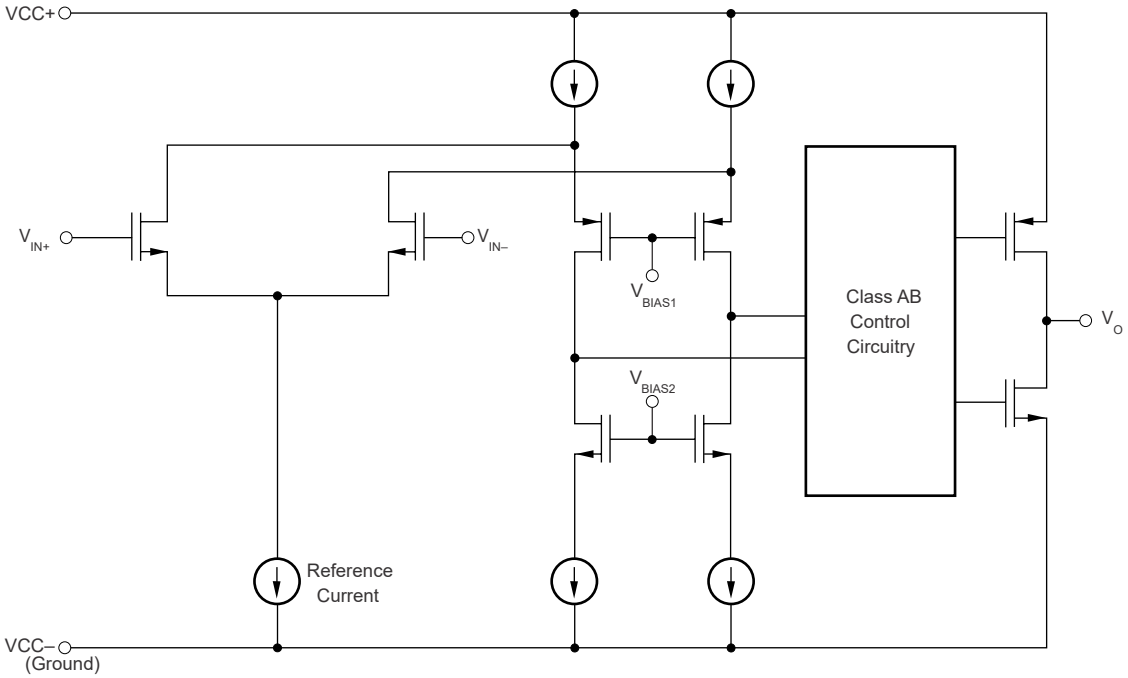
7 详细说明

7.1 概述

TL08xH 系列（包括 TL081H、TL082H 和 TL084H）是业界通用的 TL08x 系列（TL081、TL082 和 TL084）高压通用放大器的下一代产品。这些器件为对成本敏感且需要在高电压信号下实现高压摆率的应用（例如电机驱动和逆变器系统）提供了卓越的价值。

强大的多路复用器友好型输入级可提高设计灵活性、将共模电压范围扩展至正电源轨，并缩短多通道应用中的趋稳时间。低偏移电压（典型值 1mV）和低偏移电压漂移 (2μV/°C) 使得 TL08xH 系列可用于要求精确电流和电压检测的严苛应用场合。高电压工作能力（高达 40V）和高压摆率 (20V/μs) 使 TL08xH 系列成为具有快速瞬变特性的高压应用的首选。

7.2 功能方框图



7.3 特性说明

7.3.1 总谐波失真

电路内的电子元件会在音频信号中产生谐波失真。总计谐波失真 (THD) 是衡量音频系统中信号所积累的谐波失真的指标。这些器件具有 0.003% 的极低 THD，这意味着 TL08x 器件用在音频信号应用中时几乎不生成谐波失真。

7.3.2 压摆率

转换率是指运算放大器在输入发生变化时可以改变输出的速率。这些器件具有 20V/μs 的转换率。

7.4 器件功能模式

这些器件会在连接电源时通电。该器件可根据应用情况作为单电源运算放大器或双电源放大器使用。

Copyright © 2025 Texas Instruments Incorporated

8 应用和实施

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 应用信息

TL08x 系列运算放大器可用于多种应用。本节中的几个应用展示了这些器件在所有应用中所采用的原理。

8.2 典型应用

8.2.1 反相放大器应用

运算放大器的典型应用是反相放大器。该放大器在输入端接受正电压，然后将该电压变为同样幅度的负电压。该放大器还会以相同的方式将负电压变为正电压。

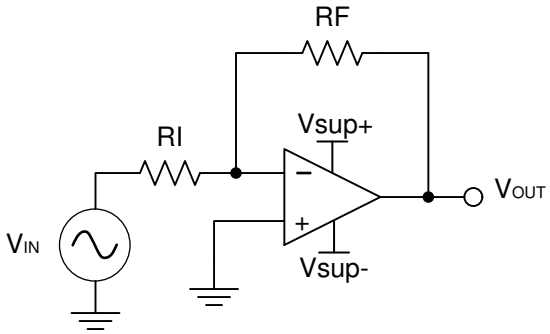


图 8-1. 反相放大器应用原理图

8.2.1.1 设计要求

选择的电源电压应高于输入和输出范围。例如，此应用将 ±0.5V 的信号扩展到 ±1.8V。将电源设置在 ±12V 就足以适应此应用。

8.2.1.2 详细设计过程

确定反相放大器需要的增益：

$$A_V = \frac{VOUT}{VIN} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

确定所需增益后，选择 RI 或 RF 的阻值。由于放大器电路使用毫安级电流，因此需要选择 kΩ 级阻值。对于本示例，选择 RI 为 10kΩ，这意味着 RF 使用 36kΩ。RF 值由 方程式 3 确定。

$$A_V = -\frac{RF}{RI} \quad (3)$$

8.2.1.3 应用曲线

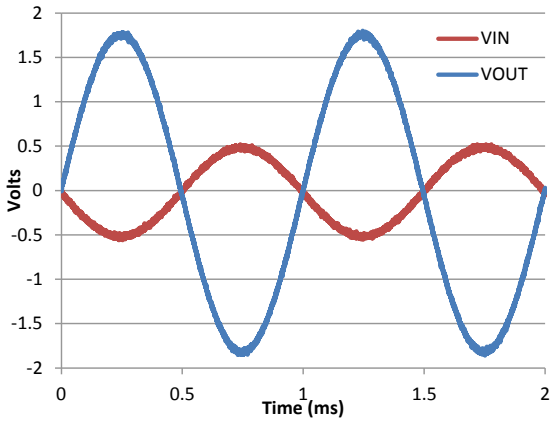


图 8-2. 反相放大器的输入和输出电压

8.3 电源相关建议

小心

单电源的电源电压超过 36V 或双电源的电源电压范围超出 ±18V 可能会对器件造成损坏（请参阅节 5.1）。

将 0.1µF 旁路电容器置于电源引脚附近，以减少来自高噪声电源或高阻抗电源的耦合误差。有关旁路电容器放置的更多详细信息，请参阅节 8.4。

8.4 布局

8.4.1 布局指南

为了实现器件的出色工作性能，请采用良好的 PCB 布局实践，包括：

- 噪声可通过全部电路电源引脚以及运算放大器自身传入模拟电路。旁路电容器用于为局部模拟电路提供低阻抗电源，从而降低耦合噪声。
  - 在每个电源引脚和接地端之间连接低等效串联电阻 (ESR) 0.1 µ F 陶瓷旁路电容器，并尽量靠近器件放置。针对单电源应用，V+ 与接地端之间可以接入单个旁路电容器。
- 将电路中的模拟部分和数字部分单独接地是最简单、最有效的噪声抑制方法之一。多层 PCB 上的一层或多层通常专门用于作为接地平面。接地层有助于散热和减少 EMI 噪声拾取。应将数字地和模拟地在物理上分开，并注意接地电流的流向。
- 为了减少寄生耦合，应让输入走线尽可能远离电源或输出走线。如果这些走线不能保持分离状态，请让敏感走线与有噪声的走线垂直相交，而不是平行相交。
- 外部元件应尽量靠近器件放置。如节 8.4.2 中所示，使 RF 和 RG 接近反相输入可尽可能减小寄生电容。
- 尽可能缩短输入走线的长度。切记，输入布线是电路中最敏感的部分。
- 考虑在关键布线周围设定驱动型低阻抗保护环。保护环能有效减少来自附近电位不同的走线的泄漏电流。

Copyright © 2025 Texas Instruments Incorporated

8.4.2 布局示例

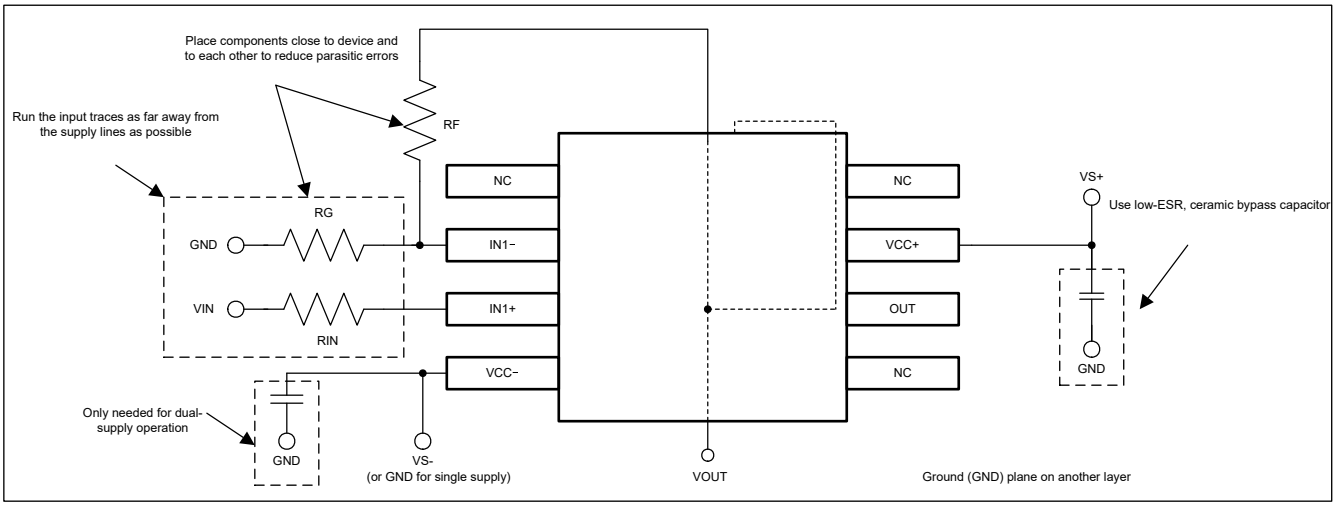


图 8-3. 非反相配置的运算放大器电路板布局

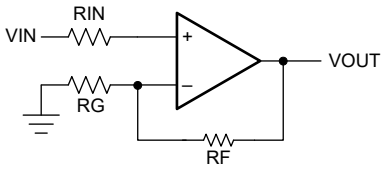


图 8-4. 非反相配置的运算放大器原理图

9 器件和文档支持

9.1 器件支持

9.1.1 器件命名规则

表 9-1. 器件命名规则

器件型号	定义
TL08*xyzzzzzz*	*x* 是通道数
	如果 *y* = H，则裸片采用最新流程制造 (CSO：RFB)。 节 5.7 和 节 5.10 描述了新裸片的性能。
	如果 *y* ≠ H 且 *y* ≠ M，则裸片采用传统流程制造 (CSO: SFAB) 或采用最新流程 (CSO: RFB)。 节 5.8 和 节 5.9 描述了原始裸片的性能。
	如果 *y* = M，则该器件适用于 –55°C 到 +125°C 的工作温度范围。裸片采用传统工艺流程 (CSO:SFAB) 制造。 *z* 所代表的字母和数字表示分级和封装选项，其说明见 节 5.8 以及数据表末尾的 *封装选项附录*。

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision N (June 2024) to Revision O (September 2025)	Page
• 将*特性* 中的 V_n = 18nV/ √Hz 更改为 V_n = 37nV/ √Hz	1
• 更新了*器件信息* 表	1
• 在*逻辑符号* 的图 1 中，将 TL081 更改为仅 TL081 SOIC；在图 2 中，将 TL081 更改为 TL081 (每个放大器)	1
• 在图 4-1 和图 4-2 中，将引脚名称从 V– 更新为 VCC –、将 V+ 更新为 VCC +	3
• 更新了图 4-3 的标题	3

Copyright © 2025 Texas Instruments Incorporated

- 更新了图 4-4 的标题 3
- 将表 4-2 中的 TL081x 更改为 TL081C 3
- 将 HBM 值从 2000V 更新为 1500V 9
- 删除了 *THD+N 比率随频率变化*、*THD+N 随输出幅度变化*，以及 *CMRR 和 PSRR 随频率变化* 的曲线图 17
- 在图 6-4 *测试图 4* 中添加了“（仅适用于 SO 封装）” 23
- 删除了 *系统示例* 部分 26
- 更新了 *布局指南* 中的第二个要点 26
- 添加了 *器件命名规则* 表 28

Changes from Revision M (December 2021) to Revision N (June 2024) **Page**

- 通过合并 TL08xH 和 TL08xx 规格更改了绝对最大额定值、ESD 等级、建议运行条件和热性能信息部分 9
- 通过合并 TL08xC、TL08xAC、TL08xBC、TL08xI 和 TL08xM 规格更改了电气特性表 14
- 将所有非 NS/非 PS 封装和非 TL08xM 器件的增益带宽从 3MHz 增加到 5.25MHz 14
- 合并了 TL08xC、TL08xAC、TL08xBC、TL08xI 和 TL08xM 开关特性表，并重命名为电气特性（交流）表 16
- 将所有非 PS/非 NS 封装和所有非 TL08xM 器件的 1kHz 输入电压噪声密度更改为 37nV/ √Hz 16
- 将所有非 PS/非 NS 封装和所有非 TL08xM 器件的 THD+N 更改为 0.00012% 16
- 更新了 *功能方框图* 和 *特性说明* 部分 24

Changes from Revision L (July 2021) to Revision M (December 2021) **Page**

- 更正了 *引脚配置和功能* 部分的 DCK 引脚图和引脚表 3

11 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

Copyright © 2025 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9851501Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9851501Q2A TL082MFKB
5962-9851501QPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9851501QPA TL082M
5962-9851503Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9851503Q2A TL084 MFKB
5962-9851503QCA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9851503QCA TL084MJB
TL081ACD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	081AC
TL081ACDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	081AC
TL081ACDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	081AC
TL081ACP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL081ACP
TL081ACP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL081ACP
TL081BCD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	081BC
TL081BCDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	081BC
TL081BCDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	081BC
TL081BCP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL081BCP
TL081BCP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL081BCP
TL081CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	TL081C
TL081CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL081C
TL081CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL081C
TL081CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL081CP
TL081CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL081CP
TL081CPE4	Active	Production	PDIP (P) | 8	50 | TUBE	-	Call TI	Call TI	0 to 70	
TL081CPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T081
TL081CPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T081
TL081HIDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	T81V

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL081HIDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T81V
TL081HIDCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1IP
TL081HIDCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1IP
TL081HIDR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL081D
TL081HIDR.A	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL081D
TL081IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL081I
TL081IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL081I
TL081IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL081IP
TL081IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL081IP
TL082ACD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	082AC
TL082ACDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC
TL082ACDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	082AC
TL082ACDRE4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	0 to 70	
TL082ACP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL082ACP
TL082ACP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL082ACP
TL082ACPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082A
TL082ACPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082A
TL082BCD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	082BC
TL082BCDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC
TL082BCDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC
TL082BCDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC
TL082BCDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	082BC
TL082BCP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL082BCP
TL082BCP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL082BCP
TL082BCPE4	Active	Production	PDIP (P) | 8	50 | TUBE	-	Call TI	Call TI	0 to 70	
TL082CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C
TL082CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL082C
TL082CDRE4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	0 to 70	
TL082CDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	0 to 70	
TL082CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL082CP
TL082CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL082CP

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL082CPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082
TL082CPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082
TL082CPSRG4	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082
TL082CPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082
TL082CPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T082
TL082CPWRG4	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	-	Call TI	Call TI	0 to 70	
TL082HIDDFR	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	082F
TL082HIDDFR.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	082F
TL082HIDR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL082D
TL082HIDR.A	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL082D
TL082HIPWR	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	082HPW
TL082HIPWR.A	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	082HPW
TL082IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I
TL082IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL082I
TL082IDRE4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
TL082IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL082IP
TL082IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL082IP
TL082IPE4	Active	Production	PDIP (P) | 8	50 | TUBE	-	Call TI	Call TI	-40 to 85	
TL082IPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z082
TL082IPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z082
TL082MFKB	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9851501Q2A TL082MFKB
TL082MFKB.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9851501Q2A TL082MFKB
TL082MJG	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL082MJG
TL082MJG.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL082MJG
TL082MJGB	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9851501QPA TL082M
TL082MJGB.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9851501QPA TL082M

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL084ACD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	TL084AC
TL084ACDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC
TL084ACDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084AC
TL084ACN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL084ACN
TL084ACN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL084ACN
TL084ACNSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084A
TL084ACNSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084A
TL084BCDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC
TL084BCDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC
TL084BCDR1G4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC
TL084BCDR1G4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084BC
TL084BCDRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	-	Call TI	Call TI	0 to 70	
TL084BCN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL084BCN
TL084BCN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL084BCN
TL084BCNE4	Active	Production	PDIP (N) | 14	25 | TUBE	-	Call TI	Call TI	0 to 70	
TL084CD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	TL084C
TL084CDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C
TL084CDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084C
TL084CDRG4	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	TL084C
TL084CN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL084CN
TL084CN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL084CN
TL084CNSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084
TL084CNSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL084
TL084CPW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	0 to 70	T084
TL084CPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	T084
TL084CPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T084
TL084CPWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T084
TL084HIDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084HID
TL084HIDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084HID
TL084HIDYYR	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T084HDYY

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL084HIDYYR.A	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T084HDYY
TL084HIDYYRG4	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T084HDYY
TL084HIDYYRG4.A	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T084HDYY
TL084HIPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	TL084PW
TL084HIPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084PW
TL084IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I
TL084IDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL084I
TL084IDR1G4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084I
TL084IDR1G4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084I
TL084IDRE4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
TL084IDRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
TL084IN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL084IN
TL084IN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL084IN
TL084ING4	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TL084IN
TL084ING4.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TL084IN
TL084MFK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL084MFK
TL084MFK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL084MFK
TL084MFKB	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9851503Q2A TL084 MFKB
TL084MFKB.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9851503Q2A TL084 MFKB
TL084MJ	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL084MJ
TL084MJ.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TL084MJ
TL084MJB	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9851503QCA TL084MJB

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL084MJB.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9851503QC A TL084MJB
TL084QD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 125	TL084Q
TL084QDG4	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 125	TL084Q
TL084QDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q
TL084QDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q
TL084QDRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q
TL084QDRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL084Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TL082, TL082M, TL084, TL084M :

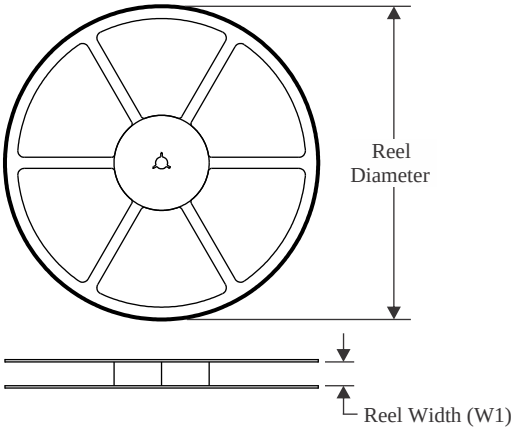
- Catalog : TL082, TL084
- Automotive : TL082-Q1, TL082-Q1
- Military : TL082M, TL084M

NOTE: Qualified Version Definitions:

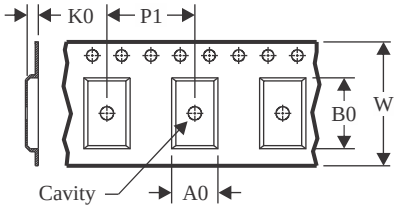
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

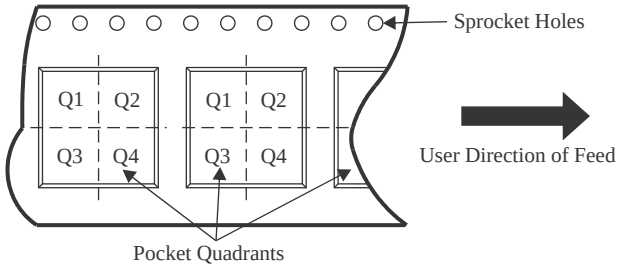


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

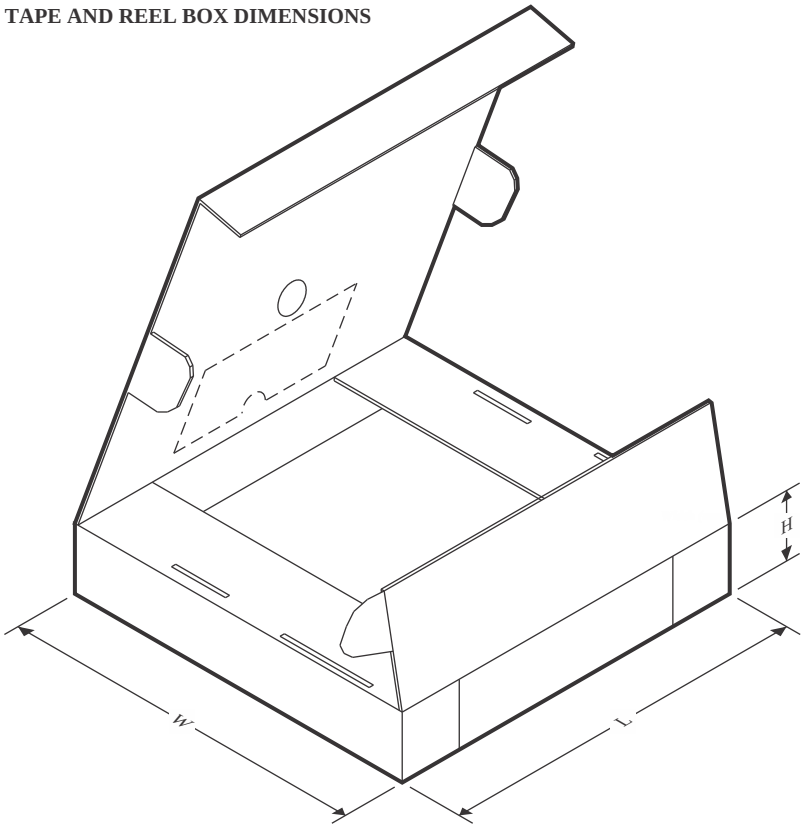


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL081ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL081HIDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL081HIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TL081HIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL081IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082ACPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL082BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082BCDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL082CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL082HIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL082HIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082HIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082HIPWR	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL082IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL082IDR	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
TL082IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL084ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084ACNSR	SOP	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
TL084BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084BCDR1G4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
TL084CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084CNSR	SOP	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
TL084CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL084CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL084CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL084CPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL084CPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL084HIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084HIDYYR	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TL084HIDYYRG4	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TL084HIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL084HIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL084IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
TL084IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084IDR1G4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084QDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL084QDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

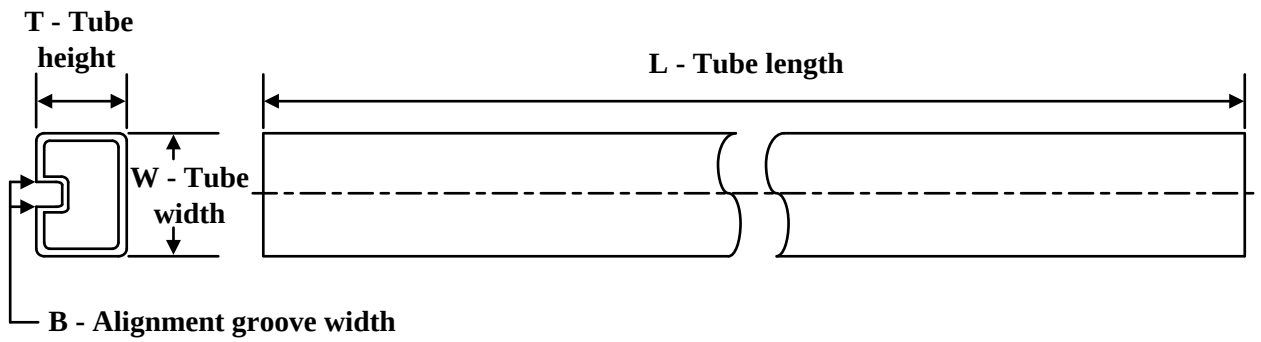


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL081ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL081BCDR	SOIC	D	8	2500	353.0	353.0	32.0
TL081CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL081CPSR	SO	PS	8	2000	353.0	353.0	32.0
TL081HIDBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TL081HIDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TL081HIDR	SOIC	D	8	3000	353.0	353.0	32.0
TL081IDR	SOIC	D	8	2500	353.0	353.0	32.0
TL082ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL082ACDR	SOIC	D	8	2500	367.0	367.0	35.0
TL082ACPSR	SO	PS	8	2000	353.0	353.0	32.0
TL082BCDR	SOIC	D	8	2500	353.0	353.0	32.0
TL082BCDRG4	SOIC	D	8	2500	353.0	353.0	32.0
TL082CDR	SOIC	D	8	2500	367.0	367.0	35.0
TL082CDR	SOIC	D	8	2500	353.0	353.0	32.0
TL082CPSR	SO	PS	8	2000	353.0	353.0	32.0
TL082CPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TL082HIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL082HIDR	SOIC	D	8	3000	367.0	367.0	35.0
TL082HIDR	SOIC	D	8	3000	353.0	353.0	32.0
TL082HIPWR	TSSOP	PW	8	3000	353.0	353.0	32.0
TL082IDR	SOIC	D	8	2500	353.0	353.0	32.0
TL082IDR	SOIC	D	8	2500	353.0	353.0	32.0
TL082IDR	SOIC	D	8	2500	367.0	367.0	35.0
TL082IPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TL084ACDR	SOIC	D	14	2500	353.0	353.0	32.0
TL084ACDR	SOIC	D	14	2500	353.0	353.0	32.0
TL084ACNSR	SOP	NS	14	2000	353.0	353.0	32.0
TL084BCDR	SOIC	D	14	2500	353.0	353.0	32.0
TL084BCDR1G4	SOIC	D	14	2500	353.0	353.0	32.0
TL084CDR	SOIC	D	14	2500	367.0	367.0	35.0
TL084CDR	SOIC	D	14	2500	353.0	353.0	32.0
TL084CNSR	SOP	NS	14	2000	353.0	353.0	32.0
TL084CPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TL084CPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL084CPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TL084CPWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
TL084CPWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
TL084HIDR	SOIC	D	14	2500	353.0	353.0	32.0
TL084HIDYYR	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TL084HIDYYRG4	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TL084HIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL084HIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TL084IDR	SOIC	D	14	2500	367.0	367.0	35.0
TL084IDR	SOIC	D	14	2500	353.0	353.0	32.0
TL084IDR1G4	SOIC	D	14	2500	353.0	353.0	32.0
TL084QDR	SOIC	D	14	2500	353.0	353.0	32.0
TL084QDRG4	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9851501Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9851503Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
TL081ACP	P	PDIP	8	50	506	13.97	11230	4.32
TL081ACP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL081BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL081BCP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL081CP	P	PDIP	8	50	506	13.97	11230	4.32
TL081CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL081IP	P	PDIP	8	50	506	13.97	11230	4.32
TL081IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL082ACP	P	PDIP	8	50	506	13.97	11230	4.32
TL082ACP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL082BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL082BCP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL082CP	P	PDIP	8	50	506	13.97	11230	4.32
TL082CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL082IP	P	PDIP	8	50	506	13.97	11230	4.32
TL082IP	P	PDIP	8	50	506	13.97	11230	4.32
TL082IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL082IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL082MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TL082MFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA
TL084ACN	N	PDIP	14	25	506	13.97	11230	4.32
TL084ACN	N	PDIP	14	25	506	13.97	11230	4.32
TL084ACN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL084ACN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL084BCN	N	PDIP	14	25	506	13.97	11230	4.32
TL084BCN	N	PDIP	14	25	506	13.97	11230	4.32
TL084BCN.A	N	PDIP	14	25	506	13.97	11230	4.32

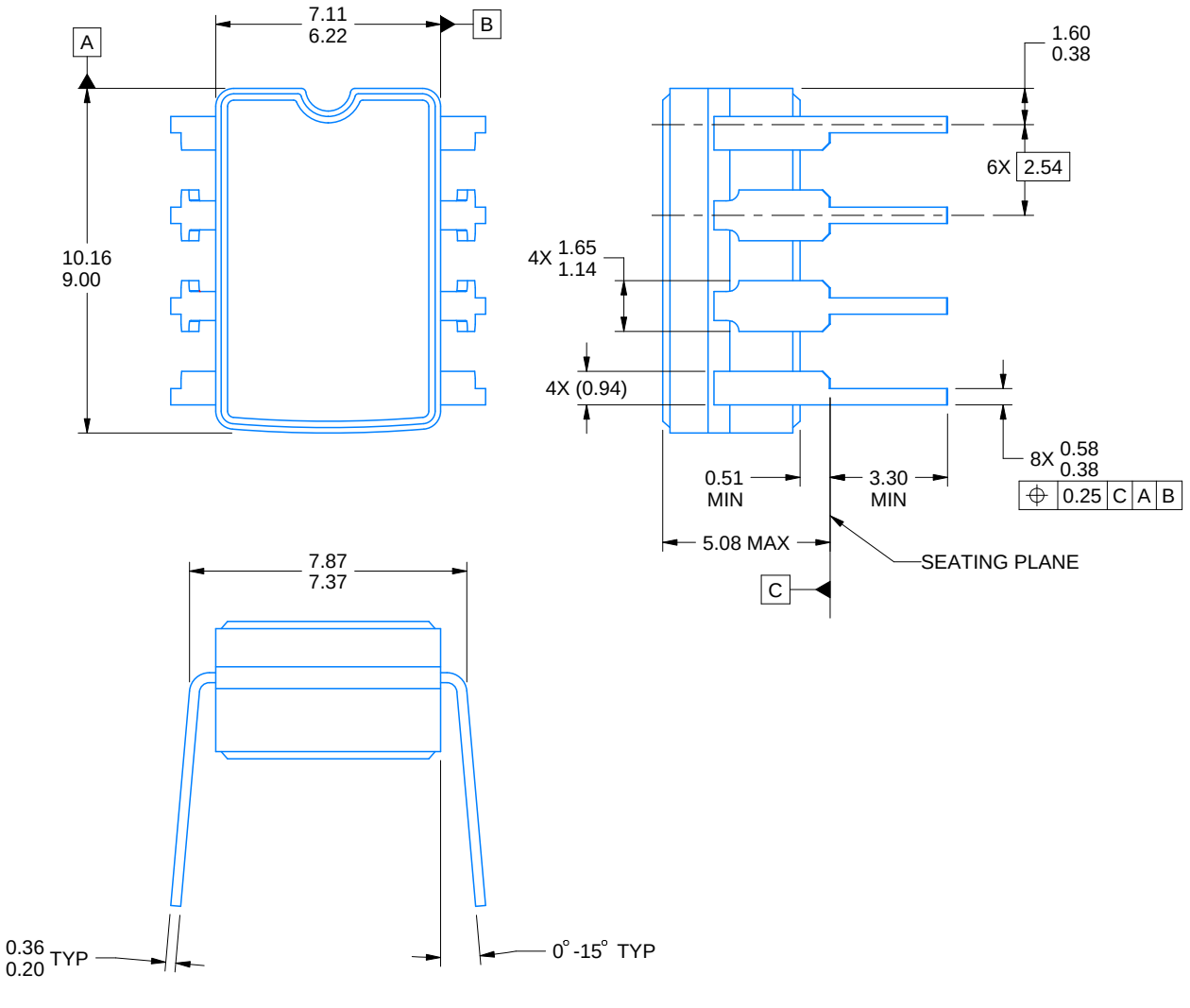
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL084BCN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL084CN	N	PDIP	14	25	506	13.97	11230	4.32
TL084CN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL084IN	N	PDIP	14	25	506	13.97	11230	4.32
TL084IN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL084ING4	N	PDIP	14	25	506	13.97	11230	4.32
TL084ING4.A	N	PDIP	14	25	506	13.97	11230	4.32
TL084MFK	FK	LCCC	20	55	506.98	12.06	2030	NA
TL084MFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
TL084MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TL084MFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

NOTES:

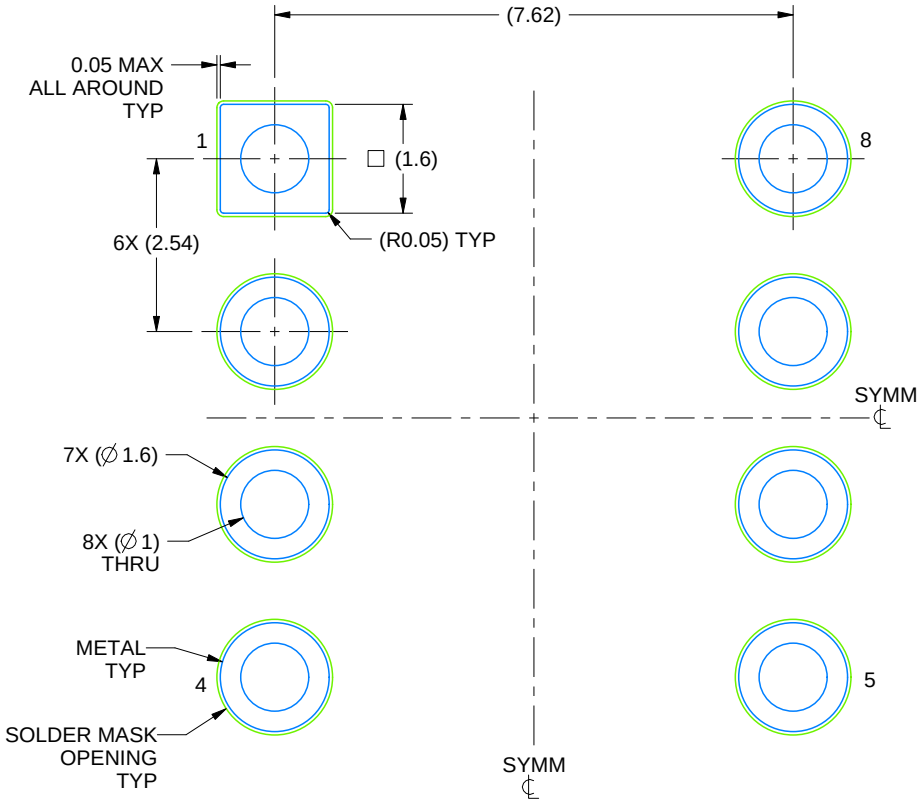
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

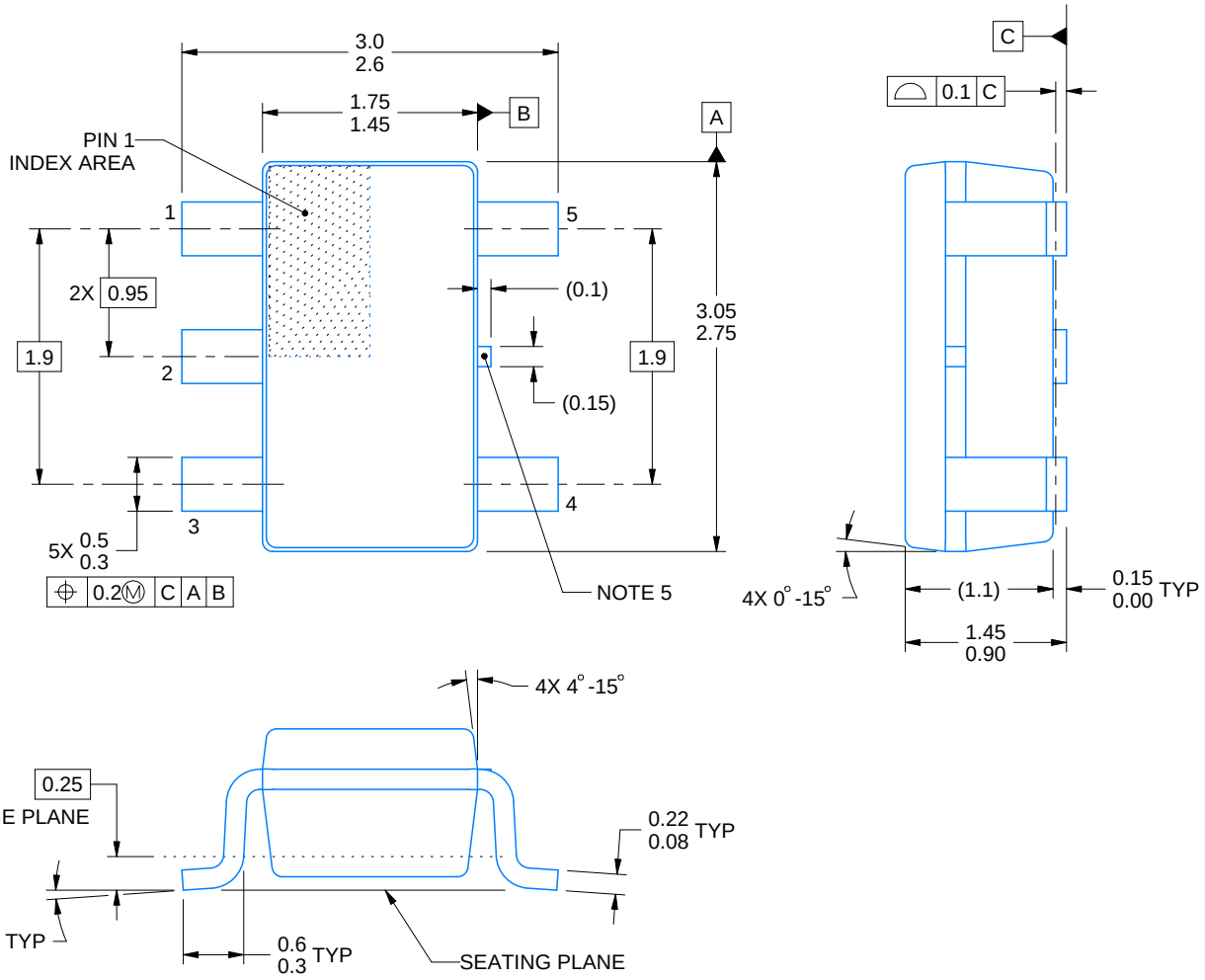
4230036/A 09/2023

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

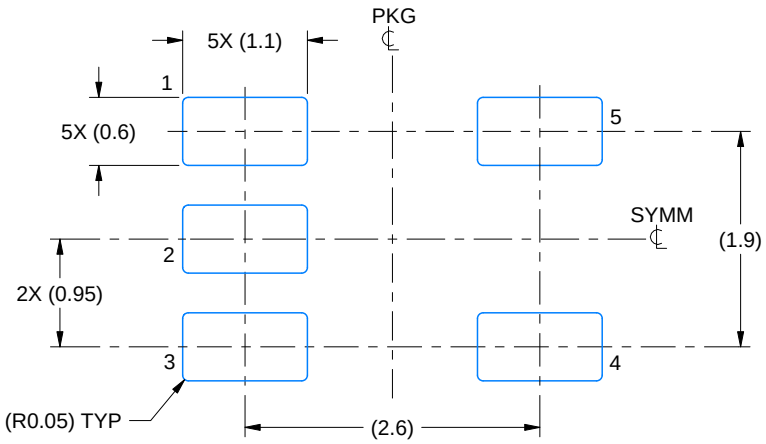
SMALL OUTLINE TRANSISTOR



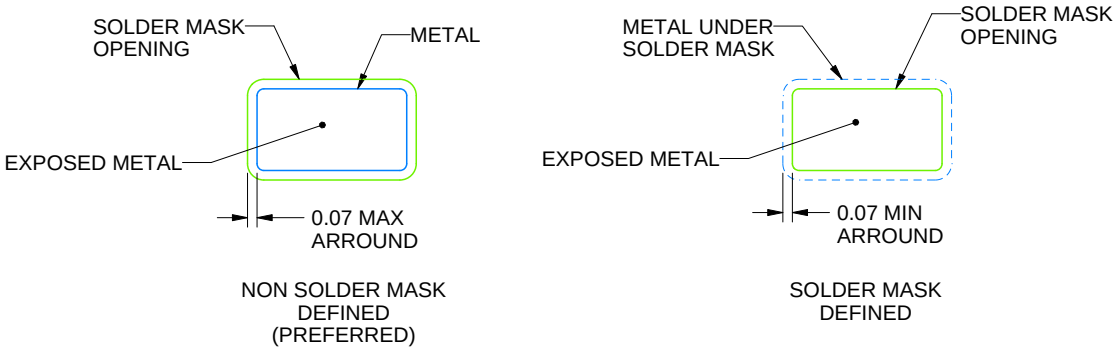
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

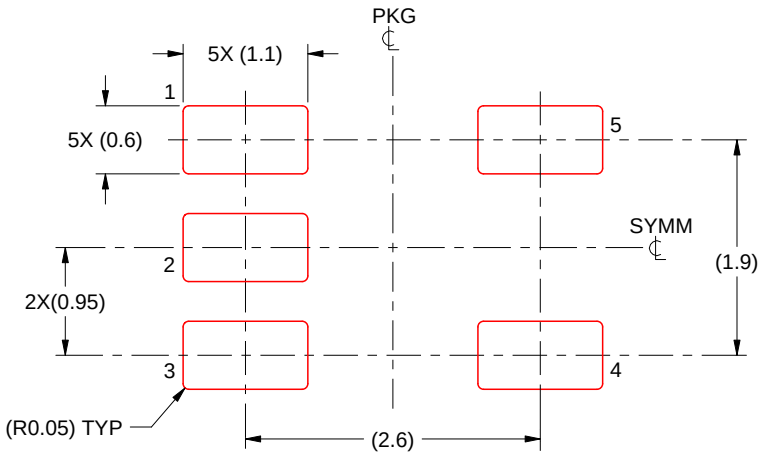


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

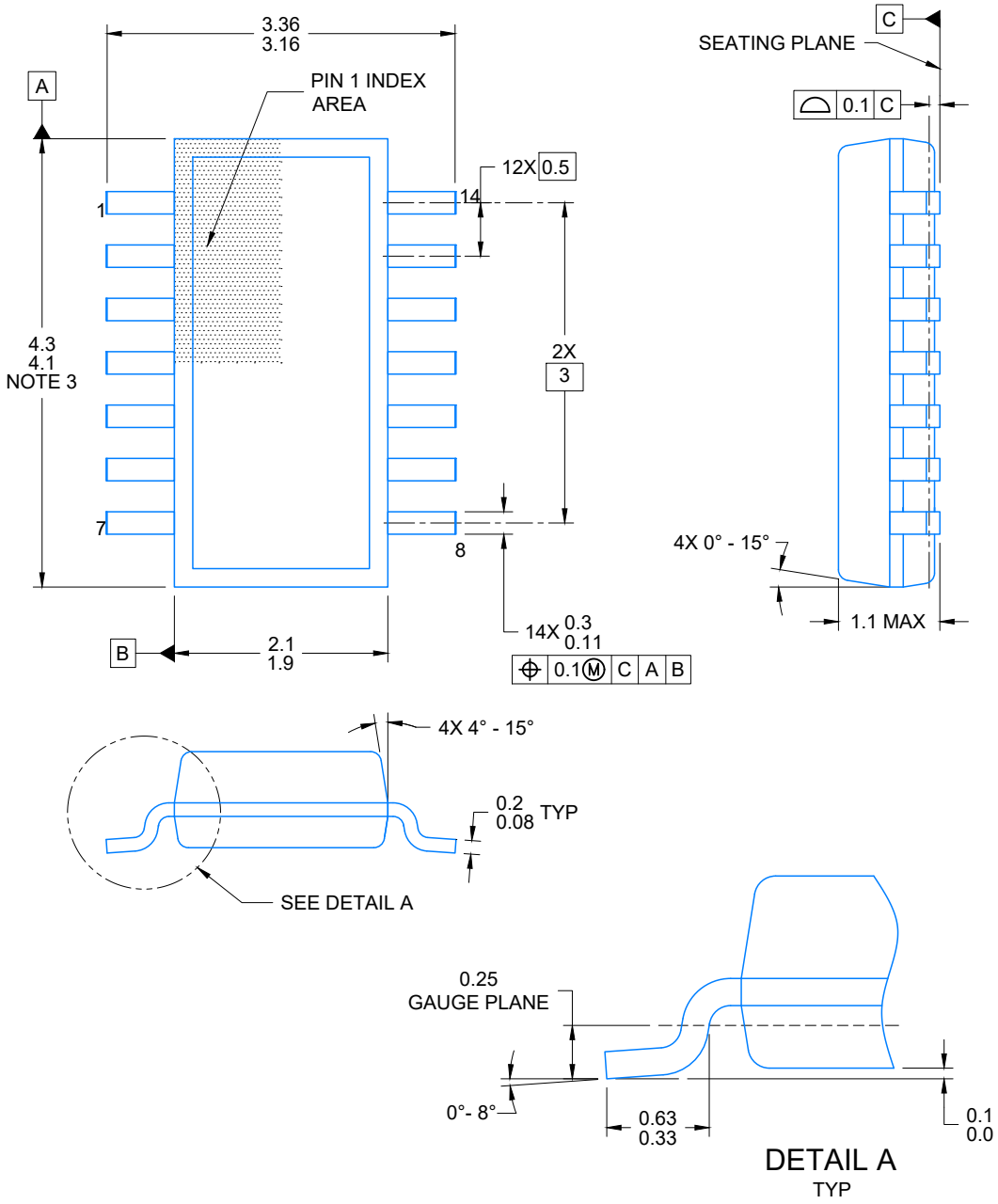
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DYY0014A

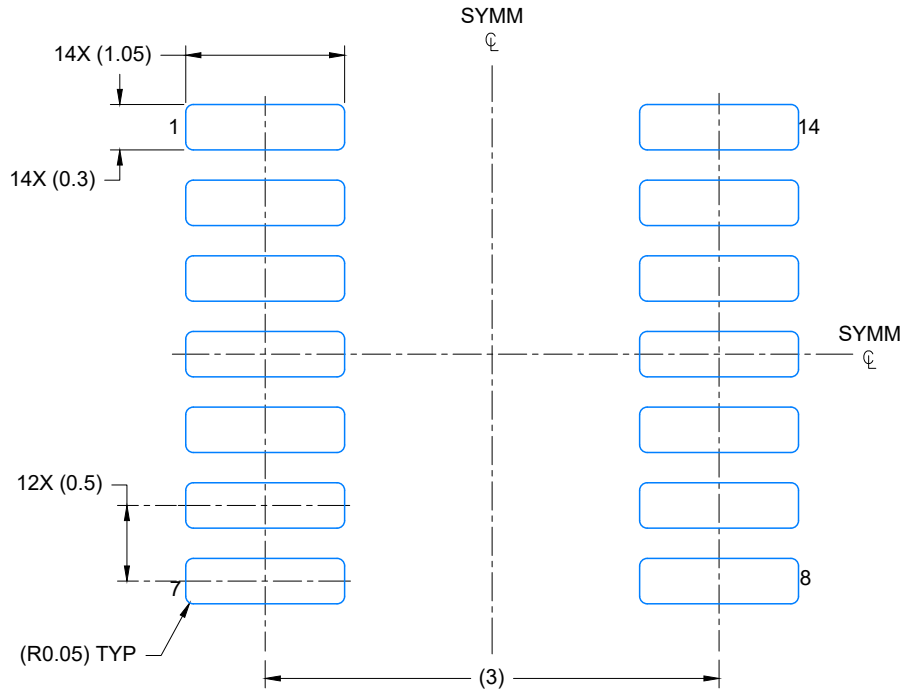
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

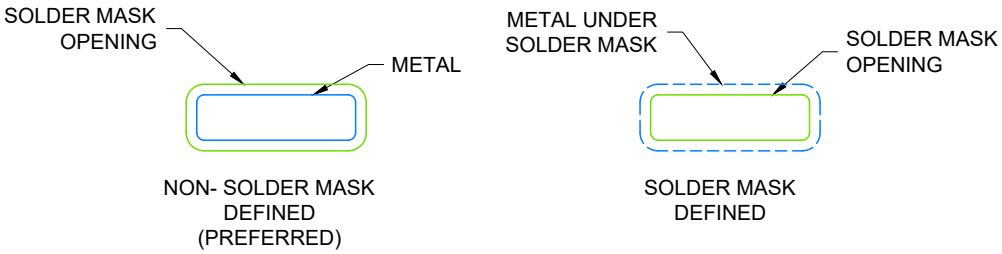


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

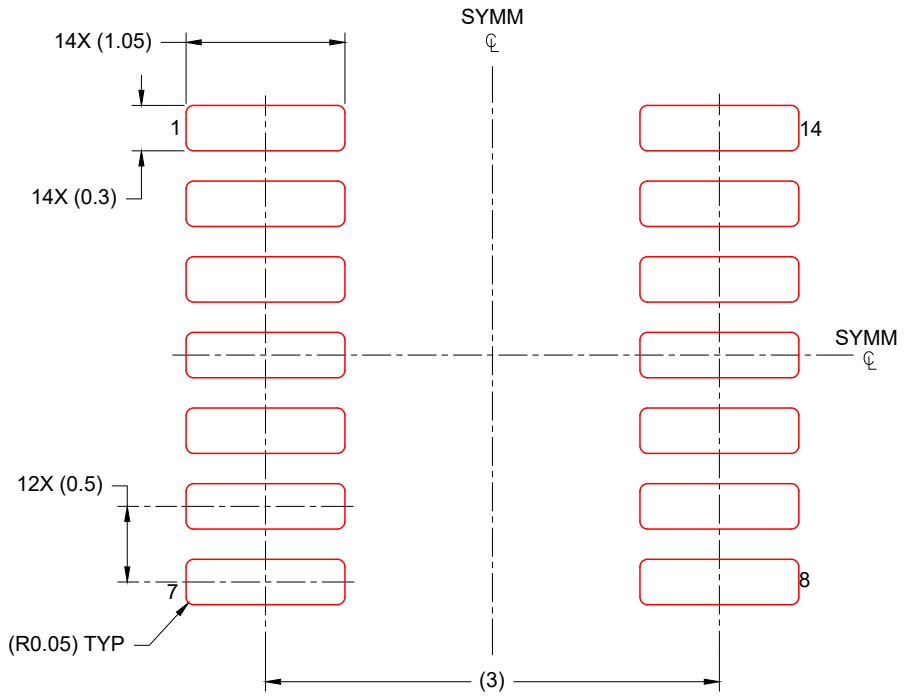


SOLDER MASK DETAILS

4224643/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

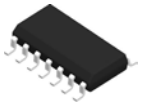


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

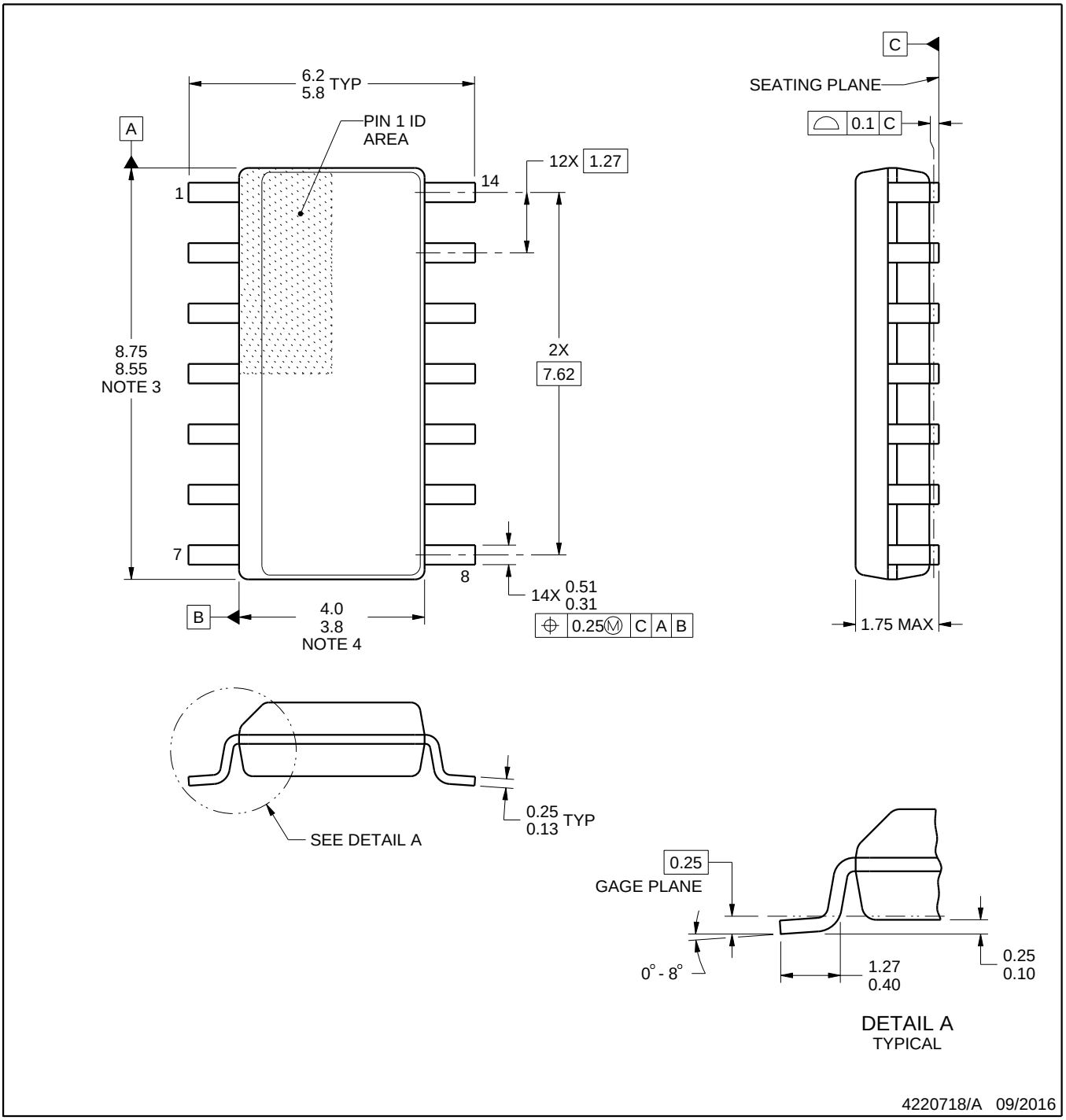


PACKAGE OUTLINE

D0014A

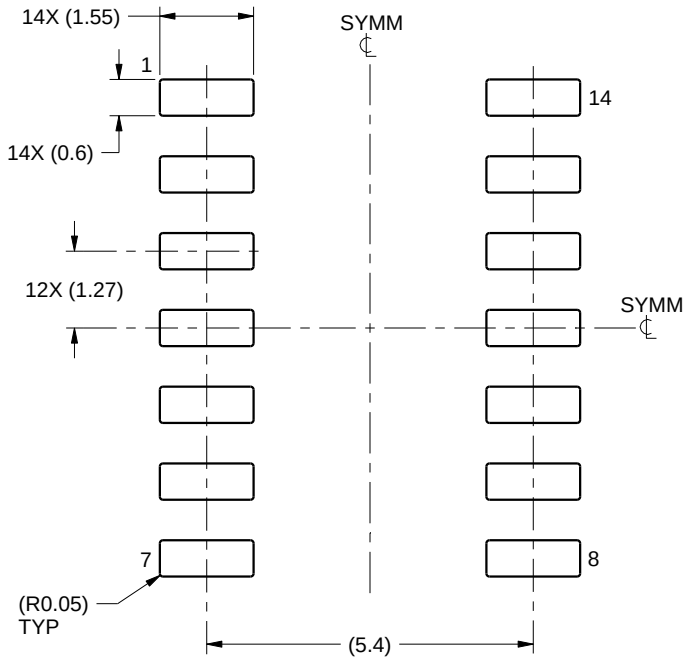
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

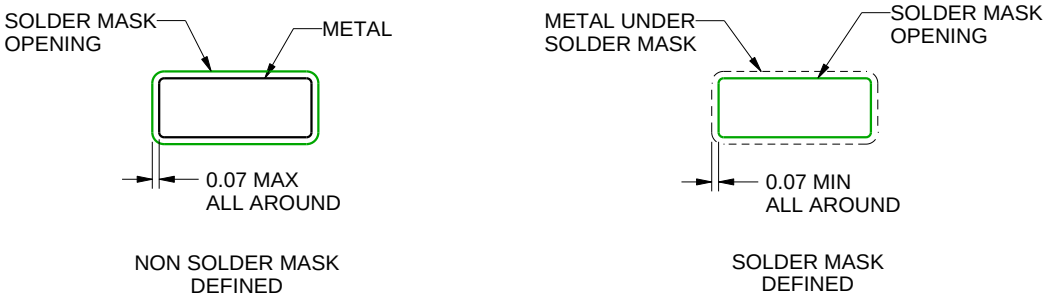


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

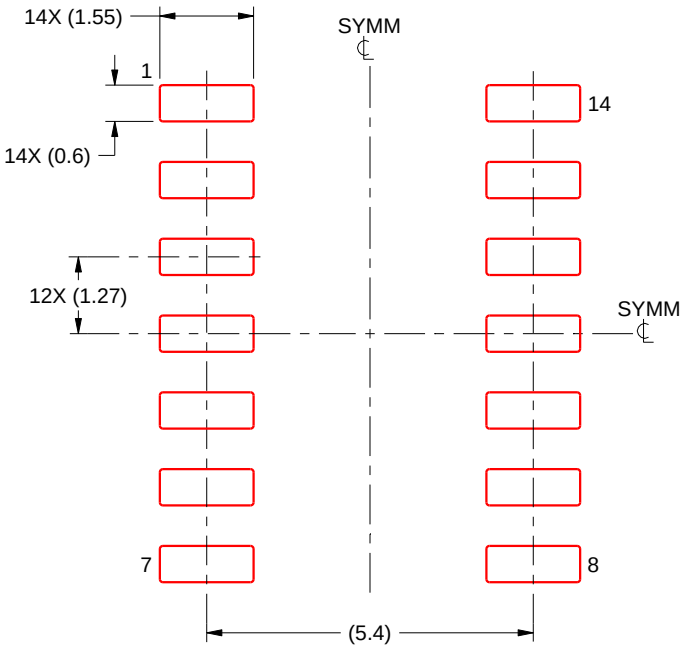
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

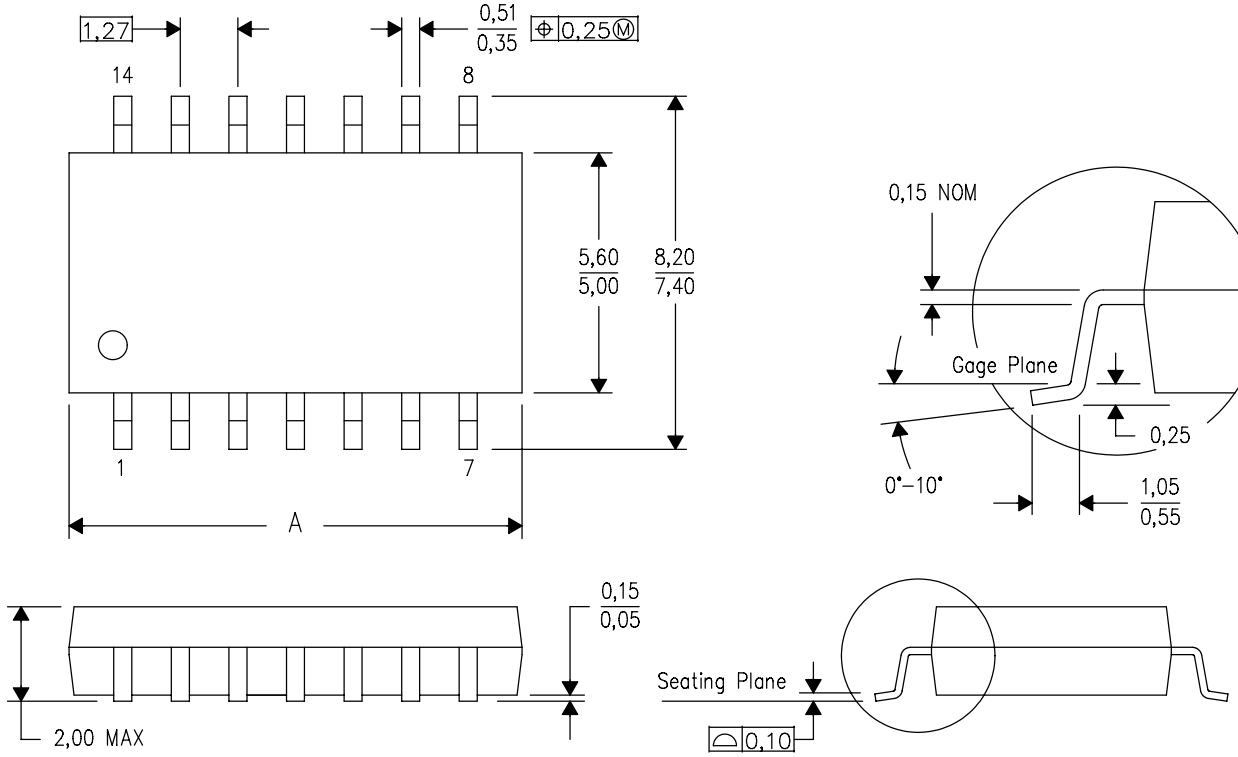
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

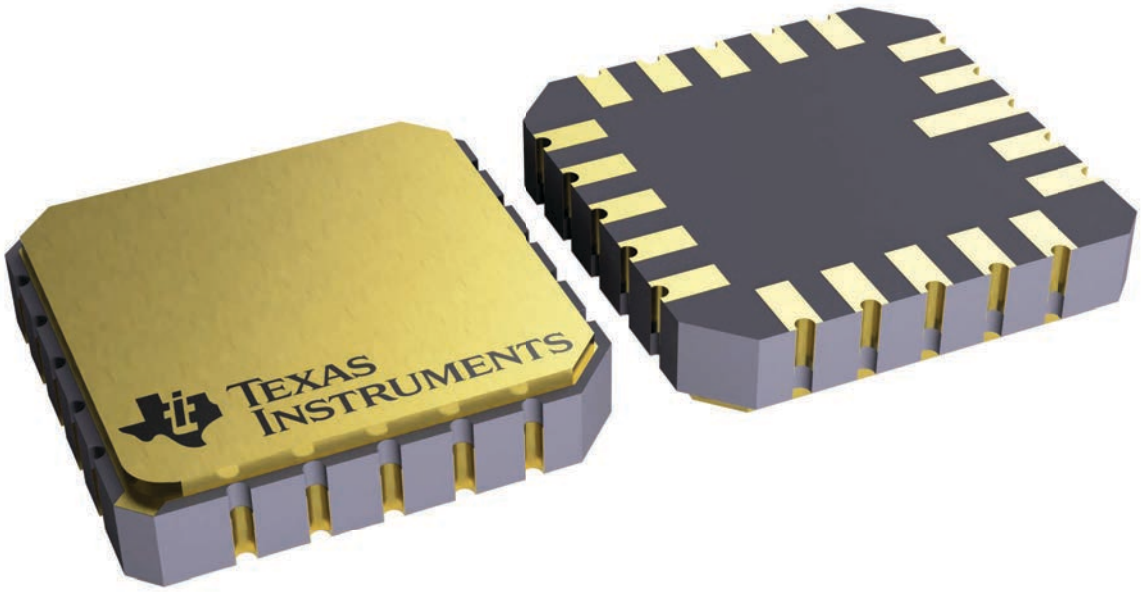
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

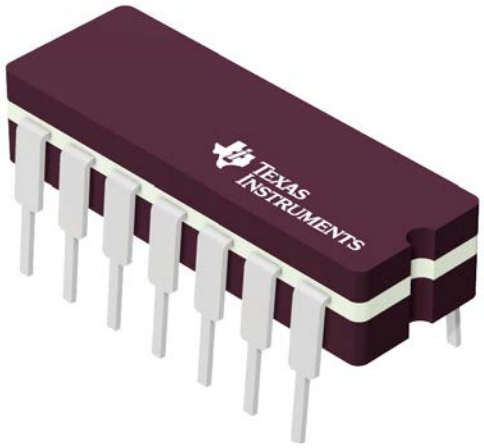


4229370VA\

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

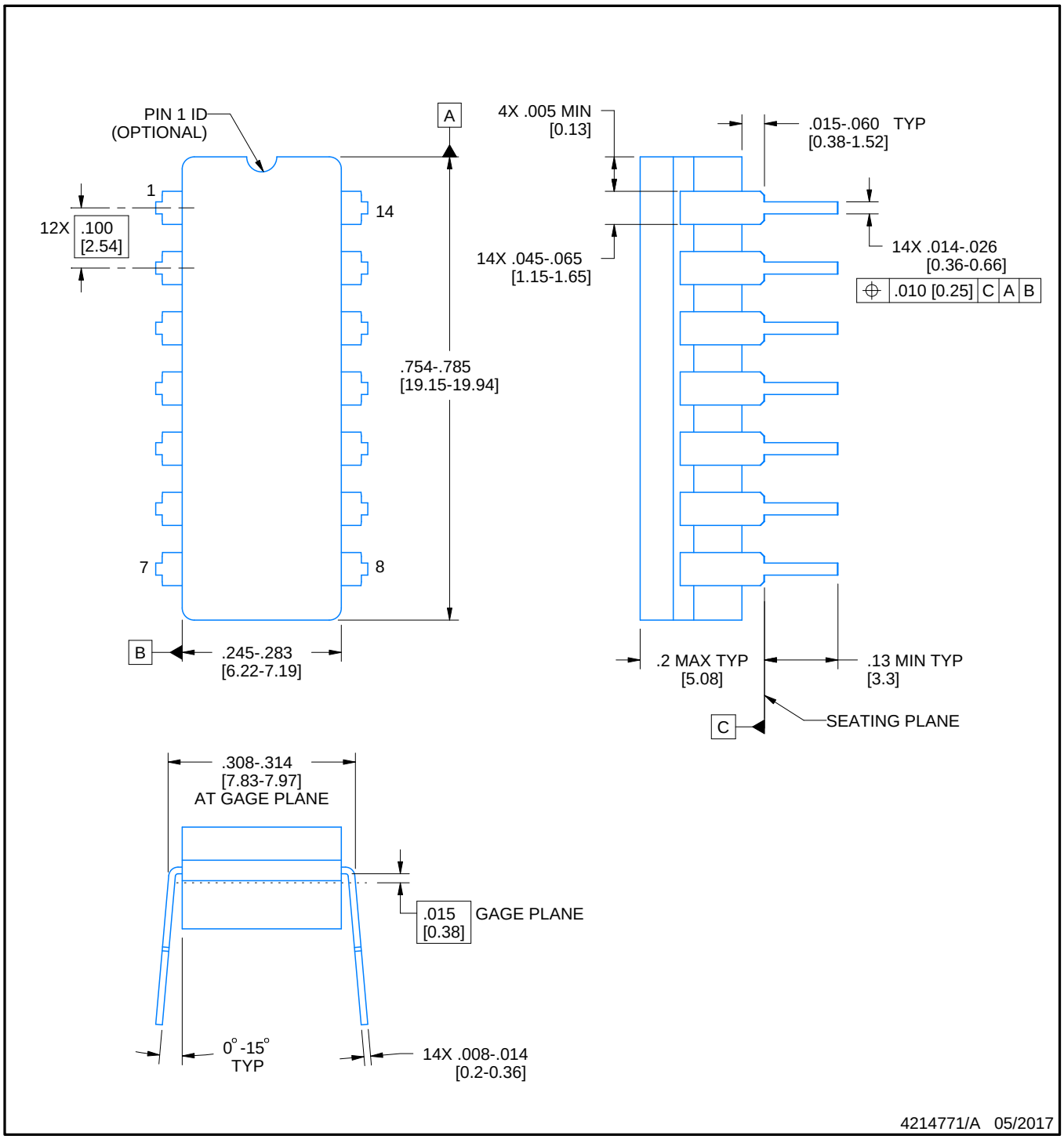


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

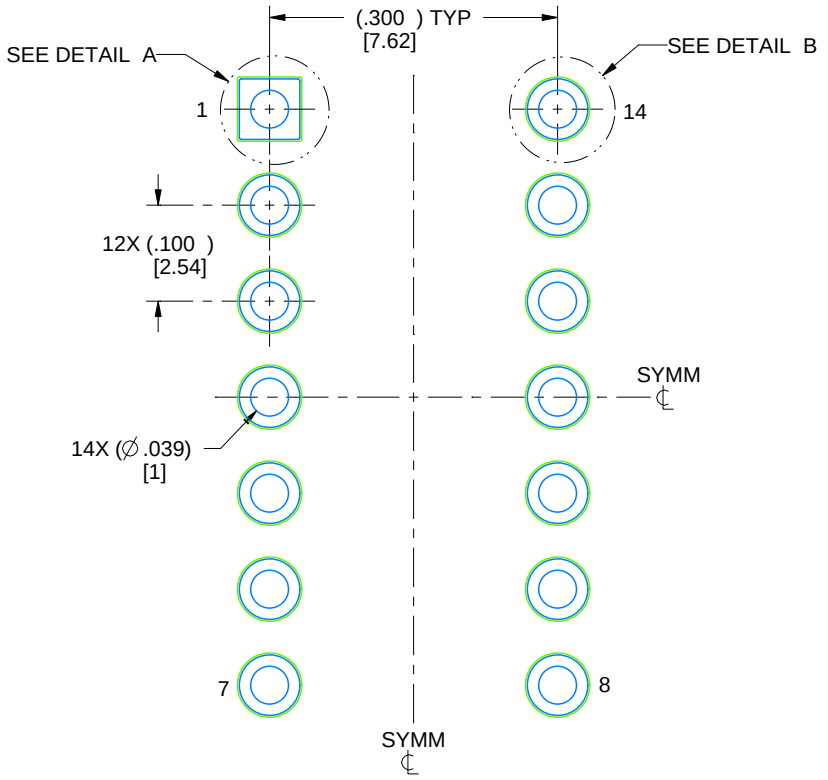
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

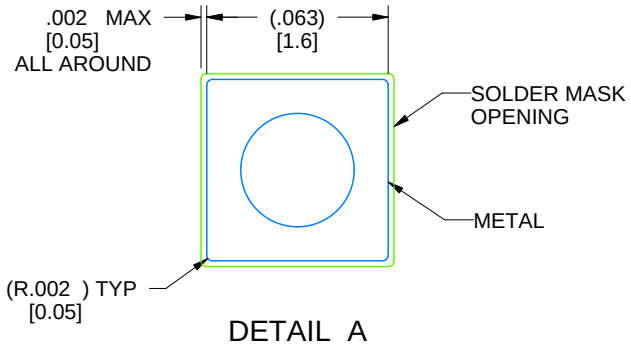
J0014A

CDIP - 5.08 mm max height

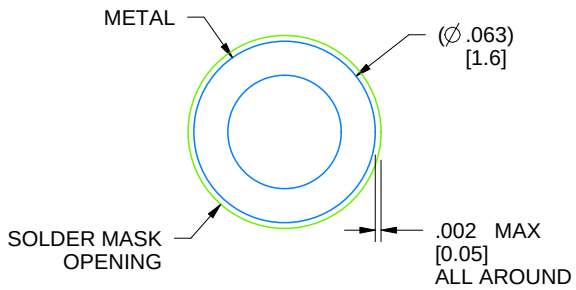
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

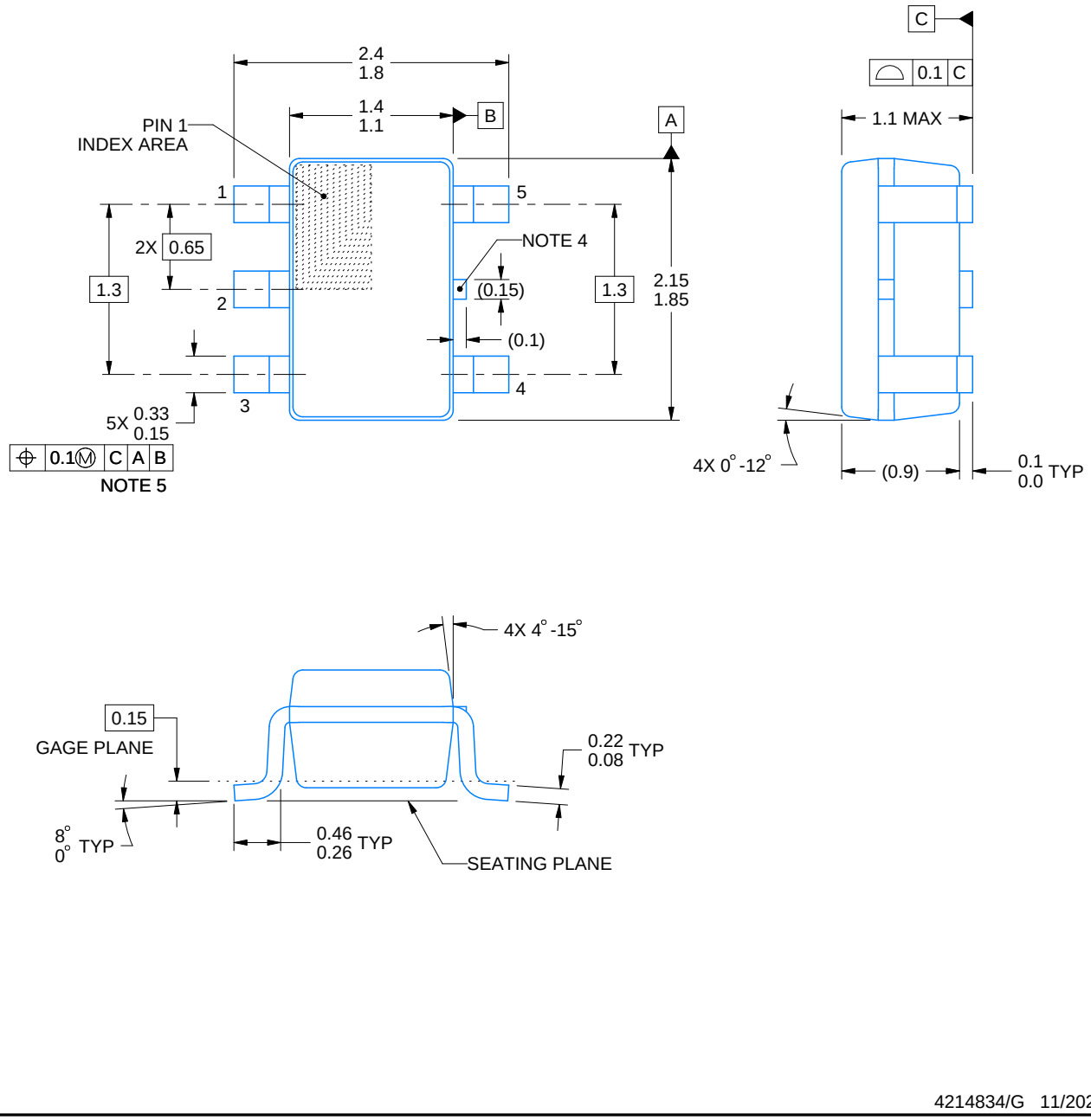
4214771/A 05/2017

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

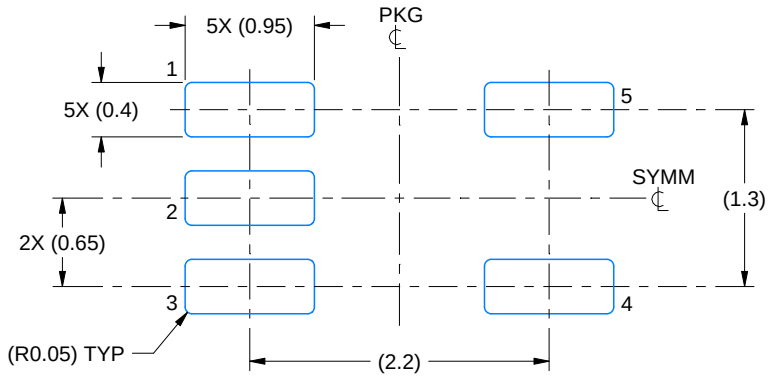
SMALL OUTLINE TRANSISTOR



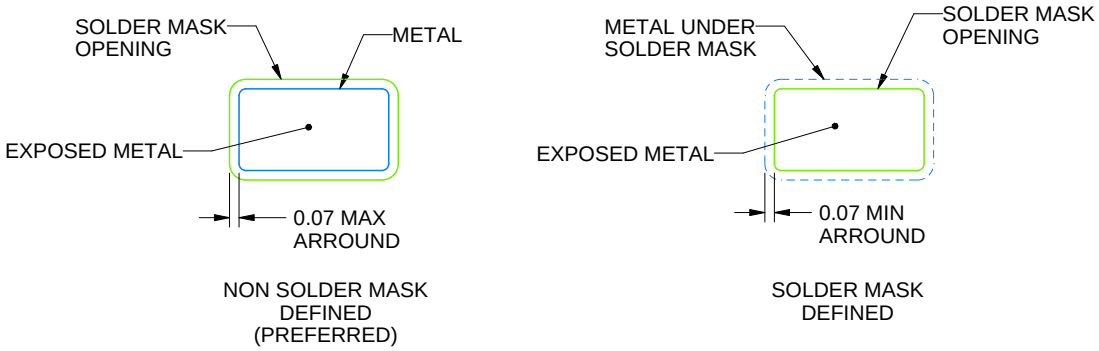
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

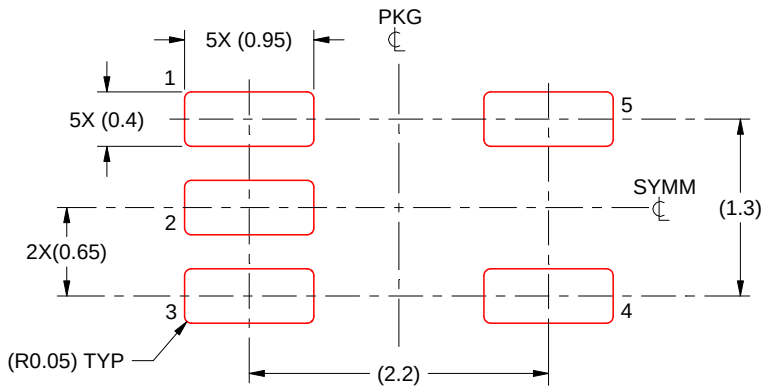


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

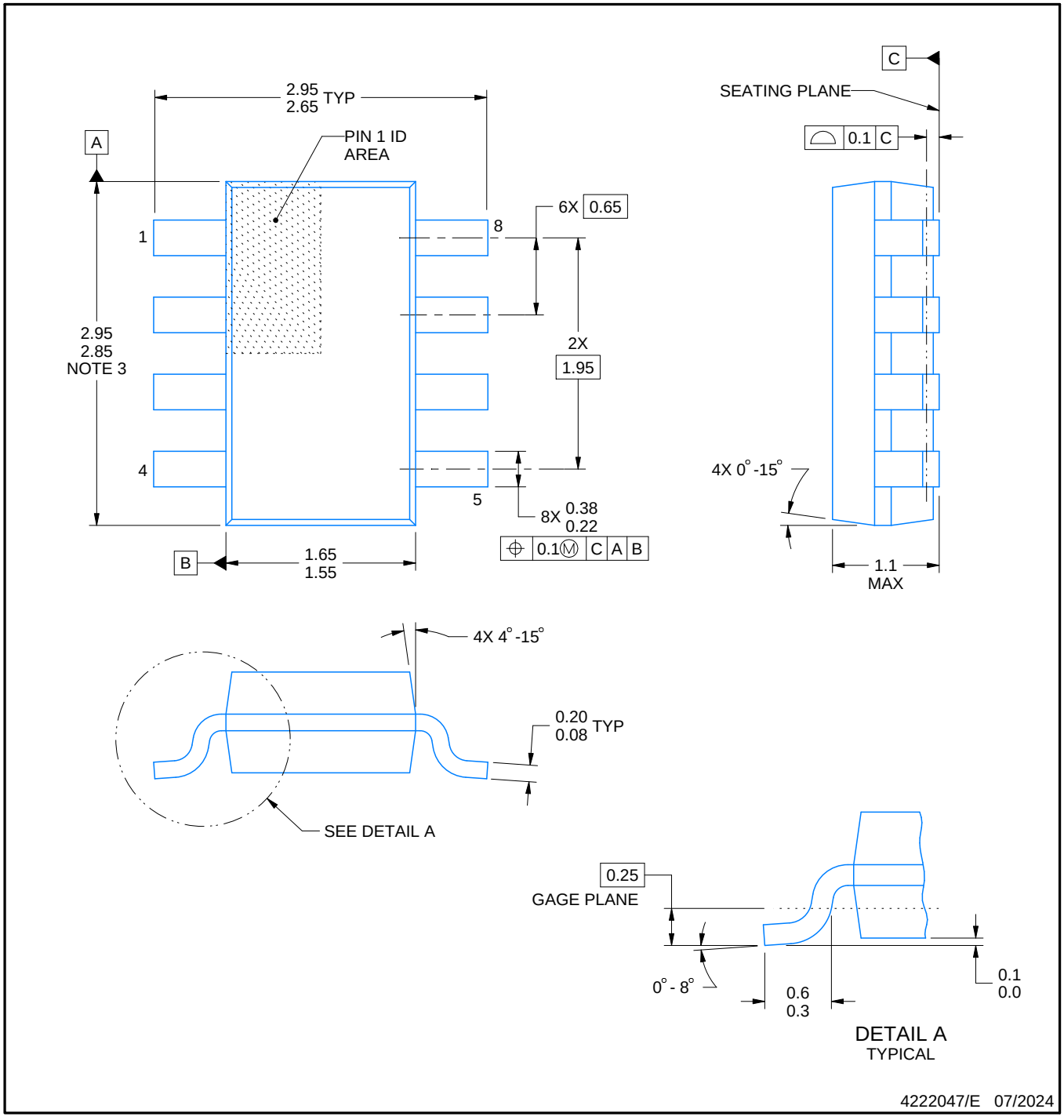
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DDF0008A

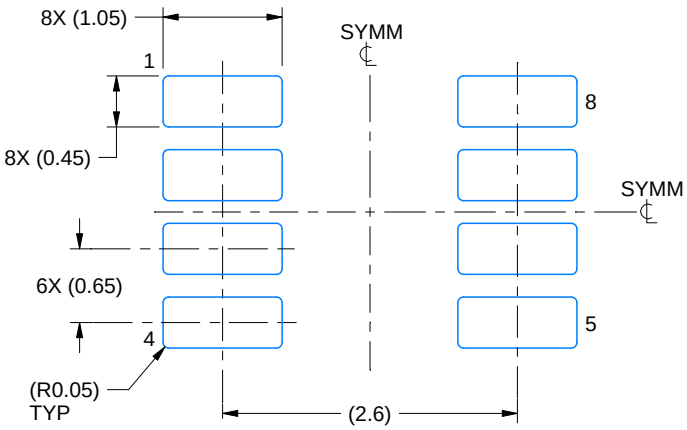
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

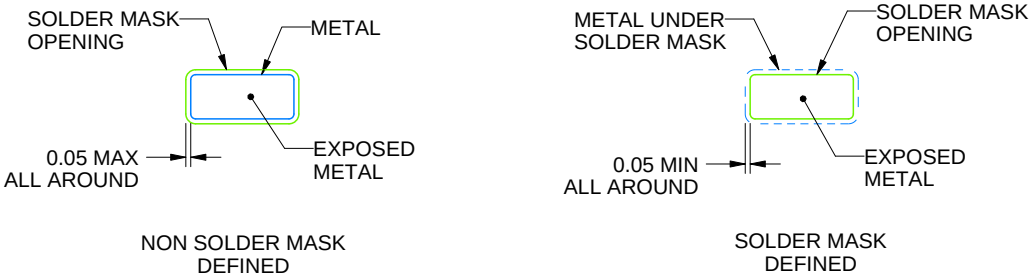


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

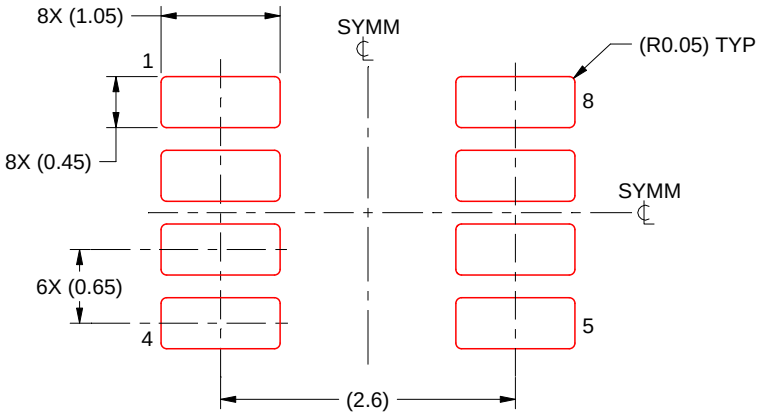
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

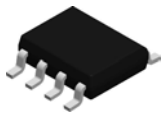


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

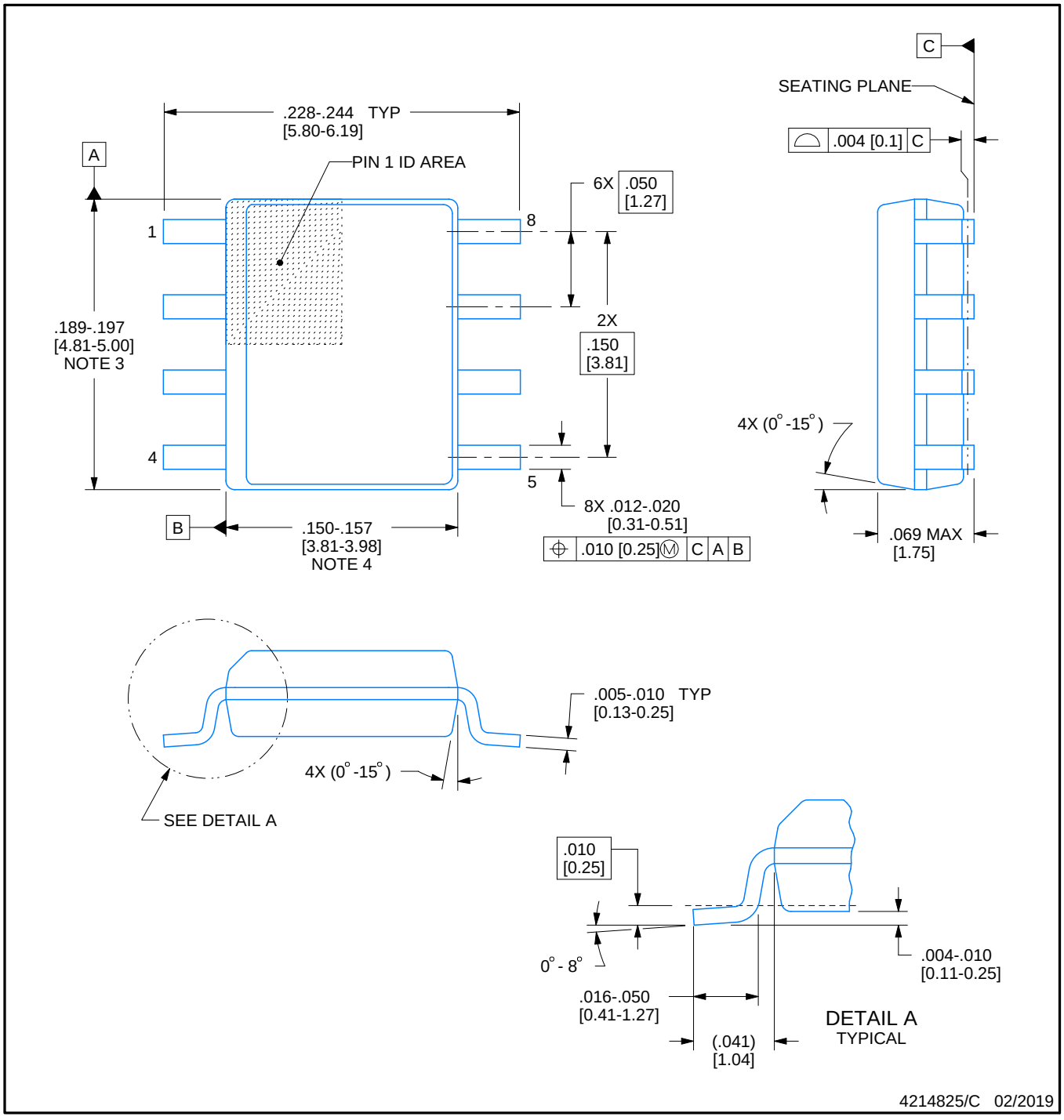


PACKAGE OUTLINE

D0008A

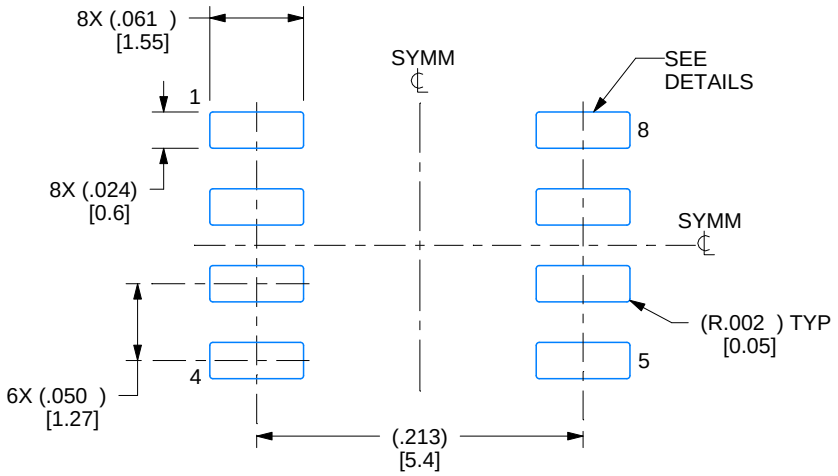
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

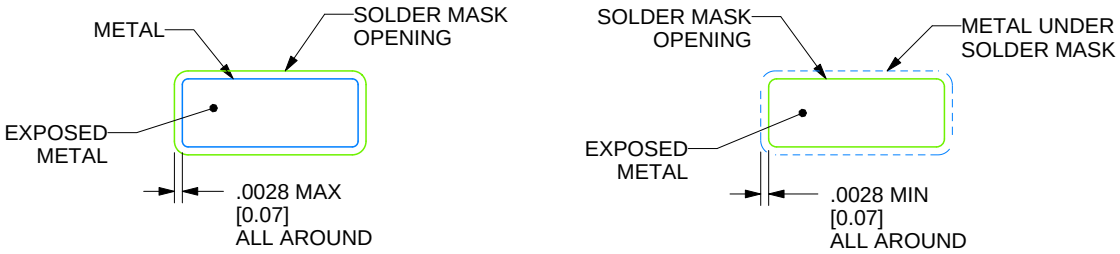


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

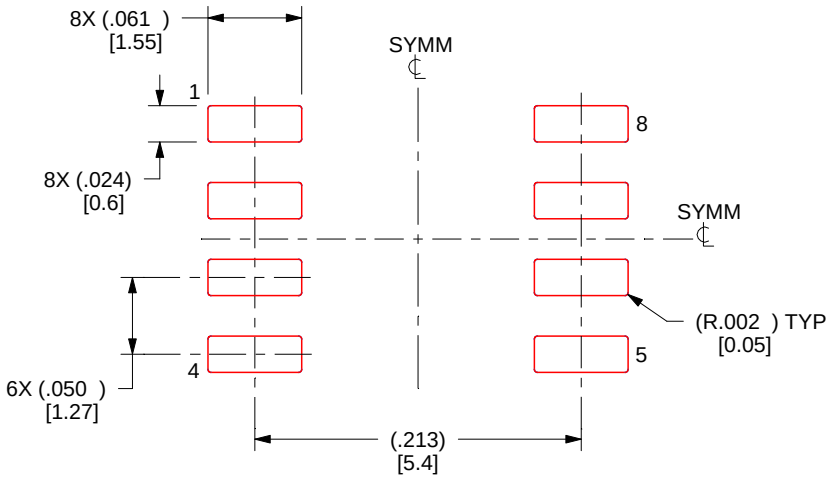
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

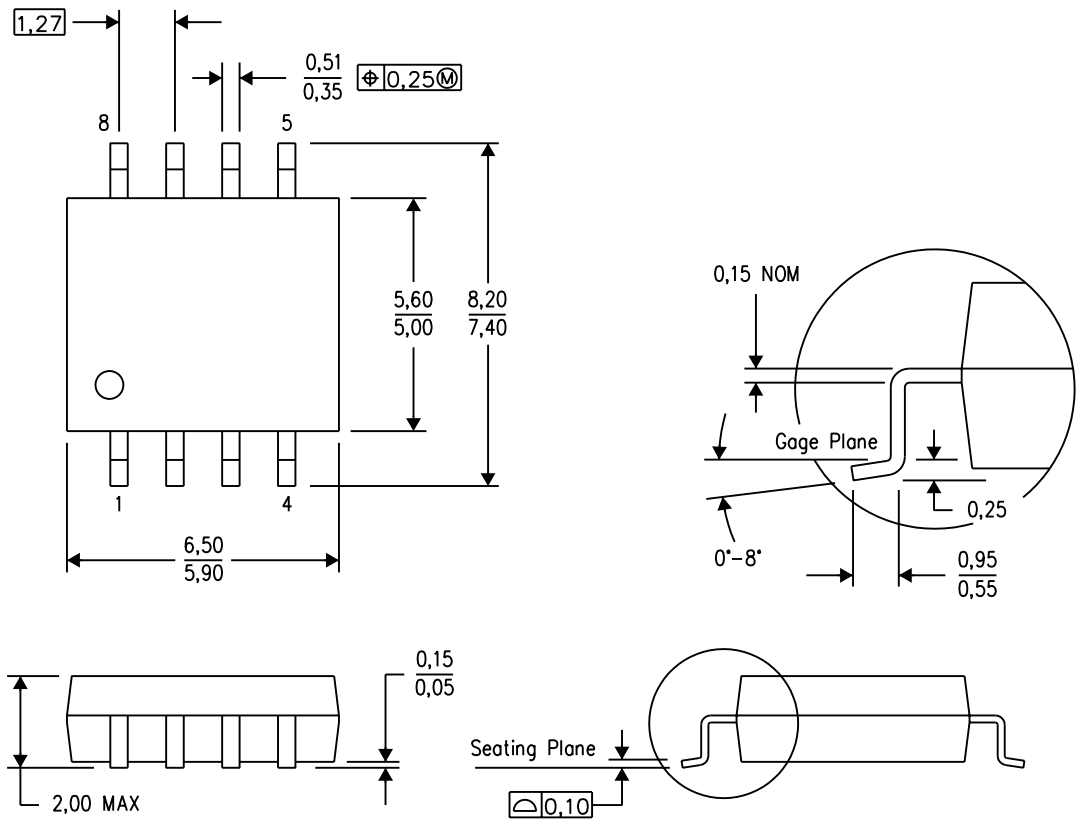
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

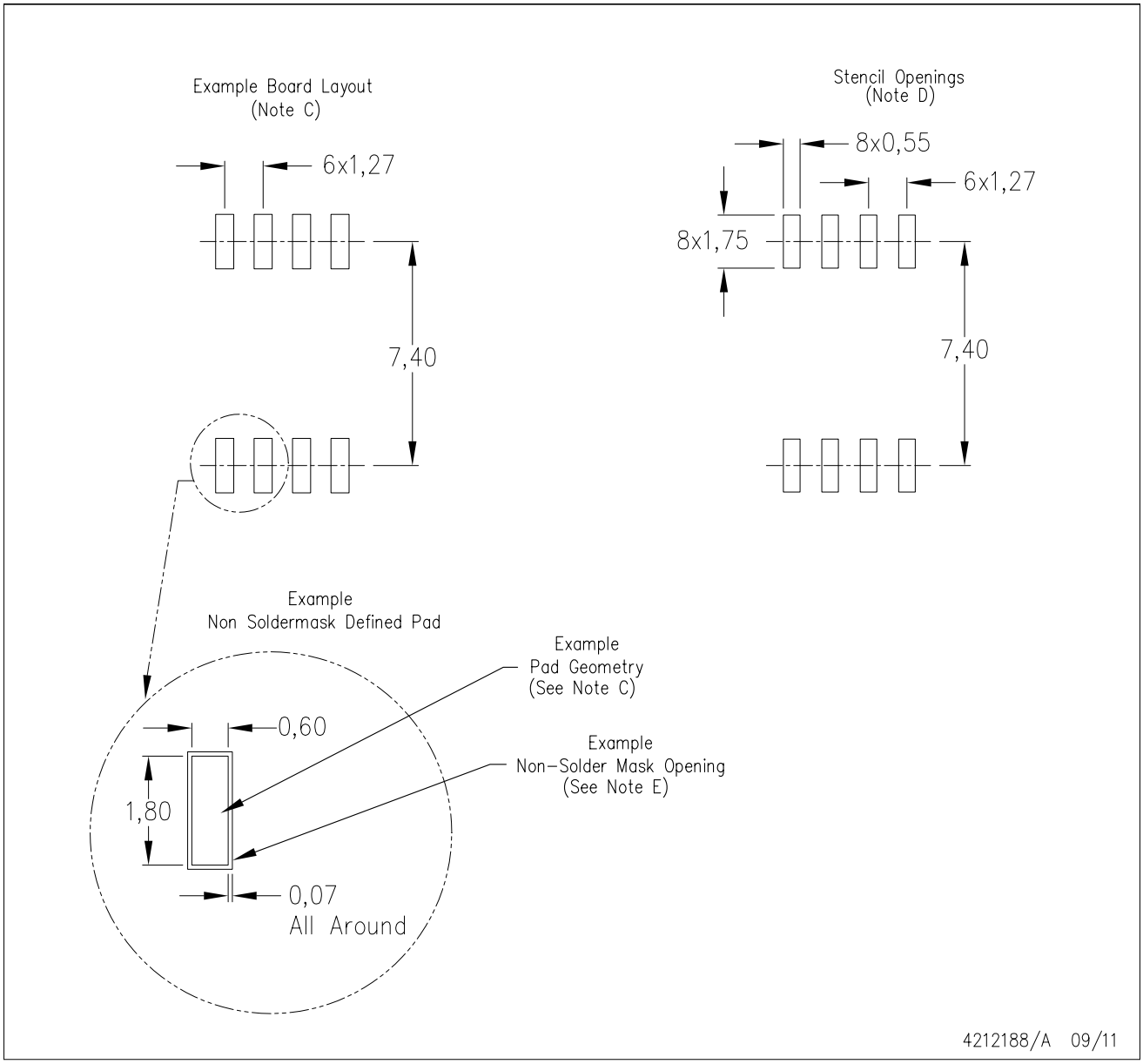
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

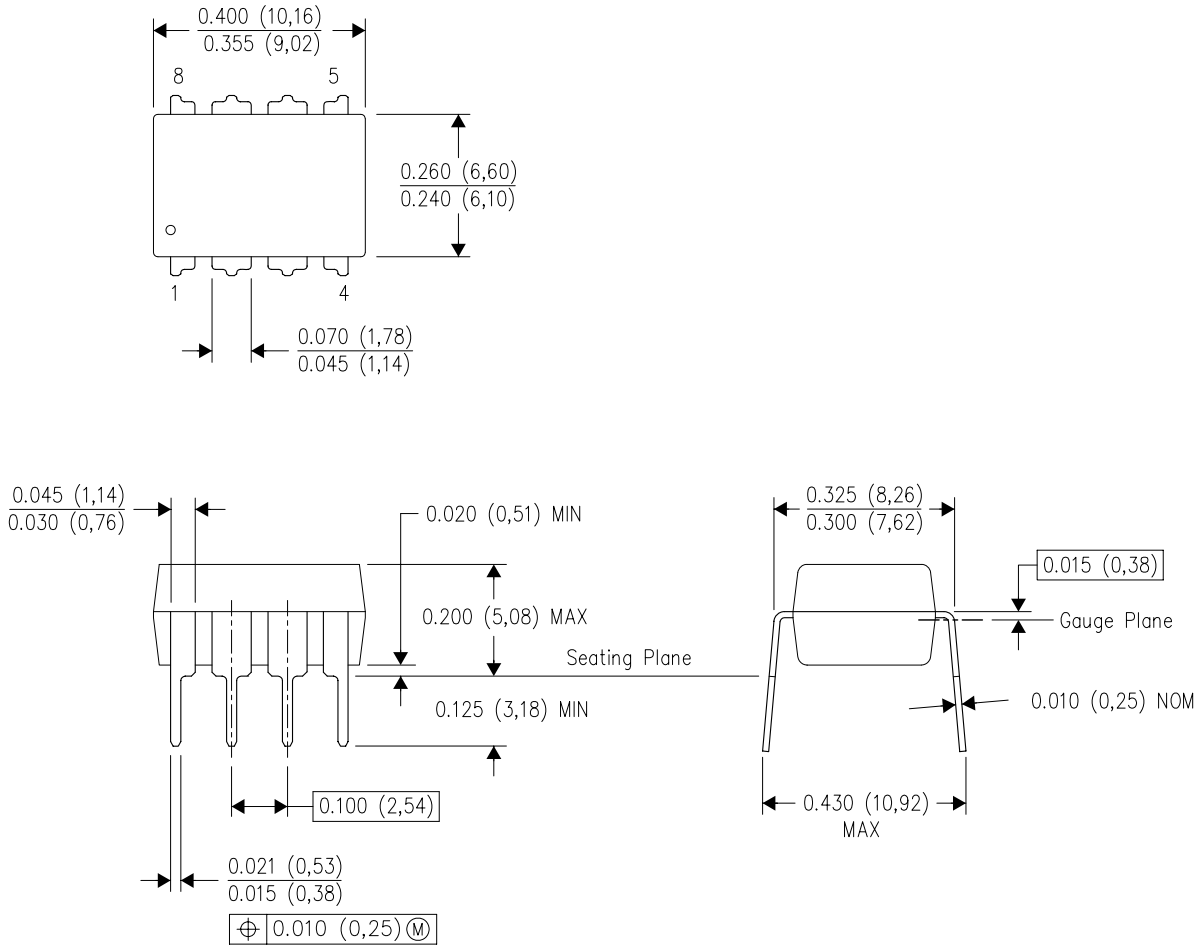
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

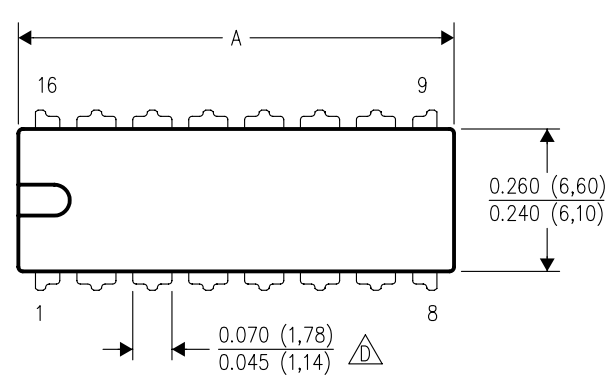


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

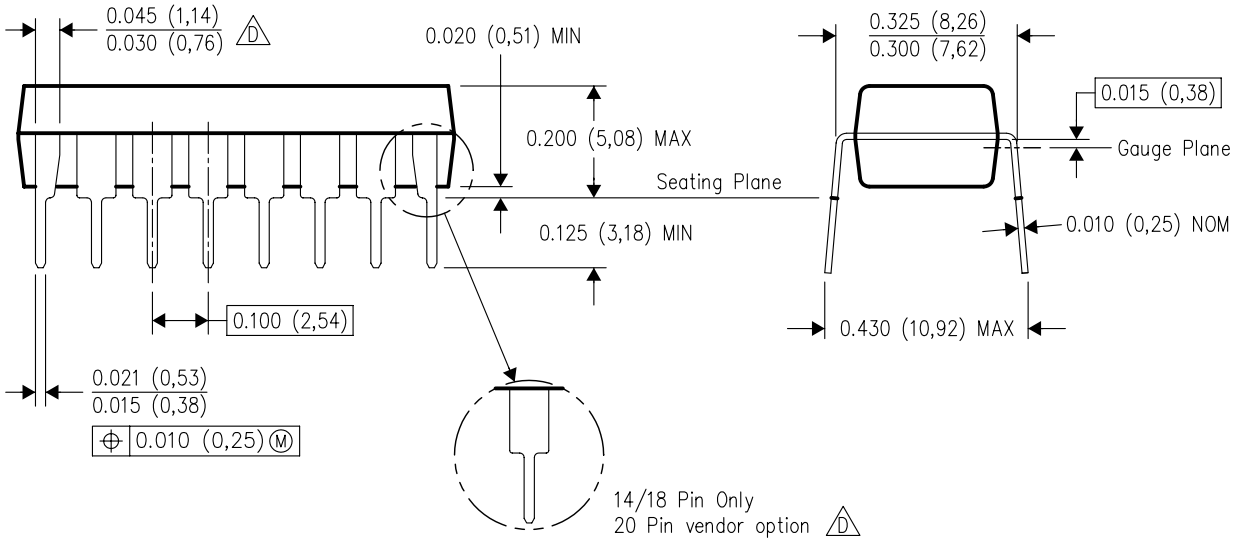
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

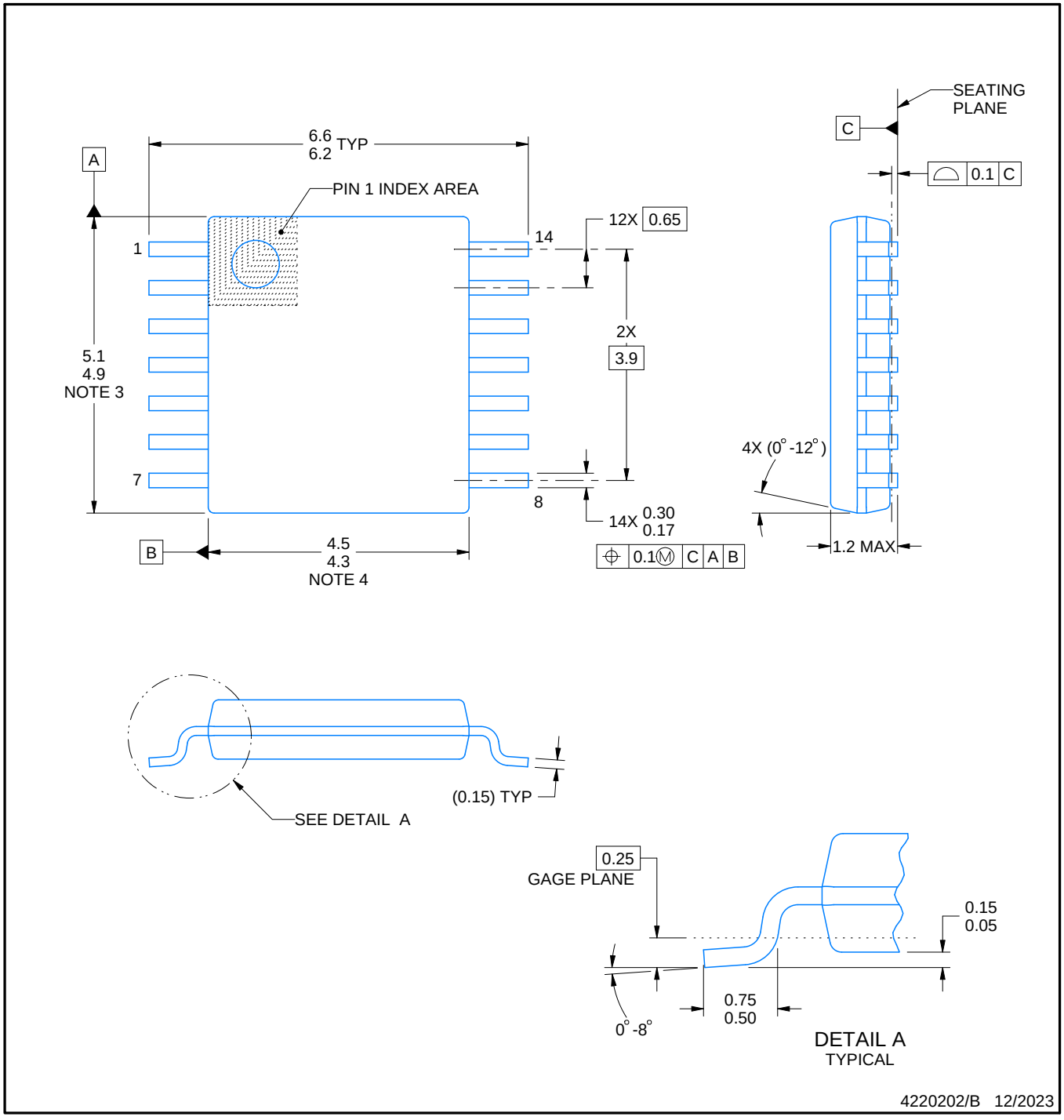
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

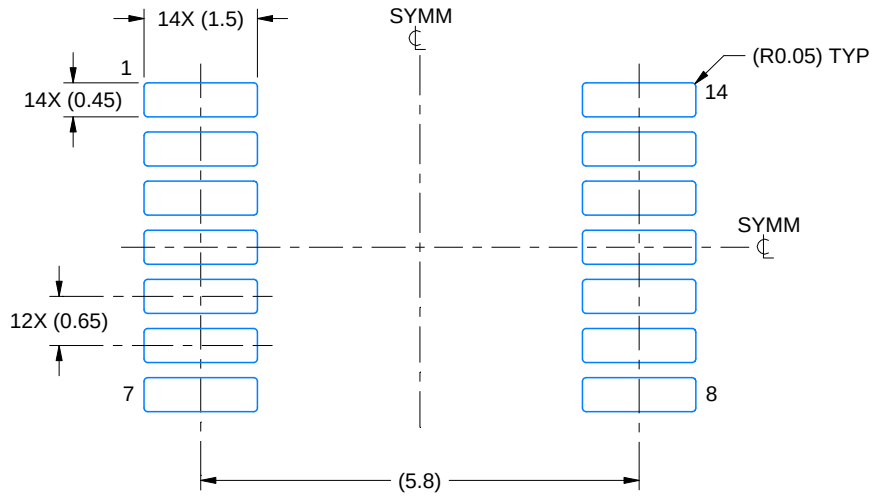
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

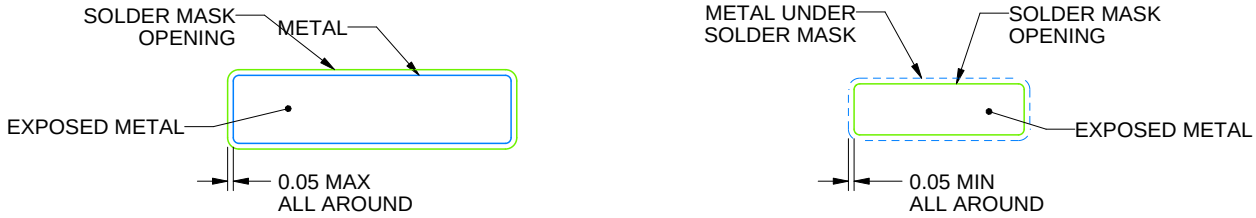


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

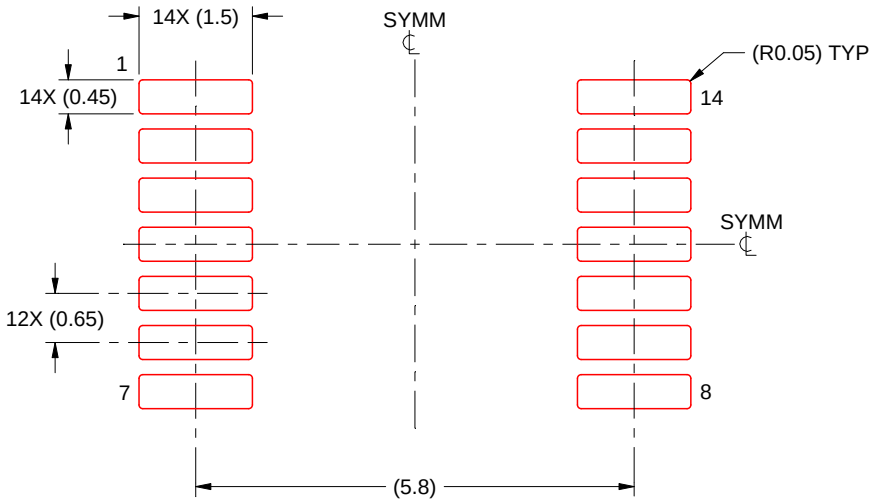


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

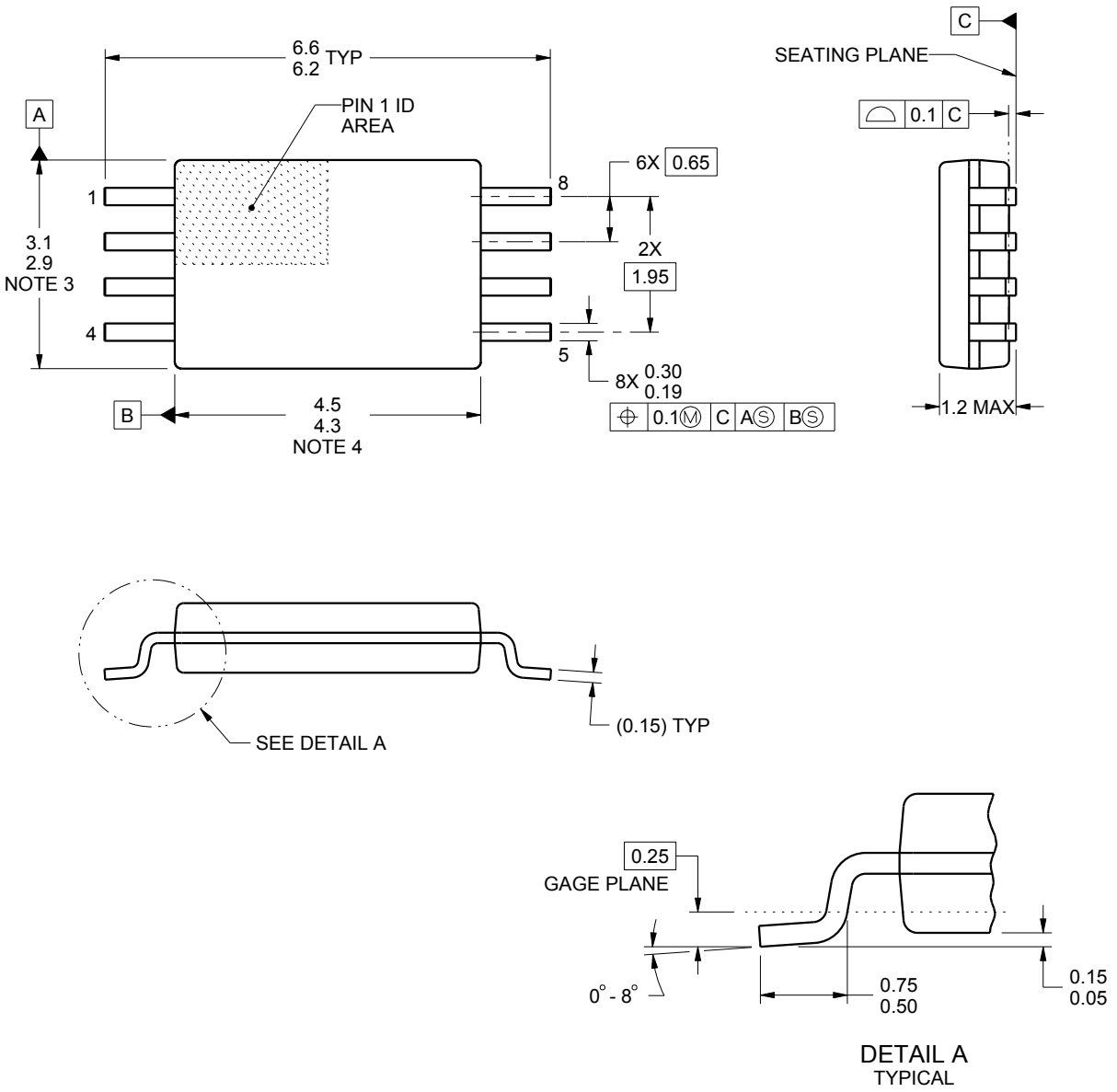
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

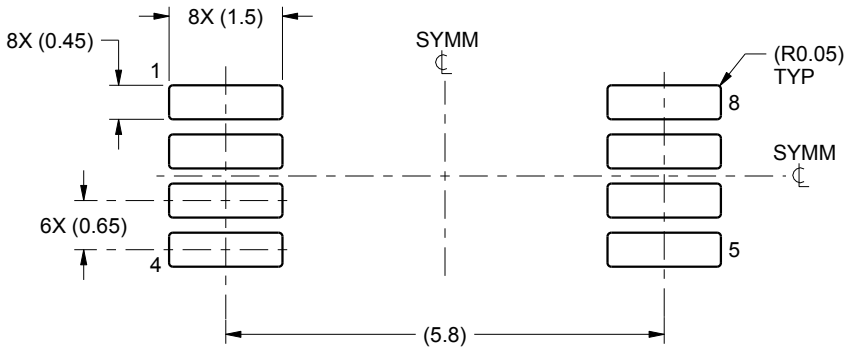
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

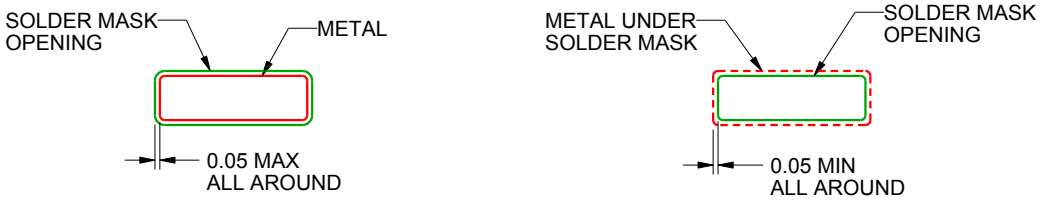


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

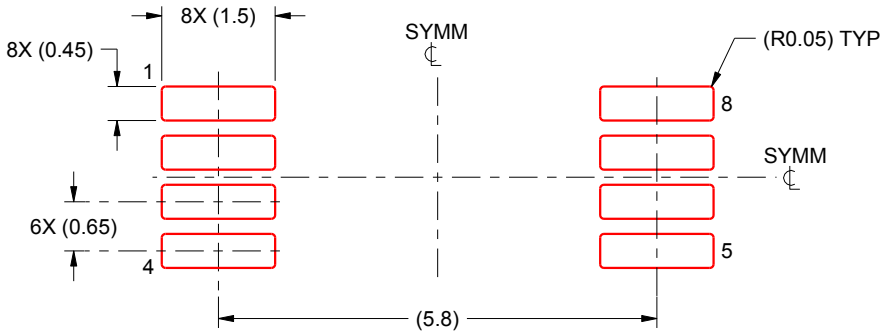


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2026，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月